Functional Safety Information

TPS2HC120-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS2HC120-Q1 (DGQ (HVSSOP, 28) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

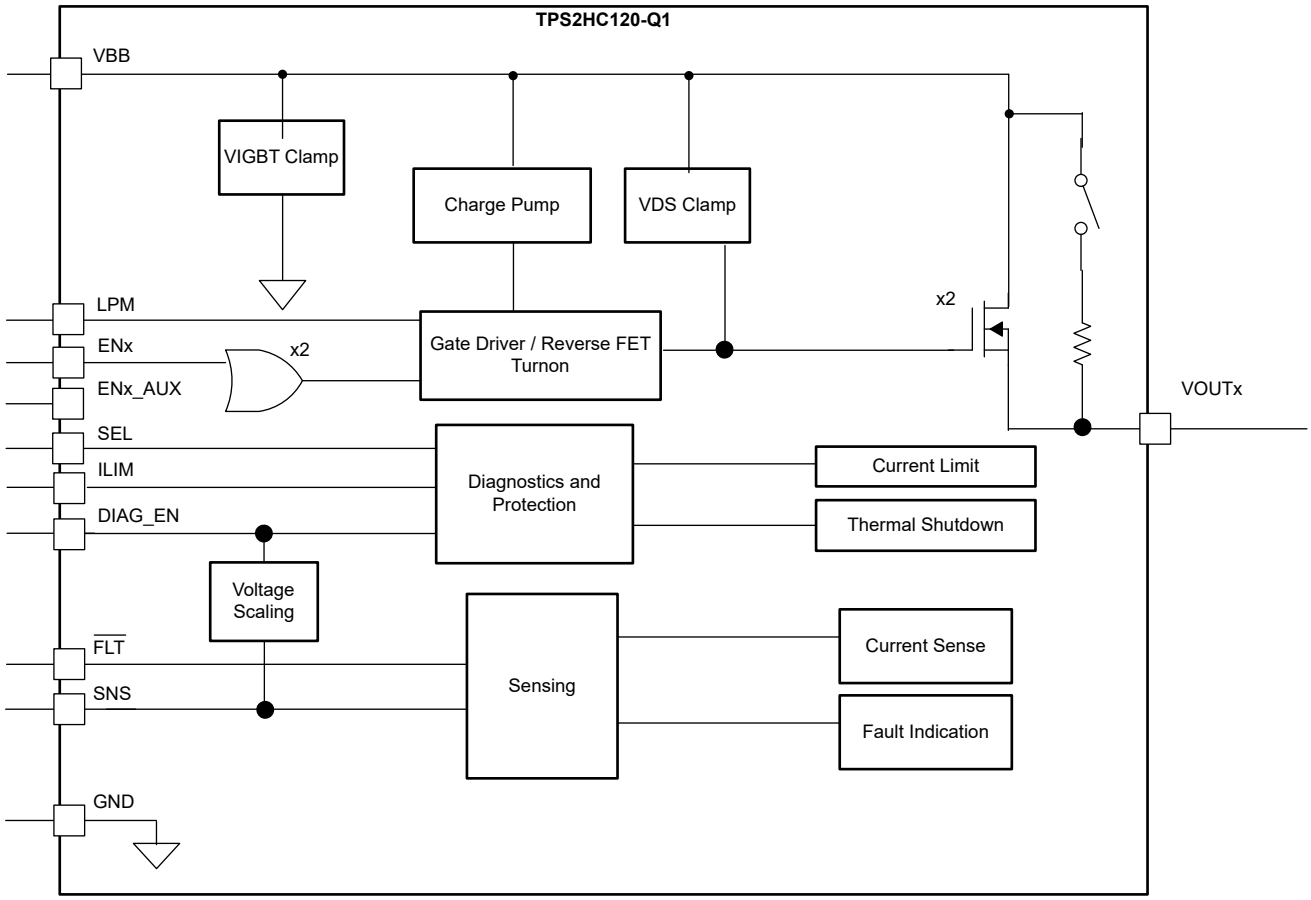

Figure 1-1. Functional Block Diagram

The TPS2HC120-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS2HC120-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	5
Package FIT rate	12

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS2HC120-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck ON	10
VOUT functional, not within specified voltage or timing	50
Diagnostics not within specification	10
Protection function fails to trigger	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS2HC120-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS2HC120-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS2HC120-Q1 datasheet.

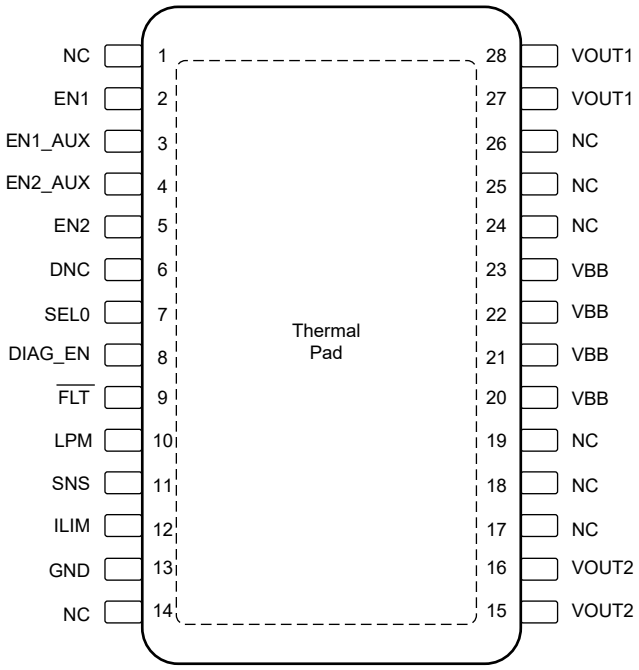

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the datasheet, including pullup and pulldown resistors, as needed.
- The datasheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect on the device.	D
EN1	2	The FET of CH1 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high.	B
EN1_AUX	3	There is no effect if EN1 is not also shorted to ground.	D
EN2_AUX	4	There is no effect if EN2 is not also shorted to ground.	D
EN2	5	The FET of CH2 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high.	B
DNC	6	There is no effect on the device.	D
SEL	7	The reported SNS current or fault status on the SNS pin is always of CH1 when the DIAG_EN pin is high.	B
DIAG_EN	8	The diagnostic features do not function, including current sense and fault reporting.	B
FLT	9	The reported fault status is potentially erroneous.	B
LPM	10	The reported LPM status is potentially erroneous.	B
SNS	11	The reported SNS current or fault status on the SNS pin is erroneous.	B
ILIM	12	The current limit is set per the shorted to ground setting of the ILIM pin of the device, as mentioned in the datasheet.	C
GND	13	Any GND network, connected for protection, is bypassed.	B
NC	14	There is no effect on the device.	D
VOUT2	15	The current limit of the device engages, and thermal protection turns off the FET of CH2.	B
	16		
NC	17	There is no effect on the device.	D
	18		
	19		
VBB	20	The output stages are not powered, and the FET of both channels do not turn ON.	B
	21		
	22		
	23		
NC	24	There is no effect on the device.	D
	25		
	26		
VOUT1	27	The current limit of the device engages, and thermal protection turns off the FET of CH1.	B
	28		

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect on the device.	D
EN1	2	The FET of CH1 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high (internal pulldown).	B
EN1_AUX	3	There is no effect if EN1 is also not open circuited.	D
EN2_AUX	4	There is no effect if EN2 is also not open circuited.	D
EN2	5	The FET of CH2 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high (internal pulldown).	B
DNC	6	The operation is as expected.	D
SEL	7	The reported SNS current or fault status on the SNS pin is always of CH1 when the DIAG_EN pin is high. (internal pulldown).	B
DIAG_EN	8	The diagnostic features do not function, including current sense and fault reporting (internal pulldown).	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FLT	9	The fault condition is not reported.	B
LPM	10	The LPM condition is not reported.	B
SNS	11	The current sense and fault at the SNS pin are not reported.	B
ILIM	12	The current limit is set per the OPEN setting of the ILIM pin of the device, as mentioned in the datasheet.	C
GND	13	The loss of ground detection engages, and the device turns OFF.	B
NC	14	There is no effect on the device.	D
VOUT2	15	During the ON state of the device, CH2 is disconnected. During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
	16		
NC	17	There is no effect on the device.	D
	18		
	19		
VBB	20	The device is not powered and both the channels are kept OFF.	B
	21		
	22		
	23		
NC	24	There is no effect on the device.	D
	25		
	26		
VOUT1	27	During the ON state of the device, CH1 is disconnected. During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
	28		

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	1	2 (EN1)	There is no effect on the device.	D
EN1	2	3 (EN1_AUX)	There is no effect on the device.	D
EN1_AUX	3	4 (EN2_AUX)	There is a loss of enable control for both channels and an erroneous fault is potentially reported at the SNS and FLT pins when the DIAG_EN pin is high.	B
EN2_AUX	4	5 (EN2)	There is no effect on the device.	D
EN2	5	6 (DNC)	Channel control of CH2 and channel selection is affected.	B
DNC	6	7 (SEL0)	Channel selection is affected.	B
SEL0	7	8 (DIAG_EN)	There is a loss of control of the DIAG_EN and SEL0 pins and the current and fault reporting of the SNS pin is erroneous.	B
DIAG_EN	8	9 (FLT)	The reported fault status and fault reporting of the SNS pin are erroneous.	B
FLT	9	10 (LPM)	The reported fault status and LPM status are erroneous.	B
LPM	10	11 (SNS)	The reported LPM status and the SNS pin output are erroneous.	B
SNS	11	12 (ILIM)	The current limit setting and the SNS pin output are erroneous.	B
ILIM	12	13 (GND)	The current limit is set per the shorted to ground setting of the ILIM pin of the device, as mentioned in the datasheet.	C
GND	13	14 (NC)	There is no effect on the device.	D
VOUT2	15, 16	17, 18, 19 (NC)	There is no effect on the device.	D
NC	17, 18, 19	20, 21, 22, 23 (VBB)	There is no effect on the device.	D
VBB	20, 21, 22, 23	24, 25, 26 (NC)	There is no effect on the device.	D
NC	24, 25, 26	27, 28 (VOUT1)	There is no effect on the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect on the device.	D
EN1	2	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
EN1_AUX	3	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
EN2_AUX	4	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
EN2	5	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
DNC	6	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
SEL	7	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
DIAG_EN	8	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
FLT	9	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
LPM	10	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
SNS	11	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
ILIM	12	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
GND	13	The supply power is bypassed, and the device stays OFF.	B
NC	14	There is no effect on the device.	D
VOUT2	15	The output of CH2 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
	16		
NC	17	There is no effect on the device.	D
	18		
	19		
VBB	20	There is no effect on the device.	D
	21		
	22		
	23		
NC	24	There is no effect on the device.	D
	25		
	26		
VOUT1	27	The output of CH1 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

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Last updated 10/2025