*Functional Safety Information*

# *TPS7A43-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

All trademarks are the property of their respective owners.

# 1 Overview

This document contains information for the TPS7A43-Q1 (DGQ (HVSSOP, 10) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagrams for reference.

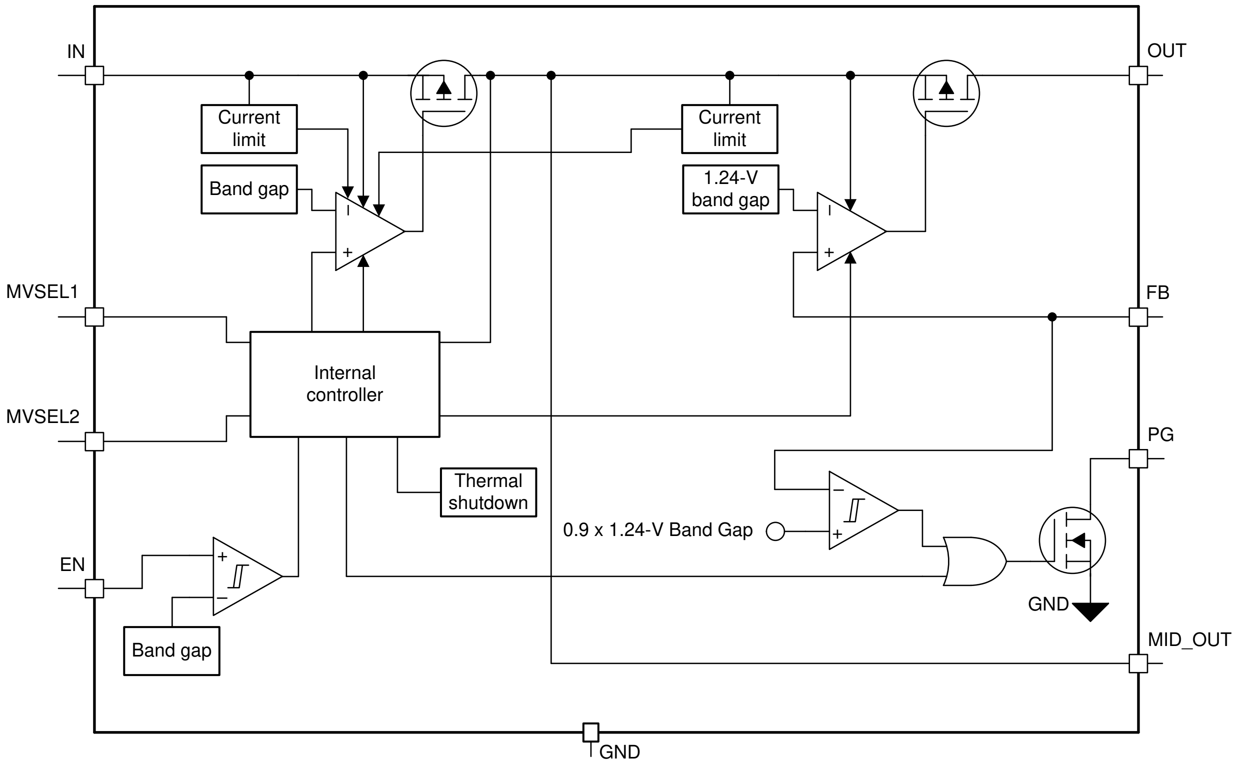


**Figure 1-1. Functional Block Diagram (TPS7A43-Q1, Adjustable)**

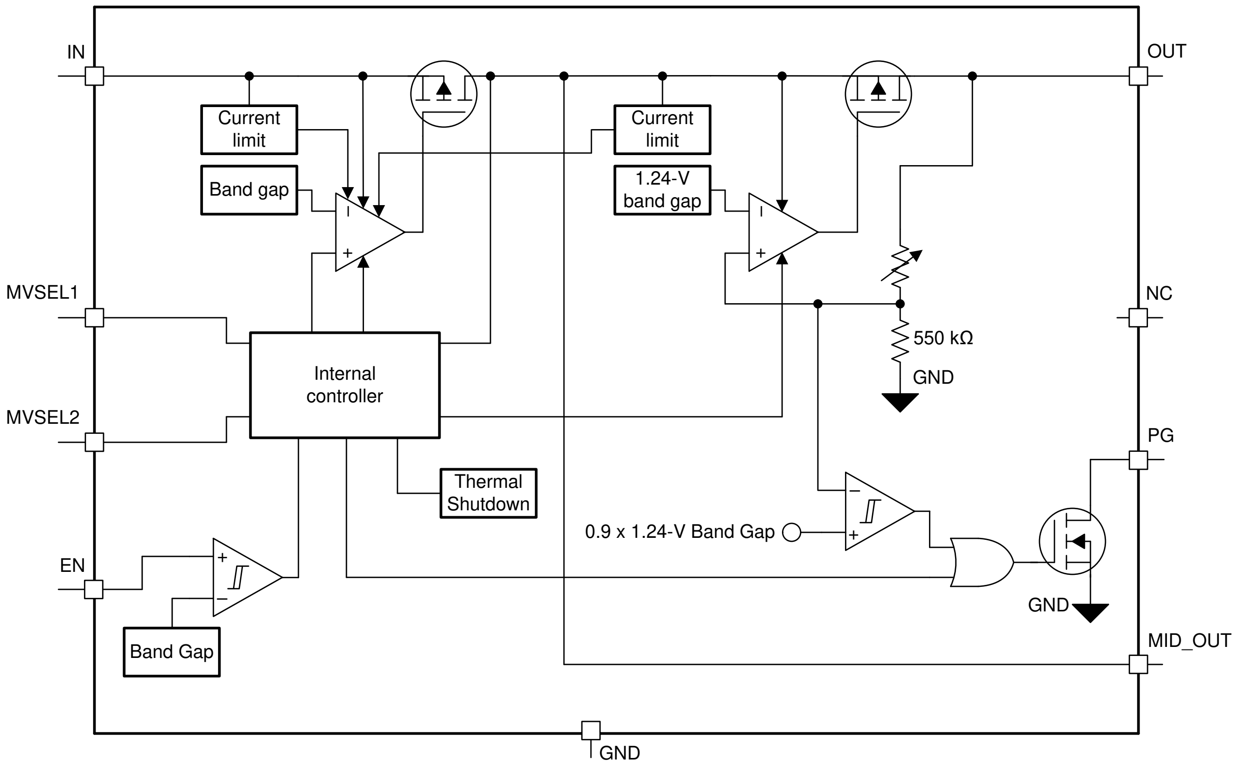


**Figure 1-2. Functional Block Diagram (TPS7A43-Q1, Fixed)**

The TPS7A43-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

**ADVANCE INFORMATION for preproduction products; subject to change without notice.**

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7A43-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 15 |
| Die FIT rate | 11 |
| Package FIT rate | 4 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 970mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog, or mixed | 30 FIT | 75°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7A43-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| $V_{OUT}$ low (no output), with $V_{MID\_OUT}$ in specification | 10 |
| $V_{OUT}$ and $V_{MID\_OUT}$ low (no output) | 10 |
| $V_{OUT}$ high (following regulated $V_{MID\_OUT}$) | 5 |
| $V_{OUT}$ and $V_{MID\_OUT}$ high (following $V_{IN}$) | 10 |
| $V_{OUT}$ not in specification (voltage or timing), with $V_{MID\_OUT}$ in specification | 25 |
| $V_{OUT}$ and $V_{MID\_OUT}$ not in specification (voltage or timing) | 30 |
| PG false trigger, fails to trigger | 5 |
| Short circuit any two pins | 5 |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7A43-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
| --- | --- |
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

Figure 4-1 and Figure 4-2 show the TPS7A43-Q1 pin diagrams. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A43-Q1 datasheet.

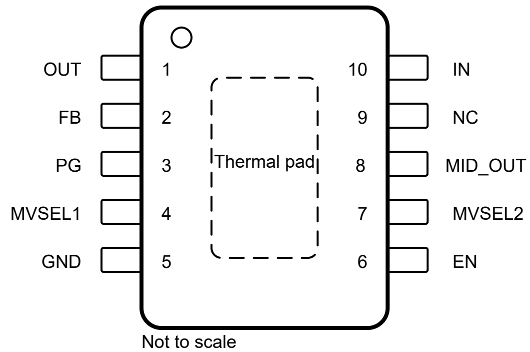


**Figure 4-1. Pin Diagram DGQ (HVSSOP, 10), Adjustable**

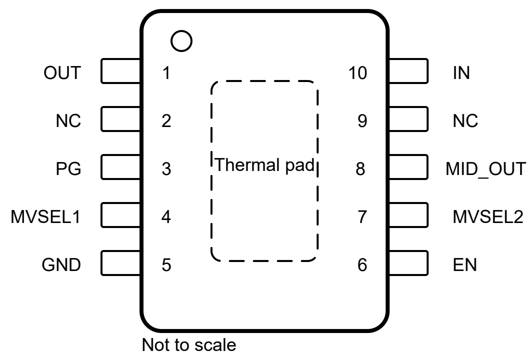


**Figure 4-2. Pin Diagram DGQ (HVSSOP, 10), Fixed**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device operates according to the recommended operating conditions and does not exceed the absolute maximum ratings.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT | 1 | Regulation is not possible. The device operates at current limit and can cycle in and out of thermal shutdown. | B |
| FB | 2 | Adjustable output variant: The device is in dropout mode and operates as a switch. The output tracks the input voltage ($V_{IN}$) minus the voltage dropout across the device ($V_{DO(OUT)}$ from $V_{IN}$ to $V_{OUT}$). | B |
| NC | 2 | Fixed output variants: There is no effect and the device operates as normal. | D |
| PG | 3 | Power-good does not assert when the output voltage is at target. Power sequencing can be affected. | B |
| MVSEL1 | 4 | For $V_{MID\_OUT}$ intentional setpoint of 12V or 15V: There is no effect and the device operates as normal. | D |
| | | For $V_{MID\_OUT}$ intentional setpoint of 10V: $V_{MID\_OUT}$ is programmed to and regulates 15V. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. | B |
| GND | 5 | There is no effect and the device operates as normal. | D |
| EN | 6 | The device is disabled, resulting in no output voltage. | B |
| MVSEL2 | 7 | For $V_{MID\_OUT}$ intentional setpoint of 10V or 15V: There is no effect and the device operates as normal. | D |
| | | For $V_{MID\_OUT}$ intentional setpoint of 12V: $V_{MID\_OUT}$ is programmed to and regulates either 10V or 15V, depending on the logic level of MVSEL1. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. | B |
| MID_OUT | 8 | Regulation is not possible. The device operates at current limit and can cycle in and out of thermal shutdown. | B |
| NC | 9 | There is no effect and the device operates as normal. | D |
| IN | 10 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT | 1 | The device output is disconnected from the load. | B |
| FB | 2 | Adjustable output variant: The state of the device is unknown. If the device is on, the output voltage is indeterminate. | B |
| NC | 2 | Fixed output variants: There is no effect and the device operates as normal. | D |
| PG | 3 | The power-good signal is not accessible. Power sequencing can be affected. | B |
| MVSEL1 | 4 | Setpoint voltage of $V_{MID\_OUT}$ is unknown and can assert as 10V, 12V, or 15V. Power dissipation across the device can be different than expected due to unpredictable $V_{MID\_OUT}$. | B |
| GND | 5 | There is no current loop for the supply voltage. The device is not operational and does not regulate. | B |
| EN | 6 | The enable circuit is in an unknown state. The device is either enabled or disabled. | B |
| MVSEL2 | 7 | The setpoint voltage of $V_{MID_OUT}$is unknown and can assert as 10V, 12V, or 15V. Power dissipation across the device can be different than expected due to unpredictable $V_{MID\_OUT}$. | B |
| MID_OUT | 8 | Stability of the device can be affected if there is insufficient capacitance to counteract effects of input source resistance and inductance. The device output is disconnected from the MID_OUT load, if present. | B<br>D |
| NC | 9 | There is no effect and the device operates as normal. | D |
| IN | 10 | Power is not supplied to the device, resulting in no output voltage. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| OUT | 1 | FB | Output voltage is equal to the internal reference voltage; the error amplifier is configured in unity gain. | B |
| | | NC | There is no effect and the device operates as normal. | D |

### Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| FB | 2 | PG | Adjustable output variant: FB can be damaged if the absolute maximum rating (5.5V) is violated. If the device is on and absolute maximum ratings are not exceeded, the output voltage is not regulated to the intended $V_{OUT}$. Power-good does not assert when the output voltage is at target. Power sequencing can be affected. | A<br>B |
| NC | | | Fixed output variants: There is no effect and the device operates as normal. | D |
| PG | 3 | MVSEL1 | Setpoint voltage of $V_{MID\_OUT}$ is unknown and can output 10V or 12V. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. Power-good does not assert predictably when the output voltage is at target. Power sequencing can be affected. | B |
| MVSEL1 | 4 | GND | For $V_{MID\_OUT}$ intentional setpoint of 12V or 15V: There is no effect and the device operates as normal. | D |
| | | | For $V_{MID\_OUT}$ intentional setpoint of 10V: $V_{MID\_OUT}$ is programmed to and regulates 15V. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. | B |
| EN | 6 | MVSEL2 | The enable circuit is in an unknown state. The device is either enabled or disabled. $V_{MID\_OUT}$ setpoint is impacted by the voltage of the EN-MVSEL2 shorted node and can output 10V, 12V, or 15V. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. | B |
| MVSEL2 | 7 | MID_OUT | Setpoint voltage of $V_{MID\_OUT}$ can be changed depending on the voltage on MID_OUT at the time of the short. If voltage on MID_OUT > $V_{MVSEL2(HIGH)}$, $V_{MID\_OUT}$ setpoint is 12V. If voltage on MID_OUT < $V_{MVSEL2(LOW)}$, $V_{MID\_OUT}$ setpoint can be 10V or 15V, depending on logic level of MVSEL1. As a result of changed $V_{MID\_OUT}$, power dissipation across the device can also change. | B |
| MID_OUT | 8 | NC | There is no effect and the device operates as normal. | D |
| NC | 9 | IN | There is no effect and the device operates as normal. | D |

### Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT | 1 | Damage can occur if the absolute maximum rating of OUT is exceeded (5.5V max for fixed, $V_{MID}$+0.3V for adjustable). Reverse current can destroy the device. | A |
| FB | 2 | Adjustable output variant: Damage can occur if the absolute maximum rating of FB is exceeded (5.5V max). If the absolute maximum ratings are not exceeded, the device can have no output voltage. | A<br>B |
| NC | | Fixed output variants: There is no effect and the device operates as normal. | D |
| PG | 3 | Damage can occur if the absolute maximum rating of PG is exceeded (20V max). There is a loss of the functionality of the PG pin. System-level issues can potentially occur due to unintended current flow in the pullup resistor, depending on the relative magnitudes of the supply voltage and the pullup voltage. | A<br>B |
| MVSEL1 | 4 | Damage can occur if the absolute maximum rating of MVSEL1 is exceeded (20V max). If supply voltage is within absolute maximum and exceeds $V_{MVSEL1(HIGH)}$, $V_{MID\_OUT}$ regulates to either 10V or 12V, depending on the logic level of MVSEL2. | A<br>B |
| GND | 5 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| EN | 6 | Damage can occur if the absolute maximum rating of EN is exceeded (20V max). If the absolute maximum rating is not exceeded, the device is always enabled when the input is powered. | A<br>B |
| MVSEL2 | 7 | Damage can occur if the absolute maximum rating of MVSEL2 is exceeded (20V max). If supply voltage is within absolute maximum and exceeds $V_{MVSEL2(HIGH)}$, $V_{MID\_OUT}$ regulates to 12V. | A<br>B |
| MID_OUT | 8 | Reverse current can destroy the device. If not damaged by reverse current, the device can have increased power dissipation across the secondary LDO, which can cause the device to cycle in and out of thermal shutdown. | A<br>B |
| NC | 9 | There is no effect and the device operates as normal. | D |
| IN | 10 | There is no effect and the device operates as normal. | D |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| January 2026 | * | Initial Release |

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.