Functional Safety Information

TPSI2260-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPSI2260-Q1 (DWQ (SOIC, 11) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the functional block diagram of TPSI2260-Q1 for reference.

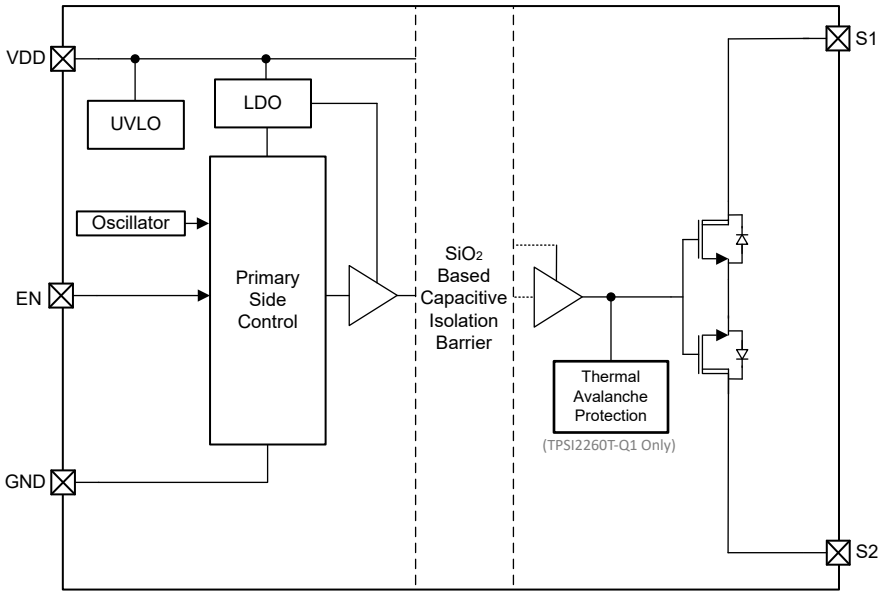

Figure 1-1. TPSI2260-Q1 Functional Block Diagram

TPSI2260-Q1 was developed using a quality-managed development process, but was not developed in accordance with IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPSI2260-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	4
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPSI2260-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Switch stuck OFF	7.5
Switch OFF – current higher than specification	40
Switch partially ON when enabled	45
Primary side ON – current higher than specification	7.5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSI2260-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin short-circuited to VDD (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to adjacent pin (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Note

When a pin short-to-ground case is discussed, only the primary side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Below is the TPSI2260-Q1 pin diagram package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPSI2260-Q1 data sheet.

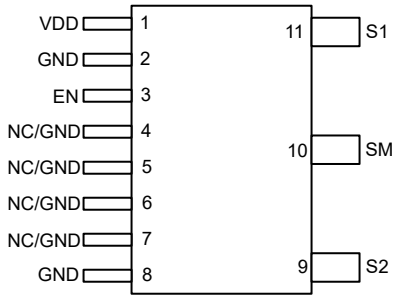

Figure 4-1. TPSI2260-Q1 Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is in the OFF state (UVLO), the secondary-side switch is in the OFF state.	B
GND	2	There is no effect on the device.	D
EN	3	The device is in the OFF state, the secondary-side switch is in the OFF state.	B
NC/GND	4	There is no effect on the device.	D
NC/GND	5	There is no effect on the device.	D
NC/GND	6	There is no effect on the device.	D
NC/GND	7	There is no effect on the device.	D
GND	8	There is no effect on the device.	D
S2	9	N/A	N/A
SM	10	N/A	N/A
S1	11	N/A	N/A

Table 4-3. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	There is no effect on the device.	D
GND	2	The device is in the OFF state (UVLO), the secondary-side switch is in the OFF state.	B
EN	3	The device is in the ON state, the secondary-side switch is in the ON state.	B
NC/GND	4	There is no effect on the device.	D
NC/GND	5	There is no effect on the device.	D
NC/GND	6	There is no effect on the device.	D
NC/GND	7	There is no effect on the device.	D
GND	8	The device is in the OFF state (UVLO), the secondary-side switch is in the OFF state.	B
S2	9	N/A	N/A
SM	10	N/A	N/A
S1	11	N/A	N/A

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is in the OFF state (UVLO), the secondary-side switch is in the OFF state.	B
GND	2	The device is in the OFF state, the secondary-side switch is in the OFF state.	D
EN	3	The device is in the OFF state, the secondary-side switch is in the OFF state.	B
NC/GND	4	There is no effect on the device.	D
NC/GND	5	There is no effect on the device.	D
NC/GND	6	There is no effect on the device.	D
NC/GND	7	There is no effect on the device.	D
GND	8	There is no effect on the device.	D
S2	9	There is no effect on the device.	D
SM	10	There is no effect on the device.	D
S1	11	There is no effect on the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	2	The device is in the OFF state (UVLO), the secondary-side switch is in the OFF state.	B
GND	2	3	There is no effect on the device.	B
EN	3	4	No effect if pin 4 is NC, if pin 4 is GND the device is in the OFF state, the secondary-side switch is in the OFF state.	D
				B
NC/GND	4	5	There is no effect on the device.	D
NC/GND	5	6	There is no effect on the device.	D
NC/GND	6	7	There is no effect on the device.	D
NC/GND	7	8	There is no effect on the device.	D
GND	8	9	N/A	N/A
S2	9	10	The device is only capable of blocking positive voltage from the S1 to S2 pins when the switches are OFF.	C
SM	10	11	The device is only capable of blocking negative voltage from the S1 to S2 pins when the switches are OFF.	C
S1	11	1	N/A	N/A

5 Revision History

Changes from December 2, 2025 to December 5, 2025 (from Revision * (December 2025) to Revision A (December 2025)) **Page**

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Last updated 10/2025