Functional Safety Information

LM25137
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the LM25137 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

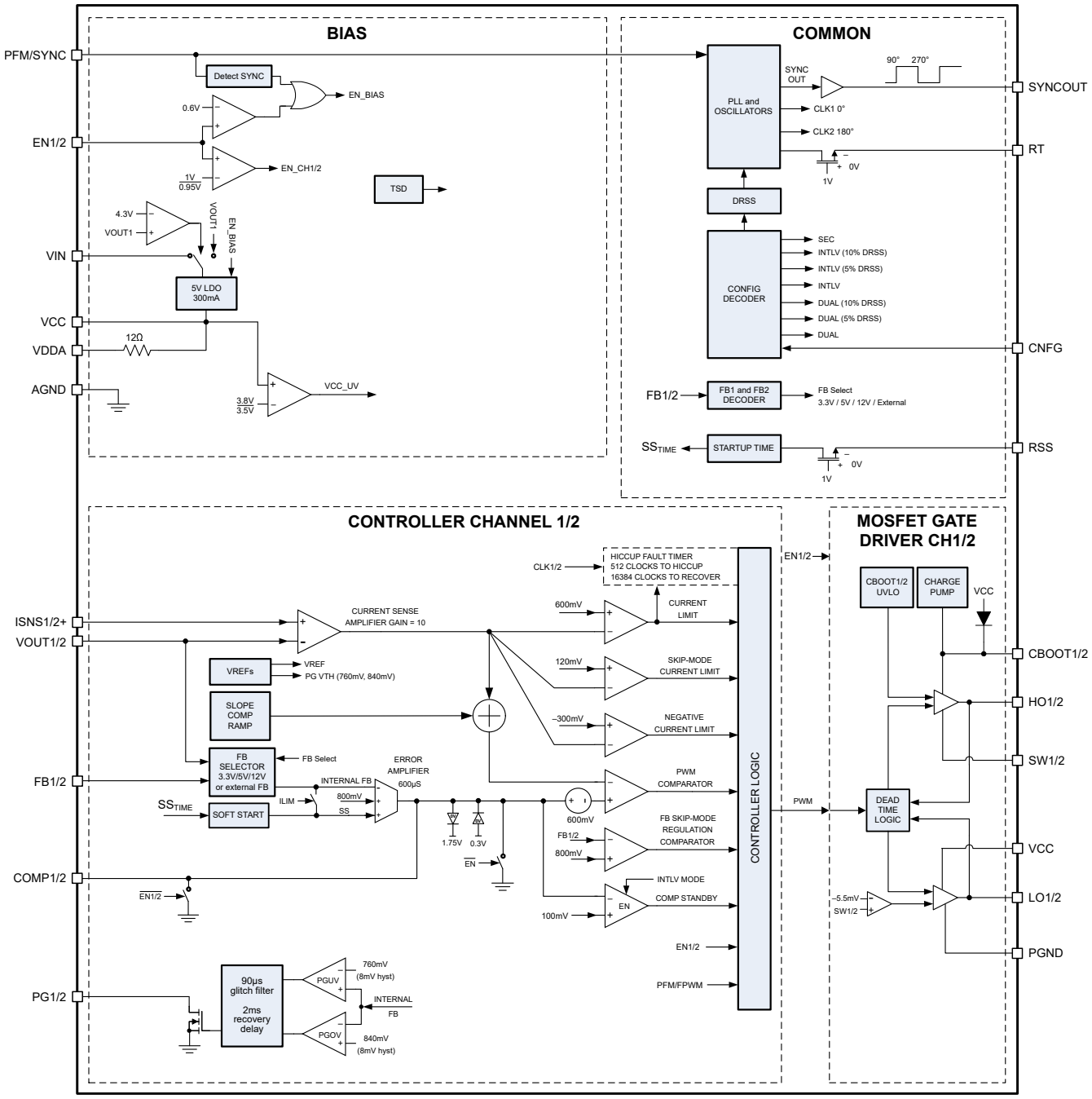

Figure 1-1. Functional Block Diagram

The LM25137 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standard.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM25137 based on the industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25.37
Die FIT rate	2.22
Package FIT rate	23.15

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 800mW
- Climate type: Worldwide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASIC, analog and mixed HV > 50V supply	26 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM25137 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output voltage not in specification	45
HO1/2 or LO1/2 gate driver stuck on, off or Hi-Z	30
No output voltage	17
Short circuit any two pins	5
PG1/2 – false trip or fails to trip	3

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM25137. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM25137 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM25137 data sheet.

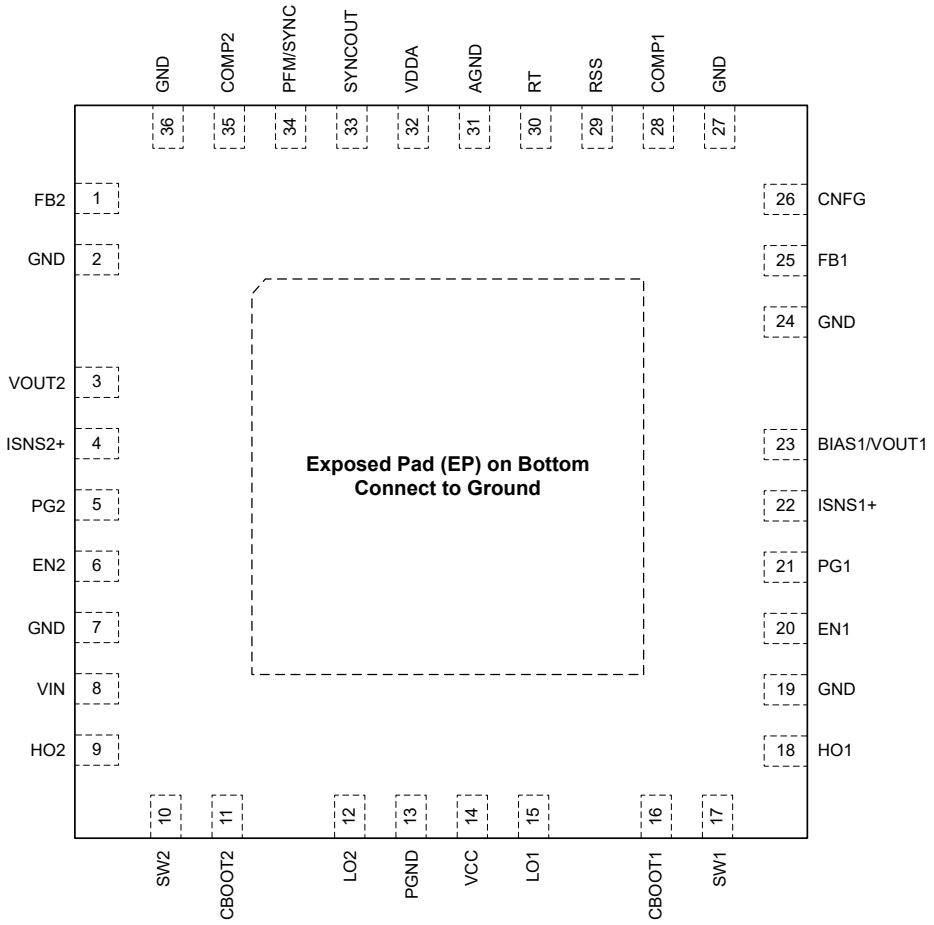

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit from the LM25137 data sheet is used
- PG1 and PG2 are pulled up to VOUT1 and VOUT2, respectively

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB2	1	VOUT1 as expected, VOUT2 = VIN.	B
GND	2	VOUT1 and VOUT2 as expected.	D
VOUT2	3	VOUT1 as expected, VOUT2 = 0V. Excessive current from VIN.	B
ISNS2+	4	VOUT2 as expected, VOUT2 = oscillation.	B
PG2	5	VOUT1 and VOUT2 as expected. PG2 forced low.	B
EN2	6	VOUT1 as expected, VOUT2 = 0V (disabled).	B
GND	7	VOUT1 and VOUT2 as expected.	D
VIN	8	VOUT1 = 0V, VOUT2 = 0V.	A
HO2	9	VOUT1 = 0V, VOUT = 0V. VCC regulator in current limit.	B
SW2	10	VOUT1 as expected, VOUT2 = VIN.	B
CBOOT2	11	VOUT1 = 0V, VOUT2 = 0V. VCC in current limit.	B
LO2	12	VOUT1 = 0V, VOUT2 = 0V. VCC oscillation due to short through LO2 driver.	B
PGND	13	VOUT1 and VOUT2 as expected.	D
VCC	14	VOUT1 = 0V, VOUT2 = 0V. VCC regulator in current limit.	B
LO1	15	VOUT1 = 0V, VOUT2 = 0V. VCC regulator in current limit.	B
CBOOT1	16	VOUT1 = 0V, VOUT2 = 0V. VCC regulator in current limit.	B
SW1	17	VOUT1 = 0V, VOUT2 as expected.	B
HO1	18	VOUT1 = 0V, VOUT2 = 0V. VCC regulator in current limit.	B
GND	19	VOUT1 and VOUT2 as expected.	B
EN1	20	VOUT1 = 0V (disabled), VOUT2 as expected.	B
PG1	21	VOUT1 and VOUT2 as expected. PG1 forced low.	B
ISNS1+	22	VOUT1 oscillation, VOUT2 as expected.	B
BIAS1/VOUT1	23	VOUT1 = 0V, VOUT2 as expected, VOUT1 in current limit.	B
GND	24	VOUT1 and VOUT2 as expected.	D
FB1	25	VOUT1 = VIN, VOUT2 as expected.	B
CNFG	26	(Dual) VOUT1 and VOUT2 as expected. (Interleaved) VOUT1 = as expected, VOUT2 = VIN.	B
GND	27	VOUT1 and VOUT2 as expected.	D
COMP1	28	VOUT1 = 0V and VOUT2 as expected.	B
RSS	29	VOUT1 and VOUT2 as expected. The soft-start time is at the minimum.	B
RT	30	VOUT1 and VOUT as expected. The oscillator is at the maximum.	B
AGND	31	VOUT1 and VOUT2 as expected.	D
VDDA	32	VOUT1 = 0V, VOUT2 = 0V, no switching.	B
SYNCOUT	33	VOUT1 and VOUT2 as expected. No SYNCOUT signal.	B
PFM/SYNC	34	VOUT1 and VOUT2 as expected. FPWM mode is always enabled.	B
COMP2	35	VOUT1 as expected, VOUT2 = 0V.	B
GND	36	VOUT1 and VOUT2 as expected.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB2	1	(Dual) VOUT1 as expected, VOUT2 = VIN. Possible damage.	B
GND	2	VOUT1 and VOUT2 as expected.	D
VOUT2	3	(Internal FB) VOUT1 as expected, VOUT2 = 0V, CH2 in current limit. (External FB) VOUT1 as expected, VOUT2 = 0V, CH2 in current limit.	B
ISNS2+	4	VOUT1 as expected, VOUT2 oscillation, loss of current limit.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PG1	5	VOUT1 and VOUT2 as expected. No PG1 signal information.	B
EN2	6	(Floats low) VOUT1 as expected, VOUT2 = 0V, CH2 disabled. (Floats high) VOUT1 and VOUT2 as expected.	B
GND	7	VOUT1 and VOUT2 as expected.	D
VIN	8	VOUT1 = 0V, VOUT2 = 0V.	B
HO2	9	(Dual) VOUT1 as expected, VOUT2 = VIN. (Interleaved) VOUT1 as expected, VOUT2 = VOUT1.	B
SW2	10	(Dual) VOUT1 as expected, VOUT2 = 0V. (Interleaved) VOUT1 as expected, VOUT2 = VOUT1.	B
CBOOT2	11	(Dual) VOUT1 as expected, VOUT2 = VCC – external MOSFET V_{TH}. (Interleaved) VOUT1 as expected, VOUT2 = 0V.	B
LO2	12	VOUT1 as expected, VOUT2 = VIN.	B
PGND	13	VOUT1 and VOUT2 as expected. PGND connects to AGND internally.	C
VCC	14	Results in erratic switching.	B
LO1	15	VOUT1 = VIN, low-side MOSFET damaged, VOUT2 as expected.	B
CBOOT1	16	VOUT1 < VCC – external MOSFET V_{TH}, VOUT2 as expected.	B
SW1	17	VOUT1 = VCC – external MOSFET V_{TH}, VOUT2 as expected.	B
HO1	18	VOUT1 = VIN, VOUT2 as expected.	B
GND	19	VOUT1 and VOUT2 as expected.	D
EN1	20	If EN1 floats high, VOUT1 as expected. If EN1 falls to < 1V, VOUT1 disables. VOUT2 as expected.	B
PG1	21	VOUT1 as expected, VOUT2 as expected. No PG1 information.	B
ISNS1+	22	VOUT1 oscillation, VOUT2 as expected.	B
BIAS1/VOUT1	23	Fixed VOUT setting: VOUT2 as expected and VOUT1 = 0V, CH1 in current limit. Adjustable VOUT setting: VOUT2 as expected and VOUT1 = 0V, CH2 in current limit.	C
GND	24	VOUT1 and VOUT2 as expected.	D
FB1	25	VOUT1 = VIN, VOUT2 as expected.	B
CNFG	26	VOUT1 and VOUT2 start in secondary mode. FB has no effect on COMP. If COMP voltage floats high, VOUT1 = VOUT2 = VIN. If no input on SYNCIN, then no switching and VOUT1 = VOUT2 = 0V.	B
GND	27	VOUT1 and VOUT2 as expected.	D
COMP1	28	VOUT1 oscillation, VOUT2 as expected.	D
RSS	29	VOUT1 and VOUT2 as expected. Soft-start extends to maximum time.	
RT	30	VOUT1 = 0V and VOUT2 = 0V. No switching.	B
AGND	31	AGND connected to PGND through two internal diodes. VOUT1 3X as expected, VOUT2 3X as expected.	B
VDDA	32	VOUT1 and VOUT2 as expected.	C
SYNCOUT	33	VOUT1 and VOUT2 as expected. No SYNCOUT signal.	C
PFM/SYNC	34	VOUT1 and VOUT2 as expected. No SYNC input signal. Operation is possible in PFM or FPFM (if PFM/SYNC floats high or low, respectively).	C
COMP2	35	(Dual) VOUT1 as expected, VOUT2 oscillation. (Interleaved) VOUT2 = VOUT1.	B
GND	36	VOUT1 and VOUT2 as expected.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB2	1	GND	VOUT1 as expected, VOUT2 = VIN.	B
GND	2	VOUT2	VOUT1 as expected, VOUT2 = 0V.	B
VOUT2	3	ISNS2+	VOUT1 as expected, VOUT2 oscillation, loss of current limit for CH2. Safety mechanisms shut down CH2.	B
ISNS2+	4	PG2	VOUT1 oscillation, VOUT2 as expected.	B
PG2	5	EN2	EN2 directly connected to V_{IN}, VOUT1 as expected, VOUT2 as expected. PG2 functionality lost. Resistive divider to VIN, VOUT1 as expected, PG2 clamps EN2 low, VOUT2 disables (0V).	B
EN2	6	VIN	VOUT1 as expected, VOUT2 as expected. Cannot disable CH2.	C
GND	7	VIN	VOUT1 = 0V, VOUT2 = 0V.	
VIN	8	HO2	VOUT1 as expected, VOUT2 driver damage, VOUT2 = VIN – V_{GS} (of high-side MOSFET).	B
HO2	9	SW2	VOUT1 as expected, VOUT2 = 0V. VCC overcurrent condition.	B
SW2	10	CBOOT2	VCC regulator to hit current limit. VOUT1, VOUT2 = 0V.	B
CBOOT2	11	LO2	VCC regulator to hit current limit. VOUT1, VOUT2 = 0V.	D
LO2	12	PGND	VOUT1 = 0V, VOUT2 = 0V, VCC regulator in current limit.	B
PGND	13	VCC	VOUT1 = 0V, VOUT2 = 0V.	B
VCC	14	LO1	VOUT1 = 0V, VOUT2 = 0V.	B
LO1	15	CBOOT1	VOUT1 and VOUT2 as expected.	D
CBOOT1	16	SW1	VCC to hit current limit. VOUT1, VOUT2 = 0V.	B
SW1	17	HO1	VOUT1 = 0V, VOUT2 as expected.	B
HO1	18	GND	VOUT1 = 0V, VOUT2 = 0V, VCC regulator in current limit.	B
GND	19	EN1	If EN1 is connected through a resister divider to VIN, VOUT1 disables, VOUT2 as expected. If EN1 is connected directly to VIN, VIN is shorted to GND and VOUT1, VOUT2 disabled.	B
EN1	20	PG1	EN1 directly connected to V_{IN}, VOUT2 as expected, VOUT1 as expected. PG1 functionality lost. Resistive divider to VIN, VOUT2 as expected, PG1 clamps EN1 low, VOUT1 disables (0V).	B
PG1	21	ISNS1+	ISNS1+ is a low-impedance pin. Very minimal loading of ISNS1+ by PG1. VOUT1 as expected with minimal error. VOUT2 as expected.	B
ISNS1+	22	BIAS1/VOUT1	VOUT1 oscillation, loss of current limit. VOUT2 as expected. Safety mechanisms shut down CH1.	B
BIAS1/VOUT1	23	GND	VOUT1 = 0V, VOUT2 as expected, VOUT1 in current limit.	B
GND	24	FB1	VOUT1 = VIN, VOUT2 as expected.	B
FB1	25	CNFG	FB1 resistor to VDDA, the LM25137 either starts up in secondary mode or interleaved (INTLV) mode. VOUT1 = oscillated between 0V and VIN, VOUT2 = oscillation 0V to VIN. FB1 resistor divider to VOUT1, R_{CNFG} < 71.5kΩ. The LM25137 either starts up in INTLV or single mode. VOUT1 and VOUT2 are random.	B
CNFG	26	GND	(Dual) VOUT1 as expected, VOUT2 as expected. (Interleaved) cannot reach steady-state voltage regulation.	B
GND	27	COMP1	VOUT1 = 0V, VOUT2 as expected.	D
COMP1	28	RSS	VOUT1 uncontrolled due to RSS amplifier setting COMP1 to 1V, VOUT2 as expected.	B
RSS	29	RT	VOUT1 as expected, VOUT2 as expected. Oscillator frequency is potentially altered.	B
RT	30	AGND	VOUT1 and VOUT2 as expected. Oscillator frequency is at the maximum.	C
AGND	31	VDDA	VOUT1 = 0V, VOUT2 = 0V, VDDA = 0V.	B
VDDA	32	SYNCOUT	VOUT1 as expected. VOUT2 as expected.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SYNCOUT	33	PFM/SYNC	If PFM/SYNC = VDDA or GND, VOUT1 as expected, VOUT2 as expected. SYNCOUT injects noise on VDDA. If there is an external CLK, the SYNCOUT driver applies a clock.	B
PFM/SYNC	34	COMP2	PFM/SYNC = 0V, VOUT1 = 0V, VOUT2 as expected. PFM/SYNC = 5V, VOUT1 as expected, VOUT2 = VIN. PFM/SYNC = SYNC, VOUT1 as expected, VOUT2 oscillation.	B
COMP2	35	GND	VOUT1 as expected, VOUT2 = 0V.	B
GND	36	FB2	VOUT1 as expected, VOUT2 = VIN.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB2	1	If V_{IN} < 6.5V and FB2 = VDDA, then VOUT1 as expected, VOUT2 = 3.3V.	B
		If V_{IN} > 6.5V, FB2 exceeds the maximum voltage rating, and FB2 is damaged.	A
GND	2	VOUT1 and VOUT2 = 0V, excessive current from VIN.	B
VOUT2	3	If V_{IN} < 47V, VOUT1 as expected, VOUT2 = VIN.	B
		If V_{IN} > 47V, VOUT2 exceeds the maximum voltage rating, and VOUT2 is damaged.	A
ISNS2+	4	If V_{IN} < 47V, VOUT1 as expected, VOUT2 = VIN.	B
		If V_{IN} > 47V, VOUT1 as expected, ISNS2+ exceeds the maximum voltage rating, and ISNS2+ is damaged.	A
PG2	5	If V_{IN} < 47V, VOUT1 and VOUT2 as expected, PG2 pulled up to VIN.	D
		If V_{IN} > 47V, PG2 exceeds the maximum voltage rating, and PG2 is damaged.	A
EN2	6	VOUT1 and VOUT2 as expected.	D
GND	7	VOUT1 and VOUT2 = 0V, excessive current from VIN.	B
VIN	8	VOUT1 and VOUT2 as expected.	D
HO2	9	If V_{IN} < 6.5V, VOUT1 as expected, VOUT2 = VIN.	B
		If V_{IN} > 6.5V, HO2 exceeds the maximum voltage rating, and HO2 is damaged.	A
SW2	10	VOUT1 as expected, VOUT2 = VIN, excessive current from VIN.	B
CBOOT2	11	If V_{IN} < 6.5V, VOUT1 and VOUT2 as expected.	B
		If V_{IN} > 6.5V, the pin exceeds the maximum voltage rating for CBOOT2 to SW2, and CBOOT2 is damaged.	A
LO2	12	If V_{IN} < 6.5V, VOUT1 and VOUT2 = 0V, excessive current from VIN.	B
		If V_{IN} > 6.5V, LO2 exceeds the maximum voltage rating, and LO2 is damaged.	A
PGND	13	VOUT1 and VOUT2 = 0V, and there is excessive current from VIN.	B
VCC	14	If V_{IN} < 6.5V, VOUT1 and VOUT2 as expected.	D
		If V_{IN} > 6.5V, VCC exceeds the maximum voltage rating, and VCC is damaged.	A
LO1	15	If V_{IN} < 6.5V VOUT1 and VOUT2 = 0V, excessive current from VIN.	B
		If V_{IN} > 6.5V, LO1 exceeds the maximum voltage rating, and LO1 is damaged.	A
CBOOT1	16	If V_{IN} < 6.5V, VOUT1 and VOUT2 as expected.	B
		If V_{IN} > 6.5V, the pin exceeds the maximum rating for CBOOT1 to SW1, and CBOOT1 is damaged.	A
SW1	17	VOUT1 = VIN, VOUT1 as expected, excessive current from VIN.	B
HO1	18	If V_{IN} < 6.5V, VOUT1 = VIN, VOUT2 as expected.	B
		If V_{IN} > 6.5V, HO1 exceeds the maximum voltage rating, and HO1 is damaged.	A
GND	19	VOUT1 and VOUT2 = 0V, and there is excessive current from VIN.	B
EN1	20	VOUT1 and VOUT2 as expected.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PG1	21	If V_{IN} < 47V, VOUT1 and VOUT2 as expected, PG1 pulled up to VIN.	D
		If V_{IN} > 47V, PG1 exceeds the maximum voltage rating, and the PG1 pin is damaged.	A
ISNS1+	22	If V_{IN} < 47V, VOUT1 = VIN, VOUT2 as expected.	B
		If V_{IN} > 47V, VOUT1 as expected, ISNS1+ exceeds the maximum voltage rating, and ISNS1+ is damaged.	A
BIAS1/VOUT1	23	If V_{IN} < 47V, VOUT1 = VIN, VOUT2 as expected.	B
		If V_{IN} > 47V, BIAS1/VOUT1 exceeds the maximum voltage rating, and BIAS1/VOUT1 is damaged.	A
GND	24	VOUT1 and VOUT2 = 0V, and there is excessive current from VIN.	B
FB1	25	If V_{IN} < 6.5V and FB2 = VDDA, then VOUT1 as expected, VOUT2 = 3.3V.	B
		If V_{IN} > 6.5V, FB1 exceeds the maximum voltage rating, and FB1 is damaged.	A
CNFG	26	If V_{IN} < 6.5V, then VOUT1 and VOUT2 as expected.	B
		If V_{IN} > 6.5V, CNFG exceeds the maximum voltage rating, and CNFG is damaged.	A
GND	27	VOUT1 and VOUT2 = 0V, and there is excessive current from VIN.	B
COMP1	28	If V_{IN} > 5V and < 6.5V, then VOUT1 and VOUT2 = 0V.	B
		If V_{IN} > 6.5V, COMP1 exceeds the maximum voltage rating, and COMP1 is damaged.	A
RSS	29	If V_{IN} < 6.5V, then VOUT1 and VOUT2 as expected.	D
		If V_{IN} > 6.5V, RSS exceeds the maximum voltage rating, and RSS is damaged.	A
RT	30	If V_{IN} < 6.5V, then VOUT1 and VOUT2 = 0V.	B
		If V_{IN} > 6.5V, the pin exceeds the RT maximum rating, and RT is damaged.	A
AGND	31	VOUT1 and VOUT2 = 0V, and there is excessive current from VIN.	B
VDDA	32	If V_{IN} < 6.5V, then VOUT1 and VOUT2 as expected.	D
		If V_{IN} > 6.5V, VDDA exceeds the maximum voltage rating, and VDDA is damaged.	A
SYNCOUT	33	If V_{IN} < 6.5V, then VOUT1 and VOUT2 as expected.	B
		If V_{IN} > 6.5V, SYNCOUT exceeds the maximum voltage rating, and SYNCOUT is damaged.	A
PFM/SYNC	34	If V_{IN} < 6.5V, then VOUT1 and VOUT2 as expected.	B
		If V_{IN} > 6.5V, PFM/SYNC exceeds the maximum voltage rating, and PFM/SYNC is damaged.	A
COMP2	35	If V_{IN} > 5V and < 6.5V, then VOUT1 and VOUT2 = 0V.	B
		If V_{IN} > 6.5V, COMP2 exceeds the maximum voltage rating, and COMP2 is damaged.	A
GND	36	VOUT1 = 0V, VOUT2 = 0V, and there is excessive current from VIN.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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