Functional Safety Information

TPS7C84-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7C84-Q1 (SOIC and VSON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

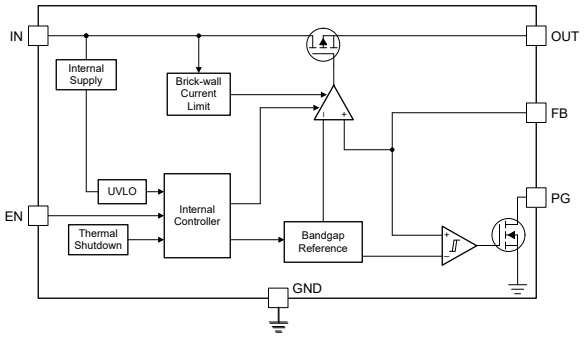

Figure 1-1. Functional Block Diagram (Adjustable)

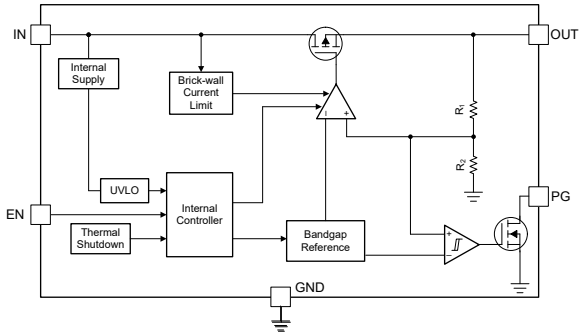

Figure 1-2. Functional Block Diagram (Fixed)

The TPS7C84-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC Package

This section provides functional safety failure in time (FIT) rates for the SOIC package of the TPS7C84-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50V supply	20	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS7C84-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50V supply	20	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7C84-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT low (no output)	45
VOUT high (following input)	10
VOUT not in specification (voltage, or timing)	35
Short circuit any two pins	5
PG false trip, fails to trip	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7C84-Q1 (SOIC and VSON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device must maintain the same pin configuration as with the SOIC-8 and VSON-8 packages.
- The device operates across virtual junction temperatures ranging from –40°C to 125°C.
- The device operates at an input voltage less than 5.5V and output current less than 1.5A.
- The device operates according to the recommended operating conditions and does not exceed the absolute maximum ratings.

4.1 SOIC Package

Figure 4-1 shows the TPS7C84-Q1 pin diagram for the SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7C84-Q1 datasheet.

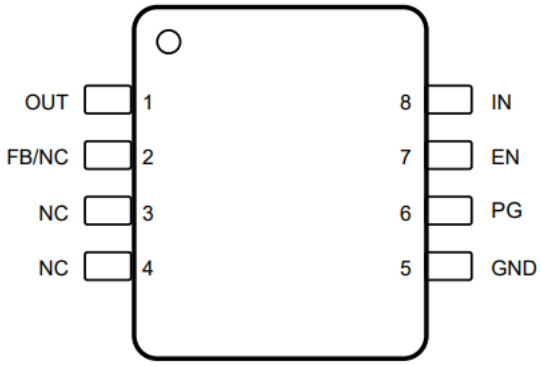

Figure 4-1. Pin Diagram (SOIC) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation of the device is not possible, the device operates at current limit. The device can cycle in an out of thermal shutdown.	B
FB/NC	2	(Adjustable) The device operates as a switch in dropout mode. The output tracks the input voltage (VIN) minus the voltage drop out (VDO).	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	There is no effect on the device. The device operates normally.	D
PG	6	The output of the open drain power good pin is pulled low.	C
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device. System performance depends on limiting the upstream current.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The output of the device is disconnected from the load.	B
FB/NC	2	(Adjustable) The state of the device is unknown. If the device is on, the output voltage is indeterminate.	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
PG	6	The output of the open drain power good pin is left floating.	C
EN	7	The device potentially does not turn on.	B
IN	8	The device is not powered. The device is not functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB	The error amplifier is configured in unity gain: output voltage = reference voltage.	B
		NC	(Fixed) There is no effect on the device. The device operates normally.	D
FB	2	NC	There is no effect on the device. The device operates normally.	D
NC	3	NC	There is no effect on the device. The device operates normally.	D
	4			
GND	5	PG	The output of the open drain power good pin is pulled low.	C
PG	6	EN	The device remains on. Regulation of the device is possible.	C
EN	7	IN	The device remains on. Regulation of the device is possible.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation of the device is not possible, leading to an undesired output state.	B
FB/NC	2	(Adjustable) The device can have no output voltage.	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	Power is not supplied to the device.	B
PG	6	There is a loss of the functionality of the PG pin. System-level issues can potentially occur due to unintended current flow in the pullup resistor, depending on the relative magnitudes of the supply voltage and the pullup voltage.	A
EN	7	The device remains on. Regulation of the device is possible.	C
IN	8	There is no effect on the device. The device operates normally.	D

4.2 VSON Package

Figure 4-2 shows the TPS7C84-Q1 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7C84-Q1 datasheet.

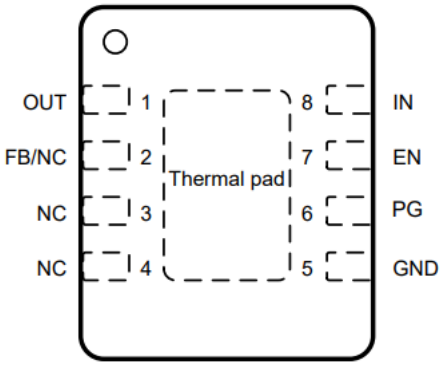

Figure 4-2. Pin Diagram (VSON Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation of the device is not possible, the device operates at current limit. The device can cycle in an out of thermal shutdown.	B
FB/NC	2	(Adjustable) The device operates as a switch in dropout mode. The output tracks the voltage in (VIN) minus the voltage drop out (VDO).	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	There is no effect on the device. The device operates normally.	D
PG	6	The output of the open drain power good pin is pulled low.	C
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device. System performance depends on limiting the upstream current.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The output of the device is disconnected from the load.	C
FB/NC	2	(Adjustable) The state of the device is unknown. If the device is on, the output voltage is indeterminate.	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
PG	6	The output of the open drain power good pin is left floating.	C
EN	7	The device potentially does not turn on.	B
IN	8	The device is not powered. The device is not functional.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB/NC	The error amplifier is configured in unity gain: output voltage = reference voltage.	B
			(Fixed) There is no effect on the device. The device operates normally.	D
FB	2	NC	(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	NC	There is no effect on the device. The device operates normally.	D
	4			
GND	5	PG	The output of the open drain power good pin is pulled low.	C
PG	6	EN	There is no effect on the device. The device operates normally.	D
EN	7	IN	The device remains on. Regulation of the device is possible.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation of the device is not possible, leading to an undesired output state.	B
FB/NC	2	(Adjustable) The device can have no output voltage.	B
		(Fixed) There is no effect on the device. The device operates normally.	D
NC	3	There is no effect on the device. The device operates normally.	D
	4		
GND	5	Power is not supplied to the device.	B
PG	6	There is a loss of the functionality of the PG pin. System-level issues can potentially occur due to unintended current flow in the pullup resistor, depending on the relative magnitudes of the supply voltage and the pullup voltage.	A
EN	7	The device remains on. Regulation of the device is possible.	C
IN	8	There is no effect on the device. The device operates normally.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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