Functional Safety Information

TPS3842-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS3842-Q1 (DRL package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

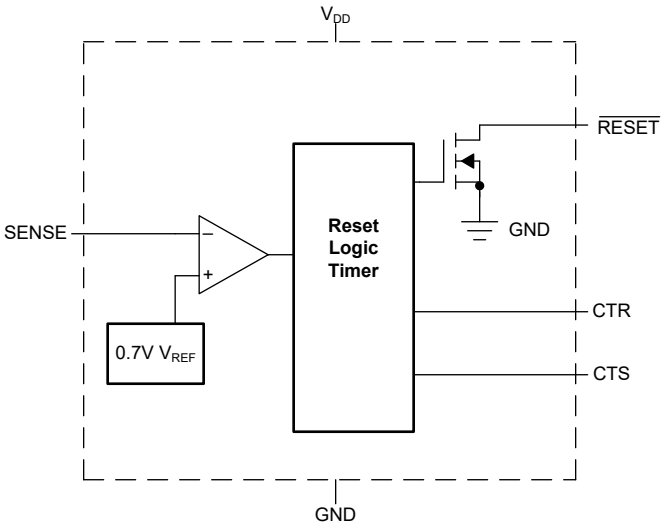

Figure 1-1. Adjustable Threshold Functional Diagram

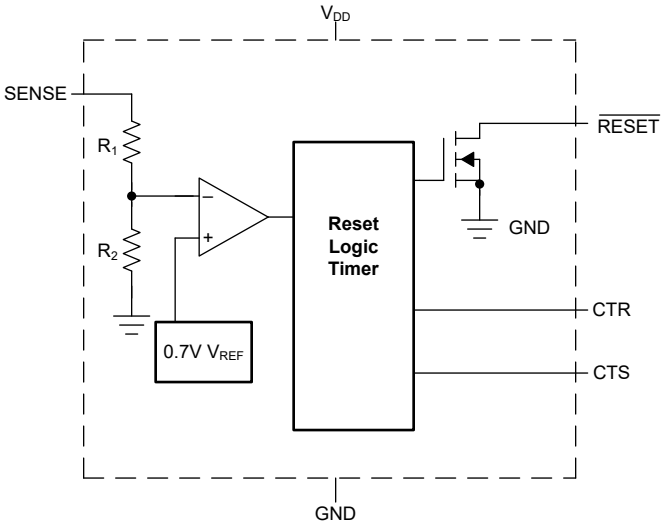

Figure 1-2. Fixed Threshold Functional Diagram

TPS3842-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS3842-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	3
Package FIT rate	1

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 60mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3842-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
RESET | fails to trip	35
RESET | false trip	25
RESET | trip outside specification (voltage or time)	30
RESET | delay outside specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS3842-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS3842-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section of the *TPS3842-Q1* data sheet.

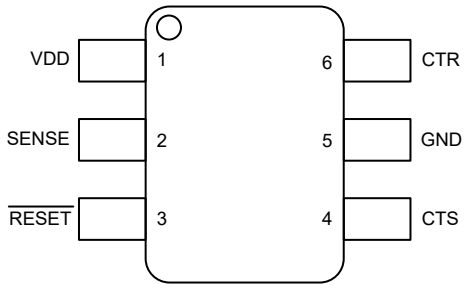

Figure 4-1. Pin Diagram DRL Package 6-Pin SOT5X3

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- At $V_{DD\ (MIN)} \leq VDD \leq V_{DD\ (MAX)}$
- CTS = Open, CTR = Open
- Output reset pullup resistor (R_{PULLUP}) = 10kΩ, output reset pullup voltage (V_{PULLUP} = 3.3V)
- Sense is monitoring VDD
- Typical values are at T_A = 25°C, V_{DD} = 3.3V, C_{VDD}= 0.1µF, and V_{ITN} = 0.7V; unless stated otherwise.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description Of Potential Failure Effects	Failure Effect Class
VDD	1	VDD short to GND; device has no power for normal operation.	B
SENSE	2	$\overline{\text{RESET}}$ asserts.	B
$\overline{\text{RESET}}$	3	Forces $\overline{\text{RESET}}$ low.	B
CTS	4	$\overline{\text{RESET}}$ is unable to assert.	B
GND	5	No damage to the device. No impact to the functionality of the device.	D
CTR	6	$\overline{\text{RESET}}$ asserts normally but does not deassert.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	Device is not powered.	B
SENSE	2	No damage to the device. Reset asserts.	B
$\overline{\text{RESET}}$	3	Reset functionality is lost since reset is not pulled up to VDD.	B
CTS	4	Normal operation.	D
GND	5	Device is not powered.	B
CTR	6	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
VDD	1	SENSE	Normal functionality if SENSE is monitoring VDD rail. $\overline{\text{RESET}}$ asserts if VDD < V_{itn}.	D
	2			
SENSE	2	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ follows V_{SENSE}; giving instances of wrong outputs.	C
	3			
CTS	4	GND	$\overline{\text{RESET}}$ is unable to assert.	B
	5			
GND	5	CTR	$\overline{\text{RESET}}$ asserts normally but does not deassert.	B
	6			

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No damage to the device. No impact to the functionality of the device.	D
SENSE	2	$\overline{\text{RESET}}$ asserts if VDD < V_{itn}; otherwise, normal functionality.	D
$\overline{\text{RESET}}$	3	Forces $\overline{\text{RESET}}$ high.	B
CTS	4	No damage to the device. No impact to the functionality of the device.	D
GND	5	GND short to VDD; device has no power for normal operation.	D
CTR	6	$\overline{\text{RESET}}$ asserts.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

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