Functional Safety Information

TMUX405x-Q1 Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	
2.1 TSSOP Package	
2.2 SOT-23-THIN Package	
2.3 WQFN Package	
3 Failure Mode Distribution (FMD)	
4 Pin Failure Mode Analysis (Pin FMA)	
4.1 TMUX4051-Q1: TSSOP and SOT-23-THIN Packages	
4.2 TMUX4051-Q1: WQFN Package	
4.3 TMUX4052-Q1: TSSOP and SOT-23-THIN Packages	
4.4 TMUX4052-Q1: WQFN Package	

Trademarks

All trademarks are the property of their respective owners.

ISTRUMENTS Overview www.ti.com

1 Overview

This document contains information for the TMUX405x-Q1 (TSSOP, SOT-23-THIN, and WQFN packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

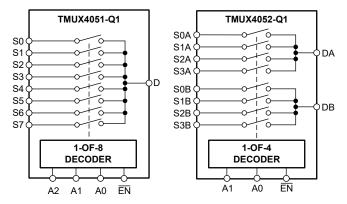


Figure 1-1. Functional Block Diagram

The TMUX405x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.



2 Functional Safety Failure In Time (FIT) Rates 2.1 TSSOP Package

This section provides functional safety failure in time (FIT) rates for the TSSOP package of the TMUX405x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	15
Die FIT rate	5
Package FIT rate	10

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

· Mission profile: motor control from table 11

Power dissipation: 130 mW
Climate type: world-wide table 8
Package factor (lambda 3): table 17b

Substrate material: FR4EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	BICMOS ASICs Analog and Mixed =< 50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



2.2 SOT-23-THIN Package

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the TMUX405x-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	10
Die FIT rate	5
Package FIT rate	5

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- · Power dissipation: 130 mW
- · Climate type: world-wide table 8
- · Package factor (lambda 3): table 17b
- · Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Table Category		Reference Virtual T _J
5	BICMOS ASICs Analog and Mixed =< 50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



2.3 WQFN Package

This section provides functional safety failure in time (FIT) rates for the WQFN package of the TMUX405x-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

	le de la companya de
FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	10
Die FIT rate	5
Package FIT rate	5

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- · Mission profile: motor control from table 11
- · Power dissipation: 130 mW
- · Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- · Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Table Category		Reference Virtual T _J
5	BICMOS ASICs Analog and Mixed =< 50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMUX405x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
MUX no output (HIZ)	30
MUX channel stuck on	15
MUX channel stuck off	15
MUX functional out of specification voltage or timing	40



4 Pin Failure Mode Analysis (Pin FMA)

- Pin short-circuited to ground (see Table 4-2, Table 4-7, Table 4-12, and Table 4-17)
- Pin open-circuited (see Table 4-3, Table 4-8, Table 4-13, and Table 4-18)
- Pin short-circuited to an adjacent pin (see Pin FMA for Devices Short-Circuited to Adjacent Pin, Table 4-9, Table 4-14, and Table 4-19)
- Pin short-circuited to supply (see Table 4-5, Table 4-6, Table 4-10, Table 4-11, Table 4-15, Pin FMA for Devices Short-Circuited to VSS, Table 4-20 and Table 4-21)

Table 4-2 through Table 4-21 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
В	No device damage, but loss of functionality
С	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 TMUX4051-Q1: TSSOP and SOT-23-THIN Packages

Figure 4-1 and Figure 4-2 show the TMUX4051-Q1 pin diagram for the TSSOP and SOT-23-THIN packages. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMUX405x-Q1 data sheet.

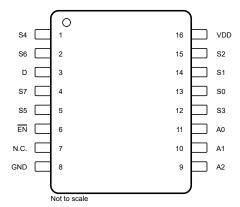


Figure 4-1. Pin Diagram (TSSOP) Package

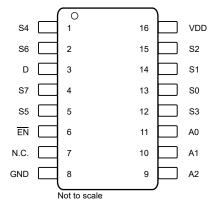


Figure 4-2. Pin Diagram SOT-23-THIN Package



Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
EN	6	EN stuck low. Can no longer disable the device without power down.	В
VSS	7	There is no effect; this is normal operation, if the switch path signal voltages are positive. Possible damage to the device if the switch path signal voltages are negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	No effect, normal operation.	D
A2	9	Address stuck low. Cannot control switch states.	В
A1	10	Address stuck low. Cannot control switch states.	В
A0	11	Address stuck low. Cannot control switch states.	В
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α

Table 4-3. Pin FMA for Device Open-Circuited

Table 4-6.1 III I MA for Device Open-on culted			
Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin.	В
S6	2	Corruption of the signal passed onto the D pin.	В
D	3	Corruption of the signal passed onto the S pins.	В
S7	4	Corruption of the signal passed onto the D pin.	В
S5	5	Corruption of the signal passed onto the D pin.	В
EN	6	Loss of control of the EN pin. Cannot turn off the device.	В
VSS	7	Device is unpowered and not functional.	В
GND	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	А
A2	9	Control of the address pin is lost. Cannot control switch.	В
A1	10	Control of the address pin is lost. Cannot control switch.	В
A0	11	Control of the address pin is lost. Cannot control switch.	В
S3	12	Corruption of the signal passed onto the D pin.	В
S0	13	Corruption of the signal passed onto the D pin.	В
S1	14	Corruption of the signal passed onto the D pin.	В
S2	15	Corruption of the signal passed onto the D pin.	В
VDD	16	Device is unpowered. Device is not functional.	В



Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

	Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin			
Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class	
1	S6	Possible corruption of the signal passed onto the D pin.	В	
2	D	Possible corruption of the signal passed onto the SX and D pin.	В	
3	S7	Possible corruption of the signal passed onto the SX and D pin.	В	
4	S5	Possible corruption of the signal passed onto the D pin.	В	
5	EN	Possible corruption of the signal passed onto the D pin. Switch state will be undefined.	В	
6	VSS	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А	
7	GND	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А	
8	A2	Not considered, corner pin.	D	
9	A1	Control of the address pin is lost. Cannot control switch.	В	
10	A0	Control of the address pin is lost. Cannot control switch.	В	
11	S3	Control of the address pin is lost. Cannot control switch.	В	
12	S0	Corruption of the signal passed onto the D pin.	В	
13	S1	Corruption of the signal passed onto the D pin.	В	
14	S2	Corruption of the signal passed onto the D pin.	В	
15	VDD	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α	
16	S4	Not considered, corner pin.	D	
	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	Pin No. to 1 S6 2 D 3 S7 4 S5 5 EN 6 VSS 7 GND 8 A2 9 A1 10 A0 11 S3 12 S0 13 S1 14 S2 15 VDD	Pin No. to Description of Potential Failure Effect(s) 1 S6 Possible corruption of the signal passed onto the D pin. 2 D Possible corruption of the signal passed onto the SX and D pin. 3 S7 Possible corruption of the signal passed onto the SX and D pin. 4 S5 Possible corruption of the signal passed onto the D pin. 5 EN Possible corruption of the signal passed onto the D pin. Switch state will be undefined. Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible. Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible. Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible. Not considered, corner pin. Not considered, corner pin. Control of the address pin is lost. Cannot control switch. Control of the address pin is lost. Cannot control switch. Control of the address pin is lost. Cannot control switch. Corruption of the signal passed onto the D pin. S1 Corruption of the signal passed onto the D pin. Corruption of the signal passed onto the D pin. Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	



Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck high. Can no longer enable the device.	В
VSS	7	Device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
GND	8	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A2	9	Address stuck high. Cannot control switch.	В
A1	10	Address stuck high. Cannot control switch.	В
A0	11	Address stuck high. Cannot control switch.	В
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	No effect, normal operation.	D



Table 4-6. Pin FMA for Device Pins Short-Circuited to VSS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
VSS	7	No effect, normal operation.	D
GND	8	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	Α
A2	9	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A1	10	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A0	11	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α



4.2 TMUX4051-Q1: WQFN Package

Figure 4-3 shows the TMUX405x-Q1 pin diagram for the WQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMUX405x-Q1 data sheet.

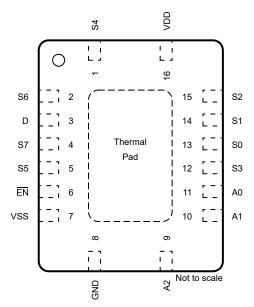


Figure 4-3. Pin Diagram (WQFN Package)



Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S 7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck low. Can no longer disable the device without power down	В
VSS	7	There is no effect; this is normal operation, if the switch path signal voltages are positive. Possible damage to the device if the switch path signal voltages are negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	No effect, normal operation	D
A2	9	Address stuck low. Cannot control switch.	В
A1	10	Address stuck low. Cannot control switch.	В
A0	11	Address stuck low. Cannot control switch.	В
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
Thermal Pad	-	No effect, normal operation.	D



Table 4-8. Pin FMA for Device Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin.	В
S6	2	Corruption of the signal passed onto the D pin.	В
D	3	Corruption of the signal passed onto the S pins.	В
S7	4	Corruption of the signal passed onto the D pin.	В
S5	5	Corruption of the signal passed onto the D pin.	В
EN	6	Loss of control of the EN pin. Cannot turn off the device.	В
VSS	7	Device is unpowered and not functional.	В
GND	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	Α
A2	9	Control of the address pin is lost. Cannot control switch.	В
A1	10	Control of the address pin is lost. Cannot control switch.	В
A0	11	Control of the address pin is lost. Cannot control switch.	В
S3	12	Corruption of the signal passed onto the D pin.	В
S0	13	Corruption of the signal passed onto the D pin.	В
S1	14	Corruption of the signal passed onto the D pin.	В
S2	15	Corruption of the signal passed onto the D pin.	В
VDD	16	Device is unpowered. Device is not functional.	В
Thermal Pad	-	No effect, normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	S6	Possible corruption of the signal passed onto the D pin.	В
S6	2	D	Possible corruption of the signal passed onto the SX and D pin.	В
D	3	S7	Possible corruption of the signal passed onto the SX and D pin.	В
S7	4	S5	Possible corruption of the signal passed onto the D pin.	В
S5	5	EN	Possible corruption of the signal passed onto the D pin. Switch state will be undefined.	В
EN	6	VSS	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
VSS	7	GND	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	A2	Not considered, corner pin.	D
A2	9	A1	Control of the address pin is lost. Cannot control switch.	В
A1	10	A0	Control of the address pin is lost. Cannot control switch.	В
A0	11	S3	Control of the address pin is lost. Cannot control switch.	В
S3	12	S0	Corruption of the signal passed onto the D pin.	В
S0	13	S1	Corruption of the signal passed onto the D pin.	В
S1	14	S2	Corruption of the signal passed onto the D pin.	В
S2	15	VDD	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	S4	Not considered, corner pin.	D
Thermal Pad	-	N/A	Not considered, thermal pad.	D



Table 4-10. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck high. Can no longer enable the device.	В
VSS	7	Device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
GND	8	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A2	9	Address stuck high. Cannot control switch.	В
A1	10	Address stuck high. Cannot control switch.	В
A0	11	Address stuck high. Cannot control switch.	В
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	No effect, normal operation.	D
Thermal Pad	-	No connect pin electrically floating, no effect.	D



Table 4-11. Pin FMA for Device Pins Short-Circuited to VSS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S4	1	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S6	2	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
D	3	Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S 7	4	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S5	5	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
VSS	7	No effect, normal operation.	D
GND	8	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	Α
A2	9	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A1	10	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A0	11	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
S3	12	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0	13	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1	14	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2	15	Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
Thermal Pad	-	No connect pin electrically floating, no effect.	D

4.3 TMUX4052-Q1: TSSOP and SOT-23-THIN Packages

Figure 4-4 and Figure 4-5 show the TMUX4052-Q1 pin diagram for the TSSOP and SOT-23-THIN packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMUX405x-Q1 data sheet.

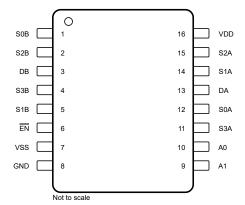


Figure 4-4. Pin Diagram (TSSOP) Package

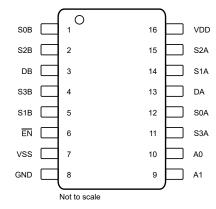


Figure 4-5. Pin Diagram (SOT-23-THIN) Package



Table 4-12. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2B	2	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DB	3	Corruption of signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S3B	4	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1B	5	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck low. Can no longer disable the device without power down.	В
VSS	7	There is no effect; this is normal operation, if the switch path signal voltages are positive. Possible damage to the device if the switch path signal voltages are negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
GND	8	No effect, normal operation.	D
A1	9	Address stuck low. Cannot control switch.	В
A0	10	Address stuck low. Cannot control switch.	В
S3A	11	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S0A	12	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DA	13	Corruption of signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S1A	14	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
VDD	16	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α



Table 4-13. Pin FMA for Device Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of the signal passed onto the DB pin.	В
S2B	2	Corruption of the signal passed onto the DB pin.	В
DB	3	Corruption of the signal passed onto the SxB pins.	В
S3B	4	Corruption of the signal passed onto the DB pin.	В
S1B	5	Corruption of the signal passed onto the DB pin.	В
EN	6	Loss of control of the EN pin. Cannot turn off the device.	В
VSS	7	Device is unpowered and not functional.	В
GND	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	А
A1	9	Control of the address pin is lost. Cannot control switch.	В
A0	10	Control of the address pin is lost. Cannot control switch.	В
S3A	11	Corruption of the signal passed onto the DA pin.	В
S0A	12	Corruption of the signal passed onto the DA pin.	В
DA	13	Corruption of the signal passed onto the SxA pins.	В
S1A	14	Corruption of the signal passed onto the DA pin.	В
S2A	15	Corruption of the signal passed onto the DA pin.	В
VDD	16	Device is unpowered. Device is not functional.	В

Table 4-14. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	S2B	Possible corruption of the signal passed onto the DB pin.	В
S2B	2	DB	Possible corruption of the signal passed onto the SxB and DB pin.	В
DB	3	S3B	Possible corruption of the signal passed onto the SxB and DB pin.	В
S3B	4	S1B	Possible corruption of the signal passed onto the DB pin.	В
S1B	5	EN	Possible corruption of the signal passed onto the DB pin. Switch state will be undefined.	В
EN	6	VSS	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	A
VSS	7	GND	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	A1	Not considered, corner pin.	D
A1	9	A0	Control of the address pin is lost. Cannot control switch.	В
A0	10	S3A	Possible corruption of the signal passed onto the DA pin. Control of the address pin is lost. Cannot control switch.	В
S3A	11	S0A	Possible corruption of the signal passed onto the DA pin.	В
S0A	12	DA	Possible corruption of the signal passed onto the SxA and DA pin.	В
DA	13	S1A	Possible corruption of the signal passed onto the SxA and DA pin.	В
S1A	14	S2A	Possible corruption of the signal passed onto the DA pin.	В
S2A	15	VDD	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	S0B	Not considered, corner pin.	D



Table 4-15. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SOB	1	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2B	2	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DB	3	Corruption of signal passed onto the SxB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S3B	4	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1B	5	Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck high. Can no longer enable the device.	В
VSS	7	Device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
GND	8	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A1	9	Address stuck high. Cannot control switch.	В
A0	10	Address stuck high. Cannot control switch.	В
S3A	11	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0A	12	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DA	13	Corruption of signal passed onto the SxA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1A	14	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	No effect, normal operation.	D



Table 4-16. Pin FMA for Device Pins Short-Circuited to VSS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2B	2	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DB	3	Corruption of the signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S3B	4	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1B	5	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
VSS	7	No effect, normal operation.	D
GND	8	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	Α
A1	9	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A0	10	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
S3A	11	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0A	12	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DA	13	Corruption of the signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1A	14	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α



4.4 TMUX4052-Q1: WQFN Package

Figure 4-6 shows the TMUX4052-Q1 pin diagram for the WQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMUX405x-Q1 data sheet.

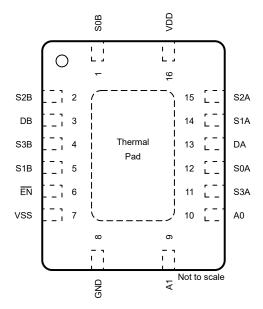


Figure 4-6. Pin Diagram (WQFN Package)



Table 4-17. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Pin No. Description of Potential Failure Effect(s)	
S0B	1	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S2B	2	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DB	3	Corruption of the signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S3B	4	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1B	5	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	EN stuck low. Can no longer disable the device without power down.	В
VSS	7	There is no effect; this is normal operation, if the switch path signal voltages are positive. Possible damage to the device if the switch path signal voltages are negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	No effect, normal operation.	D
A1	9	Address stuck low. Cannot control switch.	В
A0	10	Address stuck low. Cannot control switch.	В
S3A	11	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0A	12	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DA	13	Corruption of the signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1A	14	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
Thermal Pad	-	No effect, normal operation.	D



Table 4-18. Pin FMA for Device Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of the signal passed onto the DB pin.	В
S2B	2	Corruption of the signal passed onto the DB pin.	В
DB	3	Corruption of the signal passed onto the SxB pins.	В
S3B	4	Corruption of the signal passed onto the DB pin.	В
S1B	5	Corruption of the signal passed onto the DB pin.	В
EN	6	Loss of control of the EN pin. Cannot turn off the device.	В
VSS	7	Device is unpowered and not functional.	В
GND	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	А
A1	9	Control of the address pin is lost. Cannot control switch.	В
A0	10	Control of the address pin is lost. Cannot control switch.	В
S3A	11	Corruption of the signal passed onto the DA pin.	В
S0A	12	Corruption of the signal passed onto the DA pin.	В
DA	13	Corruption of the signal passed onto the SxA pin.	В
S1A	14	Corruption of the signal passed onto the DA pin.	В
S2A	15	Corruption of the signal passed onto the DA pin.	В
VDD	16	Device is unpowered. Device is not functional.	В
Thermal Pad	-	No effect, normal operation.	D

Table 4-19. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	S2B	Possible corruption of the signal passed onto the DB pin	В
S2B	2	DB	Possible corruption of the signal passed onto the SxB and DB pin.	В
DB	3	S3B	Possible corruption of the signal passed onto the SxB and DB pin.	В
S3B	4	S1B	Possible corruption of the signal passed onto the DB pin	В
S1B	5	EN	Possible corruption of the signal passed onto the DB pin. Switch state will be undefined.	В
EN	6	VSS	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
VSS	7	GND	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
GND	8	A1	Not considered, corner pin.	D
A1	9	A0	Control of the address pin is lost. Cannot control switch.	В
A0	10	S3A	Possible corruption of signal passed onto the DA pin. Control of the address pin is lost. Cannot control switch.	В
S3A	11	S0A	Possible corruption of signal passed onto the DA pin.	В
S0A	12	DA	Corruption of the signal passed onto the SxA and DA pin.	В
DA	13	S1A	Corruption of the signal passed onto the SxA and DA pin.	В
S1A	14	S2A	Corruption of the signal passed onto the DA pin.	В
S2A	15	VDD	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	S4	Not considered, corner pin.	D
Thermal Pad	-	N/A	Not considered, thermal pad.	D



Table 4-20. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S2B	2	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
DB	3	Corruption of the signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible.	А
S3B	4	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1B	5	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
EN	6	EN stuck high. Can no longer enable the device.	В
VSS	7	Device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
GND	8	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
A1	9	Address stuck high. Cannot control switch.	В
A0	10	Address stuck high. Cannot control switch.	В
S3A	11	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S0A	12	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
DA	13	Corruption of the signal passed onto the SxA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
S1A	14	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	А
VDD	16	No effect, normal operation.	D
Thermal Pad	-	No connect pin electrically floating, no effect.	D



Table 4-21. Pin FMA for Device Pins Short-Circuited to VSS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
S0B	1	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2B	2	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DB	3	Corruption of the signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S3B	4	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	
S1B	5	Corruption of the signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
EN	6	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
VSS	7	No effect, normal operation.	D
GND	8	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	Α
A1	9	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
A0	10	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	Α
S3A	11	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S0A	12	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
DA	13	Corruption of the signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S1A	14	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
S2A	15	Corruption of the signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible.	Α
VDD	16	Possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be possible.	А
Thermal Pad	-	No connect pin electrically floating, no effect.	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2024, Texas Instruments Incorporated