Functional Safety Information

LMP860x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LMP860x-Q1 (8-Pin SOIC and 8-Pin VSSOP packages) to aid in a functional safety system design. This document applies to the following devices:

- LMP8601-Q1
- LMP8602-Q1
- LMP8603-Q1

Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

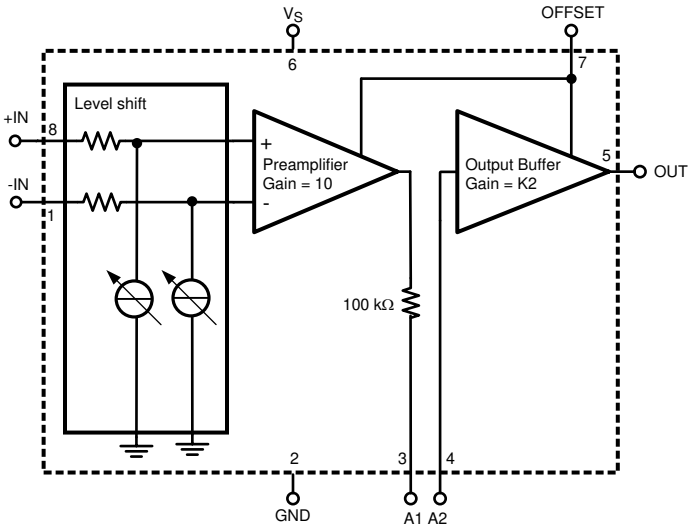

Figure 1-1. Functional Block Diagram

LMP860x-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LMP860x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)	
	8-Pin SOIC	8-Pin VSSOP
Total component FIT rate	9	6
Die FIT rate	2	2
Package FIT rate	7	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 8mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS BICMOS analog or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMP860x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	5
OUT stuck (High or Low)	5
OUT functional, not in specification	30
Preamplifier output A1 open (Hi-Z)	5
Preamplifier output A1 stuck (High or Low)	15
Preamplifier output A1 functional, not in specification	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMP860x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to Vs (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 8-Pin SOIC and 8-Pin VSSOP Packages

Figure 4-1 shows the LMP860x-Q1 pin diagram for the 8-Pin SOIC package. Figure 4-2 shows the LMP860x-Q1 pin diagram for the 8-Pin VSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMP860x-Q1 datasheets.

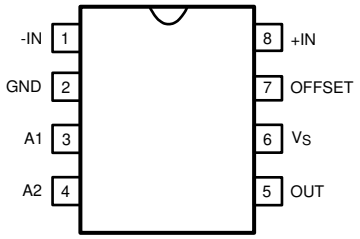

Figure 4-1. Pin Diagram (8-Pin SOIC) Package

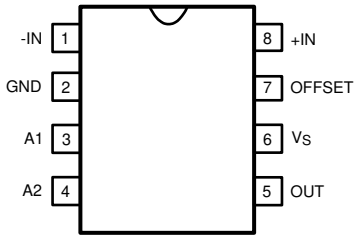

Figure 4-2. Pin Diagram (8-Pin VSSOP Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
–IN	1	In a high-side configuration, a short from the bus supply to GND occurs (through RSHUNT). High current flows from the bus supply to GND. The shunt can be damaged. In a low-side configuration, The device operates as normal.	B for high-side D for low-side
GND	2	The device operates as normal.	D
A1	3	The preamplifier output is pulled down to GND and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
A2	4	The input-to-output amplifier is shorted to ground, the output is stuck.	B
OUT	5	The output is pulled down to GND and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
V_S	6	The power supply is shorted to GND.	B
OFFSET	7	The output of the DC offset is equal to GND.	D if OFFSET=GND by design C otherwise
+IN	8	In a high-side configuration, a short from the bus supply to GND occurs.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
–IN	1	The shunt resistor is not connected to the amplifier. The IN+ pin can float to an unknown value. The output goes to an unknown value, not to exceed Vs or GND.	B
GND	2	There is no power to the device. The device can be biased through inputs. The output is no longer referenced to GND.	B
A1	3	The preamplifier output can be left open. There is no effect on the device, but the output is not measured.	C
A2	4	The input to the output buffer is floating. The output is not measured.	B
OUT	5	The output can be left open. There is no effect on the device, but the output is not measured.	C
V_S	6	There is no power to device. The device can be biased through inputs. The output is incorrect and close to GND.	B
OFFSET	7	The DC offset is not defined. The output is not referenced to known voltage levels.	B
+IN	8	The shunt resistor is not connected to the amplifier. The IN- pin can float to an unknown value. The output goes to an unknown value, not to exceed Vs or GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
–IN	1	2 – GND	In a high-side configuration, a short from the bus supply to GND occurs (through RSHUNT). High current flows from the bus supply to GND. The shunt can be damaged. In a low-side configuration, the device operates as normal.	B for high-side D for low-side
GND	2	3 – A1	The preamplifier output is pulled down to GND and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
A1	3	4 – A2	The device operates as normal.	D
A2	4	5 – OUT	The output amplifier is bypassed.	C
OUT	5	6 – V_S	The output is pulled to Vs and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
V_S	6	7 – OFFSET	The output of the DC offset is equal to V_S.	D if OFFSET=V_S by design C otherwise
OFFSET	7	8 – +IN	In a high-side configuration, the absolute maximum voltage rating can be violated. In a low-side configuration, the output of the DC offset varies with shunt voltage.	A C
+IN	8	1 – –IN	The inputs are shorted, the output is not measured.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Vs

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
–IN	1	In a high-side configuration, the power supply of the device is shorted to the bus supply (through RSHUNT). In a low-side configuration, the power supply of the device is shorted to GND.	B
GND	2	The power supply is shorted to GND.	B
A1	3	The preamplifier output is shorted to V_S and output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
A2	4	The input-to-output amplifier is shorted to V_S, the output is stuck.	B
OUT	5	The output is pulled to Vs and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
V_S	6	The device operates as normal.	D
OFFSET	7	The output of the DC offset is equal to V_S.	D if OFFSET=V_S by design C otherwise
+IN	8	In a high-side configuration, the power supply of the device is shorted to the bus supply. In a low-side configuration, the power supply of the device is shorted to GND (through RSHUNT).	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

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