Functional Safety Information

TPS22968-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS22968-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

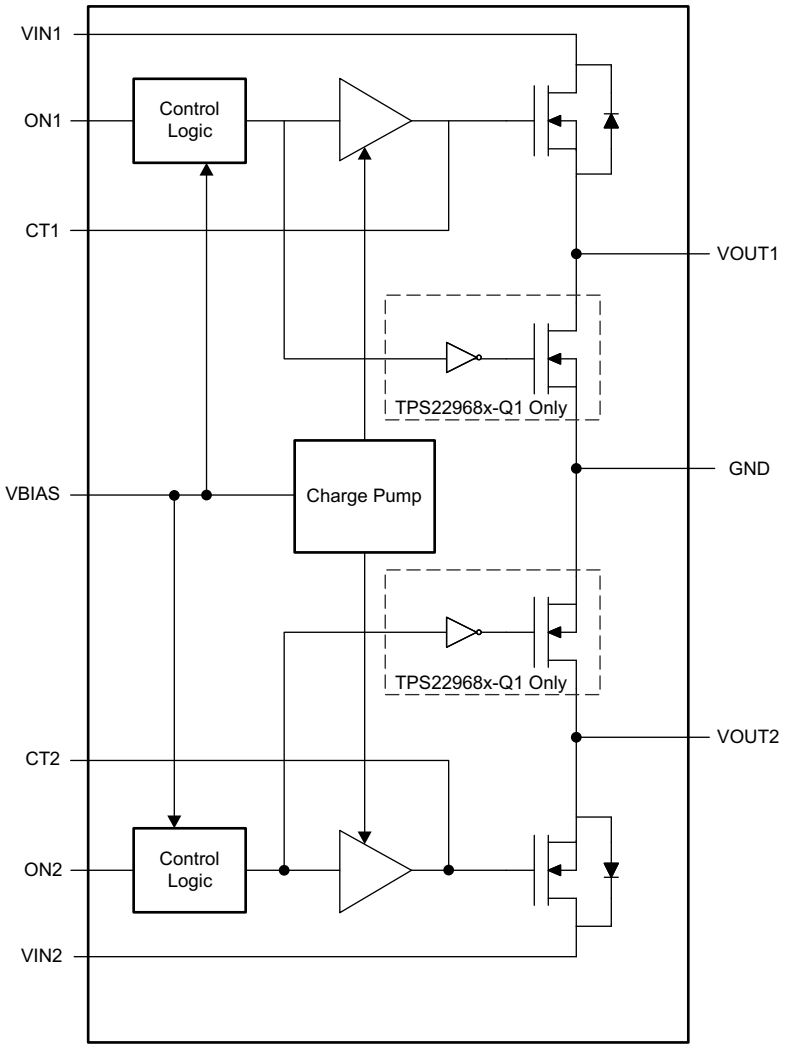

Figure 1-1. Functional Block Diagram

TPS22968-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS22968-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	3
Package FIT rate	3

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS22968-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT to GND	40
VOUT open or Hi-Z	20
VOUT outside specification (voltage or rise time)	30
QOD short to GND	5
Pin to pin short (any two pins)	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS22968-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (see Table 4-5)
- Pin short-circuited to supply (see Table 4-6)

Table 4-3 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The absolute maximum ratings for the device are not exceeded.

Figure 4-1 shows the TPS22968-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS22968-Q1 datasheet.

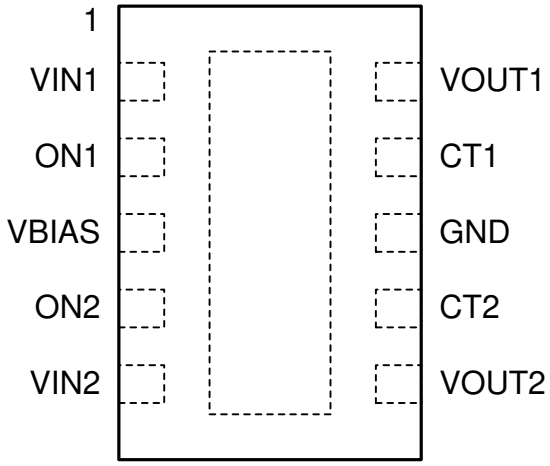

Figure 4-1. Pin Diagram (Top View)

Table 4-2. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND.
2	ON1	I	Active-high switch 1 control input. Do not leave floating.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
4	ON2	I	Active-high switch 2 control input. Do not leave floating.
5	VIN2	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND.
6	VOUT2	O	Switch 2 output.
7	CT2	O	Switch 2 slew rate control. Can be left floating.
8	GND	—	Ground.
9	CT1	O	Switch 1 slew rate control. Can be left floating.

Table 4-2. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
10	VOUT1	O	Switch 1 output.

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN1	1	Channel 1 power supply is shorted.	D
ON1	2	Channel 1 is disabled.	D
VBIAS	3	There is no power supply to the device. The device does not pass through voltage to the VOUT1 or VOUT2 pins.	B
ON2	4	Channel 2 is disabled.	D
VIN2	5	The power supply of Channel 2 is shorted.	D
VOUT2	6	If channel 2 is enabled, the device does not limit power supply current and is damaged.	A
CT2	7	Grounding this pin prevents the device from enabling Channel 2 and potentially damages the device.	A
GND	8	This is the GND pin. Normal operation.	D
CT1	9	Grounding this pin prevents the device from enabling Channel 1 and potentially damages the device.	A
VOUT1	10	If channel 1 is enabled, the device does not limit power supply current and is damaged.	A

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN1	1	There is no power supply to Channel 1. The device does not pass through voltage to the VOUT1 pin.	D
ON1	2	The ON1 pin potentially floats high or low, the state of the output is unknown.	B
VBIAS	3	There is no power supply to the device. The device does not pass through voltage to the VOUT1 or VOUT2 pins.	B
ON2	4	The ON2 pin potentially floats high or low, the state of the output is unknown.	B
VIN2	5	There is no power supply to Channel 2. The device does not pass through voltage to the VOUT2 pin.	D
VOUT2	6	Channel 2 does not deliver the voltage to the load.	D
CT2	7	Opening this pin quickens the Channel 2 rise time if a CT capacitor is attached.	C
GND	8	There is no GND pin connection to the device. The device is not functional.	B
CT1	9	Opening this pin quickens the Channel 2 rise time if a CT capacitor is attached.	C
VOUT1	10	Channel 1 does not deliver the voltage to the load.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIN1	1	ON1	Channel 1 is enabled if the power supply is above the ON threshold (V_{IH}).	D
ON1	2	VBIAS	Channel 1 is enabled if the power supply is above the ON threshold (V_{IH}).	D
VBIAS	3	ON2	Channel 2 is enabled if the power supply is above the ON threshold (V_{IH}).	D
ON2	4	VIN2	Channel 2 is enabled if the power supply is above the ON threshold (V_{IH}).	D
VOUT2	6	CT2	Biasing the CT pin potentially damages the device.	A
CT2	7	GND	Grounding this pin prevents the device from enabling Channel 2 and potentially damages the device.	A
GND	8	CT1	Grounding this pin prevents the device from enabling Channel 1 and potentially damages the device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CT1	9	VOUT1	Biasing the CT pin potentially damages the device.	A

Table 4-6. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN1	1	The device operates normally and as expected.	D
ON1	2	Channel 1 is enabled if the power supply is above the ON threshold (V_{IH}).	D
VBIAS	3	The device operates normally and as expected.	D
ON2	4	Channel 2 is enabled if the power supply is above the ON threshold (V_{IH}).	D
VIN2	5	The device operates normally and as expected.	D
VOUT2	6	The power MOSFET is shorted. Disabling the device no longer blocks power to the VOUT2 pin.	B
CT2	7	Biasing the CT pin potentially damages the device.	A
GND	8	The power supply is shorted.	D
CT1	9	Biasing the CT pin potentially damages the device.	A
VOUT1	10	The power MOSFET is shorted. Disabling the device no longer blocks power to the VOUT1 pin.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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