Application Report

TCA9548A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TCA9548A-Q1 (RGE package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

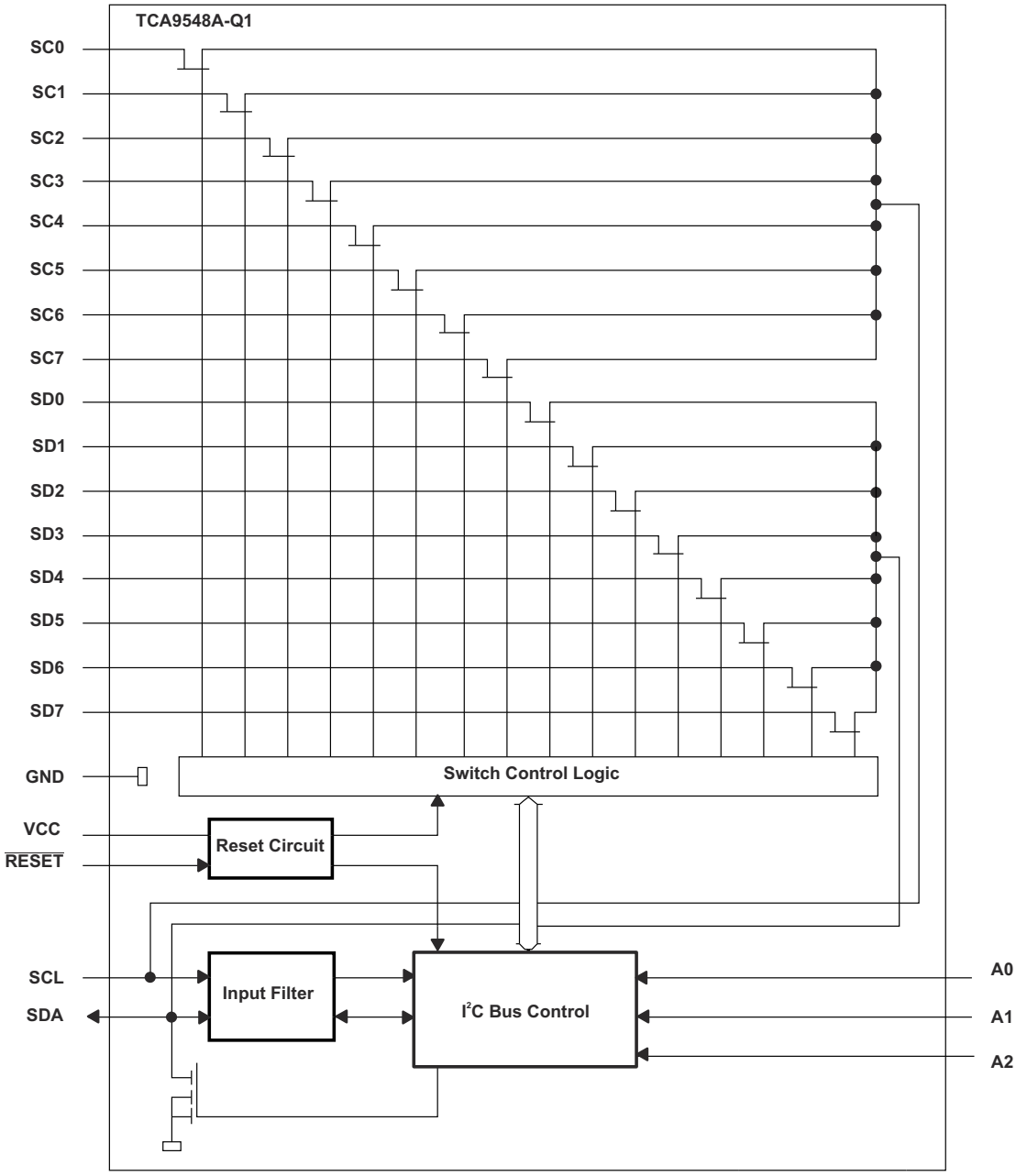

Figure 1-1. Functional Block Diagram

TCA9548A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCA9548A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	2
Package FIT Rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCA9548A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
I2C Control/ communication error	25%
I/O Configuration error	15%
I/O data bit error	60%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCA9548A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TCA9548A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCA9548A-Q1 data sheet.

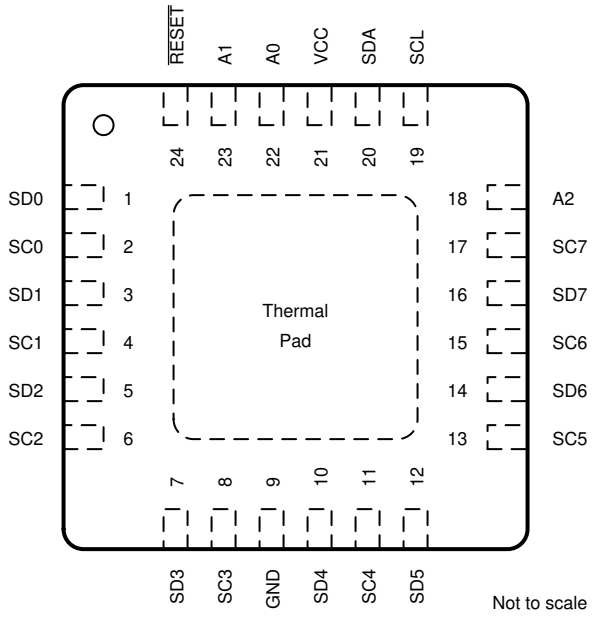

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section

- Assumption1: Reset is tied to Vcc through a pull-up resistor
- Assumption2: All secondary channels have pull-ups resistors to V_{cc}

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SD0	1	If CH0 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC0	2	If CH0 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SD1	3	If CH1 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC1	4	If CH1 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SD2	5	If CH2 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC2	6	If CH2 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SD3	7	If CH3 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC3	8	If CH3 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
GND	9	None	D
SD4	10	If CH4 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC4	11	If CH4 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SD5	12	If CH5 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC5	13	If CH5 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SD6	14	If CH6 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC6	15	If CH6 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SD7	16	If CH7 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
SC7	17	If CH7 is enabled, I2C bus will get stuck. On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality will be lost until PoR or reset pin is toggled.	B
A2	18	If pin is currently biased to GND, no change in performance or damage expected. If pin is biased to V_{CC} with a pull up resistor, then the device address changes. Damage from this short is not expected but some additional leakage current from the pull-up resistor to V_{CC} occurs. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B
SDA	19	On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality is lost due to an I2C stuck bus.	B
SCL	20	On a system level, I2C communication would no longer work but from a device perspective there would not be any expected damage. Functionality is lost due to an I2C stuck bus.	B
V_{CC}	21	V_{cc} short to GND. System level short circuit. Voltage at V_{CC} is unknown in this state.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A0	22	If pin is currently biased to GND, no change in performance or damage expected. If pin is biased to V_{CC} with a pull up resistor, then the device address changes. Damage from this short is not expected but some additional leakage current from the pull-up resistor to V_{CC} occurs. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B
A1	23	If pin is currently biased to GND, no change in performance or damage expected. If pin is biased to V_{CC} with a pull up resistor, then the device address changes. Damage from this short is not expected but some additional leakage current from the pull-up resistor to V_{CC} occusr. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B
#RESET	24	Damage from this short is not expected but some additional leakage current from the pull up resistor to V_{CC} occurs. Device funtionality is lost due to the device being held in the reset state. Device will NACK its address and secondary channels cannot be enabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SD0	1	I2C host is not able to communicate with downstream devices on this channel.	B
SC0	2	I2C host is not able to communicate with downstream devices on this channel.	B
SD1	3	I2C host is not able to communicate with downstream devices on this channel.	B
SC1	4	I2C host is not able to communicate with downstream devices on this channel.	B
SD2	5	I2C host is not able to communicate with downstream devices on this channel.	B
SC2	6	I2C host is not able to communicate with downstream devices on this channel.	B
SD3	7	I2C host is not able to communicate with downstream devices on this channel.	B
SC3	8	I2C host is not able to communicate with downstream devices on this channel.	B
GND	9	Floating GND pin, device may enter an unknown state since body substrates of silicon biased to GND pin is now floating while other pins may be biased.	A
SD4	10	I2C host is not able to communicate with downstream devices on this channel.	B
SC4	11	I2C host is not able to communicate with downstream devices on this channel.	B
SD5	12	I2C host is not able to communicate with downstream devices on this channel.	B
SC5	13	I2C host will not be able to communicate with downstream devices on this channel.	B
SD6	14	I2C host is not able to communicate with downstream devices on this channel.	B
SC6	15	I2C host is not able to communicate with downstream devices on this channel.	B
SD7	16	I2C host is not able to communicate with downstream devices on this channel.	B
SC7	17	I2C host will not be able to communicate with downstream devices on this channel.	B
A2	18	Device address is in an unknown state. I2C host may receive a NACK when trying to communicate with the device intermittently. Signal integrity could also be a concern if device address is no longer uniqueon the I2C bus. Due to a floating input, higher supply current is expected due to shoot-through current.	B
SCL	19	I2C host receives a NACK when trying to communicate with the device. Enabling secondary channels is not possible. Due to a floating input, higher supply current due to shoot-through current.	B
SDA	20	I2C host receives a NACK when trying to communicate with the device. Enabling secondary channels is not possible. Due to a floating input, higher supply current due to shoot-through current.	B
V_{CC}	21	I2C host receives a NACK when trying to communicate with the device. Enabling secondary channels is not possible.	B
A	22	Device address is in an unknown state. I2C host may receive a NACK when trying to communicate with the device intermittently. Signal integrity could also be a concern if device address is no longer unique on the I2C bus. Due to a floating input, higher supply current is expected due to shoot through-current.	B
A1	23	Device address is in an unknown state. I2C host may receive a NACK when trying to communicate with the device intermittently. Signal integrity could also be a concern if device address is no longer uniquev on the I2C bus. Due to a floating input, higher supply current is expected due to shoot-through current.	B
#RESET	24	Device is in an unknown state. I2C host may receive a NACK when trying to communicate with the device intermittently. Device may intermittenly reset, causing secondary channels to be disabled which could occur while communication through the channels is ongoing.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SD0	1	SC0	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC0	2	SD1	Damage to device is unlikely, but functionality is lost if either channel is enabled.	B
SD1	3	SC1	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC1	4	SD2	Damage to device is unlikely, but functionality is lost if either channel is enabled.	B
SD2	5	SC2	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SD3	7	SC3	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC3	8	GND	If this channel is enabled, the I2C bus is stuck until a power cycle occurs or #RESET is toggled. Functionality is lost, but no damage is expected to occur from this kind of short.	B
GND	9	SD4	If this channel is enabled, the I2C bus is stuck until a power cycle occurs or #RESET is toggled. Functionality is lost, but no damage is expected to occur from this kind of short.	B
SD4	10	SC4	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC4	11	SD5	Damage to device is unlikely, but functionality is lost if either channel is enabled.	B
SC5	13	SD6	Damage to device is unlikely, but functionality is lost if either channel is enabled.	B
SD6	14	SC6	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC6	15	SD7	Damage to device is unlikely, but functionality is lost if either channel is enabled.	B
SD7	16	SC7	Damage to device is unlikely, but functionality is lost if the channel is enabled.	B
SC7	17	A2	Device may NACK its address, but functionality may be lost.	B
SCL	19	SDA	I2C bus is compromised. Device is not able to communicate, but no damage is expect from this kind of short.	B
SDA	20	V_{CC}	Damage to device could occur during ACK or read transactions since SDA is directly shorted to V_{CC} and can draw large I_{OL} current which could exceed I_{OL} absolute max. SDA driver could also saturate and VoL could become larger than I2C V_{IL} spec causing a system level NACK seen by the I2C host.	A
Vcc	21	A0	If pin is biased to GND with a pull-up resistor, then the device address is now changed. Damage from this short is not expected but some additional leakage current from the pull-down resistor to GND occurs. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B
A0	22	A1	If A0 and A1 are biased to the same reference voltage, then functionality will continue. If A0 and A1 are biased to different voltage points (like V_{CC} and GND) then a resistor divider forms and floats somewhere close to mid rail assuming the resistors are both the same value. A0 and A1 are in an unknown state and may float to logic high or low intermittenly as noise couples onto the pins. The device may NACK its own address and may also intermittently work. Functionality is affected, but damage to the device is not expected from this short.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A1	23	#RESET	If A1 and #RESET are biased to V_{cc} then no errors should be expected. If A1 is biased to with a pull-down resistor to GND, and #RESET is biased to V_{cc} with a pull-up resistor, then a resistor divider forms and floats somewhere close to mid rail assuming the resistors are both the same value. The device is in an undefined state since #RESET is not above the recommended V_{IH} level and A1 is in an unknown state. The device may NACK its own address and may also intermittently work and stop working and go back into reset mode. Functionality is affected but damage to the device is not expected from this short.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SD0	1	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC0	2	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD1	3	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC1	4	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD2	5	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC2	6	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD3	7	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC3	8	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
GND	9	Short to GND from V_{CC}.	A
SD4	10	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC4	11	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD5	12	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC5	13	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD6	14	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC6	15	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SD7	16	If the channel is enabled, a short between the I2C host or I2C devices through the SDA driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
SC7	17	If the channel is enabled, a short between the I2C host or I2C devices through the SCL driver could occur. The pass-through current the TCA9548A-Q1 device sees may be larger than what it is rated for. Potential damage to the TCA9548A-Q1 or other devices and the I2C host could occur.	A
A2	18	If pin is currently biased to Vcc, no change in performance or damage expect. If pin is biased to GND with a pull-up resistor, then the device address is changed. Damage from this short is not expected but some additional leakage current from the pull-down resistor to GND will occur. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCL	19	SCL is an INPUT so it cannot drive low. No damage is expected to this pin if short to V_{CC}, but the host on the system driving the SCL line may see damage. The V_{OL} could exceed the V_{IL} for this device, and functionality could be lost due to system level issue.	B
SDA	20	Damage to device could occur during ACK or read transactions since SDA is directly shorted to V_{CC}, and can draw large I_{OL} current which could exceed I_{OL} absolute max. SDA driver could also saturate and V_{OL} could become larger than I2C V_{IL} spec causing a system level NACK seen by the I2C host.	A
V_{CC}	21	None	D
A0	22	If pin is currently biased to V_{CC}, no change in performance or damage expected. If pin is biased to GND with a pull-up resistor, then the device address is changed. Damage from this short is not expected, but some additional leakage current from the pull-down resistor to GND occurs. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended.	B
A1	23	If pin is currently biased to V_{CC}, no change in performance or damage expected. If pin is biased to GND with a pull-up resistor, then the device address is changed. Damage from this short is not expected, but some additional leakage current from the pull-down resistor to GND occurs. This causes a functionality issue, where the device will NACK its expected address and potentially ACK if there is another I2C device on the bus with the same address. This could result in signal integrity issues during a read or programming of the device when not intended	B
#RESET	24	Device may not be able to be reset if host tries to toggle it. Functionality is lost if reset toggle is required or used in the system.	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265