Application Note

Phase Compensation and Multi-Device Synchronization with the ADS131M0x

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ABSTRACT

Phase error in power measurement systems, introduced by measurement hardware such as current transformers and signal conditioning circuits, corrupts voltage and current calculations. Even a 0.1° phase error produces a 0.3% measurement error, which accumulates significantly in energy metering applications. The ADS131M0x is a 2-, 3-, 4-, 6-, and 8-channel, simultaneous-sampling, 24-bit delta-sigma ADC family designed for accurate power measurements. This application note targets system designers developing energy metering, motor control, and power quality monitoring systems. It describes how to use the ADS131M0x built-in phase compensation feature to calibrate out phase errors introduced by external measurement hardware, and how to synchronize multiple ADS131M0x devices to eliminate inter-device phase offsets. Following the guidance in this document enables accurate, reliable power measurements in single and multi-device ADS131M0x-based systems.

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Trademarks

1 Introduction

Accurate power measurements in energy metering, motor control, and power quality monitoring systems require precise phase alignment between voltage and current channels. Measurement hardware such as current transformers (CTs), signal conditioning circuits, or ADC timing mismatches can introduce a phase error between these channels, corrupting power calculations.

The ADS131M0x is a 2-, 3-, 4-, 6-, and 8-channel, simultaneous-sampling, 24-bit delta-sigma ADC family designed for accurate power measurements. Two key features address phase error in ADS131M0x-based systems:

- **Phase compensation** - the PHASEn[9:0] bits in the CHn_CFG register apply a programmable phase shift per channel, compensating for phase errors introduced by external measurement hardware.
- **Multi-device synchronization** - higher channel count systems requiring multiple ADS131M0x devices introduce an additional unknown phase shift between devices, even when sharing the same clock source. Simultaneously pulsing the SYNC/RESET pin on all devices eliminates this inter-device phase shift, establishing a common time reference for simultaneous conversions.

This application note explains the sources and impact of phase error, demonstrates how to use the phase compensation feature of the ADS131M08, and describes how to synchronize multiple ADS131M0x devices to eliminate inter-device phase shifts.

2 What is phase shift and phase error?

Phase shift refers to the horizontal shift of a sinewave along the x-axis. Equation 1 specifies the standard sinewave equation centered around the origin with no phase shift:

$$A(t) = A_{max}*\sin(\omega t) \quad (1)$$

Where:

- A_{max} is the max amplitude of the wave
- ωt is the angular frequency of the waveform

Figure 2-1 shows this equation graphically as a single sinewave.

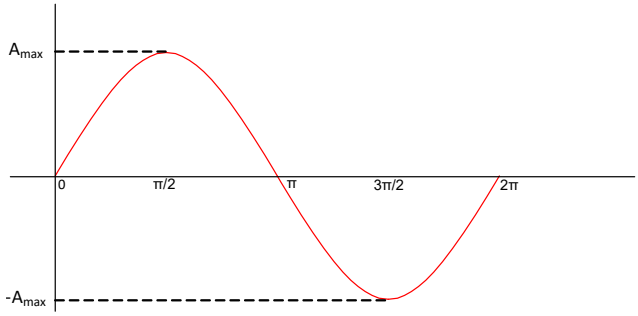

Figure 2-1. Graph of standard Sinewave equation

A phase shift can exist between two measured sinewave signals. This phase shift is denoted by φ and the equation for a sinewave with a phase shift is given by Equation 2:

$$A(t) = A_{max}*\sin(\omega t \pm \varphi) \quad (2)$$

Where:

- A_{max} is the max amplitude of the waveform
- ωt is the angular frequency of the waveform
- φ is the load phase angle between two waveforms in degrees or radians

Figure 2-2 shows two sinewaves plotted with a phase shift of φ between them.

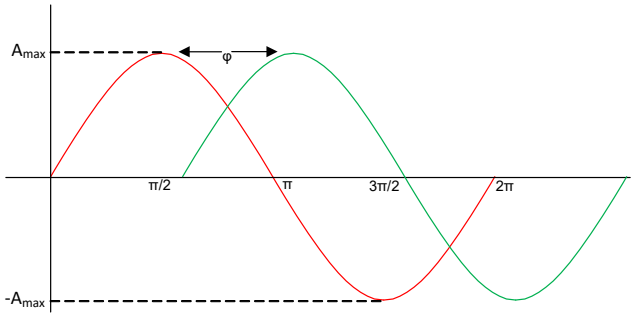

Figure 2-2. Two Sine wave graphs with shift of φ

As an example, a load phase angle can exist between the voltage and current waveforms of a power measurement system. This phase shift breaks into two distinct components:

- Load phase angle (φ) – an expected phase shift caused by the reactive nature of the load. Use the load phase angle to determine the power factor and real power calculation.
- Phase error (Δφ) – an unwanted phase shift introduced by measurement hardware such as CTs, signal conditioning circuits, or ADC timing mismatches. Unlike the load phase angle, this component disrupts the

power measurement and needs to be compensated.component disrupts the power measurement and needs to be compensated.

Figure 2-3 shows typical power measurement systems waveforms, with a green voltage signal V(t) and a red current signal I(t) :

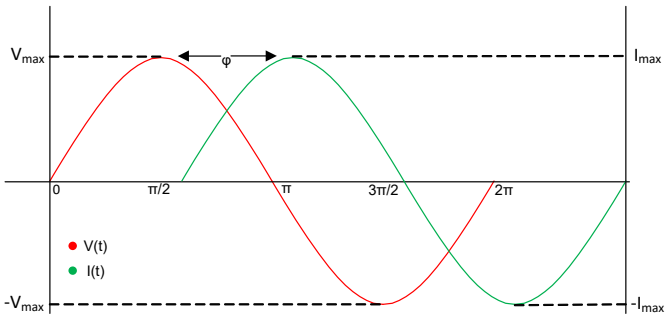

Figure 2-3. Voltage and Current graphs with shift of φ

The signals in Figure 2-3 can be expressed as:

$$3\ V(t) = V_{max}{*}\sin(\omega t) \tag{3}$$

$$4\ I(t) = I_{max}{*}\sin(\omega t - \varphi) \tag{4}$$

Where:

- V_{max} is the max voltage amplitude
- I_{max} is the max current amplitude

Equation 4 shows that the load phase angle is subtracted from the angular frequency ωt – φ. This subtraction shifts I(t) to the right along the x-axis relative to V(t) as shown in Figure 2-3.This relationship is referred to as I(t) lagging V(t) and is common for an inductive load. The phase shift expressed as $(\omega t + \varphi)$ shifts $I(t)$ leftward along the x-axis relative $V(t)$. This relationship is referred to as $I(t)$ leading the $V(t)$ and is common for a capacitive load. In a purely resistive load $\varphi = 0$ and the two waveforms are aligned. As the reactive component of the load increases, φ increases and the misalignment between the waveforms grows.

Equation 5 uses Equation 3 and Equation 4 to calculate instantaneous power - the power at any single point in time:

$$5\ P(t) = V_{max}{*}\sin(\omega t){*}I_{max}{*}\sin(\omega t - \varphi) \tag{5}$$

Equation 5 calculates the ideal instantaneous power with a phase shift resulting from only the load phase angle. As described earlier, however, phase error also contributes to the total phase shift. Equation 6 calculates the instantaneous power with a phase shift resulting from both the load phase angle and phase error:

$$6\ P(t) = V_{max}{*}\sin(\omega t){*}I_{max}{*}\sin(\omega t - \varphi - \Delta\varphi) \tag{6}$$

Where:

- $\Delta\varphi$ is the phase error from the system measurement hardware (7)

Equation 6 provides a power value at a single point in time that will change as the voltage and current waveforms oscillate. Therefore, an actual power measurement system needs to average the instantaneous power over a complete cycle to determine the real power consumed by the load during operation. Averaging Equation 6 over a complete cycle yields the average real power formula shown in Equation 7:

$$7\ P_{real} = V_{rms}{*}I_{rms}{*}\cos(\varphi + \Delta\varphi) \tag{8}$$

A phase error, $\Delta\varphi$, remaining in the system without calibration introduces systematic error into the power measurement. Equation 8 calculates the resulting power measurement error due to the phase error:

$$8\ \text{Error} = \frac{\cos(\varphi + \Delta\varphi) - \cos(\varphi)}{\cos(\varphi)} * 100\% \quad (9)$$

For example, apply Equation 8 to a 50 Hz system with a 0.5 power factor (60° phase angle) to observe the impact of a 0.1° phase error on a power measurement.

$$9\ \text{Error} = \frac{\cos(60 + 0.1) - \cos(60)}{\cos(60)} * 100\% \quad (10)$$

$$9\ \text{Error} = \frac{-0.0015}{0.5} * 100\% \quad (11)$$

$$9\ \text{Error} = -0.3\% \quad (12)$$

A phase error of 0.1° produces a 0.3% measured power error compared to the real power. A phase error of 1° - common among class 1.0 CTs at a power factor of 0.5 -produces a 3% measured power error compared to the real power. Calibrating out the phase error is critical to ensuring accurate power measurements.

3 How to calibrate out phase error with the ADS131M08

The ADS131M08 is an 8-channel, 24-bit, simultaneous-sampling delta-sigma ADC. Subsequent sections use the ADS131M08 as an example, but the information applies to any device in the ADS131M0x family. The ADS131M08 provides a built-in feature to compensate for phase errors introduced by external measurement hardware such as CTs. The PHASEn[9:0] bits in the CHn_CFG register implement the phase compensation. Replace the *n* in PHASE*n*[9:0] with the specific channel number to apply the phase adjustment to that channel. The remainder of this section describes how to calculate the desired phase shift and write to the PHASEn[9:0] bits in the CHn_CFG register.

3.1 Determining the phase error

Determining the system phase error is the first step to implement the ADS131M08 phase compensation feature. CTs, potential transformers (PT), and any front-end circuit including amplifiers and RC filters can introduce phase errors. This application note uses a CT as an example to demonstrate the phase calibration process, but the ADS131M08 phase calibration feature can compensate for any of these error sources. CTs are commonly used to measure AC current in power measurement systems. However, CTs inherently introduce a phase shift between the measured current and the actual current due to the magnetic characteristics of the core. The CT manufacturer typically specifies the phase error in arc minutes or degrees. Table 1 shows the phase error of multiple CT accuracy classes.

Accuracy Class	Phase error in angular minutes	Phase error in degree
0.1	±5 minutes	±0.083°
0.2	±10 minutes	±0.0167°
0.5	±30 minutes	±0.5°
1.0	±60 minutes	±1°
3.0	±180 minutes	±3°

Table 1. Common CT specification by accuracy class

Revenue grade meters use a CT with a 0.2 accuracy class and a ±0.0167° phase error.

3.2 Converting to the time domain

Once the phase error is determined the next step is to convert it to the time domain. Equation 9 shows how to convert the phase error from the CT into the time domain:

$$\Delta t = \frac{\Delta \varphi}{f * 360°} \tag{13}$$

Where:

- Δt is the time delay in seconds
- $\Delta\varphi$ is the phase error from the CT in degrees
- f is the power line frequency usually 50Hz or 60Hz

Assuming a 50Hz power line frequency and applying the CT class 0.2 specifications into equation 9 yields a time shift of 9.28:

$$\Delta t = \frac{0.0167°}{50Hz * 360°} = 9.28\mu s \tag{14}$$

The 9.28µs represents the time shift in the system due to the phase error of a standard class 0.2 CT.

3.3 Converting to modulator clock cycles

Write the phase compensation value to the PHASE*n*[9:0] register as a binary representation of the required modulator clock periods t_{MOD}. Use Equation 10 to calculate t_{MOD} and Equation 11 to calculate the modulator frequency f_{MOD}.

$$10\ t_{MOD} = \frac{1}{f_{MOD}} \quad (15)$$

$$11\ f_{MOD} = \frac{f_{CLK}}{2} \quad (16)$$

Where:

- f_{CLK} is the master clock frequency (usually 8.192 MHz in the ADS131M08 for high resolution mode)
- f_{MOD} is the modulator clock frequency
- t_{MOD} is the modulator clock period

Equation 12 determines the number of modulator clock cycles using the time delay from the CT, Δt and t_{MOD}:

$$12\ N = \frac{\Delta t}{t_{MOD}} \quad (17)$$

Where:

- N is the number of modulator clock cycles that should be written to the PHASEn[9:0] bits in the CHn_CFG register
- Δt is the time delay in seconds from the CT
- t_{MOD} is the modulator clock period

Using the class 0.2 CT time shift of 9.28µs and combining Equations 10, 11, and 12 results in a phase delay equivalent to 38 t_{MOD}:

$$13\ N = \frac{9.28\mu s}{\left(\frac{2}{8.192MHz}\right)} = 38 \quad (18)$$

3.4 Converting to binary and writing to the PHASEn[9:0] bits

The ADS131M08 PHASEn[9:0] bits accept a 10-bit two's complement value that require converting the calculated clock cycles to binary. Using N=38 t_{MOD} from Equation 13, the binary

value is 00 0010 0110b. Additionally, the ADS131M08 oversampling ratio (OSR) impacts phase calibration by defining the range of values that can be written to the PHASEn[9:0] bits. Refer to the Phase Calibration Setting Limits for Different OSR Settings table in the ADS131M08 datasheet to confirm that the number of clock cycles is within the allowable phase shift range for the OSR.

Finally, write the converted binary value to the PHASEn[9:0] bits in the CHn_CFG register over Serial Peripheral Interface (SPI) after completing the previous steps.

3.5 Phase calibration considerations

Some important considerations apply when using the ADS131M08 phase calibration feature. Applications requiring a negative phase shift can write a negative value to the PHASEn[9:0] bits. However, a negative phase shift requires an additional step of setting the DRDY_SEL[1:0] bits in the MODE register. These bits configure $\overline{DRDY}$ to assert based on different channel conditions and availability of conversion data. By default, DRDY_SEL = 00b such that $\overline{DRDY}$ asserts when the channel with the largest positive phase calibration setting has a new conversion result. Leaving DRDY_SEL unchanged while writing a negative value to the PHASEn register causes $\overline{DRDY}$ to trigger without an offset. Set DRDY_SEL = 10b or 11b to $\overline{DRDY}$configure to assert when the channel with the most negative phase calibration setting has new conversion data. Refer to the Data Ready ($\overline{DRDY}$) section of the ADS131M08 datasheet for more information on the DRDY_SEL bits.

The phase calibration feature of the ADS131M08 is disabled when global-chop mode is used. Global-chop mode resets the digital filter of the ADC whenever it changes the input polarity, which disables phase calibration. This is explained in the Global-Chop Mode section of the ADS131M08 datasheet.

Phase shifts larger than half the sample period require specific steps for an OSR less than 2048. Refer to the Channel Phase Calibration section of the ADS131M08 datasheet for these steps.

3.6 Summarizing the phase calibration process

The following steps enable the ADS131M08 phase compensation feature:

1. *Determine the sensor phase error, typically specified in degrees or angular minutes as shown in Table 1.*
2. *Determine the time delay by converting the phase error into the time domain using equation 9.*
3. *Convert the time delay into modulator clock cycles using equations 10, 11, and 12.*
4. *Convert the modulator clock cycles to 10-bit two's complement.*
5. *Write the 10-bit two's complement value to the PHASEn[9:0] bits in the CHn_CFG register corresponding to the target channel. Note: Set DRDY_SEL[1:0] to 10b or 11b when writing a negative phase shift value.*

3.7 Using the Phase Calibration Feature

The following example compares an ADS131M08 channel with phase calibration enabled to one with no programmed phase calibration. Figure 3-1 shows a recreation of the DRDY signals of two ADS131M08 channels: ADS131M08(0) in red and ADS131M08(1) in black.

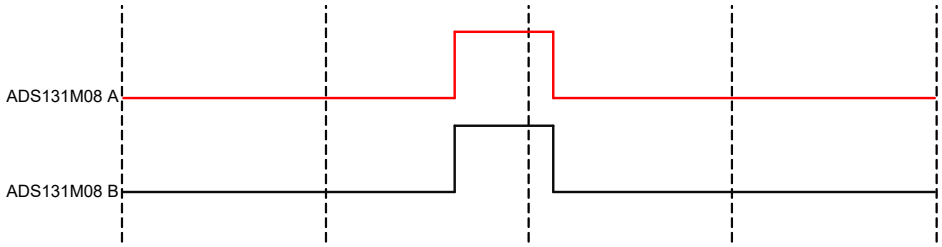

Figure 3-1. DRDY signals for two channels with no phase calibration applied

This $\overline{\text{DRDY}}$ timing difference is the digital equivalent of the waveforms shown in Figure 3-2, where the load phase angle,$\boldsymbol{\varphi}$,and the phase error, $\Delta\varphi$, are both present.

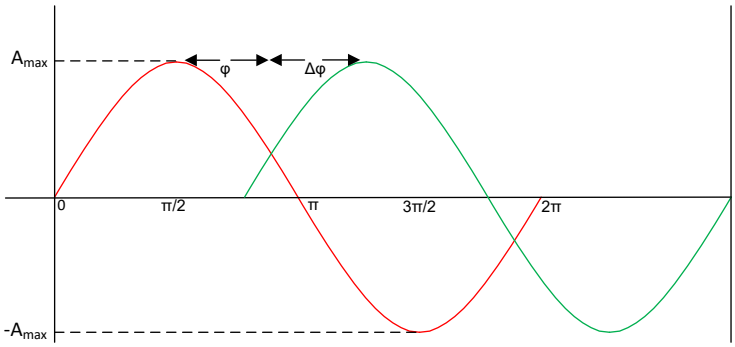

Figure 3-2. two measured signals with shift of $\boldsymbol{\varphi}$ +$\Delta\varphi$

The $\Delta\varphi$ is the unwanted phase error that needs to be removed by applying a phase shift to the ADS131M08 channels.

Assume the 38tMOD (9.28µs) from Equation 13 has been converted to binary and programmed into the PHASE0[9:0] register of ADS131M08(0). Figure 3-3 shows the $\overline{\text{DRDY}}$ signals with a positive phase shift of 9.28µs applied to ADS131M08(0).

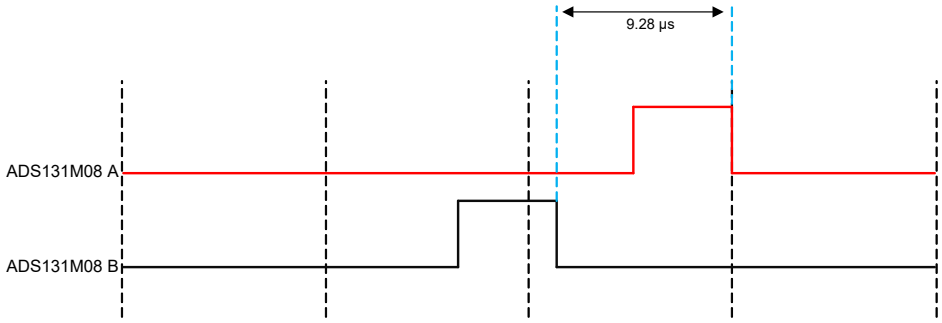

Figure 3-3. DRDY signals for two channels with 9.28µs phase shift applied to channel 0

With the phase error compensated, the resulting signals are corrected. Figure 3-4 shows the two measured signals after phase compensation is applied; the $\Delta\varphi$ component is removed, leaving only the intended load phase angle **φ**.

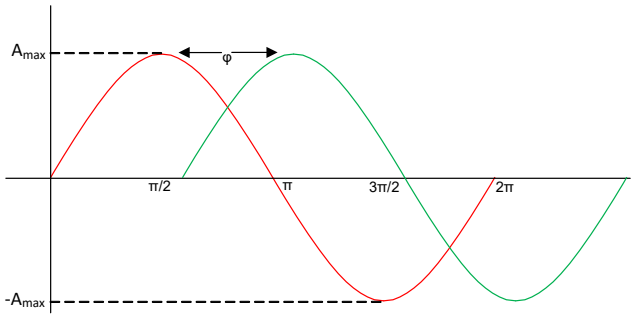

Figure 3-4. two measured signals with shift of φ

3.7.1 Phase calibration considerations examples

Refer to the Phase calibration considerations section for details on writing a negative phase shift. Set the DRDY_SEL[1:0] bit correctly before applying a negative phase shift; otherwise, the $\overline{\text{DRDY}}$ signal will not assert correctly, and the phase shift will appear unimplemented. Figure 3-5 shows a recreation of the result of applying a negative phase shift to ADS131M08(0) from Figure 3-1 without setting DRDY_SEL[1:0] correctly.

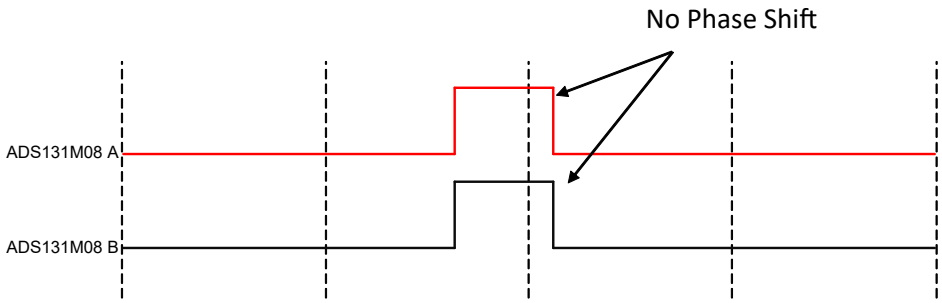

Figure 3-5. DRDY signals with negative phase calibration applied and incorrect DRDY_SEL[1:0] bit

Without the correct DRDY_SEL[1:0] setting, the $\overline{\text{DRDY}}$ signal does not assert correctly, and no phase shift appears between the ADCs. Set DRDY_SEL[1:0] to 10b or 11b so the $\overline{\text{DRDY}}$ signal asserts on the channel with the most negative calibration, accurately reflecting the programmed phase shift. Figure 3-6 shows a recreation of the phase difference between the two $\overline{\text{DRDY}}$ signals from Figure 3-1 with a -9.28 phase shift programmed to ADS131M08(0) and the DRDY_SEL[1:0] bit correctly set.

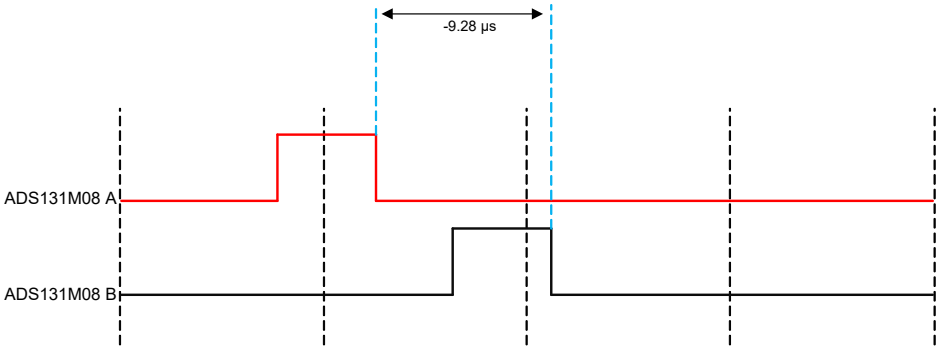

Figure 3-6. DRDY signals with -9.28µs phase calibration applied and correct DRDY_SEL[1:0] bit

4 Synchronizing the ADS131M0x

Phase error can originate from measurement hardware including the ADC when multiple unsynchronized ADCs are used. For example, multi-string solar installations that need higher channel counts require multiple ADS131M08 devices in parallel.

Systems using multiple ADS131M08 devices require ADC synchronization before data collection. Synchronization establishes a common time reference that ensures all ADCs begin conversions simultaneously. This enables accurate phase comparison across channels of different devices. Without synchronization, each device may begin its conversion cycle at an arbitrary time relative to the others, even when sharing the same clock source. This creates an unknown phase shift between devices that calibration cannot reliably compensate. Figure 4-1 shows a re-creation of the DRDY signals of two ADS131M08 devices sharing the same external clock without synchronization. Note the delay between the falling edges of the signals without synchronization.

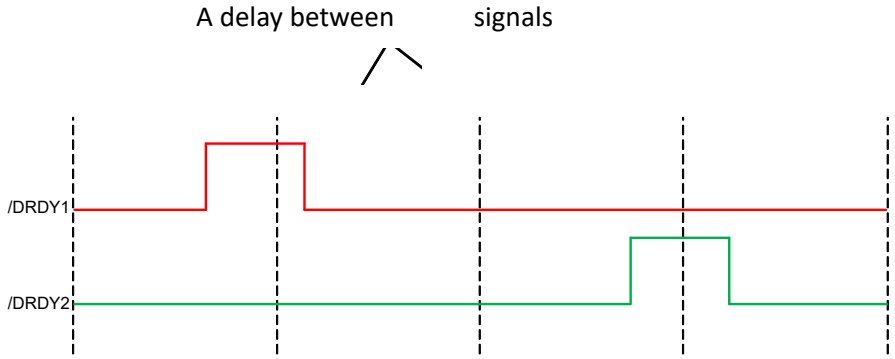

Figure 4-1. DRDY signals between two ADS131M0x with same external clock and without synchronization

4.1 The SYNC/RESET pin on the ADS131M0x

The ADS131M08 provides a SYNC/RESET pin to enable a hardware mechanism that establishes a common time reference across all devices in the system. Simultaneously pulsing the SYNC/RESET low on every ADS131M08 in the system resets each device's internal digital filter, aligning all devices to the SYNC/RESET pulse. In global-chop mode, this synchronization is particularly critical because the device starts conversions immediately upon reset, leaving no delay between the synchronization pulse and the first sample. Synchronization preserves all phase calibration settings, ensuring that previously compensated measurement hardware phase errors (such as those from CTs or amplifiers) remain corrected across all devices. After synchronization, all devices sample their inputs at precisely the same instant, eliminating inter-device phase errors and enabling accurate phase-sensitive measurements. Figure 4-2 shows the signals of two synchronized ADS131M08 devices with no delay between the falling edges.

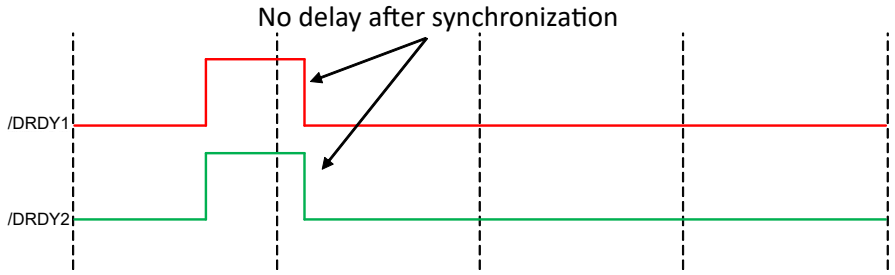

Figure 4-2. DRDY signals between two ADS131M0x with same external clock with synchronization

4.2 The importance of routing the clock signal

All ADCs must sample their respective input signals at the same instant in a multi-ADC simultaneous sampling system. A shared clock signal synchronizes this sampling across all channels. Any mismatch in clock arrival

time between ADCs caused by differences in PCB clock trace lengths introduces a time skew between sampled channels. Two options exist for routing the clock signal: a single clock buffer driving all ADCs, or individual clock buffers from one clock source each driving a separate ADC.

For either clock tree design, short clock trace lengths of no more than 5cm/ns of signal rise time generally do not need a source-termination series resistor. If this clock length is exceeded, source-terminate the clock trace with a series resistor to match the characteristic impedance of the micro-strip trace (minus that of the buffer output impedance). The source termination resistance absorbs reflected energy from the high-impedance clock inputs, keeping this energy from bouncing back to the inputs and reducing noise margin (difference between high or low input logic thresholds). With fast clock drivers, rise time can be much less than 1ns. Over-damping the PCB trace with a larger resistor value to reduce the clock signal overshoot and undershoot can increase the clock signal noise margin.

TI recommends a clock rise time of 1ns to reduce timing variances between multiple ADCs. These timing variances are a result of different logic threshold levels for the clock input due to process tolerances.

4.2.1 Single Clock Buffer

Use a single clock buffer to drive all ADCs in systems with a small number of channels, such as a 4 channel configuration. In a single-clock buffer layout, the PCB traces from the clock buffer to the ADCs must have equal path lengths to minimize sampling skew between the ADCs. Given the typical propagation delay of a micro-strip PCB design is 60ps/cm, a five-cm difference between the clock traces results in 300ps sampling skew between ADCs. This sampling skew appears as an additional 0.3ns of group delay in the input signal and must be included in the measurement error budget when phase angle between channels is important. In addition to sampling skew, matched PCB trace lengths also reduce multiple line reflections from the ADC clock inputs. Multiple line reflections can lead to excessive ringing and overshoot, therefore reducing the clock signal noise margin.

4.2.2 Multiple Clock Buffers

TI recommends using individual clock buffers for each ADC in systems with more than 4 channels. However, clock buffers introduce channel-to-channel clock skew that causes sampling skews between the ADCs. A high speed clock buffer such as LMK1C1104 has a well specified 50ps channel-to-channel output skew specification. General purpose logic buffers often have unspecified or excessively large output skew specifications of several nanoseconds. These general purpose logic buffers can often be used for low clock speeds but must be evaluated for the specific application requirements.

5 Summary

Accurate power measurements require precise phase alignment between voltage and current channels. Even a small phase error between the channels can result in large errors in the final calculations. In energy metering applications these errors accumulate over time and can lead to significant inaccuracies in energy reporting. The ADS131M0x family addresses this challenge with a built-in phase calibration feature. Following the process outlined in this document removes the phase error from of a power measurement system using the phase compensation feature.

Key considerations when implementing phase calibration in the ADS131M0x include:

- disabling global-chop mode with phase calibration
- negative phase shifts require changing the DRDY_SEL[1:0] bits in the MODE register
- phase shifts larger than half the sample period require additional steps

Higher channel count applications requiring multiple ADS131M0x devices also require synchronization. Unsynchronized devices have an unknown phase shift between them even when sharing the same external clock source. Simultaneously pulsing the SYNC/RESET pin on all devices eliminates this inter-device phase shift, establishing a common time reference and ensuring all devices begin conversions at the same instant.

6 References

1. ADS131M08 data sheet

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