Application Note

Optimizing Illumination LED Driver Design for Best Dimming Performance with TPS92205x and TPS92365x

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ABSTRACT

A key challenge in advanced LED lighting design lies in achieving high performance dimming capabilities. Critical requirements for most lighting applications encompass a wide dimming ratio with seamless transition, precise LED current regulation to ensure long-term brightness consistency, and support dynamic lighting effects such as color temperature shift. The TPS92205x and TPS92365x family of 65V, 1-4A Buck/Boost/Buck-Boost LED driver integrates analog, PWM, flexible, and hybrid dimming methods, making them well-suited for both constant and instant illumination applications. This application note addresses methodologies for optimizing dimming performance. First, it introduces innovative dimming control techniques, including inductive fast dimming and inductive pulse dimming; It also shows the experimental results of LED current dimming linearity curve. Furthermore, it offers application-focused guidance on optimizing peripheral circuit design to achieve optimal dimming performance.

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1 Introduction

LED lighting technology has rapidly evolved from simple on/off switching to sophisticated, intelligent illumination systems capable of delivering precise, dynamic, and high-quality light output. As LED drivers are deployed across an increasingly diverse range of applications — from indoor architectural lighting and projectors to machine vision and camera flash systems — the demands placed on dimming performance have grown significantly. Achieving a wide dimming ratio, maintaining accurate LED current regulation, and enabling smooth, flicker-free transitions are now essential requirements for modern lighting designs.

This application note focuses on optimizing dimming performance using the TPS92205x and TPS92365x family of 65V, 1–4A Buck/Boost/Buck-Boost LED drivers. It introduces advanced dimming control techniques, including inductive fast dimming and inductive pulse dimming, examines key factors affecting dimming quality, and provides practical design guidance for peripheral circuit optimization. Experimental results are included to validate the proposed methods and demonstrate the achievable dimming performance improvements.

2 Precise Dimming Control and Enhanced Dimming Ratio

High-power illumination LED drivers, used for single high-power LEDs or series-connected LED strings, are widely used in both constant illumination applications such as indoor/outdoor lighting, projectors, laser TVs, printers and instant illumination scenarios including machine vision, camera flash, fire alarms.

When designing LED lighting systems, particularly for applications demanding high-quality illumination such as professional lighting and smart lighting, several key factors must be considered: power topology selection, dimming methodology, dimming linearity and ratio, efficiency and thermal management. Constant current LED drivers play a crucial role in maintaining consistent brightness and color temperature over time. With the development of smart lighting, enhancing user experience has become increasingly important. Soft dimming is essential to avoid abrupt light changes that may cause visual discomfort. A wider dimming ratio enables finer control over light levels while dynamic lighting effects – such as RGB color mixing and smooth color temperature transitions can help to enrich lighting performance. Beyond simple on/off operation, combining various lights, colors and dimming levels allows the creation of customized lighting scenes. What's more, flicker-free output, typically achieved through higher PWM frequency, is necessary to eliminate flicker-related issues and protect visual comfort.

The TPS92205x and TPS92365x family is a 65V,1-4A Buck/Boost/Buck-Boost LED driver. It supports different dimming methods including PWM dimming, analog dimming, flexible dimming and hybrid dimming. Analog dimming has a continuous output current and can diminish flicker; PWM dimming's output current is discontinuous and there is no LED color temperature shift. In low flickering applications like high-speed camera, to eliminate flicker strips, >20kHz PWM frequency is required.

The latest TI solution TPS92205x and TPS92365x family, enhances lighting performance through advanced technology. With inductive fast diming, error amplifier enables sample hold which can reduce the current settle time. Figure 1-1 compares the waveform of EN/PWM and inductor current (I_L) with and without IFD. Furthermore, inductive pulse dimming can further increase the dimming accuracy and dimming ratio. Under conventional PWM dimming with a very small duty cycle – where the pulse on time is extremely short - the inductor current rising is limited by the inductor's slew rate and the pulse on time, constraining peak current. Inductor pulse dimming addresses this by introducing a predictive pulse extension mechanism, which increases the achievable peak current. Dimming performance is illustrated in Figure1-2, which shows the dimming linearity curves for TPS922053 with hybrid dimming.

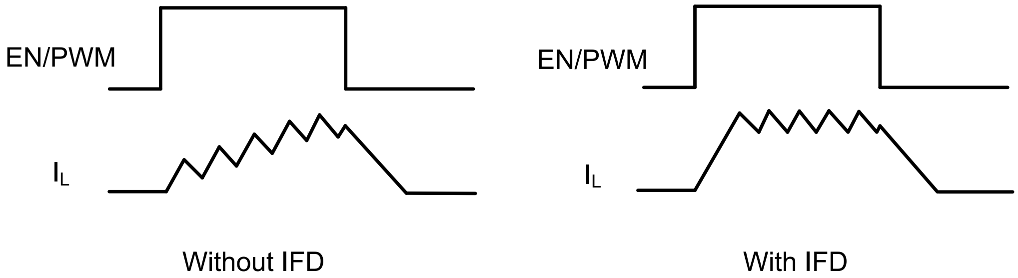

Figure 2-1. Waveform of EN/PWM and I_L With and Without IFD

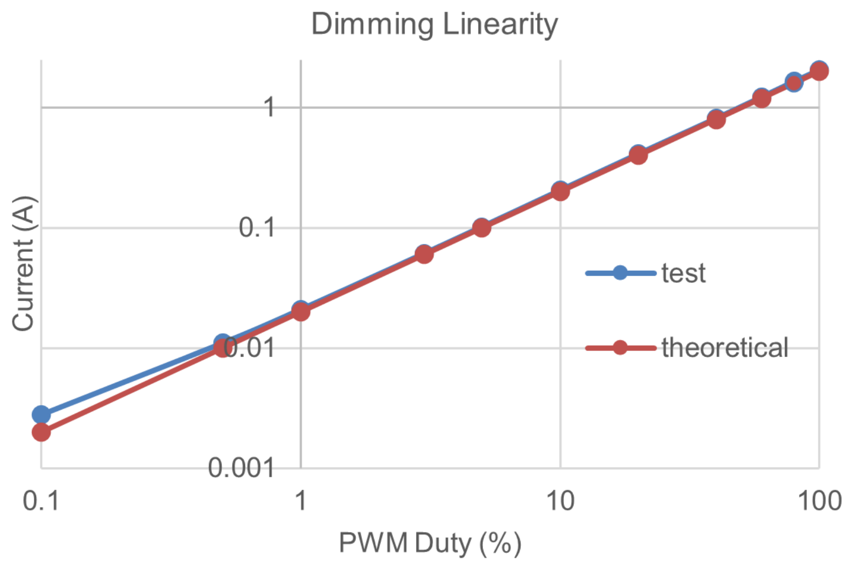

Figure 2-2. Dimming Linearity Curve of TPS922053 With Hybrid Dimming

3 Key Factors for Improved Dimming Performance

Figure 3-1 shows the typical application schematic with TPS92205x. By adjusting the parameters of external components, the dimming performance of the LED driver can be further optimized.

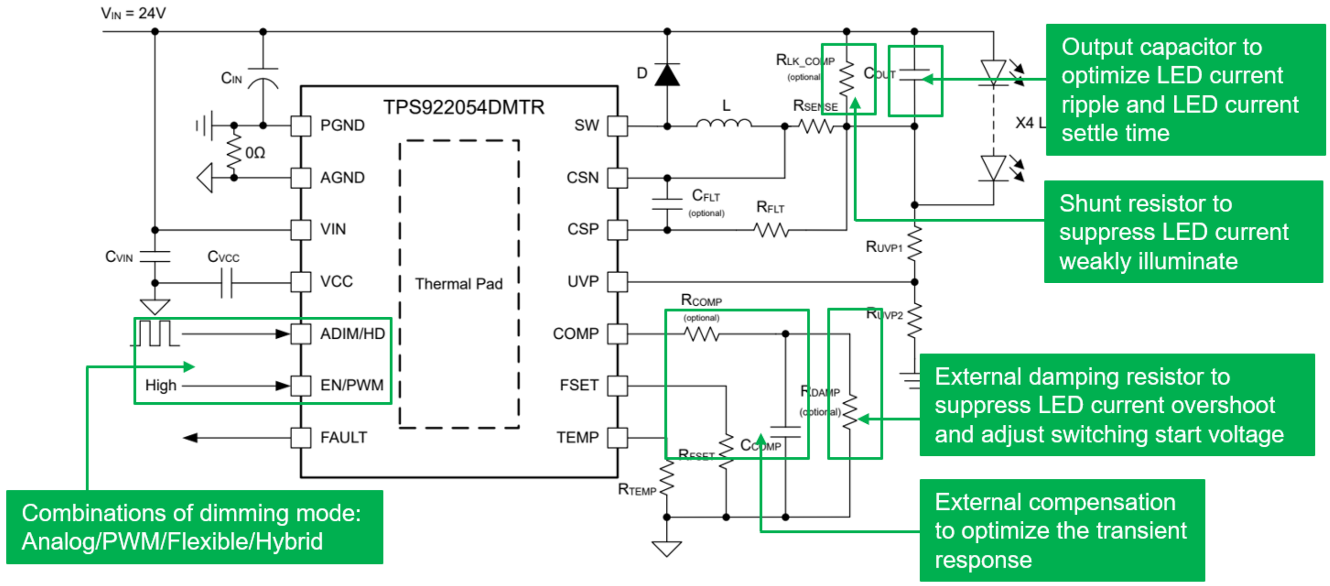

Figure 3-1. Typical Application Schematic With TPS92205x

The TPS92205x and TPS92365x device adopts an adaptive off-time current mode control. Figure 3-2 shows the block diagram. For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins is compared with the internal voltage reference, V_{REF}, through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and is then compared with the peak current feedback at the PWM comparator. During each switching cycle, when the internal NMOS FET is turned on, the peak current is sensed through the internal FET. When the sensed value of peak current reaches V_{COMP} at the input of PWM comparator, the NMOS FET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter is reset until when the NMOS FET stays off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feedforward.

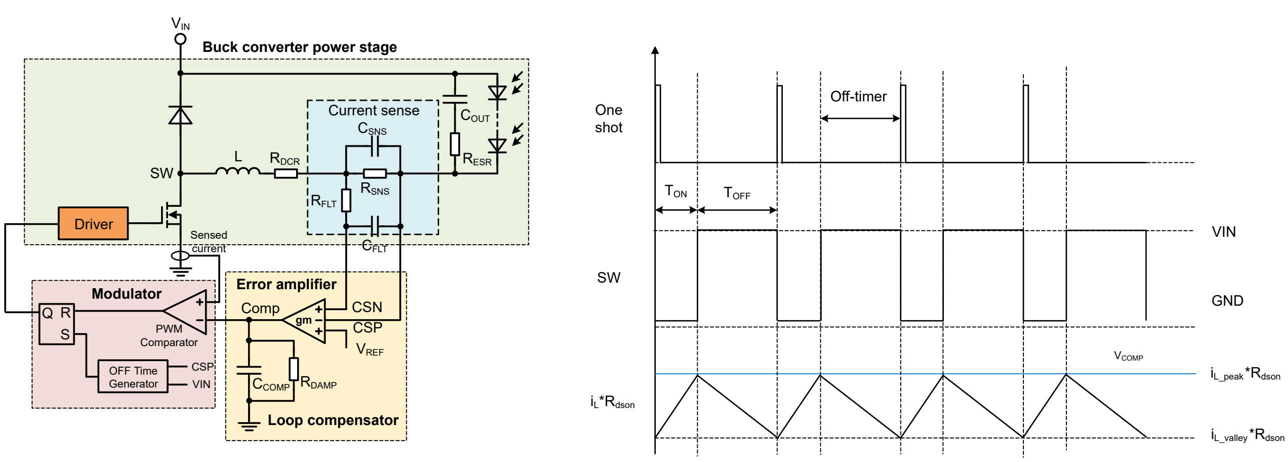

Figure 3-2. Adaptive Off Time Current Mode Control

3.1 LED Current Settling Time Reduction and Overshoot Current Suppression

The output capacitor C_{OUT} reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, thereby increasing the LED temperature. However, increasing the output capacitor also results in a longer edge-to-edge response time (from PWM control to LED current). For applications like DLP projectors and laser TVs, strict requirements exist for the rise and fall time which affects laser driver performance. Figure 3-3 shows the key parameters for laser driver performance.Figure 3-4 and Figure 3-5 show the waveform of EN/PWM, I_L and I_{LED} with effective C_{OUT}=4uF and C_{OUT}=34uF during the rising and falling edges of EN/PWM. Test condition: V_{IN}=24V, 4-pcs WLEDs, 2A maximum LED current and $Freq_{PWM}$=1kHz. With inductive fast dimming, the COMP pin voltage remains nearly constant during PWM off period, allowing the inductor current to rise quickly to the target value when PWM transitions from off to on. Moreover, experimental results show that a larger C_{OUT} leads to a longer LED current settling time.Table 3-1 shows a comparison of rise/fall time for different C_{OUT} values.

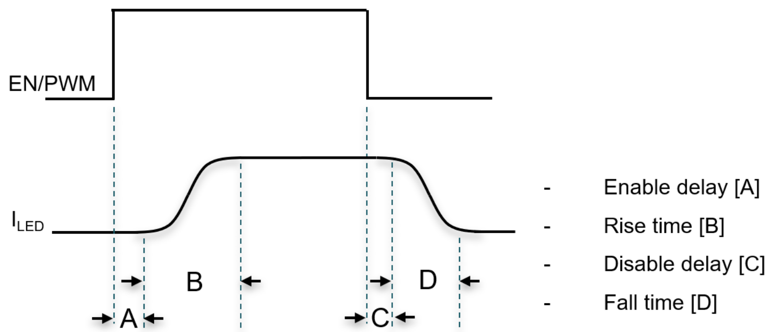

Figure 3-3. Key Parameters of Response Time

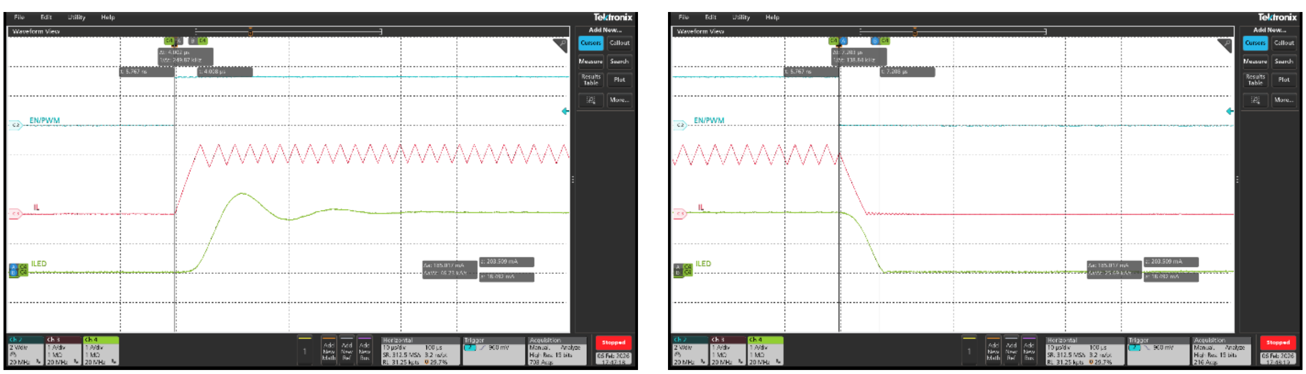

Figure 3-4. Waveform of I_L, SW and I_{LED} with C_{OUT}=4uF

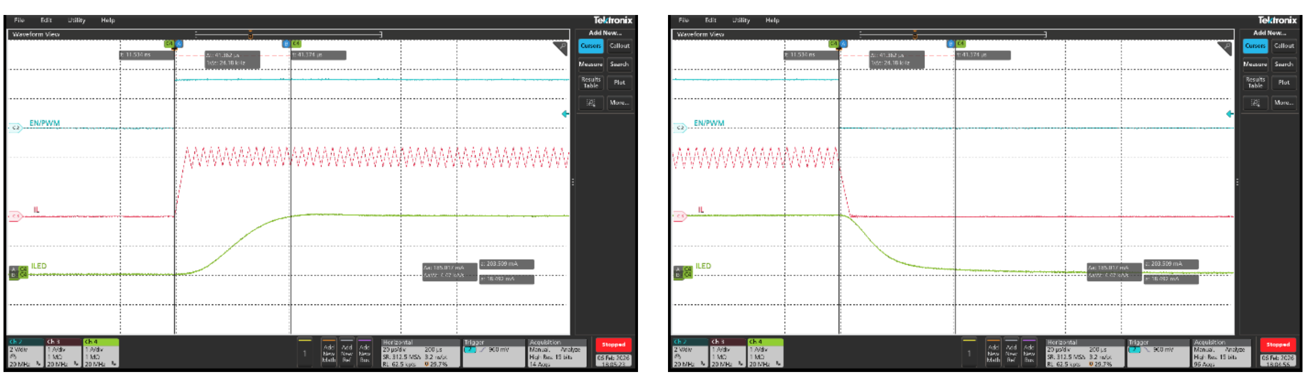

Figure 3-5. Waveform of I_L, SW and I_{LED} with C_{OUT}=34uF

Table 3-1. Rise/Fall Time Comparison of Different C_{OUT}

C_{OUT_eff}	t_{rise}	t_{fall}
34uF	41us	41us
4uF	7us	7us

A simple integral compensator is recommended to achieve stable operation over the wide operating range. Figure 3-6 shows the simulated bode plot of the loop gain and phase margin for different compensation capacitors of TPS922051. Simulation condition: V_{IN}=24V, 6-pcs WLEDs, 2A maximum LED current.

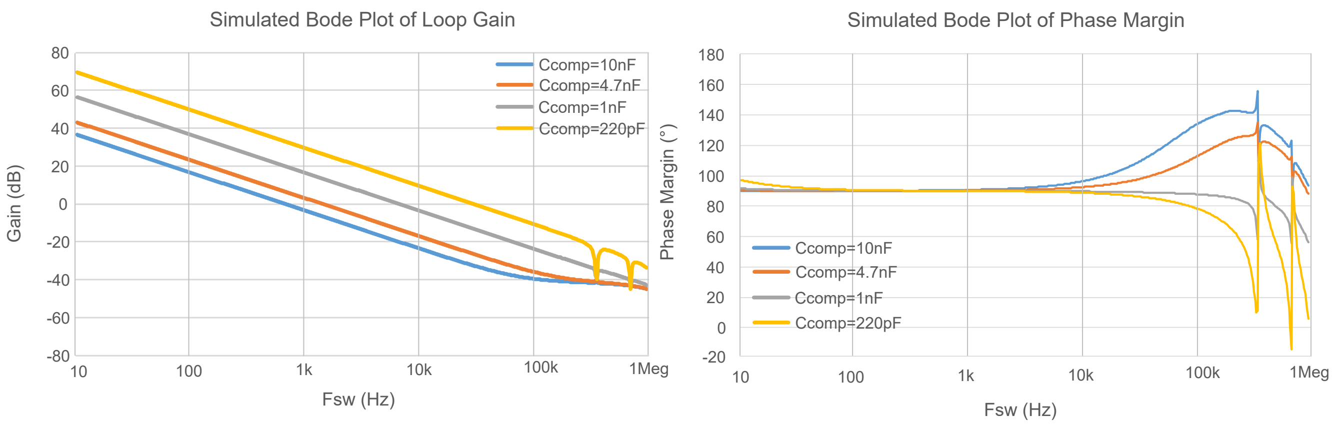

Figure 3-6. Simulated Bode Plot of Loop Gain and Phase Margin

The Buck converter behaves as a single pole system with additional phase lag caused by the switching behavior. The choice of compensation capacitor affects both the transient response and the PWM dimming performance. A larger compensation capacitor (with lower crossover frequency) is recommended to limit the LED current overshoot on the rising edge of PWM signal (PDIM). A smaller compensation capacitor (with higher crossover frequency) is recommended to improve the transient response.

For TPS922051/0, Inductive fast dimming (IFD) is implemented which means that COMP pin voltage remains nearly constant during PWM off period, allowing the inductor current to rise quickly to the target when PWM turns on again.

However, during startup (or when the PWM off time is very long), the comp voltage starts from 0V, reducing the effectiveness of IFD. This explains the longer response time. PWM dimming performance (with long PWM off time) for different C_{COMP} values (220pF, 1nF, 6.8nF) is shown in Figure 3-7, Figure 3-8 and Figure 3-9. Test condition: V_{IN}=24V, 6-pcs WLEDs, 2A maximum LED current, $Freq_{PWM}$=10Hz.

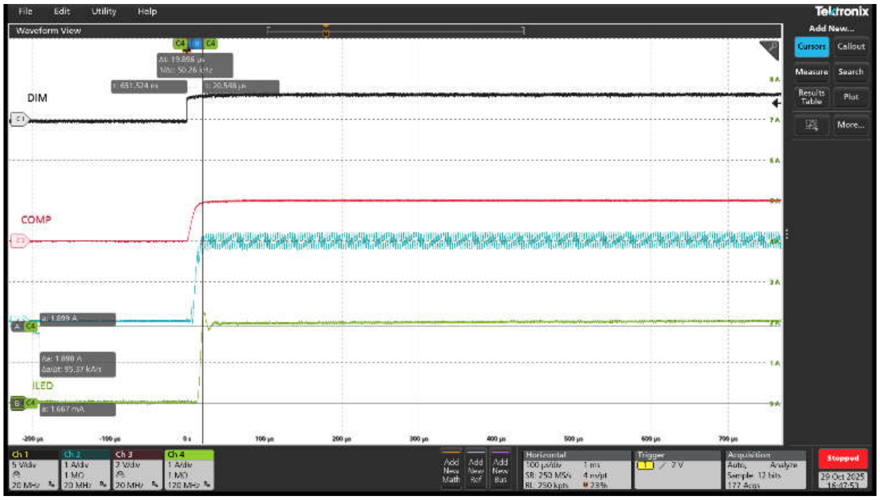

Figure 3-7. Start-up Waveform of DIM, COMP, IL and ILED with C_{COMP}=220pF

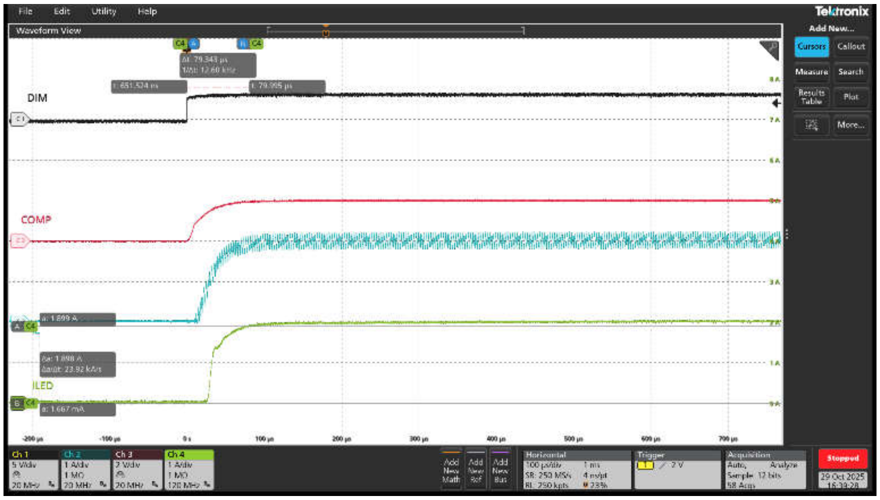

Figure 3-8. Start-up Waveform of DIM, COMP, IL and ILED with C_{COMP}=1nF

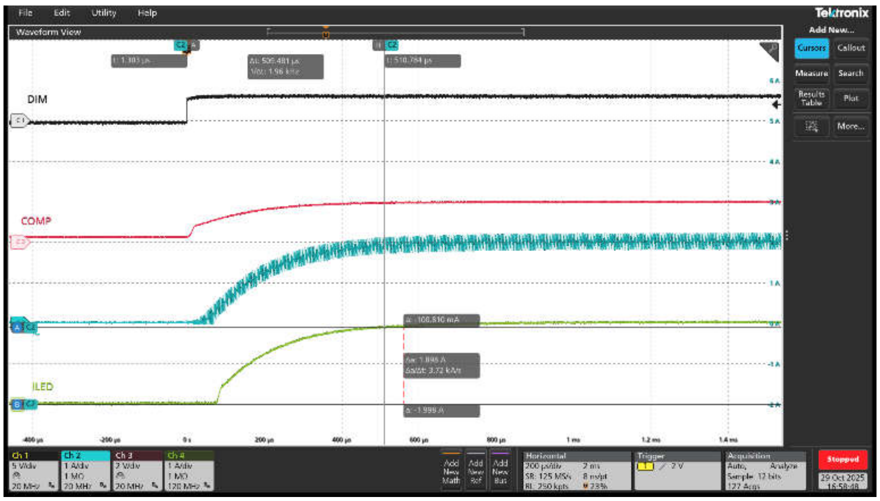

Figure 3-9. Start-up Waveform of DIM, COMP, IL and ILED with C_{COMP}=6.8nF

The results show that a smaller C_{COMP} results in a faster enable delay plus rise time (from DIM pulled high to LED current reach target value). For applications like barcode readers, where the target object moves and global shutter is used, PWM may remain low for hours and then be activated for a single pulse. The LED current must be ready on the first pulse with a fast response time, typically < 10-20us. In this case, optimizing C_{COMP} is an effective way to improve the response time.

The damping resistor R_{DAMP} is connected from the COMP pin to ground. For PWM dimming, R_{DAMP} helps suppress the current overshoot when DIM transitions from low to high. A smaller R_{DAMP} allows V_{COMP} to discharge more during PWM off, resulting in a longer LED current settling time when EN/PWM pulled high. However, a disadvantage is that it reduces LED current accuracy across the full current range due to introduced offset current.

Consider the application with V_{IN}=24V, 4-piece WLED and 4A maximum LED current. Figure 3-10 and Figure 3-11 show the waveforms of EN/PWM, SW, I_L and I_{LED} with and without R_{DAMP} (2MΩ). The results show that adding R_{DAMP} helps suppress LED current overshoot on the rising edge of PWM.

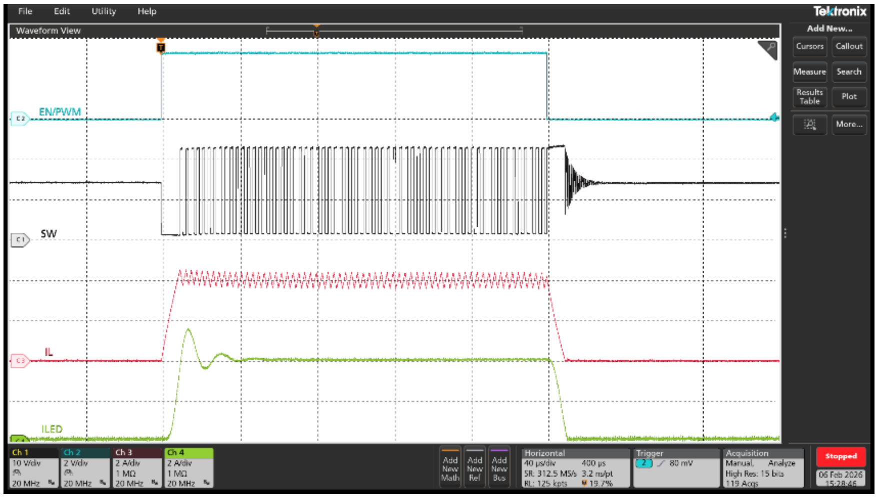

Figure 3-10. Waveform of EN/PWM, SW, I_L and I_{LED} without R_{DAMP}

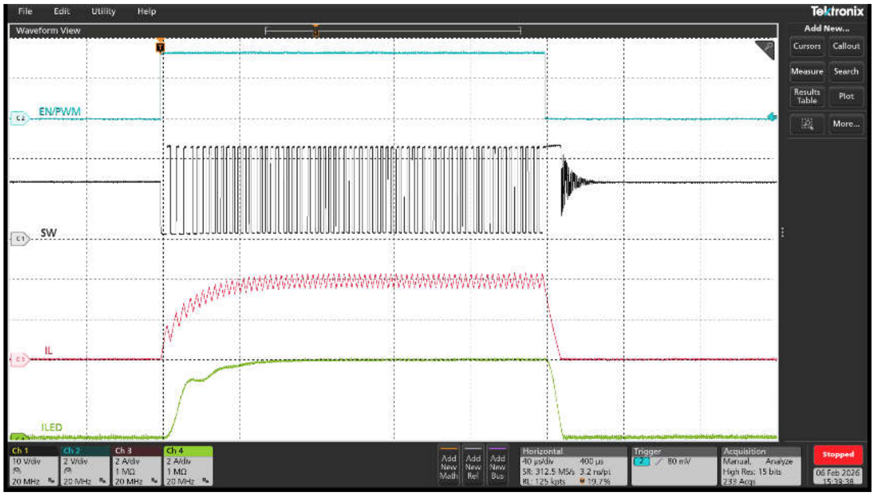

Figure 3-11. Waveform of EN/PWM, SW, I_L and I_{LED} with R_{DAMP}=2Mohm

3.2 LED String Off State Glow Suppression

Due to leakage paths through SW/CSP/CSN, the LED string may weakly illuminate even when DIM is low. As shown in Figure 3-12, an optional resistor R_{LK_COMP} can be selected to compensate for the CSP+CSN common-mode leakage current and prevent it from flowing through the LEDs. Without R_{LK_COMP}, a leakage path exists when VIN is supplied, there is leakage current path. This leakage path only exists with TPS92205x family which is Buck topology but not Boost and Buck-Boost configuration of TPS92365x family.

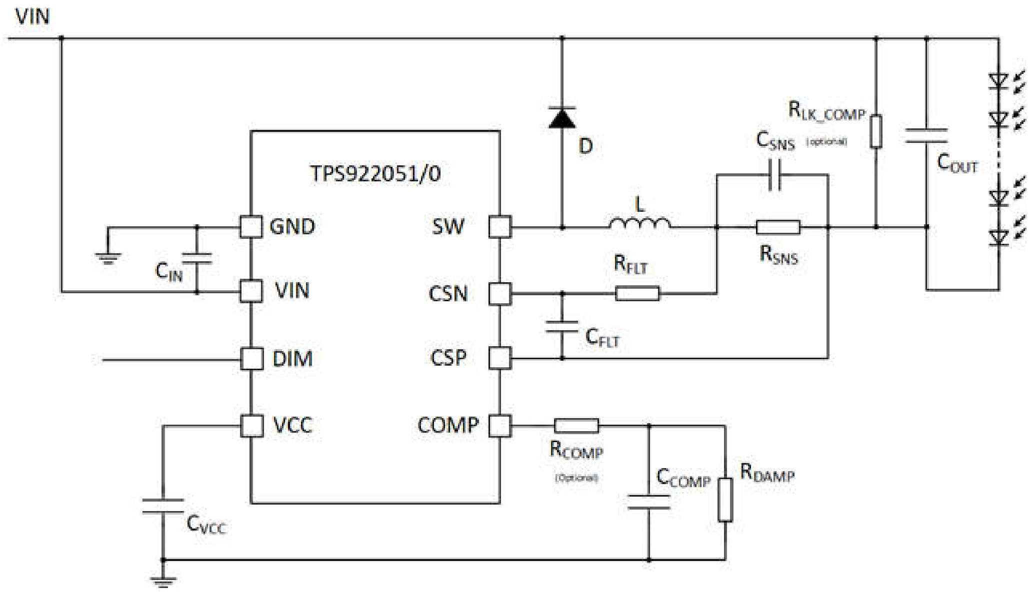

Figure 3-12. Schematic of TPS922051/0

The SW/CSN/CSP leakage current path before and after adding R_{LK_COMP} is shown in Figure 3-13 and Figure 3-14 which shows that the R_{LK_COMP} can help to compensate for the CSP+CSN common mode leakage current and avoid it passing through LEDs.

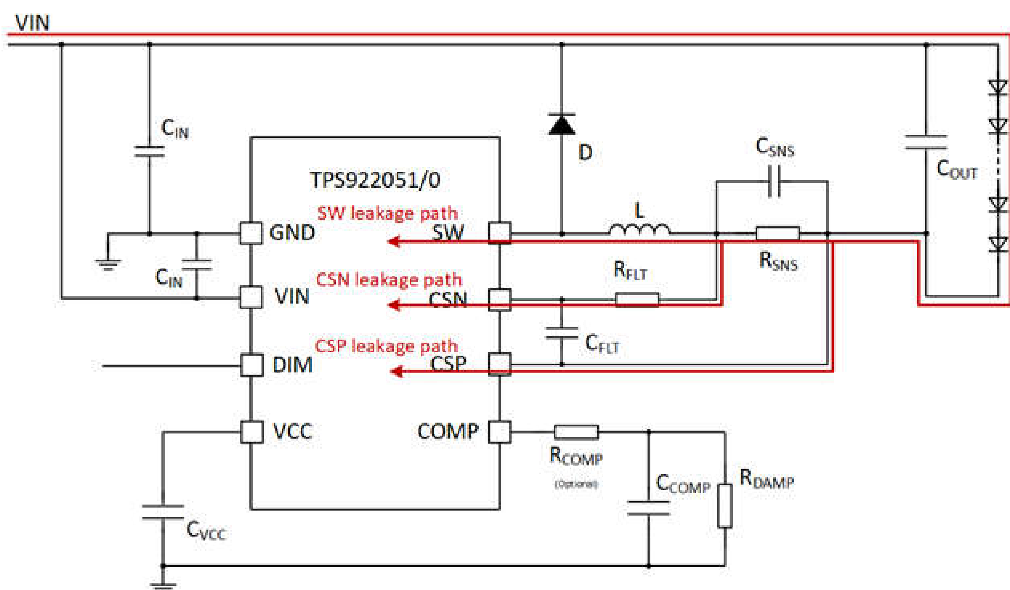

Figure 3-13. SW/CSN/CSP leakage path with R_{LK_COMP}

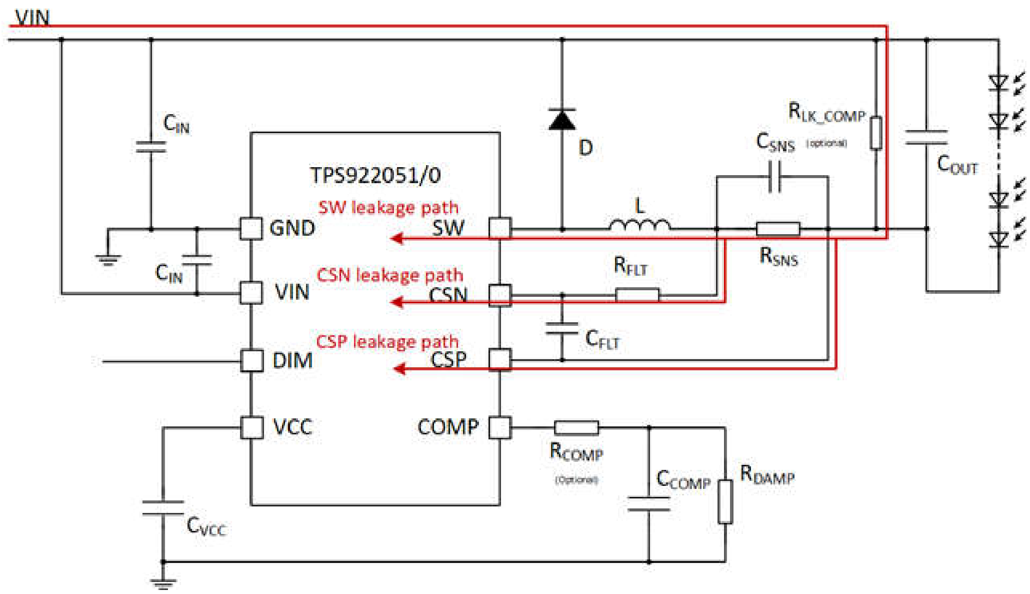

Figure 3-14. SW/CSN/CSP leakage path without R_{LK_COMP}

To design R_{LK_COMP}, measure the LED voltage and leakage current when V_{IN} is supplied and DIM is pulled down. Then calculate the shunt resistor according to it. For example, the test application is V_{IN_MAX}=54V and 5pcs LEDs. Since the larger VIN, larger leakage current. Thus, considering the worst case which is V_{IN_MAX}, When V_{IN}=54V and DIM is pulled down, I_{LED} is measured as 30.7uA. With 5pcs LEDs, V_F is measured as 11.7V. R_{LK_COMP} < 11.7V/30.7uA=381kΩ. It is an effective way to get R_{LK_COMP}.

3.3 Switching Start Voltage Adjustment

For analog dimming, TPS922051/0D2 supports analog dimming with analog input while TPS922055/4/3/2 supports analog dimming with digital input. In some applications, the DIM voltage might not be exactly 0V, to improve the system robustness to make sure that the device will not switch, R_{DAMP} can be added to generate offset voltage. With R_{DAMP} added, the LED current would be lower than target. Ideally for error amplifier, the sensed voltage across the sensing resistor should be equal to the internal reference voltage. However, after R_{DAMP} is added, EA offset is introduced, the output of error amplifier current will not only pass through the compensation network but also the damping resistor. When V_{IN}=24V, 4-piece WLED and target 4A maximum LED current, with no R_{DAMP} and 2MΩ R_{DAMP}, the measured LED current is 3.99A and 3.92A which also verifies that R_{DAMP} will cause the actual LED current lower than target.

For TPS922051/0D2, in ideal case, the relationship between V_{DIM} and V_{REF} is $V_{REF}=V_{DIM}/10$. If R_{DAMP} is added, an offset voltage is added which means that the switching start voltage of DIM pin (V_{DIM_ON}) is not exactly 0V, Equation 1 shows the relationship between V_{DIM_ON} and R_{DAMP}.

$$V_{DIM_{ON}} = \frac{10 \times V_{COMP_L}}{R_{DAMP} \times g_m} \quad (1)$$

Where

V_{DIM_ON} is the switching start voltage of DIM pin.

g_m is the transconductance gain which is 265uA/V typical.

V_{COMP_L} is the COMP low clamp voltage which is 0.8V typical.

For TPS922055/4/3/2 which is analog dimming with digital input, Equation 2 shows the relationship between D_{ADIM} and R_{DAMP}. For example, with R_{DAMP}=1Mohm, in theory, when ADIM duty cycle < 1.5%, the device will not start switching.

$$D_{ADIM} = \frac{5 \times V_{COMP_L}}{R_{DAMP} \times g_m} \quad (2)$$

Where

D_{ADIM_ON} is the switching start duty cycle of ADIM pin.

3.4 Low LED Full Scale Current Improvement

Sense capacitor is chosen to suppress the ac magnitude of sense feedback less than 200mV. For TPS92205x family, usually C_{SENSE} is not needed when the ripple ratio of the inductor current is a reasonable value. For TPS92365x family, C_{SENSE} is required as the current across R_{SENSE} is discontinuous.

In some applications, the input range is wider, the LED current is relatively low and there is no other resources to implement analog dimming or flexible dimming. It means that adjusting the R_{SENSE} is the only way to adjust the LED output current. For example, when V_{IN}=48V, 4-piece WLED and the maximum LED current is 100mA, in general, if following the equation in the datasheet, the recommended inductance is 1.125mH (choose K=0.2). With the recommended inductance, it will be good to get accurate LED current and good LED current ripple. However, this inductance is so large and will not be good for the total solution size and cost structure. Reasonable C_{SENSE} design is required to not only choose a typical inductor for optimized solution size but also get good LED current accuracy.

For the error amplifier as shown in the block diagram, it is required that the ac magnitude of the sense feedback CSPN (CSPN=CSP-CSN) should be less than 200mV. Take the application case of V_{IN} =48V, 4-piece WLED and 0.1A maximum LED current as an example. Figure 3-15 shows the waveform of LED current I_{LED}, inductor current I_L and voltage across CSP and CSN V_{CSPN} when L=1mH. From the waveform, it shows that the ac magnitude of CSPN is 60mV. In theory, the max value of V_CSPN is V_{REF}*(1+K/2), the min value of V_CSPN is V_{REF}*(1-K/2). K is the ripple ratio of the inductor current (ΔI_L / I_{LED_MAX}). A reasonable value of K is 20% to 60%. The AC magnitude is K*Vref. Thus, when K is selected in the range between 20% - 60%, there is no problem to meet the V_CSPN 200mV ac magnitude requirement.

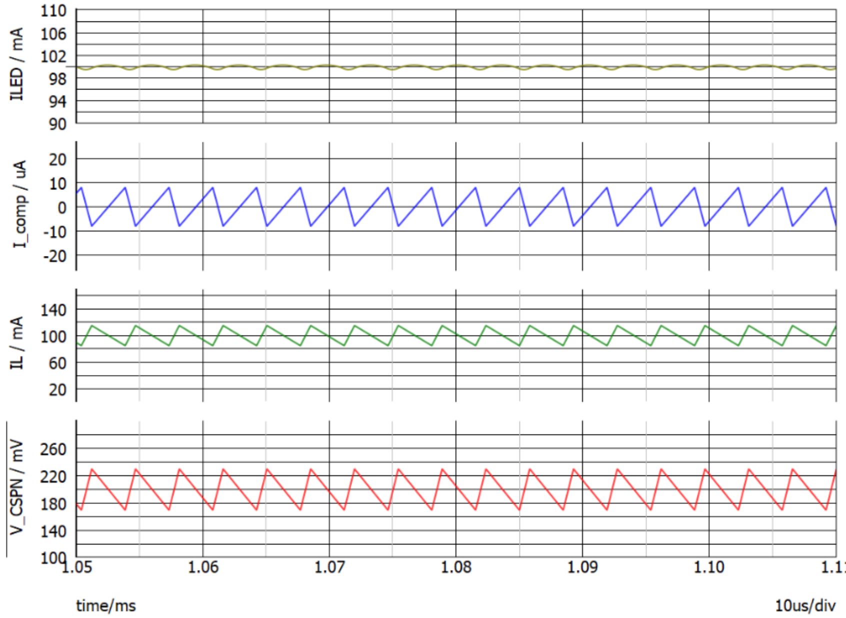

Figure 3-15. LED Current and CSPN Voltage when L=1mH

A method is proposed here to support lower inductance even with relatively low LED current: Adding a sense capacitor C_{SENSE} to suppress the ac magnitude. Figure 3-16 shows the waveform of I_{LED}, I_L, V_{CSPN} and I_{COMP} (Error amplifier output current) when L=33uH and without C_{SENSE}. Figure 3-17 shows the waveform of I_{LED}, I_L, V_{CSPN} and I_{COMP} when L=33uH and with C_{SENSE}=1uF. Without C_{SENSE} and with typical 33uH inductor, the I_{LED} is 142mA while the target LED current is 100mA which brings a big variation between the measured result and the result in theory. The reason is that the ac amplitude of the sense feedback V_{CSPN} is large so that the error amplifier is saturated and the output of the EA is clamped. With C_{SENSE} added, even if the inductor is typical as 33uH, the actual LED current can still be accurate as 100mA. Thus, when designing the circuit, if power density and good cost structure are required, adding a C_{SENSE} is good way for low LED current application. Please measure the voltage across CSPN to make sure that the ac magnitude is within 200mV. Thus, for TPS92205x family which is Buck topology, when C_{SENSE} is not properly designed, the LED current would be higher than target.

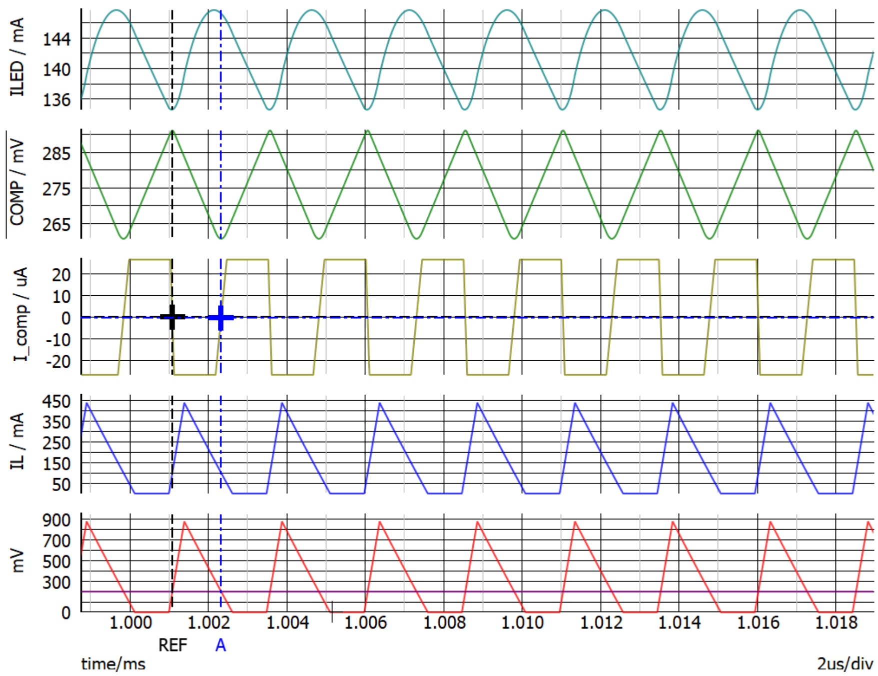

Figure 3-16. LED Current and CSPN Voltage when L=33uH and w/o C_{SENSE}

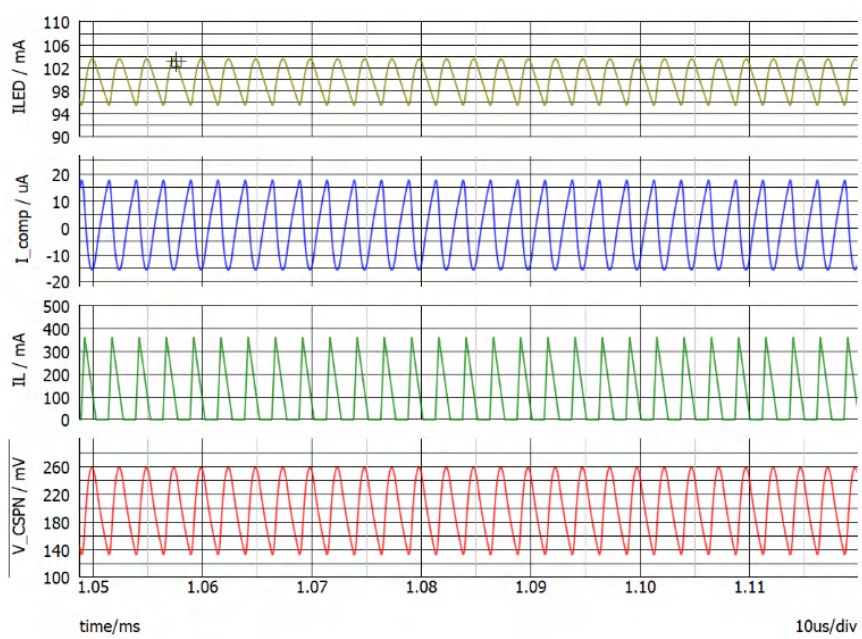

Figure 3-17. LED Current and CSPN voltage when L=33uH and With C_{SENSE}=1uF

4 Design Guidance for Application Circuit

4.1 Design of CSP and CSN C_{FLT} and R_{FLT}

A 100Ω, 0603 resistor is recommended for R_{FLT} at CSP pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is selected for C_{FLT} across CSP-CSN pins to filter high-frequency noise of sense feedback. Too large C_{FLT} is not recommended which introduces larger RC delay time and thus result in bad loop response and current accuracy. For example, when V_{IN}=24V, 6-piece WLED and the maximum LED current is 2A, Figure 4-1 shows the loop response comparison between 100nF C_{FLT} and 1nF C_{FLT}. With larger C_{FLT}, it brings in lower phase margin.

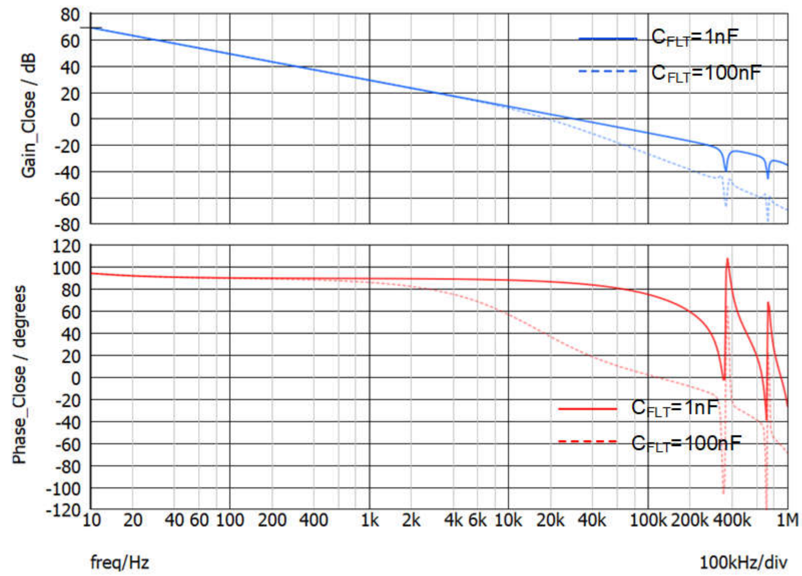

Figure 4-1. Loop Response Comparison Between 100nF C_{FLT} and 1nF C_{FLT}

4.2 Design of UVP and OVP Resistors

The TPS92205x family enables constant current (CC) / constant voltage (CV) charging operation by configuring UVP pin and the UVP pin has two thresholds which are 1.4V and 1.1V. When the voltage of the UVP pin is above 1.4V, the output current is not affected by the CV mode. When the voltage of the UVP pin is below 1V, "LED open load" protection will be triggered. To make sure that the output current won't be affected in all working conditions, make sure to meet Equation 3.

$$\left(V_{IN_{MIN}} - V_{OUT_{MAX}}\right) \times \frac{R_{UVP2}}{R_{UVP1} + R_{UVP2}} > 1.4 \quad (3)$$

Where

VIN_MIN is the minimum input voltage. VOUT_MAX is the sum of the maximum forward voltage of each LED in the LED string at your maximum target output current.

A rule of thumb is that you can design the sum of RUVP1 and RUVP2 to be around 1MΩ or 2MΩ and this normally would be a good start point. There will be leakage path from VIN, LEDs, UVP resistor dividers to ground. Too small of UVP resistors will introduce larger leakage current through LEDs. One way is to use UVP resistor divider with a larger value to decrease the leakage current so that the LED will not light up. Another way is to parallel a large resistor RLK_COMP with LED string. When the device is disabled, the RLK_COMP, RUVP1 and RUVP2 will act like voltage divider, where you should set the voltage across the LED string less than the voltage that will light up the LEDs.If the UVP resistors are not designed properly, for example, when VUVP is in the range of 1.0V to 1.4V, the LED current will be smaller than target.

The TPS92365x family enables constant current (CC) / constant voltage (CV) charging operation by configuring OVP pin and the OVP pin has two thresholds which are 1.4V and 1.15V. When the voltage of the OVP pin is below 1.15V, the output current won't be affected by the CV mode. When the voltage of the OVP pin is above 1.4V, "LED open load" protection will be triggered. To make sure that the output current won't be affected in all working conditions, please make sure to meet Equation 4.

$$V_{OUT_{MAX}} \times \frac{R_{OVP2}}{R_{OVP1} + R_{OVP2}} < 1.15V \quad (4)$$

Where

VOUT_MAX is the sum of the maximum forward voltage of each LED in the LED string at the target output current with Boost connection and is the sum of the maximum forward voltage of each LED in the LED string at the maximum target output current plus the maximum input voltage with Buck-Boost configuration.

Please do not design R_{OVP1} and R_{OVP2} with too small values. Otherwise, there will be a severe leakage current path from VIN, the inductor, the Schottky diode, the sense resistor, the OVP resistor divider and then to GND. A too-small-value OVP resistor divider will also affect the accuracy of output current as the resistor divider will shunt current from the LED. A rule of thumb is that you can design the sum of R_{OVP1} and R_{OVP2} to be around 1MΩ or 2MΩ and this normally is a good start point. Adjust the values based on your test results.

To provide LED open load protection safely, Equation 5 must also be met. 63V refers to the maximum recommended input voltage.

$$63 \times \frac{R_{OVP2}}{R_{OVP1} + R_{OVP2}} > 1.4V \quad (5)$$

To meet equations Equation 4 and Equation 5, it is required that the maximum output is limited as approximately 51V. If V_{OUT_MAX} > 51V, either of the above two conditions cannot be met. If the OVP resistors are not designed properly, for example, when V_{OVP} is in the range of 1.15V to 1.4V, the LED current is smaller than the target.

5 Summary

This application note addresses methodologies for optimizing dimming performance. Innovative dimming control techniques, including inductive fast dimming and inductive pulse dimming are introduced. It also shows the experimental results of LED current dimming linearity curve. Furthermore, it offers application-focused guidance on optimizing peripheral circuit design to achieve optimal dimming performance. The experiment verification results prove the optimized dimming performance.

6 References

1. Texas Instruments, *TPS922050/1 65V 1A/2A Buck LED Driver with PWM/Analog Dimming,* datasheet.
2. Texas Instruments, *TPS92205x 65V 2A / 4A Buck LED Driver with Inductive Fast Dimming* , datasheet.