Application Note

Preventing ICT-Induced Electrical Overstress on TCA9617 I/O Ports

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ABSTRACT

This application note describes a failure mechanism observed on the TCA9617 during In-Circuit Test (ICT) environments. The issue manifests as I/O ports becoming stuck low (particularly on SDAB, SCLB, or both) due to permanent damage of the device.

Investigation showed the root cause was not normal system operation, but rather signal integrity issues introduced by the ICT setup. Long trace lengths between the ICT host and the device generated excessive overshoot and undershoot during signal transitions. In some cases, the transient voltage exceeded the absolute maximum voltage ratings of the device pins, resulting in electrical overstress (EOS) damage.

Two effective mitigation methods were identified:

1. Adding approximately 200-Ω series resistance in the ICT signal path to dampen ringing and reduce overshoot/undershoot.
2. Modifying the ICT test pattern to use open-drain drivers rather than push-pull.

This document explains the observed behavior, root cause analysis, and recommended mitigation techniques.

Table of Contents

Trademarks

1 Introduction

The TCA9617 is a bidirectional I^2C/SMBus voltage-level translator commonly used in systems requiring communication between different voltage domains. During ICT (Inter-circuit test), several units experienced SDAB/SCLB stuck-low behavior from being permanently damaged, causing functional communication failures. Oscilloscope investigation later confirmed that the ICT setup generated excessive overshoot and undershoot events on the I/O pins.

2 Failure Analysis

Oscilloscope measurements captured significant overshoot and undershoot events during ICT operation. The worst-case overshoot measured 8.62V, while the worst-case undershoot measured -4.28V. These values exceeded the datasheet absolute maximum ratings of 6.5V and -0.5V, respectively for V_{IO} – I^2C bus voltage range. The transient spikes therefore subjected the device pins to electrical overstress conditions. See figure 2-2 note (1) of this document for overshoot behavior. See Figure 2-3 of this document for undershoot behavior.

In addition to exceeding absolute maximum V_{IO} specifications, there exists a signal contention between the driver of the ICT and the TCA9617 B-side pedestal during a low-to-high edge transition on B-side. The pedestal behavior can be seen in the TCA9617 datasheet Figure 6-4, Figure 7-1, or Figure 8-2 point 2, and is described in Application Information.

On the B-side bus of the TCA9617B, the clock and data lines have a positive offset from ground equal to the V_{OLB} of the TCA9617B. After the eighth clock pulse, the data line is pulled to the V_{OL} of the target device, which is close to ground in this example. At the end of the acknowledge, the voltage level rises only to the low level (V_{OLB}) set by the driver of the TCA9617B for a short delay, while waiting for the A side bus to rise above 30% of V_{CCA}. Once the A-side reaches 30% of V_{CCA}, the B side is released and the pullup resistors on the bus pull the bus high.

Figure 2-1. TCA9617B Datasheet Section 8.1 Application Information - Pedestal Behavior Description

When TCA9617 is driven from B-side to A-side, it expects an open-drain driver configuration. When the open-drain driver on B-side releases the bus, a pull-up resistor on B-side will pull-up to V_{CCB}. During this time, the buffer will reach a voltage pedestal (~V_{OLB} = 0.53V typical). The B-side will remain at this V_{OLB} until the A-side surpasses a 30% of V_{CCA}. Once this occurs, B-side is no longer held at V_{OLB}, and is allowed to rise fully to V_{CCB} through the pull-up resistor. If a push-pull driver is used during this edge transition from low-to-high on B-side, there will exist a contention between the pedestal voltage (V_{OLB}) and the push-pull driver, resulting in a large amount of current sink into the buffer - see Figure 2-2 of this document.

Table 2-1. Worse Case Measurements

Parameter	Measured Value	Datasheet Limit
Overshoot	8.62V	6.5V
Undershoot	-4.28V	-0.5V

Figure 2-2. Overshoot Spike Test from ICT

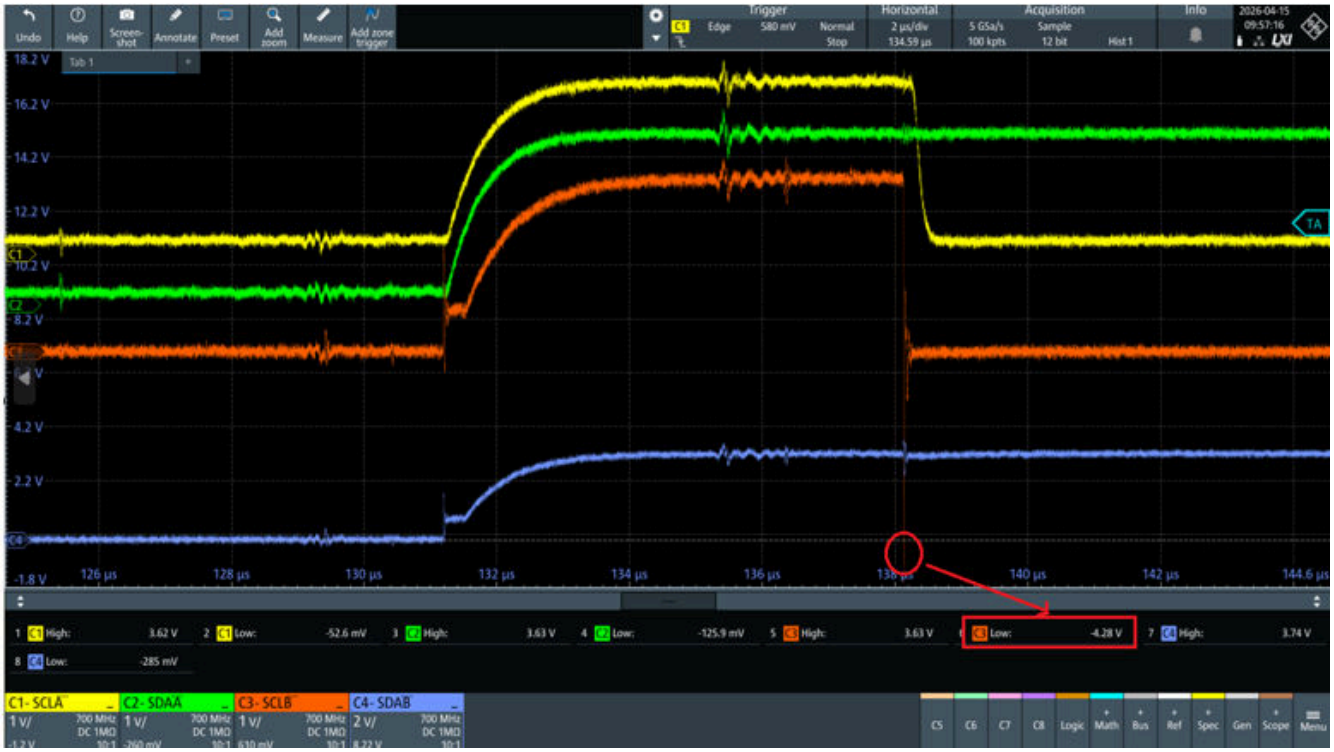

Figure 2-3. Undershoot Spike Test from ICT

2.1 Original ICT Setup

Original MAIN ICT program conducts the following:

1. A side to B side test
   a. Drive patterns on (SDAA and SCLA, measure output on SDAB and SCLB)
   b. 00 / 01 / 10 / 11, SDAA = 0, SCLA = 0, next SDAA = 0, SCLA = 1 ...
2. B side to A side test
   a. Drive patterns on (SDAB and SCLB, measure output on SDAA and SCLA)
   b. 00 / 01 / 10 / 11, SDAB = 0, SCLA = 0, next SDAB = 0, SCLB = 1 ...
3. In both tests, measure the correct output pattern (00 / 01 / 10 /11)

The tester then verified functionality by reading back the corresponding pattern on the opposite side of the device. During testing, the ICT system actively drove both logic-high and logic-low states with strong edge-rate transitions.

From a hardware setup, series resistors were not connected on channels SDAA, SCLA, SDAB, and SCLB.

2.2 Corrective Actions

To reduce electrical stress during ICT operation, two major corrective actions were implemented. The first modification changed the drive patterns from

Original patterns:

00 / 01 / 10 / 11

Were replaced with:

00 / 0X / X0 / XX,

where “X” represents a “Don’t Care” state. In this updated approach, the logic-high condition was no longer actively driven by the tester (open-drain driver). Instead, the output was allowed to rise high through the existing pull-up resistors. This significantly reduced edge-rate aggressiveness which minimized overshoot generation during a low-to-high transition. The use of open-drain also resolves any contention with the pedestal voltage from the TCA9617 on B-side.

In addition to the software changes, hardware changes were made by adding 200Ω series resistors to SCLA, SDAA, SCLB, and SDAB on the ICT test platform. The resistors provided edge-rate reduction, reflection damping, and suppression of LC resonance created by the long ICT interconnect structure. The resistors also limit the current to and from the buffer.

Figure 2-4. New ICT Setup with Software and Hardware Changes Reduces Overshoot/Undershoot Behavior and Resolves B-side Pedestal Contention

2.3 Validation Result

After implementing the updated ICT setup, waveform integrity improved significantly. The worst-case overshoot decreased from 8.62 V to 3.54 V, while the worst-case undershoot improved from -4.28 V to -0.35 V. All measured voltages were now within the datasheet absolute maximum specifications of the device. There exists no more pedestal contention.

Oscilloscope measurements also confirmed that ringing amplitude and transient spike energy were substantially reduced. Following implementation of the new ICT method and the addition of series resistors, no additional I/O damage or stuck-low conditions were observed during production testing.

Table 2-2. Before and After Measurements

Parameter	Measured Value (Before ICT changes)	Measured Value (After ICT changes)	Datasheet Limit
Overshoot	8.62V	3.54V	6.5V
Undershoot	-4.28V	-0.35V	-0.5V

2.4 Recommendations

For ICT validation of TCA9617B or TCA9617A and similar I^2C devices, Texas Instruments recommends minimizing fixture cable length whenever possible. Long cables and/or trace interconnects create inductive and capacitive parasitics that establish an environment for excessive ringing induced by strong drivers from the ICT tester. Avoiding the use of push-pull drivers by implementing open-drain drivers during ICT is necessary to avoid pedestal contention and possible overshoots above the absolute maximum voltage of the device. It is recommended to add series dampening resistors to reduce ringing, transient stress, and limit current. In addition, the system level implementation of the TCA9617B or TCA9617A should be designed to operate within the recommended operating conditions of the datasheet for all voltage and current specifications at all times.

3 Summary

An ICT (inter-circuit test) or similar functional test is often used to valdiate the use of the TCA9617 buffer within a system level design. The TCA9617A , TCA9617B, and simiar devices should always operate within the recommended operating conditions of the datasheet. There should be extensive review when developing the hardware and software of such test platform to ensure that the applied signals to the buffer do not interfere with the buffers pedestal offset on B-side, or induce an electrical overstress event (EOS) such as overshoots, undershoots, and/or over-current events that exceed the absolute maximum conditions in the datasheet. Following these parameters ensures the longevity of the buffer.

4 References

1. Texas Instruments, *TCA9617B Level-Translating FM+ I2 C Bus Repeater*, datasheet.

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