Clocking Recommendations for the DM643x EVM

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ABSTRACT

The DM643x evaluation module (EVM) requires several clock frequencies to run the system properly. The current clocking proposal of the low-cost evaluation module consists of the VCXO chip PI6CX100-27W, the PLL chip PLL1705, several bus drivers, and a few oscillators and crystals. This application report discusses several optimized clocking proposals with the Texas Instruments new clock drivers and recommends a more integrated, high-performance, and cost-saving proposal with minimum ICs.

Introduction

The system requires frequency adjustment capability to synchronize the audio and video clock. Zero-ppm accuracy for video and audio clocks is required. The phase-locked loop (PLL) also is required to generate the audio clock or clocks from the 27-MHz video clock frequency.

Besides the video and audio clocks, a 27-MHz and a 25-MHz Ethernet clock signals are generated either from a crystal or an oscillator.

Video and Audio Clocks Generation

The current clocking solution in the reference design guide is a multichip-based proposal. The modulated signal (PWM) is converted into analog control voltage (using an RC filter) before providing it to the control input of the VCXO. The VCXO chip PI6CX100-27W receives the PWM signal and adjusts the 27-MHz crystal frequency for the required synchronization.

The PLL chip PLL1705 generates a 3.3-V video clock (27 MHz) and an audio clock for the stereo codec TLV320AIC33 from the 27-MHz synchronized signal.

The single-bus buffers (74LVC1G125D and SN74CBTLV1G125) are used for video and audio clock paths.

The PLL1705 is capable of generating audio clock frequencies such as 8.192 MHz, 11.2896 MHz, 12.288 MHz, 16.384 MHz, 16.9344 MHz, 18.432MHz, 22.5792 MHz, 24.576 MHz, 33.8688 MHz, and 36.864 MHz.
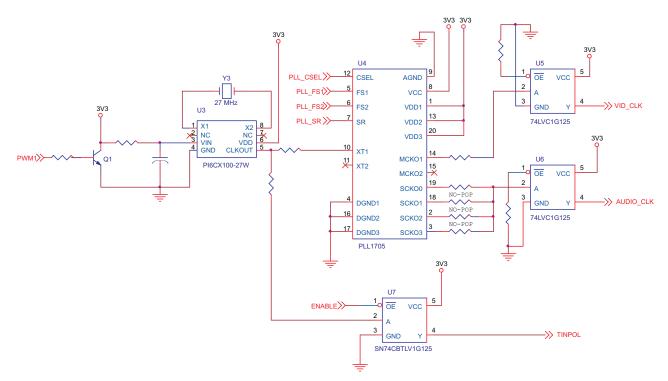
**Figure 1. Generating Synchronized Video and Audio Clocks
(The Current Clocking Proposal With Several ICs)**

Clock Proposal With CDCE913

The CDCE913 is currently in design phase. Samples availability is planned for the second quarter of 2007. The CDCE949 is a similar device with more outputs. The footprint of CDCE949 can be used for the CDCE913 devices. Samples availability of the CDCE949 is planned for February 2007.

Single-Chip Solution of Generating an Audio and Video Clock

The single-chip solution is capable of generating the synchronized video and audio clocks for the system.

CDCE913 is a single, PLL-based VCXO clock. This PLL can be programmed via an I^{2}C bus, and all audio frequencies can be generated with 0-ppm error. This device also supports nonvolatile EEPROM and factory-preprogrammed devices (according to the customer's specification). Using the control pins, one of the several preprogrammed audio frequencies can be selected.

It has three outputs. Two of the outputs (Y1 and Y2) are PLL bypassed and generate a 27-MHz video clock. Y3 outputs are PLL programmed and generate an audio clock frequency
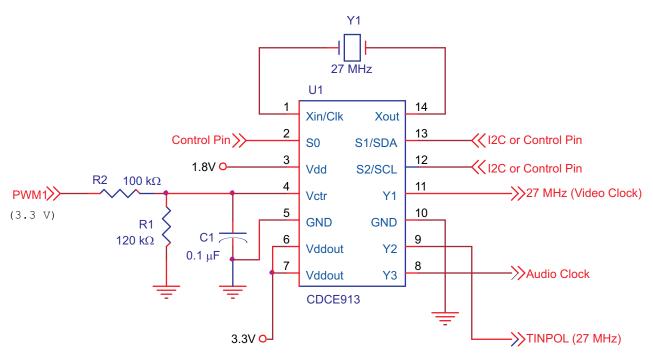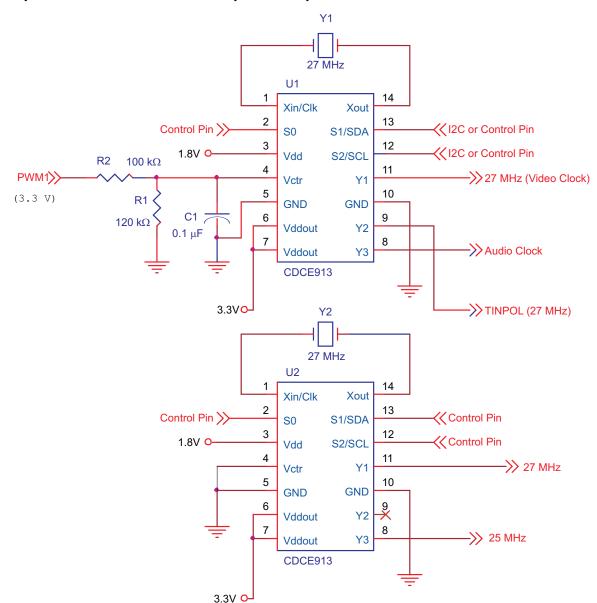
Figure 2. Single-Chip Solution to Generate Synchronized Audio and Video Clock Frequencies

The core supply voltage of the CDCE913 is 1.8 V. So, with a 3.3-V modulation signal, a resistor for a voltage divider (R1=120 kΩ) is required to maintain the correct voltage level for the Vctr pin (1.8 V). This device can generate a 3.3-V LVCMOS signal, so that any additional signal translators or buffers are unnecessary. Because the core supply voltage is low, it consumes low power compared to 3.3-V devices.

Two-Chip Solution to Generate All Required Frequencies

Figure 3. Two-Chip Solution to Generate All Frequencies for this System

Because two other frequencies (27 MHz and 25 MHz) are required and these frequencies must not be synchronized like video and audio clocks, a second CDCE913 can be used with a 27-MHz crystal to generate the rest of the clocks. The jitter performance is good and meets all jitter requirements of DSPs.

If more than three clocks are required, CDCE925[2] (five outputs), CDCE906 (six outputs), CDCE937[2] (seven outputs), or CDCE949[1] (nine outputs) can be used.

Note: [1]CDCE913 is currently in design phase. Samples availability is planned for the second quarter of 2007. CDCE949 is a similar device with more outputs. The footprint of CDCE949 can be used for the CDCE913 devices. Samples availability of CDCE949 is planned for February 2007.

[2]CDCE925 and CDCE937 are in design phase. Samples availability of these devices is planned for the third quarter of 2007.

If the availability of all 10 audio frequencies are required but the options to program the CDCE913 through an I²C bus are unavailable, then the CDCE949 is recommended. The CDCE949 is a similar device (1.8-V core and 3.3-V output buffer) to CDCE913 with four PLLs and nine outputs.
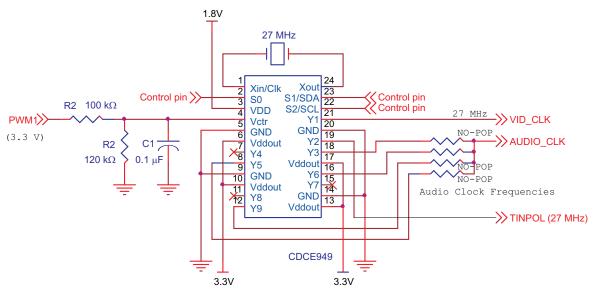

Figure 4. Single-Chip Solution to Generate Synchronized Video and All Audio Frequencies

With using the control pins and populating the right termination resistors, the required audio clock (any of the 10 frequencies) can be generated and selected for the stereo audio codec. The unused outputs cannot be used to generate other frequencies (27 MHz, 25 MHz) because they also are synchronized.

Clock Proposal With CDCE906 and PI6CX100-27W (Two-Chip Solution) [3]

Note: [3]This solution is currently available.

One clock synthesizer (CDCE906) and one VCXO clock (PI6CX100-27W) can be used to generate the synchronized video and audio clocks for the system.

The CDCE906 is a three-PLL-based, 3.3-V clock synthesizer with six outputs. All PLLs can be programmed via an SMBus (maximum 100 kHz) to generate the audio clocks and video clocks. The PI6CX100-27W generates a 27-MHz adjusted clock frequency using a PWM signal from the DSP. Then, it feeds into the clock synthesizer (CDCE906) to generate video and all audio frequencies. The 3.3-V buffers of the CDCE906 eliminate the need of extra single bus buffers (74LVC1G125D).
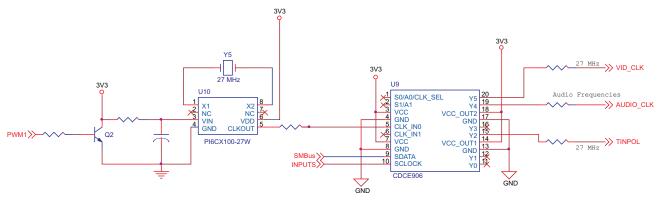

Figure 5. Two-Chip Solution Using SMBus Interface Programming

CDCE906 also supports nonvolatile EEPROM for easily customized applications. TI offers a

preprogrammed version CDCE906 so that a customer does not need to program the PLLs through an SMBus. If the customer prefers not to use the SMBus programming and needs three different unrelated audio frequencies and one integer multiple of one of the PLL frequencies available on the board after power up, then the EEPROM of the CDCE906 can be used. Four preprogrammed audio frequencies are available; to select one of them, simply populate the appropriate termination resistor.
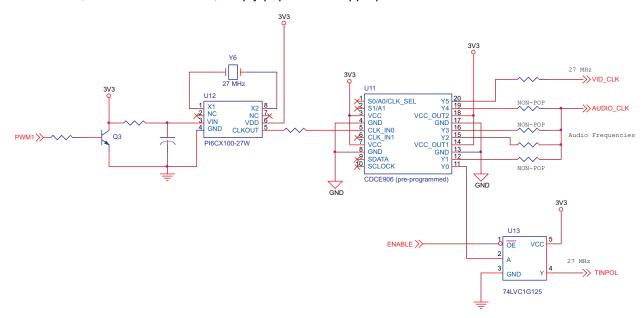

Figure 6. Multichip Solution With EEPROM

If the ENABLE is not required for the TINPOL signal, then the CDCE906 output can be used directly.

Conclusion

The CDCE913 is offered with a 14-pin TSSOP package. This single, tiny device can replace the functionality of one VCXO chip, one PLL chip, and three single-bus buffers to generate synchronized audio and video clocks. The required frequencies can be generated either through an I^2C bus or an EEPROM. This is a simple and cost-saving solution with 0-ppm error.

References

1. *CDCE906, Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* data sheet (SCAS814)

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