Application Report
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Avoid Start-up Overshoot of LDO

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Linear Power - LDO

ABSTRACT

Due to the many advantages of Low Dropout Regulators (LDO), they are widely used in almost every kind of system. Despite this, there are some things to keep in mind when designing a new application. This application note describes one potential issue LDOs may experience under a specific use case: overshoot during start-up. This application report explains the reasons for this phenomenon in detail, and covers the methods used to avoid overshoot during LDO start up.

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Trademarks

1 Output of LDO Overshoot During Start-Up

The most outstanding advantage of an LDO is that it can output a low-noise voltage, so it is used to power parts that are sensitive to power supply noise. In some applications, the LDO output voltage has overshoot during start-up, which can affect the whole system. The overshoot can trigger overvoltage protection, which can cause the system to fail to power up, cause it to restart constantly, or, even worse, result in damage to the next stage or load.

Using the TPS709 EVM as an example, the output voltage is set to 3.3 V. As Figure 1 and Figure 2 illustrate, (Green: V_{IN}; Red: V_{OUT}; Blue: V_{EN}), the test result shows the maximum overshoot of output is 3.61 V. That is an almost 10% overshoot, which is just beyond the acceptable 3 V to 3.6 V voltage range of most 3.3-V loads. Looking specifically at the no-load behavior shown in Figure 2, the overvoltage scenario can last for a long time. There is a risk that 3.61-V overshoot may trigger the system overvoltage protection or cause damage to the load, so why overshoot occurs, and how to eliminate it, must be addressed.

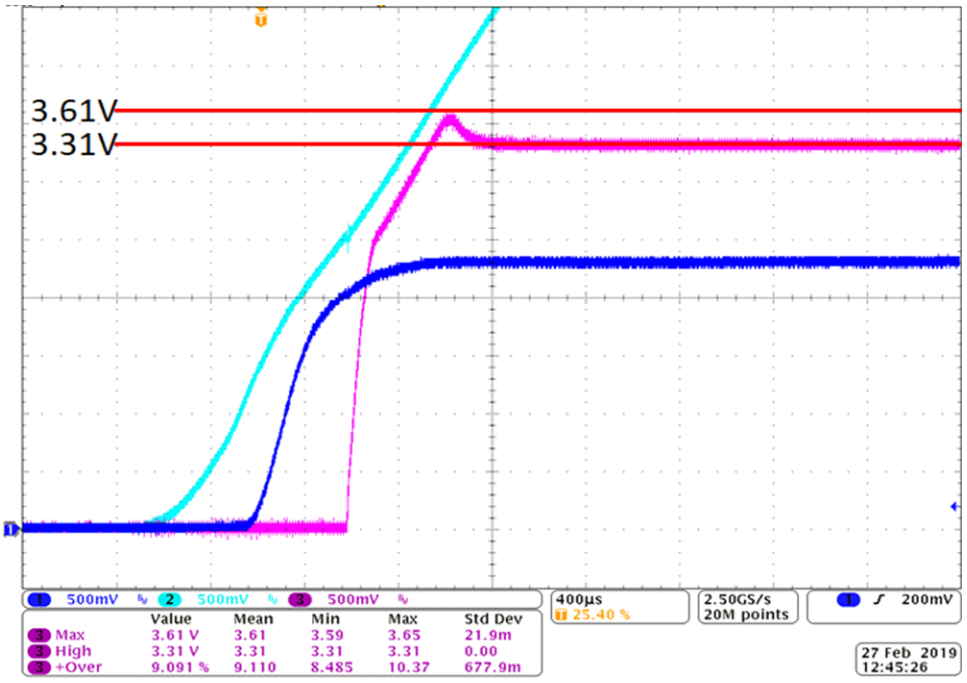

Figure 1. TPS709 EVM Test Results, V_{IN} = 0 V to 11 V, V_{OUT} = 3.3 V, I_{Load} = 0.05 A

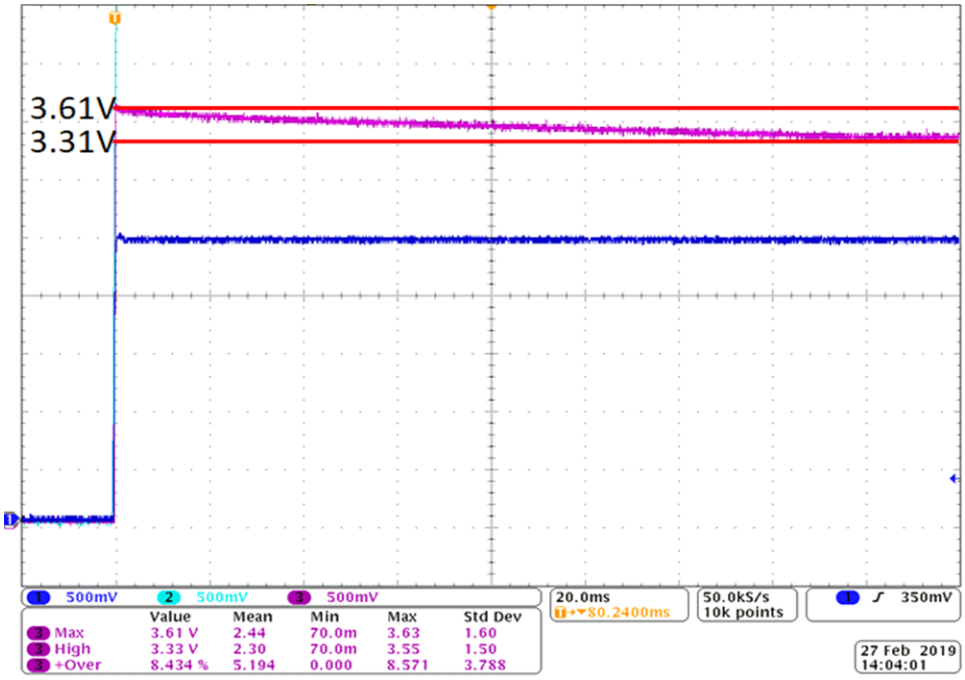

Figure 2. TPS709 EVM Test Results, V_{IN} = 0 V to 11 V, V_{OUT} = 3.3 V, I_{Load} = 0 A

2 Root Cause of Output Overshoot During Start Up

2.1 Basic Structure of LDO

LDOs can operate at a low potential difference between input and output. Figure 3 shows a block diagram of the internal circuit of a linear regulator. It basically consists of an error amplifier (used for error detection), a reference voltage source, and an output transistor. Since the operation is the same as that of a non-inverting amplifier circuit, the voltage at the non-inverting terminal (FB) of the error amplifier becomes the same as the reference voltage (V_{REF}). The gain set by the ratio of the resistor divider (R1 and R2) determines the output voltage (V_{OUT}).

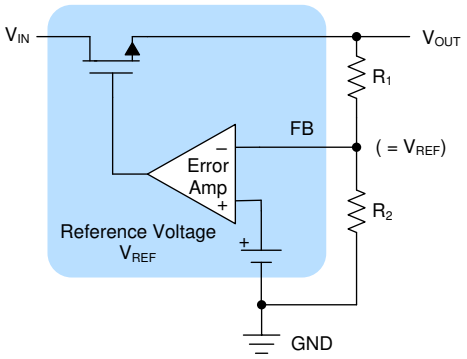

Figure 3. Basic LDO Structure

2.2 Basics of MOSFET in LDO

The working principle of the LDO is using the MOSFET to control the resistance between the source to the drain (V_{IN} and V_{OUT}). It can be simply regarded as a potentiometer controlled by the gate voltage. Since charging and discharging the parasitic gate capacitance takes time, the MOSFET resistance cannot be changed instantaneously.

2.3 Basics of an Error Amplifier in LDO

An error amplifier is essentially what the name says: it amplifies the error between the reference voltage and the feedback node (FB). Any difference between the positive and negative terminals of the error amplifier is amplified by the gain (set by R1 and R2) to generate a compensating error voltage, which then attempts to move the output voltage towards the targeted voltage. Amplifiers have slew rate and bandwidth limitations, so the output cannot change immediately. It takes time to charge, or discharge, both the parasitic gate capacitance and any external capacitor for the load.

2.4 Principle of Overshoot

As the TPS709 EVM schematic in Figure 4shows, some LDOs do not have a controlled soft-start function. When the V_{IN} begins to start up, the V_{EN} increases while the V_{IN} increases. The internal reference V_{REF} attempts to start up at the fixed slew rate once V_{EN} reaches the enable threshold. Since the output voltage is a gained version of the reference voltage, V_{OUT} tries to follow the V_{REF}, and the V_{OUT} slew rate is equal to the V_{REF} slew rate, unless the current limit is triggered, or the regulator goes into dropout. If the V_{IN} is less than $V_{REF} \times [(R1 + R2) / R2]$, the V_{IN} will not allow the V_{OUT} to track the V_{REF}, and the LDO is in dropout. At this time, the error amplifier drives the gate voltage of the pass FET to the rail, so that the FET is fully on. When the output reaches the regulation point, the error amplifier must transition the gate voltage away from the rail. This takes time because the transistor and error amplifier cannot change immediately, as discussed in Section 2.2 and Section 2.3. During this transition, the output continues to follow the input voltage, which causes an overshoot.

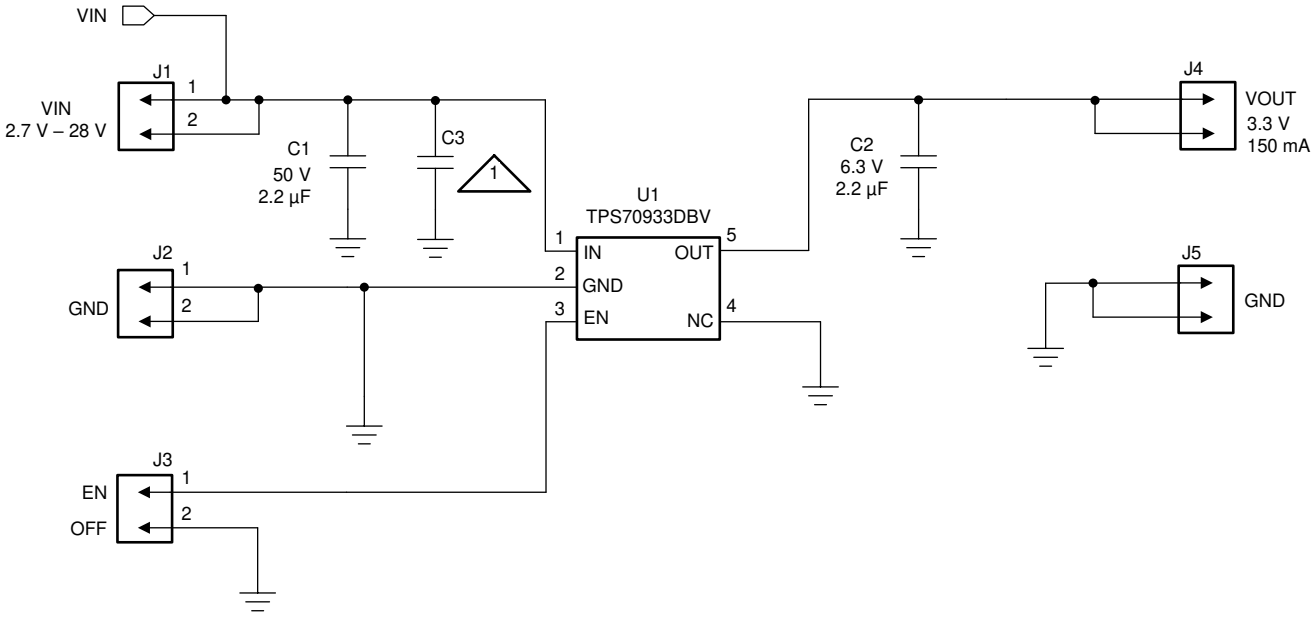

Figure 4. TPS70933EVM-110 Schematic

The comparison is as follows. In Figure 5, the slew rate of the V_{IN} is quick enough. This means the V_{IN} is ready before the V_{REF}, so there is not an overshoot. In Figure 6, the V_{IN} increases slowly, the V_{REF} is ready before the V_{IN}, and the error amplifier output drives the MOSFET fully on. Once the output reaches the regulation point, it needs time to transition from a fully on state to a more resistive state, which results in an overshoot. Figure 7 shows the gate voltage of the internal pass device during dropout. This occurs when coming out of dropout, regardless if the LDO is starting up for the first time or not. In addition, the TPS709 test results also show the same situation. When the slew rate of the V_{IN} pin is slow, there is an overshoot during start up. As shown in Figure 1 and Figure 2, when the slew rate of the V_{IN} pin is quick enough to allow enough V_{IN} when V_{EN} becomes high, the overshoot disappears. This behavior can also be interpreted as "startup in dropout" as shown in Figure 7.

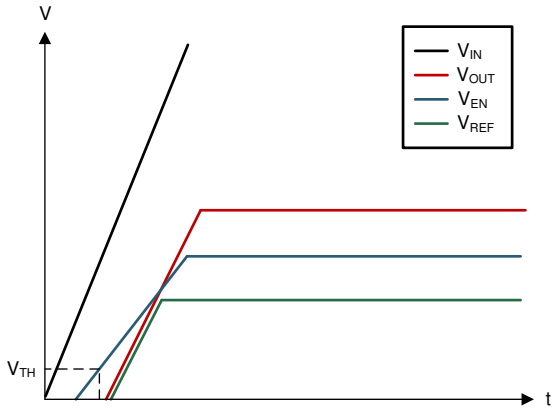

Figure 5. Start-Up Without Overshoot

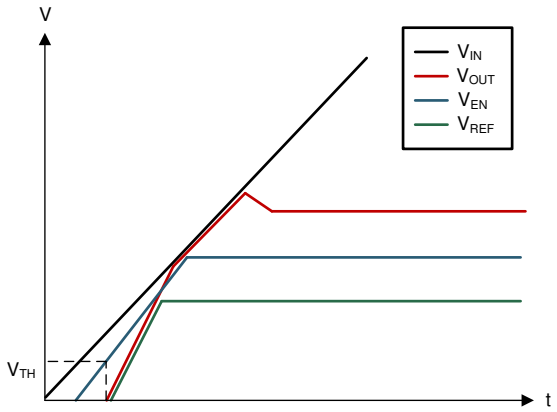

Figure 6. Start-Up With Overshoot

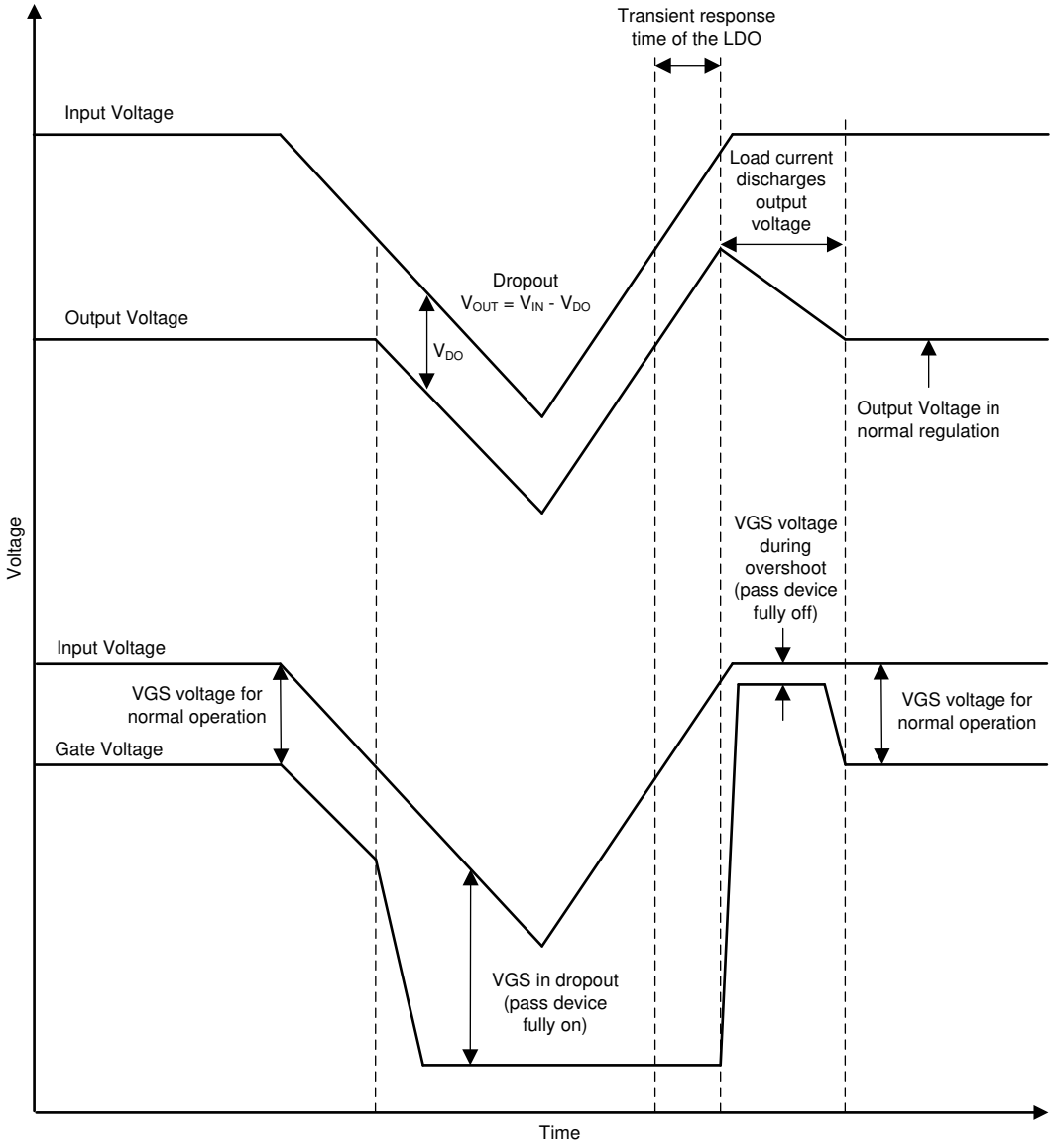

Figure 7. Internal Gate Node Voltage During Dropout

3 Methods to Avoid Overshoot

As previously described, the V_{IN} should reach the required value before LDO is enabled to avoid the overshoot. This means the LDO will not go into low dropout mode during start-up.

There are four methods to avoid overshoot:

1. Follow any instructions listed in the data sheet to keep the V_{IN} slew rate quick enough to allow V_{OUT} to follow the natural start up of the V_{REF}. If no explicit instructions are given, a plot showing the LDO starting up using the V_{EN} signal with the V_{IN} established shows how much time the LDO needs to start up naturally. Figure 8 and Figure 9 show the comparison (Green: V_{IN}; Red: V_{OUT}; Blue: V_{EN}). The slew rate of the V_{IN} in Figure 8 is 5 V / ms. The slew rate of the V_{IN} in Figure 9 is 8 V / ms.

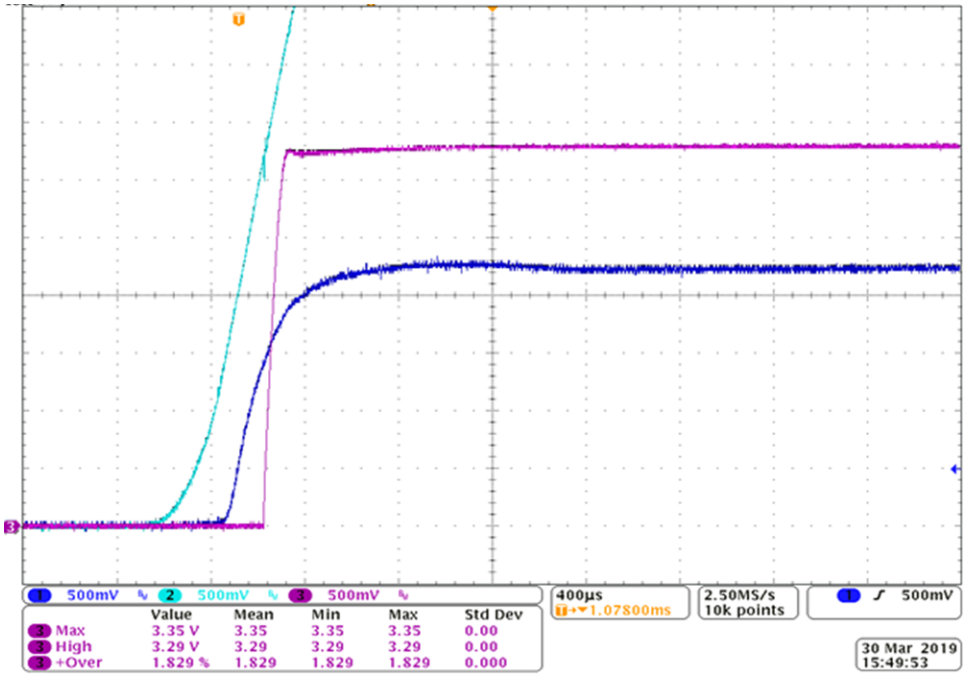

Figure 8. Quick Slew Rate of the V_{IN} Without Overshoot

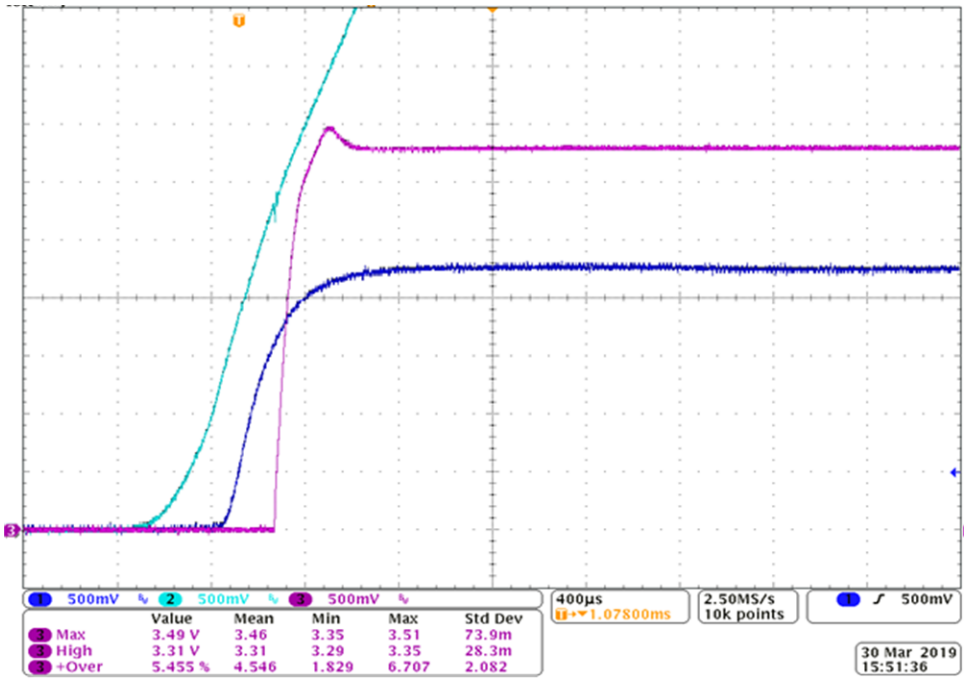

Figure 9. Slow Slew Rate of the V_{IN} with Overshoot

2. Sequence the V_{IN} and V_{EN} signals to let the V_{IN} reach the required value before the LDO is enabled. The comparison is displayed in Figure 10 and Figure 11 (Green: V_{IN}; Red: V_{OUT}; Blue: V_{EN}). The V_{EN} signal is created using a resistor divider from the V_{IN}. R1 = 10 K is close to the V_{IN}, R2 is close to the GND. In Figure 10 R2 = 10 kΩ, and in Figure 11 R2 = 1 kΩ.

3. Overshoot could happen if an LDO starts with a current limit. When the V_{IN} is unable to drive the output to the set voltage; the error amplifier will push the gate voltage of the pass FET to the rail so that the FET switch is fully on. When the output reaches the regulation point, the error amplifier must transition the gate voltage away from the rail. This transition cannot happen immediately, and the output could have an overshoot. This can be confirmed by capturing the output current during the startup of the LDO to see if the LDO is in current limit during startup. If yes, the output capacitance may need to be reduced to lower the in-rush current or an LDO with a higher current limit must be used to avoid overshoot due to current limit.

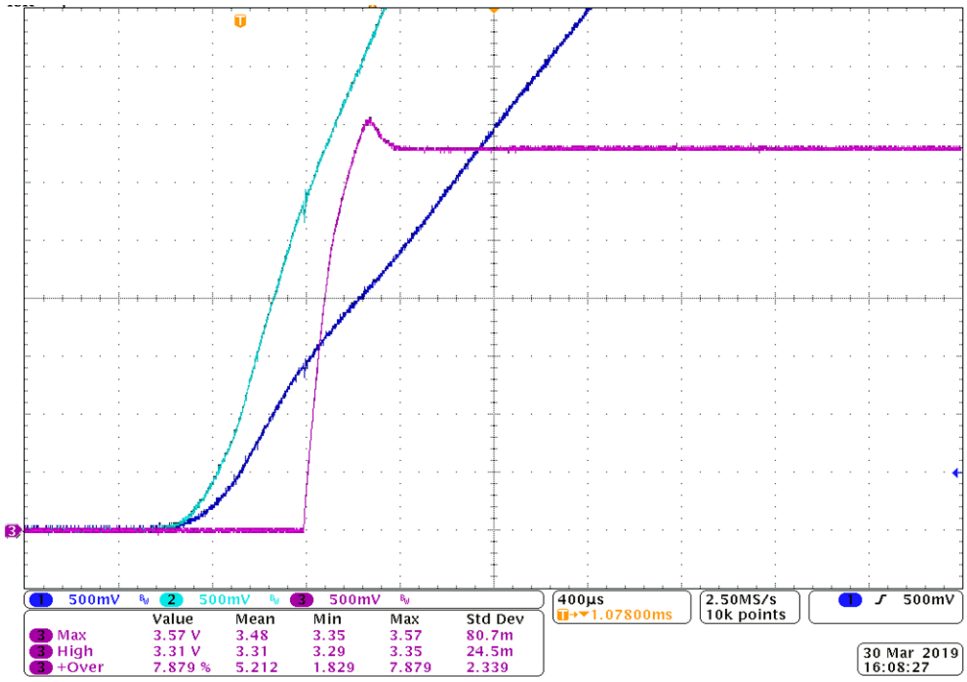

Figure 10. No Sequence With Overshoot

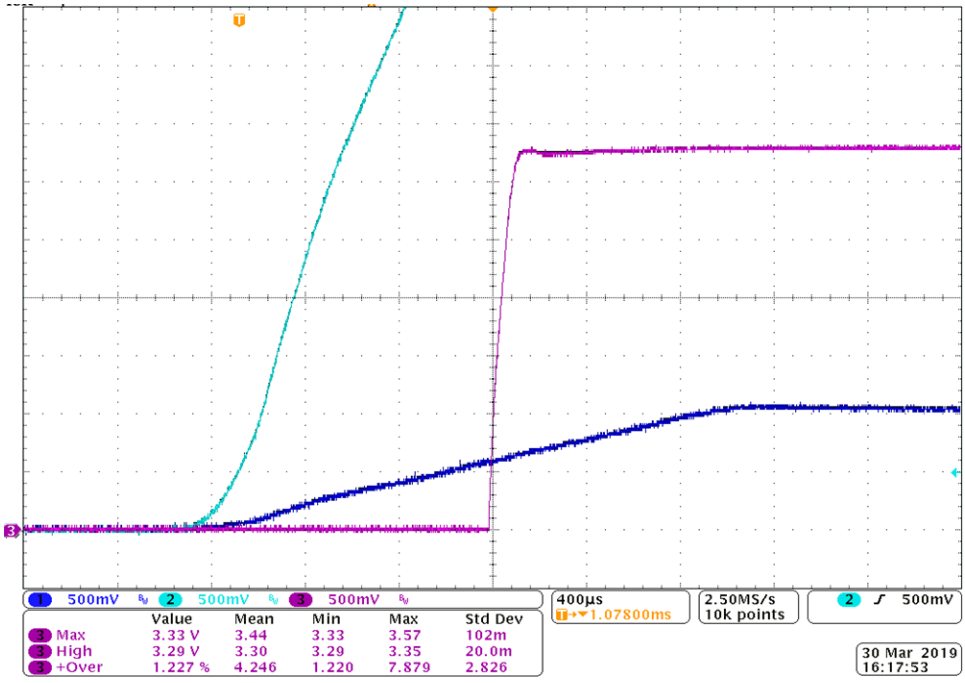

Figure 11. Add Sequence Without Overshoot

4. When using an LDO with an externally controlled soft-start function, such as the TPS7A90, TPS7A02, TPS7A05, TLV767 device, the proper soft-start value, according to the V_{IN} slew rate, is required to avoid an overshoot. Figure 12 displays the test results (Green: V_{IN}; Red: V_{OUT}). The soft-start function makes V_{OUT} take 12 ms to get ready, so there is no overshoot during start-up.

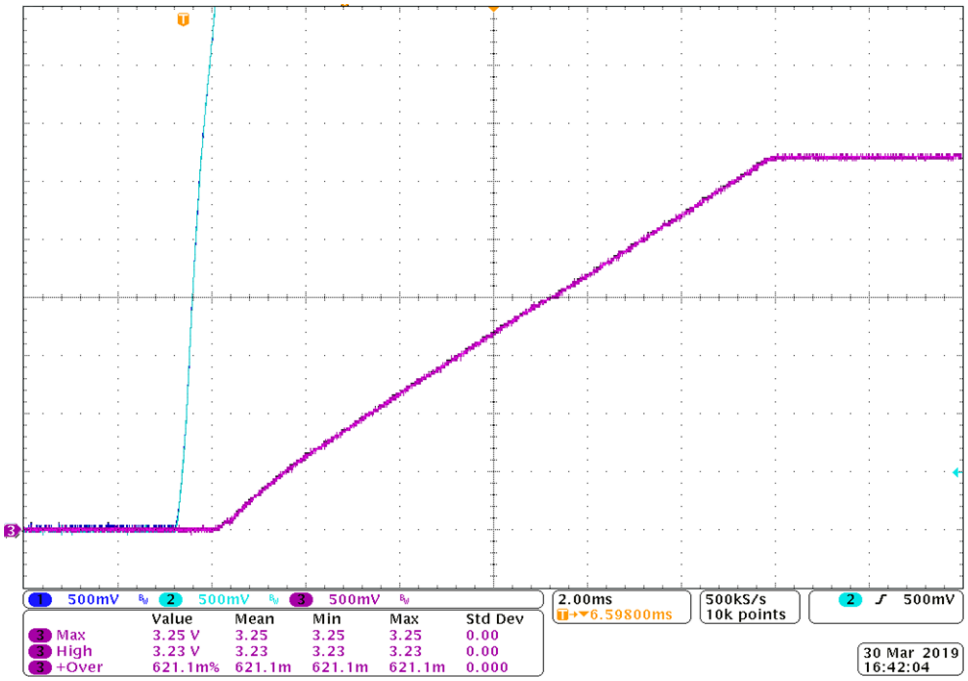

Figure 12. Soft Start With No Overshoot During Start-Up

4 Conclusion

This application report focuses on LDO output voltage overshoots at start up, then analyzes the root cause of the overshoot. Finally, four methods to avoid the overshoot are given, and example EVM test results are shown.

5 References

1. Texas Instruments, *LP2985 150-mA Low-noise Low-dropout Regulator With Shutdown Data Sheet*
2. Texas Instruments, *TPS709 150-mA, 30-V, 1-µA IQ Voltage Regulators with Enable Data Sheet*
3. Texas Instruments, *TPS7A90 500-mA, High-Accuracy, Low-Noise LDO Voltage Regulator Data Sheet*
4. Texas Instruments, *TPS7A02 Nanopower I_Q, 25-nA, 200-mA, Low-Dropout Voltage Regulator With Fast Transient Response Data Sheet*
5. Texas Instruments, *TPS7A05 1-µA Ultralow I_Q, 200-mA, Low-Dropout Regulator in a Small-Size Package Data Sheet*
6. Texas Instruments, *TLV767 1-A, 16-V Precision Linear Voltage Regulator Data Sheet*

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