Application Report

SBVA033–February 2012

TPS75005 Advanced Information: Voltage Monitor Noise Immunity

Masashi Nogawa *Power Management Products*

1 Overview

The TPS75005 is a complete power management solution for C2000™ controllers from Texas Instruments. This document contains supplemental advanced information for the TPS75005 data sheet.

In this advanced information document, the noise immunity of the supply voltage supervisors (SVS) is explained in detail.

2 Noise Created by C2000 Controllers and Reaction of TPS75005

As a result of the high-speed nature of C2000 controllers, they typically couple high-speed clock noise onto their own dc supply inputs. This wideband noise is outside of the bandwidth of the TPS75005 control loop and, therefore, could potentially cause false reset events. In other words, the noise from the controller can be the cause of the false reset. Figure 1 shows an example of the typical noise on the V_{DDIO} (3.3 V) rail when the GPIO pins are toggling. This noise may or may not be manageable by the proper use of bypass capacitors.

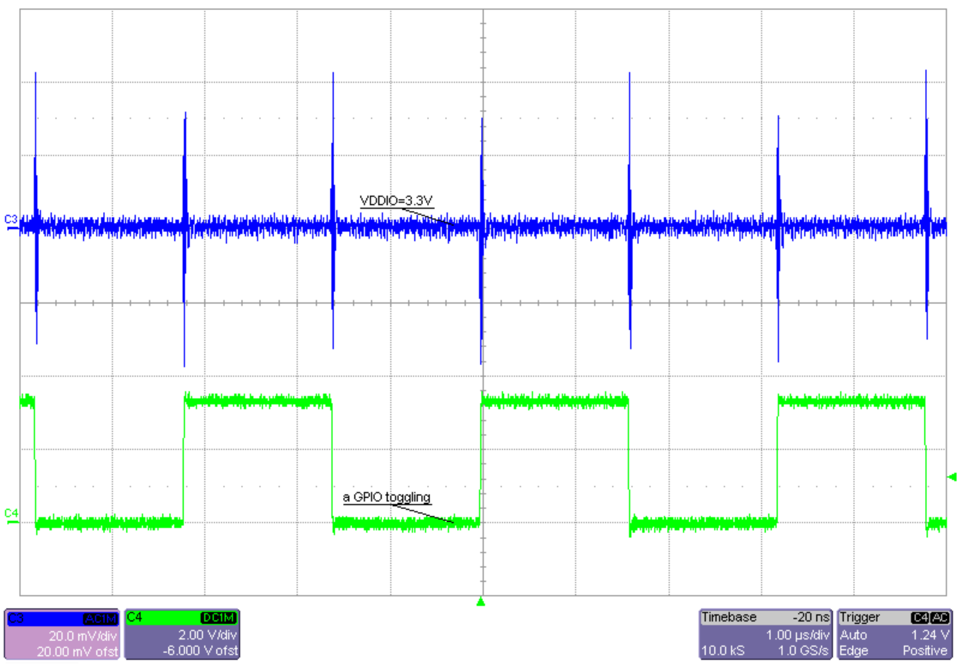

Figure 1. Example of Logic Noise Caused by the C2000

When these noise levels exceed the threshold of SVS1 or SVS2, the TPS75005 may output a reset signal (PG = L) to stop the C2000 controllers. This event can happen very frequently if preventive measures are not taken [(1)] . Common analog practice tells us that such sharp and short period logic noise is not propagated inside the controller silicon; therefore, no reset is required. It is preferable that SVS1 and/or SVS2 do not detect a *power-not-good* condition immediately when a noise pulse occurs.

(1) Note that noise amplitude of Figure 1 is very small and is not hitting the SVS1 / SVS2 threshold at all in this example.

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The TPS75005 device is designed not to react to sharp and short period noise glitches or pulses. The comparators of SVS1 and SVS2 are intentionally designed to be relatively slower than such noise pulses. This performance is specified in the product data sheet by the *minimum pulse width to sense* parameters: $t_{W(SVS1)}$ and $t_{W(SVS2)}$. A (logic) noise glitch shorter than $t_{W(SVS1)}$ or $t_{W(SVS2)}$ is not detected by SVS1 or SVS2 as a power-not-good event.

3 Minimum Pulse Width to Sense

The intentionally desensitized period of $t_{W(SVS1)}$ and $t_{W(SVS2)}$ is achieved by the use of analog circuitry in SVS1 and SVS2. This circuitry causes the duration of $t_{W(SVS1)}$ or $t_{W(SVS2)}$ to be inversely proportional to the negative-going amplitude of the glitch pulse, commonly referred to as overdrive. The larger the amplitude of the pulse, the sooner it is detected by the analog circuitry.

Figure 2 illustrates this relationship by showing the minimum glitch width, $t_{W(SVS1)}$ and $t_{W(SVS2)}$, as a decreasing function of the overdrive amplitude (expressed as a percent of the nominal output voltage).

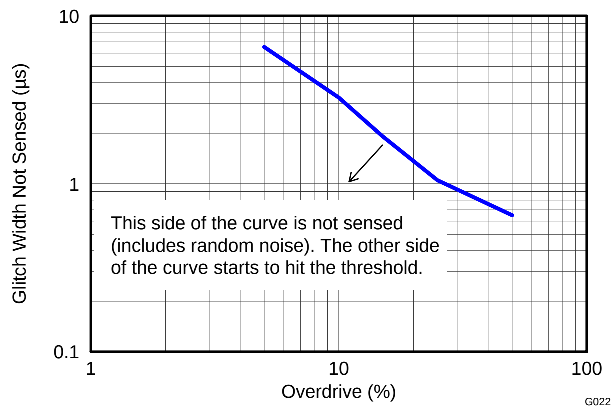

Figure 2. $t_{W(SVS1)}$ and $t_{W(SVS2)}$ Characteristics

A more detailed explanation for the X axis, Overdrive (%), is explained in Figure 3 and Figure 4 by using a 3.3-V rail; this explanation is also applicable to 1.8-V/1.9-V rail. The overdrive number is the amplitude of the negative pulse from its target value of 3.3 V. In Figure 3, negative pulses from its target of 3.3 V to 2.97 V is 10% (= 1 – 2.97 V/3.3 V); in Figure 4, negative pulses from 3.3 V to 2.31 V is 30% (= 1 – 2.31 V/3.3 V).

In Figure 3 and Figure 4, t_{1A} and t_{1B}, respectively, illustrate short, negative pulses that are not detected because of the intentionally desensitized period of SVS1 and SVS2. t_{3A} and t_{3B} illustrate negative pulses that are detected by SVS1 and SVS2 because they exceed the desensitized period. t_{2A} and t_{2B} glitch pulses occur at the sensitivity threshold and may or may not be sensed, depending on the various random noise surrounding the comparators.

Figure 3 and Figure 4 also illustrate the relative difference between a 10% overdrive and a 30% overdrive. In Figure 3, t_{1A}, t_{2A}, and t_{3A} are relatively longer than t_{1B}, t_{2B}, and t_{3B} in Figure 4. This difference is because the larger, negative-pulse amplitude accelerates circuit response time.

In Figure 3 and Figure 4, borderline pulses t_{2A} and t_{2B} may or may not cause a PG transition as a result of random noise; that is the reason that the PG transition for t_{2A} and t_{2B} are drawn using a dotted-line. Figure 2 plots the threshold detection region of the minimum pulse widths that cause a power-not-good transition (PG = L). The comment in Figure 2 means that the lower-left region of curve is where no PG transition occurs, such as with t_{1A} or t_{1B}. The curve itself and upper-right region near the curve shows pulses such as t_{2A} or t_{2B}. The upper-right region away from the curve shows pulses such as t_{3A} or t_{3B}.

By looking at Figure 2, a 10% overdrive gives 3.3 µs of desensitized time; this time is the typical value in the product data sheet. When overdrive increases to 30%, the comparators ignore pulses shorter than 0.9 µs.

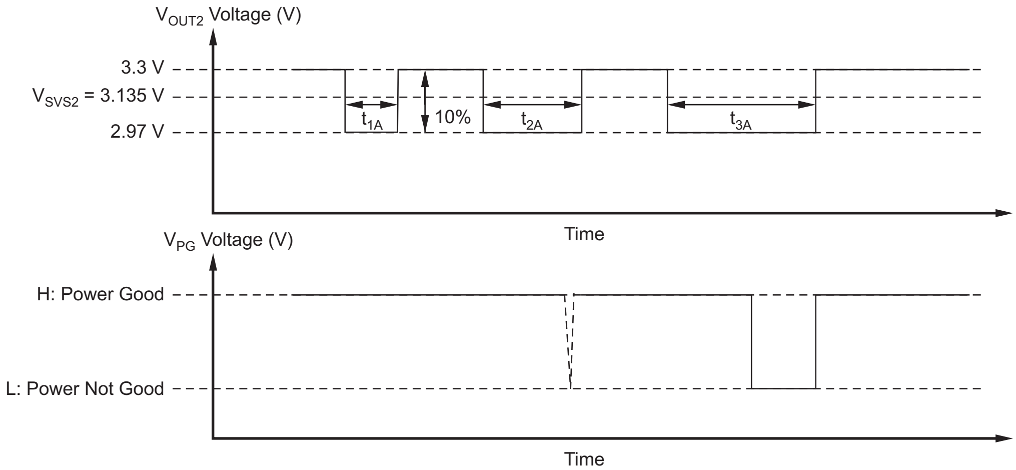

Figure 3. Timing with Overdrive = 10%

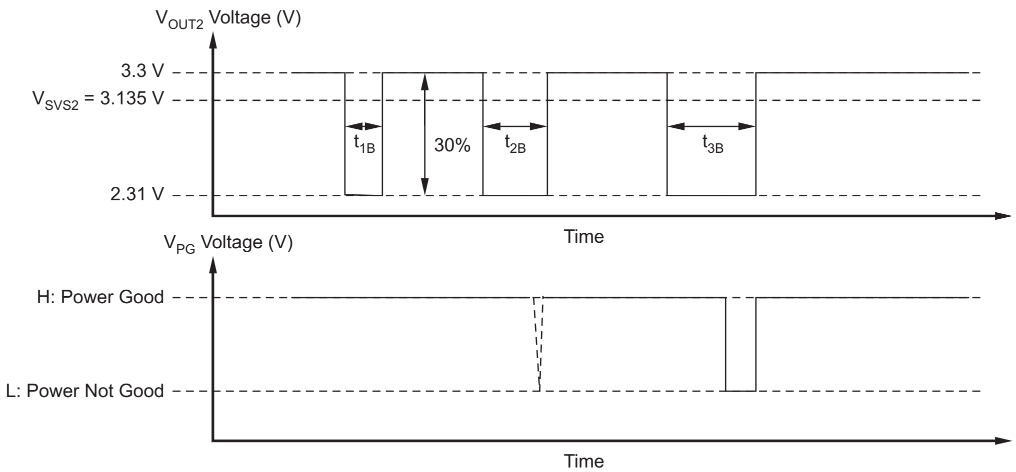

Figure 4. Timing with Overdrive = 30%

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