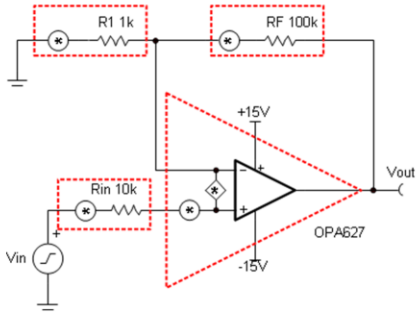
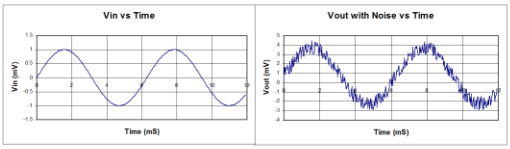
Lecture Manual

TI Precision Labs – Op Amps





$$\sigma = \sqrt{\sigma^2} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(x_i - \mu\right)^2}$$

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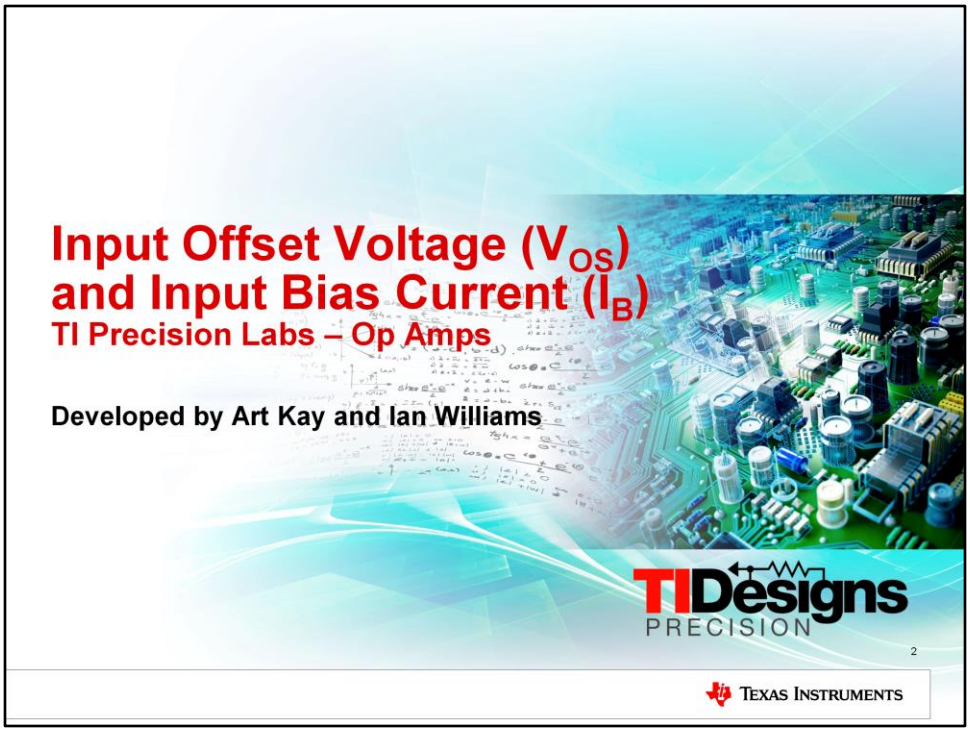
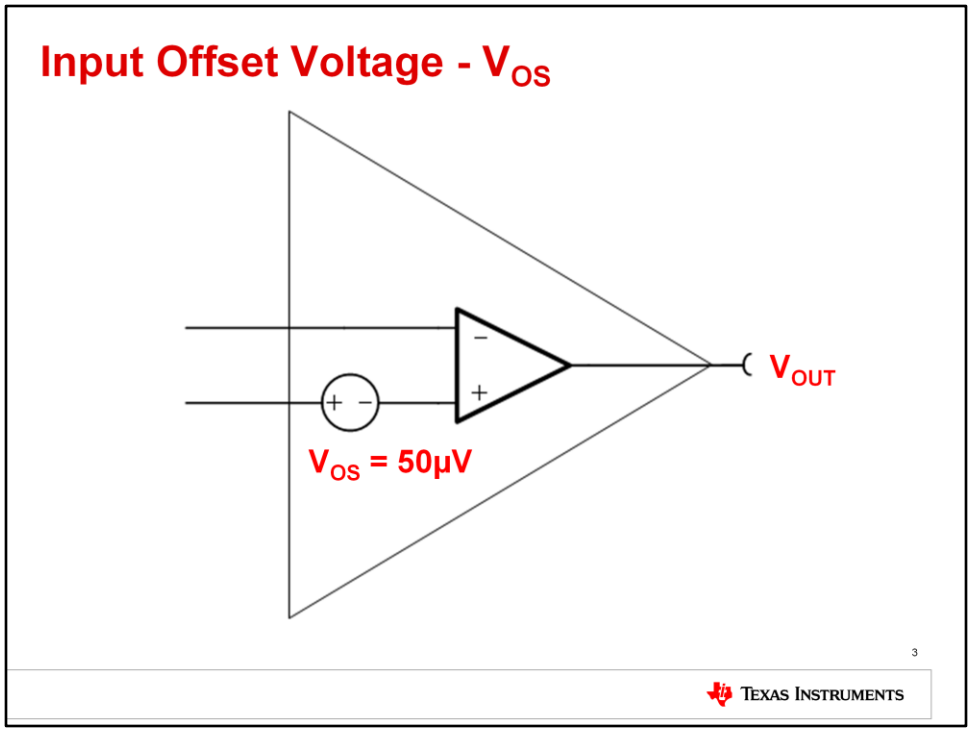
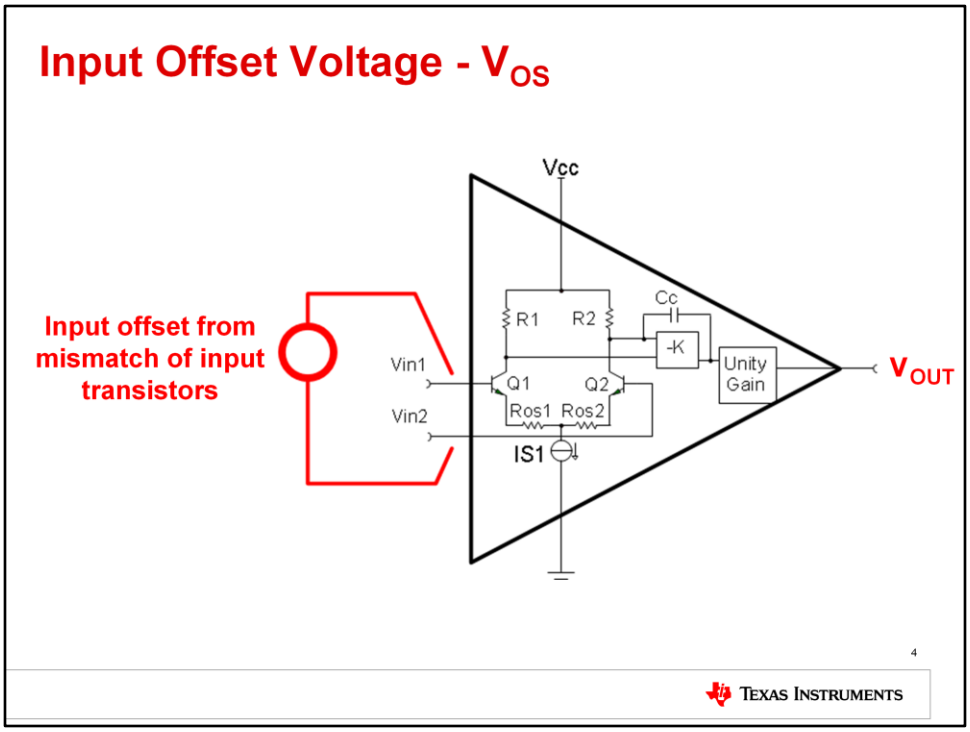


Hello, and welcome to the lecture for the TI Precision Lab discussing input offset voltage, or V_{OS}. In this lecture we'll discuss op amp V_{OS} specifications, V_{OS} drift over temperature, input bias current (or I_B), and input bias current drift over temperature. We'll also show the range of V_{OS} and I_B across many different Texas Instruments op amps.



Let's start by defining offset voltage. Offset voltage is the differential input voltage that would have to be applied to force the op amp's output to zero volts. Typical offset voltages range from mV down to µV, depending on the op amp model. Offset can be modeled as an internal dc source connected to the input of the op amp. Changing power supply voltage and common mode voltage will affect input offset voltage.



Looking at the inside of an op amp, we can see that the mismatch of transistors Q_1 and Q_2 in the differential input pair is what causes the offset voltage. In some cases, internal resistors R_{OS1} and R_{OS2} are laser trimmed in order to compensate for this mismatch and obtain very low offset voltage. In other cases, an internal digital correction circuit is used to minimize offset voltage and offset drift.

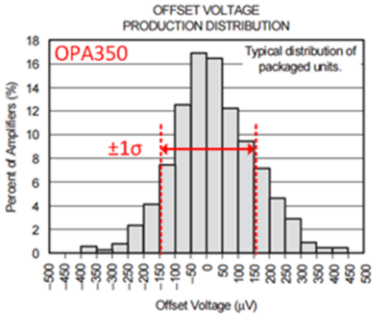
Offset Voltage Specs and Distribution

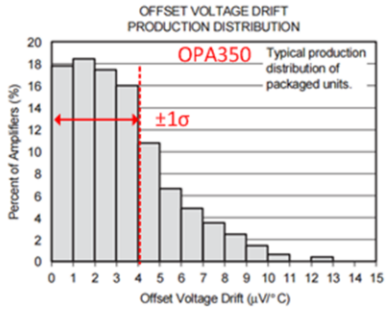
ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, T_A = −40°C to +85°C. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to $V_S/2$ and V_{OUT} = $V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		±150	±500	µV
T_A = −40°C to +85°C					±1	mV
vs Temperature		T_A = −40°C to +85°C		±4		µV/°C





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This slide introduces op amp specifications. The top of the specification table is the test conditions for all the parameters in the data sheet. In this example, the temperature is 25 °C, the load resistance is 1k Ω, the load is connected to mid supply, and the common mode voltage is set to mid supply. These conditions are true unless otherwise specified. If you look at the offset voltage specs, it lists some additional conditions. The supply voltage is 5V.

The value listed in the typical specification will cover ± one standard deviation, or ± sigma, on a Gaussian distribution. This means that 68% of the device population will be less then the typical value. So, in this example, 68% of the devices would have less then ±150 µV of V_{OS}. The maximum is a tested value, and so you will never find a device with greater than the maximum V_{OS} of ±500 µV .

We also have a V_{OS} drift specification that is measured in µV/°C, describing how V_{OS} changes with temperature. In this case the typical drift, which represents +/- 1 standard deviation, is given as 4 µV/°C. For this device, no maximum drift is given. However, the production distribution graph from the data sheet gives the designer an understanding of the drift distribution. Given one standard deviation is +/- 4uV/C, the six sigma value is approximately +/- 12uV/C. This means that about 99.7% of all devices will drift less than or equal to +/- 12uV/C. Put another way, approximately 3 out of 1000 units will drift more than +/-12uV/C.

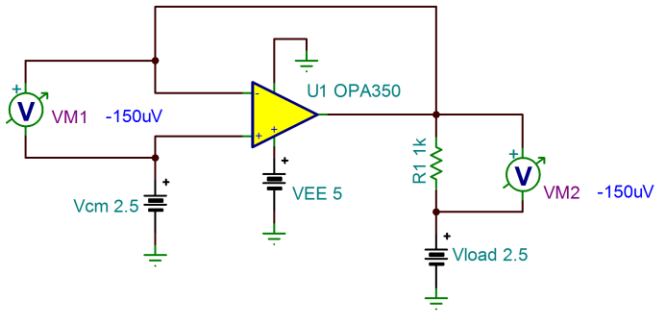
Simulate Input Offset Voltage

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, T_A = −40°C to +85°C. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		±150	±500	µV
T_A = −40°C to +85°C					±1	mV



01 - Vos - OPA350.TSC

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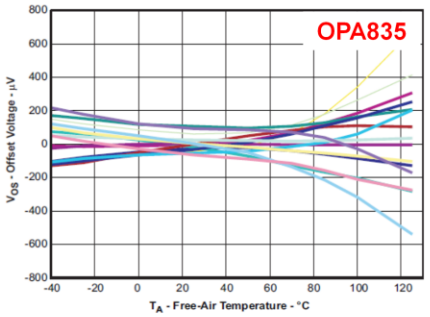
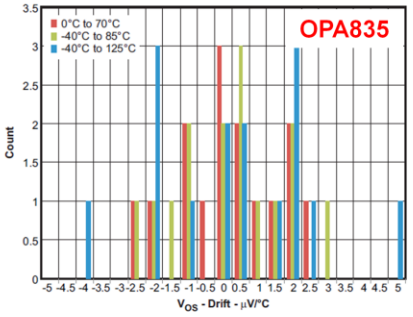
Most op amp SPICE models include the effects of offset voltage. Several external conditions, such as power supply voltage and common mode voltage, affect the offset voltage on a real world device. These effects are also included in the simulation model.

In order for the simulation result to match the offset specifications in the data sheet table, the same test conditions must to be applied to the amplifier. In this example, the power supply is set to 5 V, the common mode voltage is set to mid supply, or 2.5 V, and the load is connected to mid supply in order to match the data sheet conditions. The typical offset specification is 150 µV, and the simulated offset is also 150 µV. The goal of our models is to target typical op amp performance.

Drift Slope – Positive and Negative





For this example V_{OS} drift is defined as:

$$\frac{\Delta V_{os}}{\Delta T} = \frac{V_{os}(T_1) - V_{os}(25C)}{T_1 - 25C}$$

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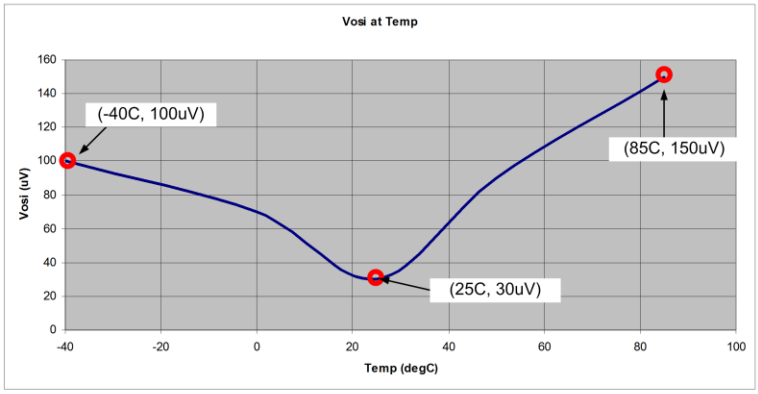
The slope on offset voltage drift can be either positive or negative. This formula shows one possible definition for offset drift. This formula will produce a positive or negative drift depending on the slope of the curve. Some other definitions use the absolute value, so you will not have a negative offset.

Drift Slope – Common Definition



$$\frac{\Delta V_{os}}{\Delta T} = \frac{\left|V_{os}(T_1) - V_{os}(25C)\right| + \left|V_{os}(T_2) - V_{os}(25C)\right|}{\left|T_1 - T_2\right|}$$

$$\frac{\Delta V_{os}}{\Delta T} = \frac{\left|100\mu V - 30\mu V\right| + \left|150\mu V - 30\mu V\right|}{\left|85C - (-40C)\right|} = 1.52\,\frac{\mu V}{^{\circ}C}$$

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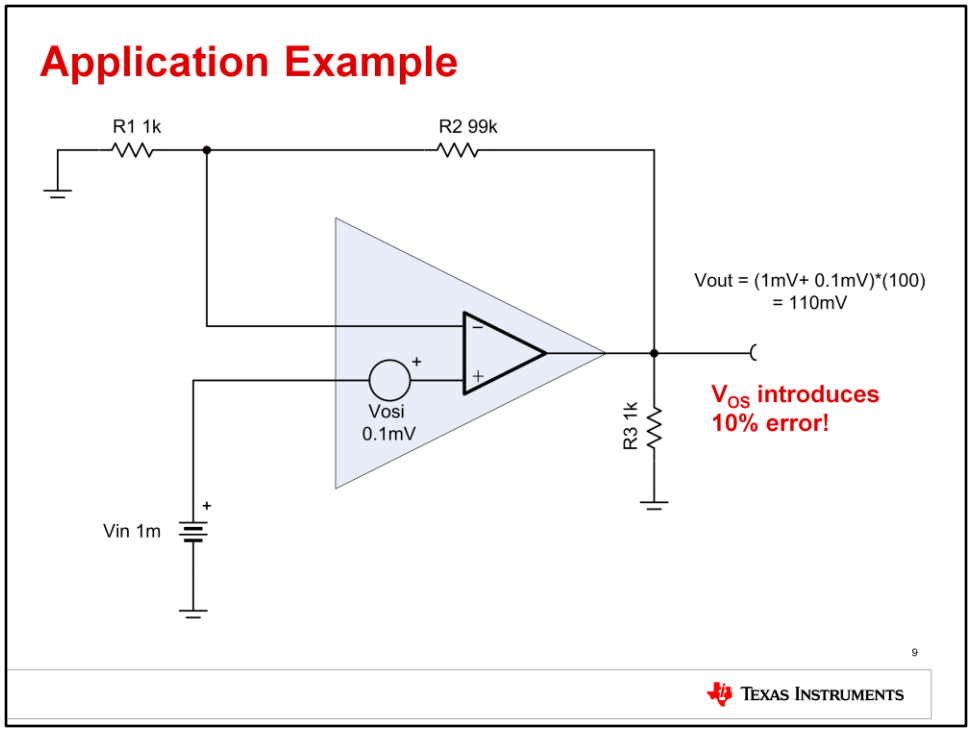
This is the more common definition for drift, which is separated into different two regions, although more than two regions could be used if desired.

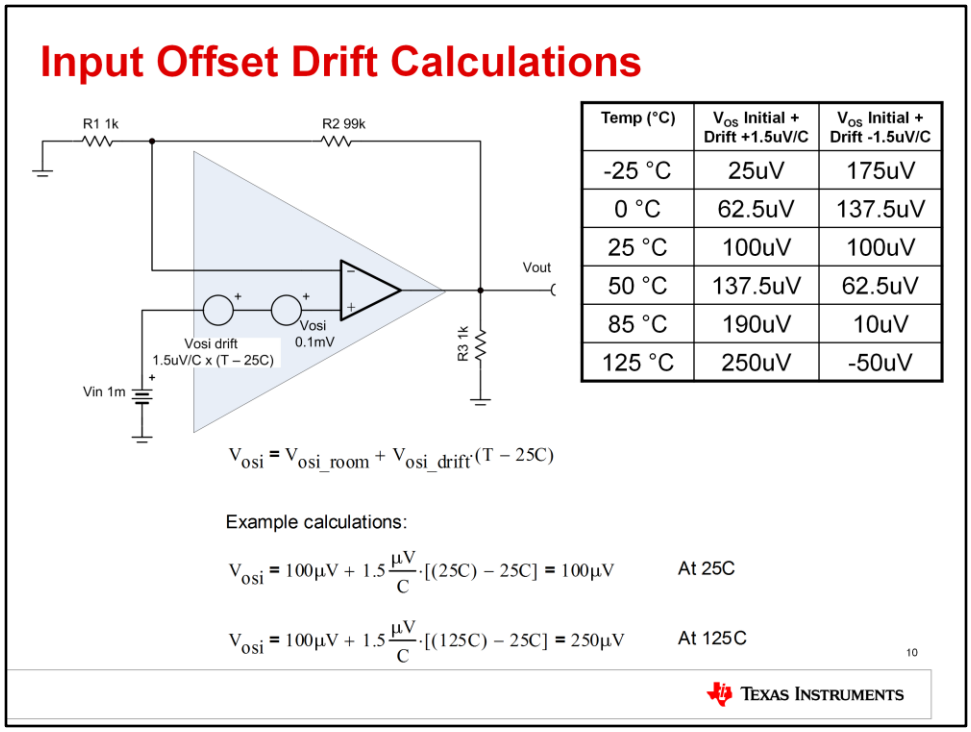
The idea with this definition is that you get a more realistic view of what the expected error would be than if you only considered the end points over the entire region. In this example, you can see that the slope of the two separate regions is much more severe than the drift of the entire range. Note that the absolute value is used in the formula, so this formula will never give a negative result.



In this application example we will see how to calculate the output voltage error from the offset voltage.

Consider offset voltage as a dc voltage source in series with the non-inverting input of the op amp. We have a 0.1mV or 100uV offset in this case. The signal source is a very small input of 1mV, so the offset will generate a fairly significant error. The gain for this part is configured as 100 V/V, which can be calculated as R2/R1 + 1.

The total output voltage is the series combination of the offset and the input signal (1mV + 0.1mV), multiplied by the gain (100), which gives us 110 mV. The offset accounts for about 10% error.



Offset drift calculations can be done in a similar manner. Notice that we have two sources: one for the initial offset and one for the offset drift. The offset drift source will be zero at 25C. As the temperature deviates from 25C, the temperature difference will be multiplied by the offset drift to generate the additional offset voltage.

For example, at 25C we have 100uV of offset, which is just the room temperature offset and no drift term. At 125C we have a total of 250uV; that is, 100uV from the initial offset, and 150uV from the drift term.

The table on the right illustrates how the offset changes over temperature. Keep in mind that the slope of the offset drift can be either positive or negative, so both cases are shown.

Drift is especially important in calibrated systems. In calibrated systems, room temperature offset is frequently measured and corrected for in software. Temperature drift, however, is often difficult and expensive to calibrate out, so devices with minimal drift are preferable.

Range of Offset - µV to mV

Op Amp	V_{OS} (max) (high grade)	V_{OS} Drift (max) (high grade)	Technology
OPA333	10 µV	0.05 µV/°C	Zero Drift CMOS
OPA277	20 µV	0.15 µV/°C	Precision Bipolar
OPA188	25 µV	0.085 µV/°C	Auto-Zero CMOS
OPA192	25 µV	0.5 µV/°C	CMOS
OPA211	50 µV	1.5 µV/°C	Precision Bipolar
OPA827	150 µV	1.5 µV/°C (typ.)	JFET input, Bipolar, Precision
OPA350	500 µV	4 µV/°C (typ.)	CMOS
OPA835	1.85 mV	13.5 µV/°C	High Speed Bipolar
LM741	3.00 mV	15 µV/°C	Bipolar commodity (lower cost)

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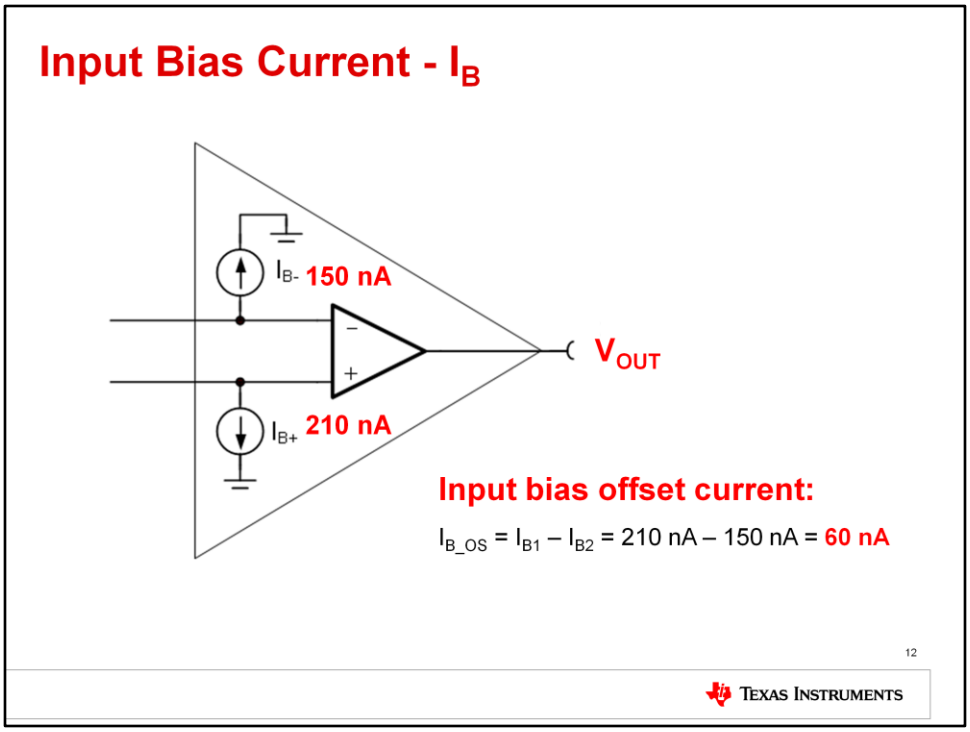
This chart shows a range of offset voltages, from uV to mV, for different types of TI amplifiers.

The first amplifier in the list, the OPA333, includes a zero drift topology which uses an internal digital calibration circuit to minimize offset and offset drift. Some precision bipolar amplifiers use laser trimming to minimize offset.

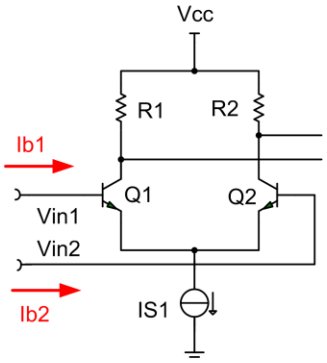
Often you must trade off bandwidth or other characteristics for low offset. For example, the OPA835 is optimized for speed, not for offset. Also, commodity, or low cost amplifiers are usually not optimized for low offset or offset drift.



Let's now move on to input bias current, or I_B, and input bias current drift.

Input bias current is the current flowing into the inputs of an op amp. These currents can be modeled as a current source connected to each input, as shown in this figure. Ideally, the two input bias currents would be equal to each other and would cancel. In reality, though, they are not equal, and the difference of these currents is defined as input offset current. If the input offset current is low, it's possible to match the impedances connected to each input and cancel the offset developed from the input bias currents.

Simple Bipolar, No I_B Cancellation



Bias current in bipolar amplifiers is from input transistor base current. It is typically larger than in FET-input amplifiers and it flows into the input terminals.

Parameter	Test Conditions	LM741C			Units
		Min	Typ	Max	
Input Offset Current	T_A = 25°C		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			300	nA
Average Input Offset Current Drift					nA/°C
Input Bias Current	T_A = 25°C		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.8	µA

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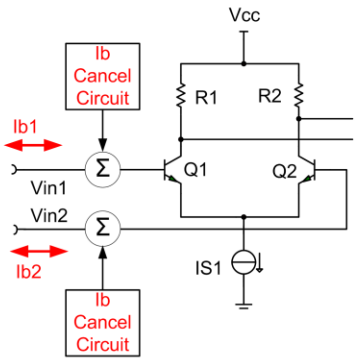
In a bipolar amplifier, input bias current is the current flowing into the base of each transistor in the input pair. Generally, the bias current for bipolar amplifiers is larger than the bias current for MOSFET and JFET amplifiers. Typical numbers are in the nA range. You can see in the case of the LM741C, the input offset current is about 200nA max, and the input bias current is about 500nA max.

Bipolar with I_B Cancellation



The input bias currents are mirrored and summed back in to cancel the bias current. This has the effect of significantly reducing input I_B. Note that when this is done, I_B can flow in both directions. Also, I_{B_OS} is no longer smaller then I_B.

$$I_{B\_OS} = I_{B1} - I_{B2}$$

PARAMETER		CONDITION	OPA277P, U OPA2277P, U MIN	TYP(1)	MAX	
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±1	nA
T_A = –40°C to +85°C					±2	nA
Input Offset Current	I_{OS}			±0.5	±1	nA
T_A = –40°C to +85°C					±2	nA

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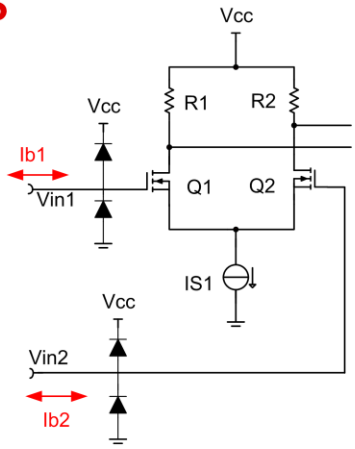
Some precision bipolar op amps use a method called bias current cancellation in order to minimize bias current. This is done inside the op amp, so no external components are required. The amplifier simply behaves like a bipolar amplifier with very low bias current.

Bias current cancellation is done by measuring the input bias current and summing in and equal, but opposite currents which cancel the bias current. This effectively takes an amplifier with hundreds of nA of bias current down to single nA of bias current.

You can see from the specification table in this example that the input bias current of the OPA277 is ±1nA maximum. In the previous example the bias current had to flow into the base of the transistor so the bias current could have only one polarity. In this case, however, the bias current can have either polarity, since the bias current cancelation circuit is not perfect and it's not known whether the polarity of the residual current will be positive or negative.

Bias Current for CMOS

Bias current in FET-input amplifiers is mainly from leakage into ESD protection diodes.



PARAMETER		CONDITIONS	OPA369, OPA2369 MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT						
Input Bias Current	I_B			10	50	pA
over Temperature				See Figure 16		**pA**
Input Offset Current	I_{OS}			10	50	pA

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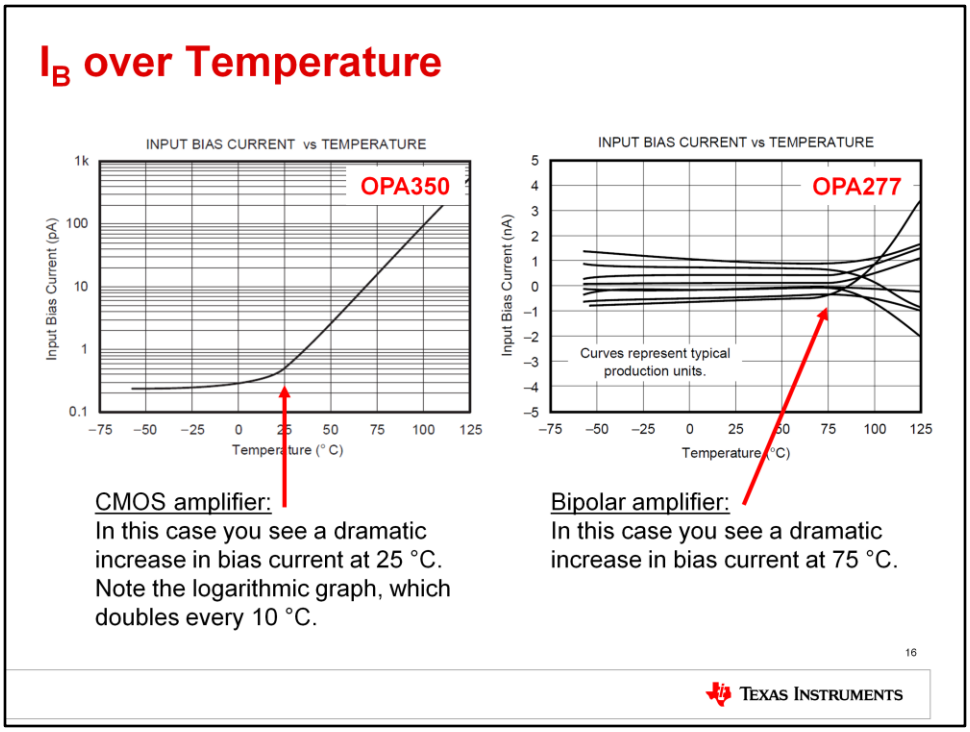
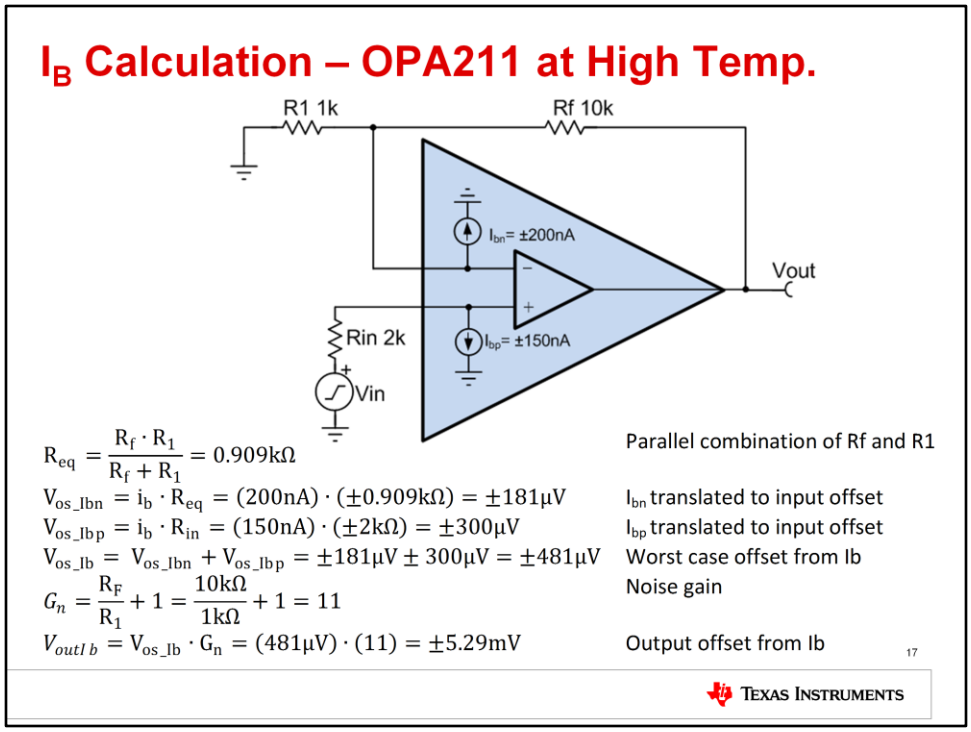
In the case of MOSFET or JFET op amps, the input bias current is primarily due to the leakage of the input ESD protection diodes. The gate of the input MOSFET transistors has extremely low leakage, so it doesn't contribute significant bias current. You can see in this example that the OPA369 has 50pA max of input bias current.



One thing to remember with low bias current amplifiers is the effect of I_B over temperature. In MOSFET amplifiers, the bias current can double every 10°C. You can see in the example on the left with the OPA350 that the input bias current increases significantly at temperatures above 25°C. If you only considered the room temperature value of I_B and then operated the amplifier at elevated temperature, you would have significant errors. Notice that the vertical axis of the plot uses a logarithmic scale.

With the bipolar amplifier, the initial input bias current at room temperature is often large enough such that the relative change in input bias current over temperature is minimized. You can see in the example on the right with the OPA277 that the input bias current starts to increase at temperatures above 75°C, but note that the vertical axis uses a linear scale.



This bias current calculation is very similar to what was done for offset voltage. First, we model the bias currents as two current sources connected to the op amp inputs. Note that an offset error is generated when bias current from the inverting input interacts with the feedback network and also when the bias current from the non-inverting input interacts with the source impedance. The error from the inverting input can be reflected back to the non-inverting input when the bias current is multiplied by equivalent parallel combination of Rf and R1. Reflecting errors back to the non-inverting input is a common practice as it allows all the errors to be added. Finally, to determine the output offset, multiply the input referred error by the non-inverting gain. Note that the non-inverting gain is also called the noise gain. In this case the total error from Ib reflected to the input is ±482µV. This is multiplied by the noise gain of 11 to get an output error of ±5.29mV.

Please keep in mind that this was an error calculation using high temperature I_B values. If this calculation was done at room temperature, the error would have been significantly smaller.

Range of Bias Current – fA to nA

Op Amp	I_B (max) (high grade)	I_B at max temp.	Technology
OPA129	100 fA	20 pA (typ.)	Difet – Ultra Low Bias Current
OPA627	5 pA	1nA	Difet – Precision High Speed
OPA350	10 pA	500 pA (typ.)	CMOS
OPA827	50 pA	50 nA max	JFET input, Bipolar, Precision
OPA333	70 pA	150 pA (typ)	Zero Drift CMOS
OPA277	1 nA	2 nA (max)	Precision Bipolar
OPA211	125 nA	200 nA	Precision Bipolar
OPA835	400 nA	530 nA	High Speed Bipolar
LM741	80 nA	0.2 µA (max)	Bipolar commodity (lower cost)

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This table gives a range of input bias currents for different TI op amps.

Values can range from fA for specialized CMOS amplifiers, all the way up to hundreds of nA for high speed and commodity op amps.

Note that bipolar op amps will always have higher input bias currents then CMOS amplifiers. Also, bipolar amplifiers with bias current cancellation circuitry, such as the OPA277, will have lower input bias current then bipolar op amps with out cancelation, such as the OPA211.

Multiple-Choice Quiz

- Which amplifier type would have the highest bias current?
  a) CMOS
  b) Bipolar
  c) Bipolar with input bias current cancellation
  d) High speed

- Which amplifier type would have the lowest input offset voltage?
  a) Zero drift
  b) High speed CMOS
  c) High speed bipolar

Multiple-Choice Quiz

- Texas Instruments SPICE models target the _____ specifications.
  a) Maximum
  b) Typical
  c) High grade
  d) Low grade

- A typical offset voltage of 10µV indicates _____.
  a) The average offset voltage is 10µV
  b) 100% of the devices will have an offset voltage less than 10µV
  c) 50% of the devices will have an offset less than 10µV
  d) ±1 standard deviation of the tested device distribution is equal to ± 10µV

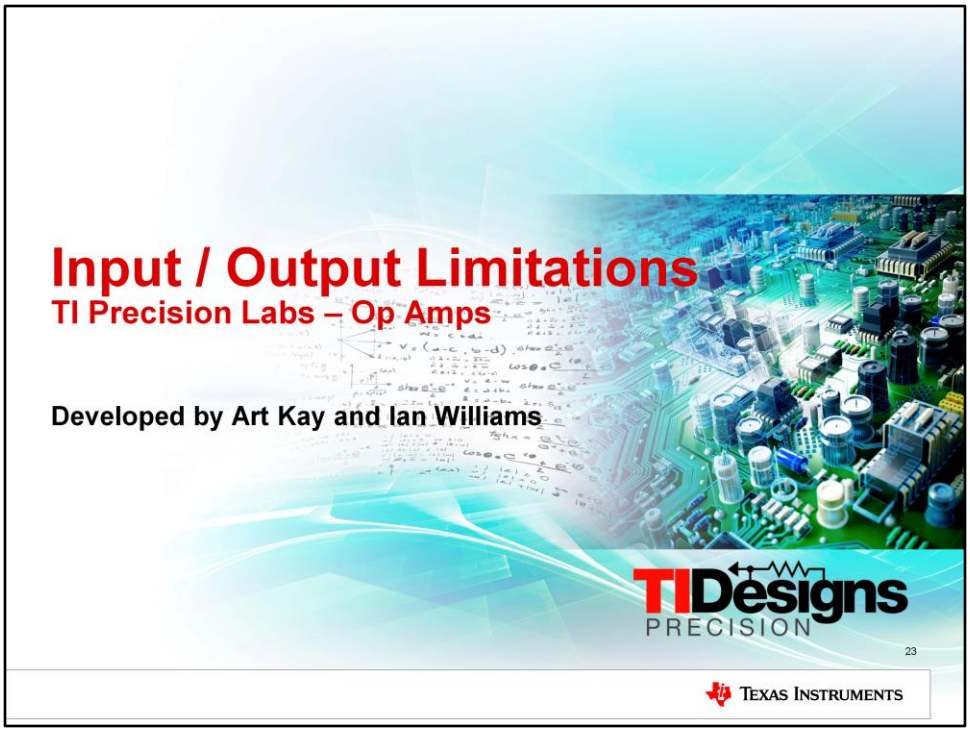
Multiple-Choice Quiz

- A maximum offset of 100µV indicates _____.
  a) 90% of the devices have less than 100µV offset
  b) The device was tested with a 100µV limit and only passing units were shipped
  c) Applying more than 100µV will damage the unit
  d) Offset can range from 0µV to 100µV

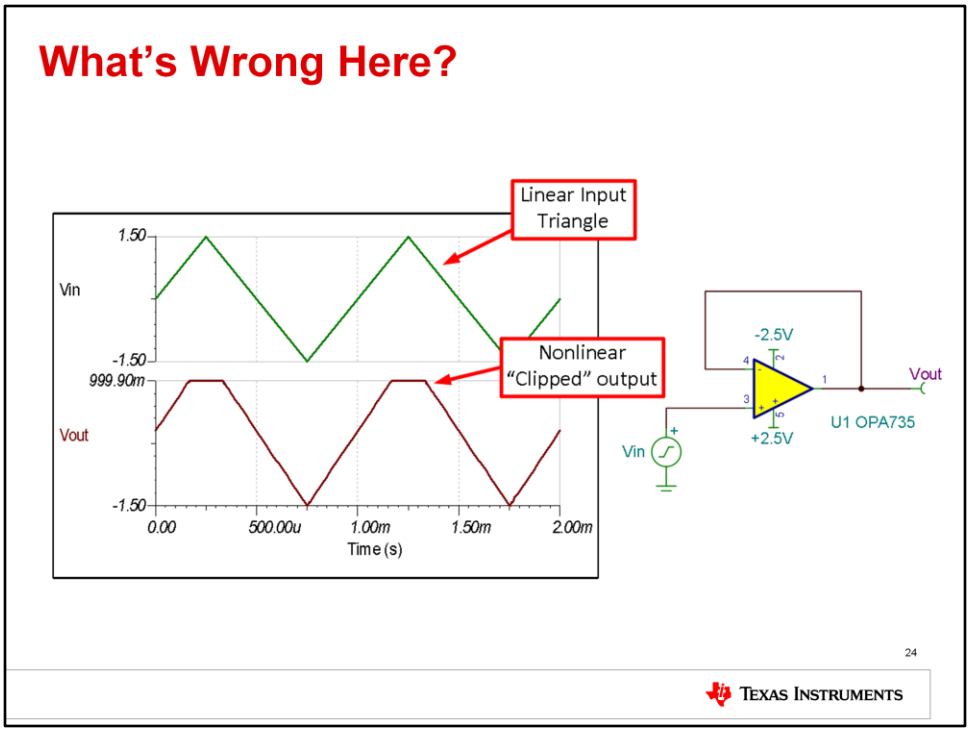
- Bias current is modeled as _____.
  a) A current source in series with each input
  b) A current source connected to each input with respect to ground
  c) A resistance between the amplifier inputs

Multiple-Choice Quiz

- Which are examples of op amp test conditions?
  a) Maximum allowable input signal and supply voltage
  b) Input common-mode voltage, output load, and power supply voltage
  c) Input bias current, input offset current, and input offset voltage
  d) Amplifier gain bandwidth and slew rate

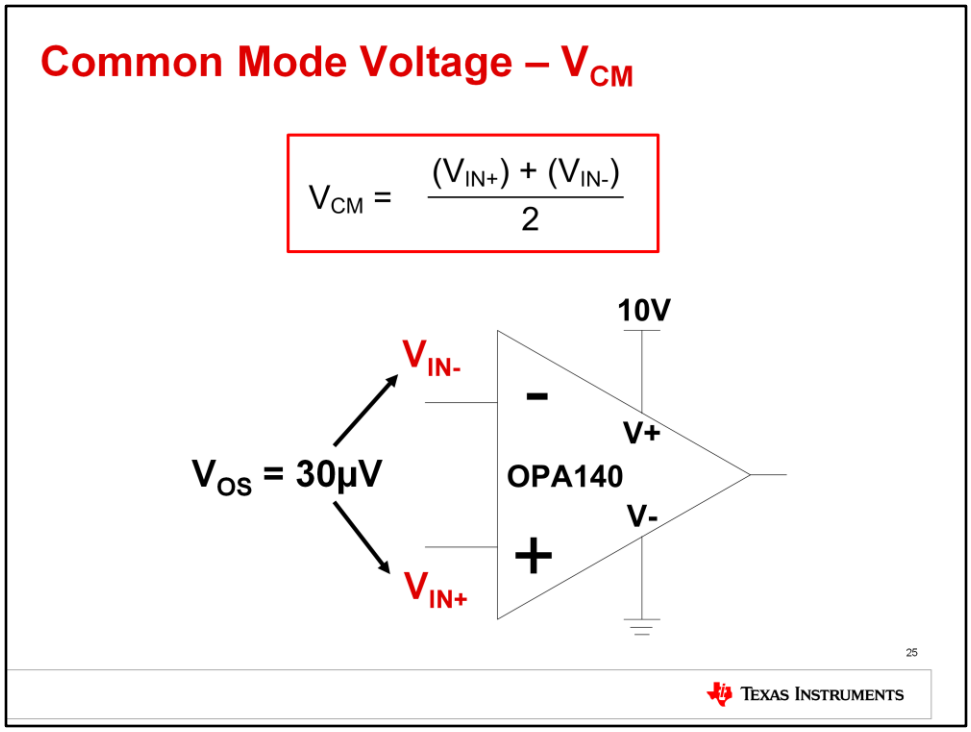


Hello, and welcome to the lecture for the TI Precision Lab discussing op amp input and output limitations. In this lecture we'll discuss op amp common-mode input voltage, input and output voltage swing limitations, and show how to determine the source of circuit errors caused by these limitations.

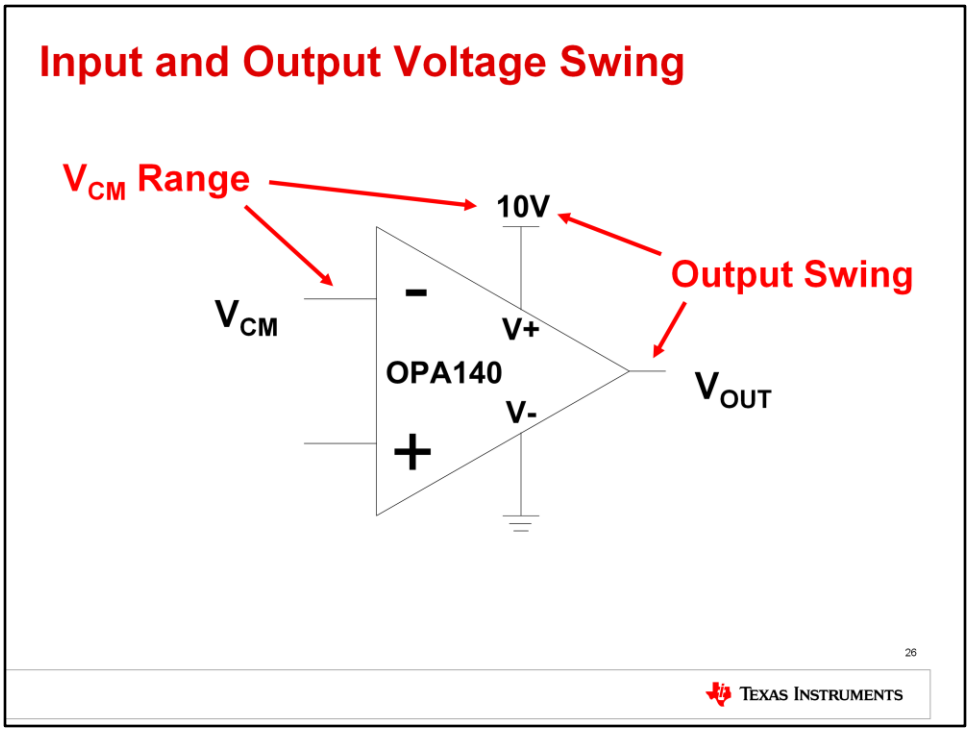


Lets start by considering this simple non-inverting buffer circuit. An triangle-wave input signal of +/- 1.5V is applied to the non-inverting input, and one might expect the output to look exactly the same. For some reason, the op amp output does not increase past +1V. This type of nonlinearity is called "clipping."

What is causing this clipping behavior? We'll answer this question later in the lecture, but first let's define some terms that are necessary to properly understand this issue.

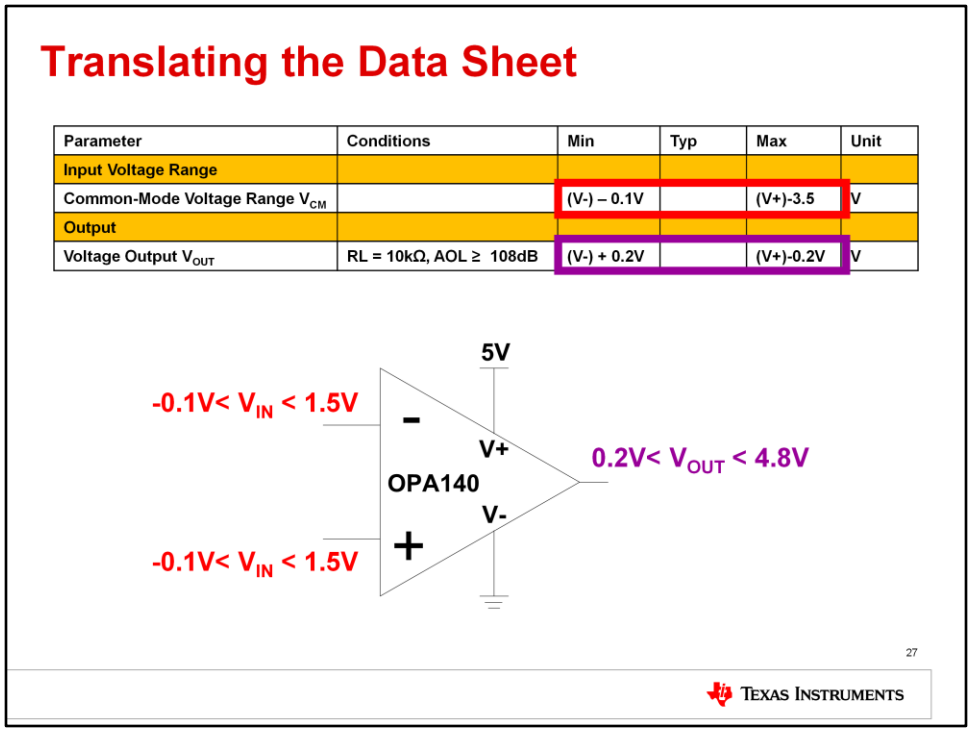


Common mode voltage is defined as the average voltage which is applied to the two inputs of an amplifier. In the case of an op amp, the two inputs are at the practically same potential, with only a small offset between them. So, effectively you can see the common mode voltage on either input.



Common mode input voltage range is also known as input voltage swing. This term describes the range of input common mode voltages that can be used for normal linear operation of the amplifier. The common mode input voltage range is always defined relative to the positive supply and the negative supply. When you exceed the common mode input range, the output becomes nonlinear.

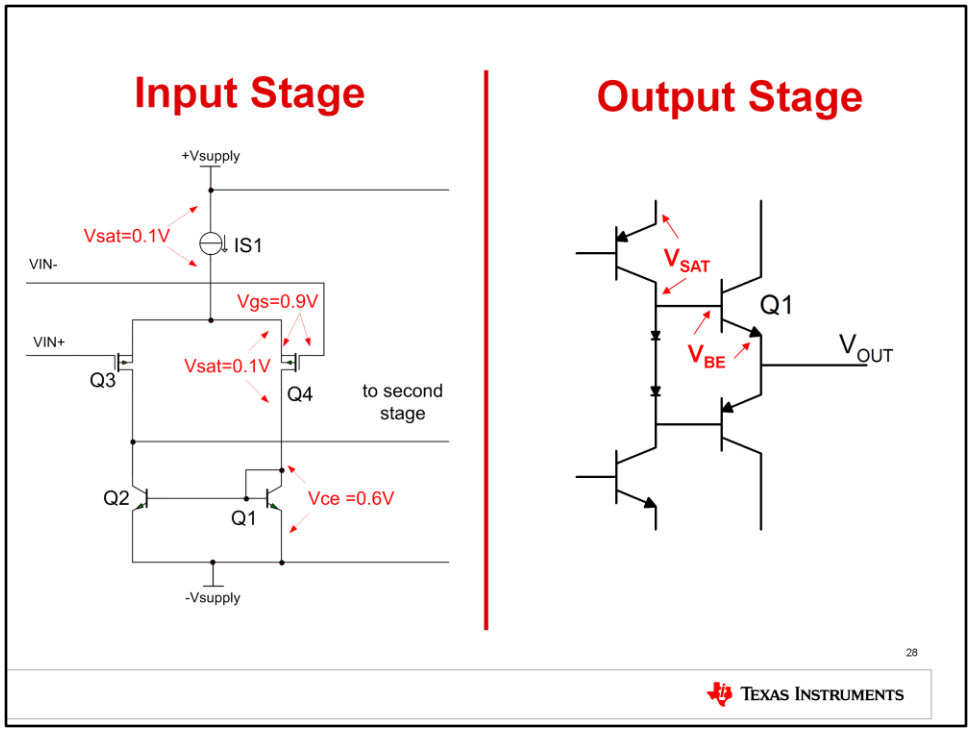
Output voltage swing is the range of output voltages that allow for linear operation of output signals. Output swing is also defined relative to the power supplies. The output signal becomes distorted and non-linear if you exceed the op amp's output swing specifications.



Let's look at how common mode voltage and input and output voltage swing are typically defined on a data sheet.

The common mode voltage range is defined here with the minimum and maximum limits given relative to the power supplies. The negative supply, V-, is zero volts in this case, so zero volts minus 0.1V gives us -0.1V for the minimum common mode limitation. The positive supply, V+, is 5V, so 5V minus 3.5V gives us 1.5V for the maximum common mode limitation. Therefore, applying an input common mode voltage below -0.1V or above 1.5V will result in nonlinear output.

The output swing is given here, and it's the same type of definition which is relative to the supply voltages. The minimum output voltage is V- + 0.2V, or 0.2V in this case, and the maximum output voltage is V+ - 0.2V, or 4.8V. Driving the output below 0.2V or above 4.8V will cause the output to become nonlinear.

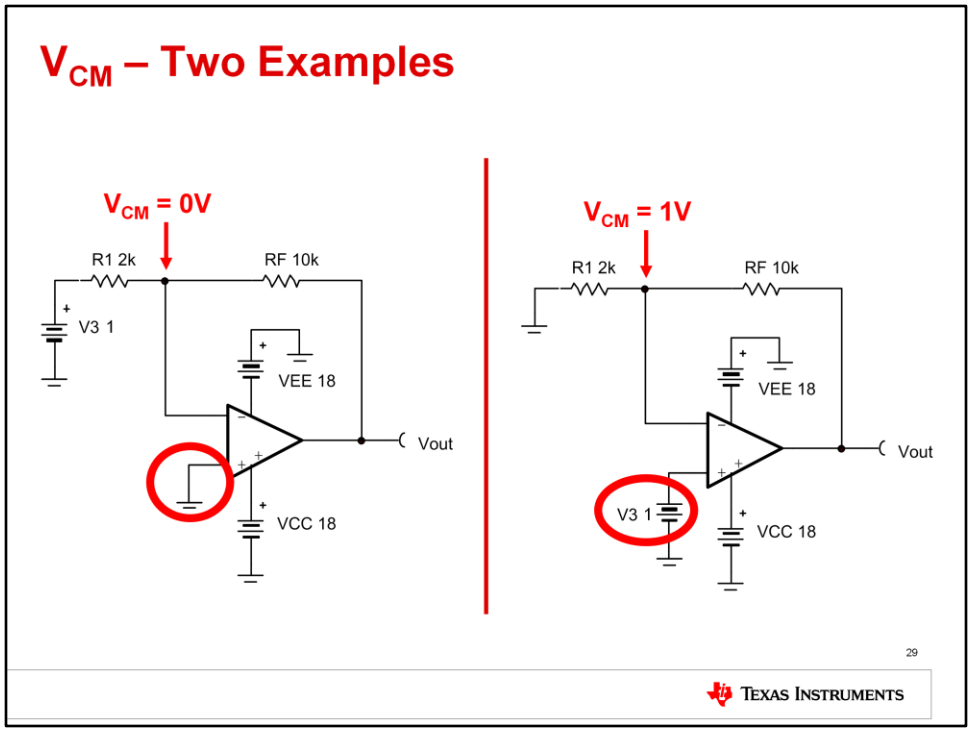


Let's discuss what elements inside the amplifier actually cause the input and output limitations.

On the left you can see a typical CMOS input stage. As the common mode input signal approaches either the positive or negative supply, the input transistors will either saturate or cutoff. Saturation and cutoff are both nonlinear modes of operation, so the amplifier cannot linearly amplify the input signal. This is what causes the common mode input voltage limitation. Please keep in mind that some CMOS amplifiers have common mode limitations which are very near or even beyond the power supply rails.

The output stage voltage swing limitation caused by the saturation and diode drops on internal transistors. CMOS amplifiers tend to have better output voltage swing limitations, because CMOS transistors can have lower saturation voltages.

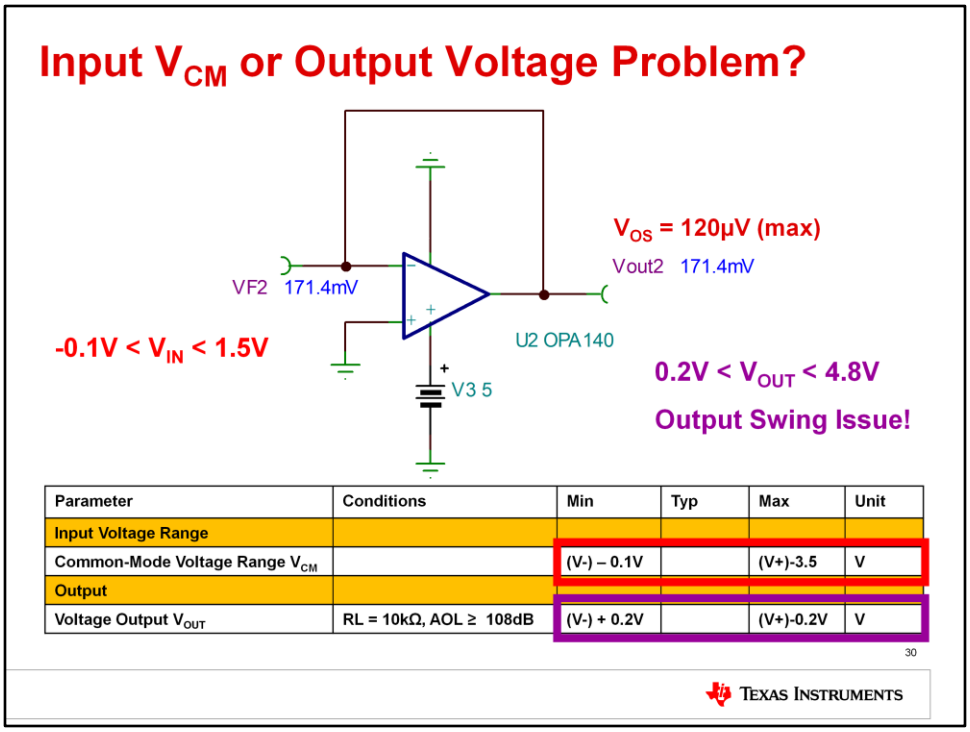
Amplifiers which can accept common mode input voltage ranges up to the power supply rails, and can swing the output voltage near the supply rails, are referred to as rail-to-rail amplifiers.



Here are two example circuits which have very different common mode considerations.

The op amp in the circuit on the left is in an inverting configuration, and notice that the non-inverting input is connected to GND, or 0V. Because of the basic properties of op amps, the inverting input will also be at approximately 0V. Therefore, the common mode input voltage of this circuit is 0V, and stays at a constant 0V regardless of the input signal. This is a good topology to use to avoid common mode limitations.

The op amp in the circuit on the right is in a non-inverting configuration, and the input signal is connected to the non-inverting input. The input signal and the common mode signal will track each other – in other words, when the input signal changes, the common mode signal will also change. Care must be taken in this configuration to avoid exceeding the common-mode voltage limitations of the amplifier.

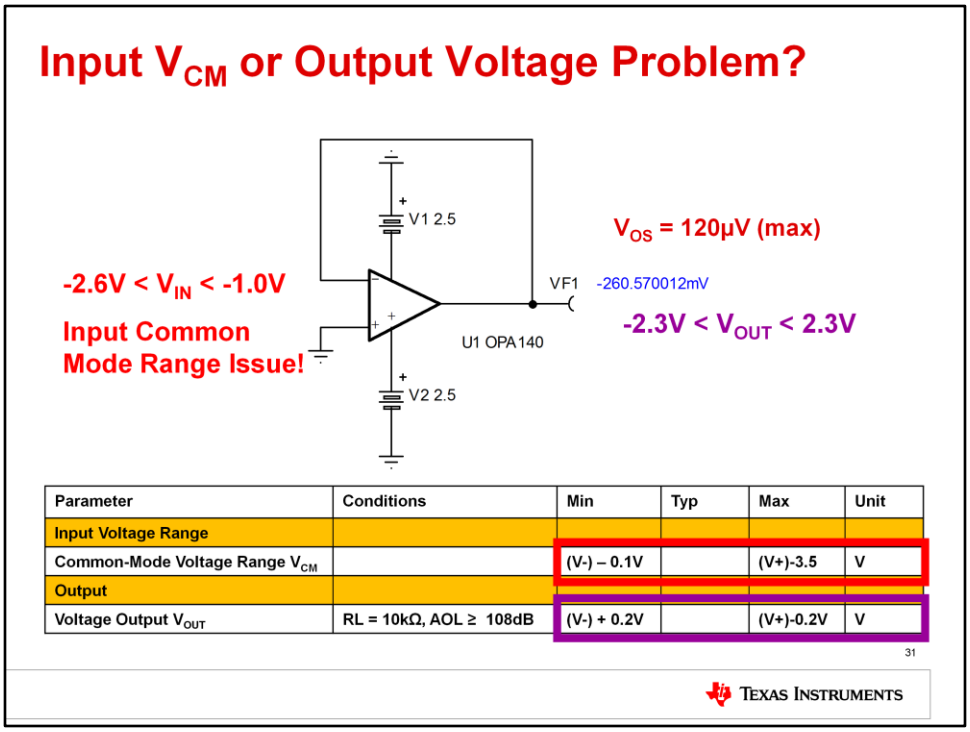


Let's now consider a real-world circuit example.

We have an op amp in a basic buffer configuration. One might expect to see 0V at the output, or a small offset depending on the V_{OS} specification of the device. However, after running a DC simulation we see that the output is almost 200mV! The maximum V_{OS} is only 120µV, so what's the problem?

First let's look at the input common mode range. Using the same technique as before, we can compute the common mode range to be from -0.1V to 1.5V. The input is connected to GND, or 0V, which is between the common mode limits of -0.1V and 1.5V, so there is no common mode input voltage violation.

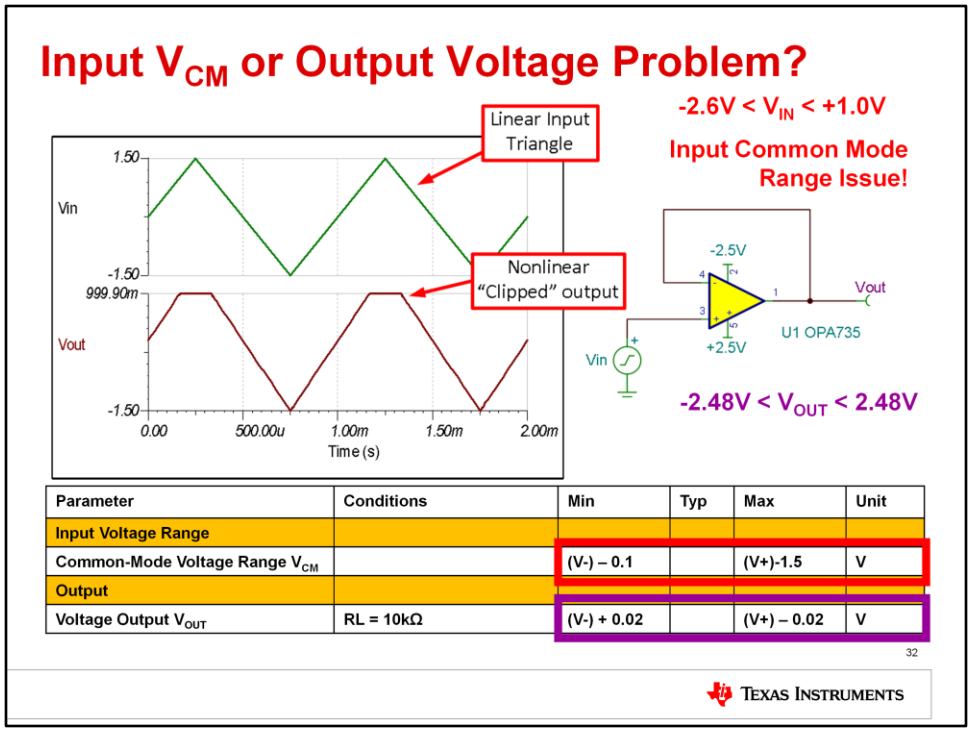
Now let's look at the output voltage swing range. Again, we can compute the output range to be from 0.2V to 4.8V. Based on the input signal, the amplifier wants to drive the output to 0V, but this is below the minimum output of 0.2V! Therefore the output voltage range is being violated, which causes the actual output to clip nearly the 0.2V limit, at 171mV.



Lets look at another example. Note that this circuit has a different power supply arrangement, where the supplies are +/-2.5V.

Let's first consider the output voltage range. Using the data sheet specifications and the given power supply voltages, the output range is calculated to be from -2.3V to +2.3V. The amplifier wants to drive the output to zero 0V, and zero is inside the output range, so this circuit does not have an output voltage swing violation.

What about the input? The applied input common mode voltage is zero volts as in the previous circuit, but the input common mode voltage range is now from -2.6V to -1V. 0V is above that range, so we have a violation of the input common mode range. That is why we see hundreds of millivolts at the output, rather than microvolts.



Finally, let's return to our original problem of output voltage clipping past 1V on the OPA735.

Let's first consider the output voltage range. Using the data sheet specifications and the given power supply voltages, the output range is calculated to be from -2.48V to +2.48V. The amplifier wants to drive the output from -1.5V to +1.5V, which is within the normal output range, so this circuit does not have an output voltage swing violation.

What about the input? Again, using the data sheet specifications, the allowed common-mode voltage range is calculated to be from -2.6V to +1V. Because this op amp is in a non-inverting buffer configuration, the VCM tracks the input, which is from -1.5V to +1.5V. Since the maximum VCM is +1V, we are exceeding the maximum by applying a triangle wave up to +1.5V. This violates the input common mode range and saturates the input stage transistors, so the output clips at 1V.

Multiple-Choice Quiz

- An amplifier's common-mode voltage is _____.
  a) The maximum input voltage
  b) The minimum input voltage
  c) The average of the voltage applied to the inputs
  d) The differential input voltage

- Exceeding the common-mode input range will _____.
  a) Cause a nonlinear response
  b) Cause damage to the device
  c) Draw excessive current
  d) Limit the circuit's bandwidth

Multiple-Choice Quiz

- Input and output swing limitations are _____.
  a) Given relative to the power supply voltage
  b) Guidelines for preventing damage to the devices
  c) Calculated using Ohm's Law
  d) Are only valid for DC signals

- An inverting op amp configuration has a constant common-mode voltage regardless of the input signal.
  a) True
  b) False

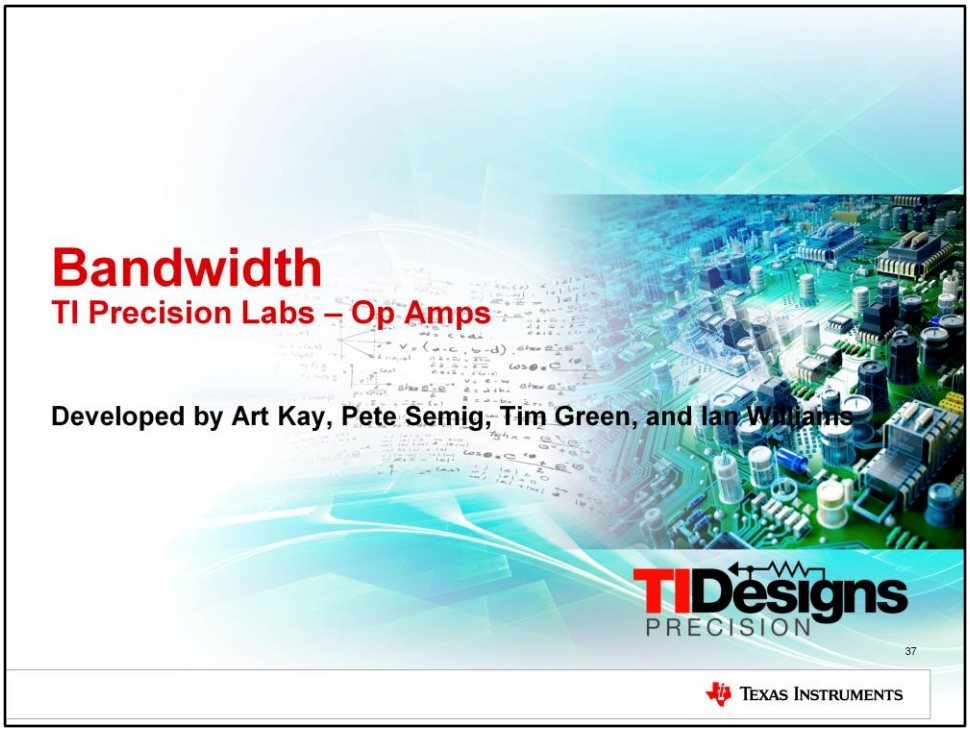
Multiple-Choice Quiz

- A non-inverting op amp configuration has a constant common-mode voltage regardless of the input signal.
  a) True
  b) False

- A rail-to-rail input amplifier allows common-mode signals _____.
  a) Near ground
  b) Near the positive power supply
  c) That cover the full range from positive to negative supply
  d) To be applied without damaging the device

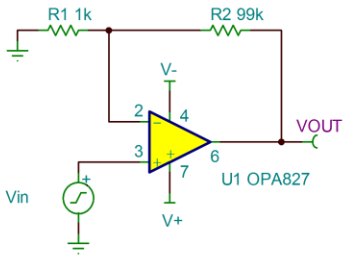
Multiple-Choice Quiz

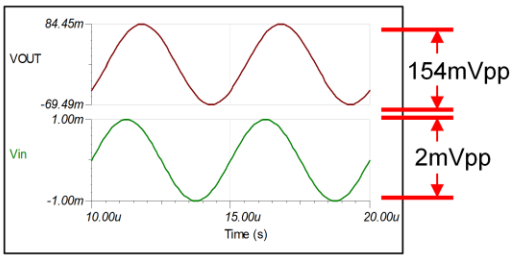
- What causes the common-mode limitations in amplifiers?
  a) Overheating semiconductor junctions and ESD diodes
  b) Internal capacitance and inductance
  c) Transistor and polysilicon resistor scaling
  d) Saturation and cutoff transistors in the input stage

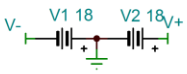


Hello, and welcome to the lecture for the TI Precision Lab discussing bandwidth. In this lecture we'll discuss an op amp's gain bandwidth product, the op amp's dominant pole and its impact on bandwidth, and the difference between inverting and non-inverting op amp configurations. Finally, we'll compare the bandwidth versus quiescent current of several TI amplifiers.

What is the Problem?







$V_{in} = 2mV_{pp}$ $G_{CL} = 1 + \frac{R_2}{R_1} = 1 + \frac{99k\Omega}{1k\Omega} = 100\frac{V}{V}$

$V_{out-calc} = V_{in} \times G_{CL} = 2mV_{pp} \times 100\frac{V}{V} = \boxed{200mV_{pp}}$

$V_{out-sim} = \boxed{154mV_{pp}}$

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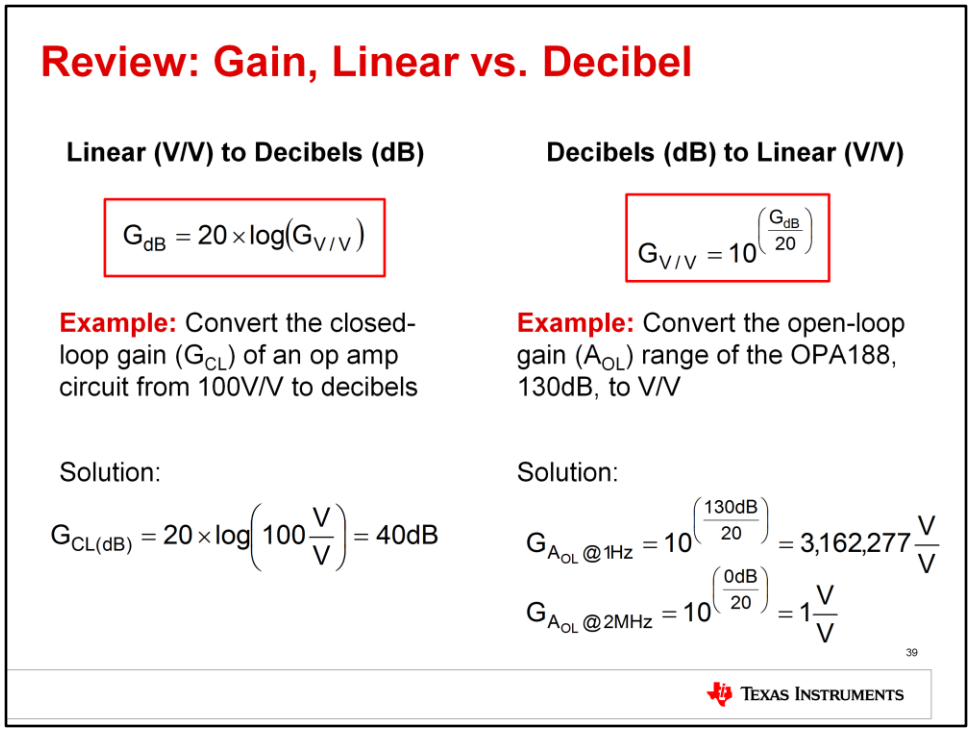
In this transient simulation, the OPA827 is set up in a non-inverting configuration with a closed loop gain of 100V/V. The input signal, Vin, is 2mVpp. The product of the input signal and closed loop gain is 200mVpp.

When simulated, however, the output voltage is only 154mVpp. Why?

In order to answer this question, we need to fully understand the concept of bandwidth. First, let's review a few topics.



When working with electronics we often need to express quantities such as op amp gain, signal-to-noise ratio, common-mode-rejection ratio, and power supply rejection ratio whose values have very large spans.

Therefore it is important to have a mechanism upon which we can represent a large range of values while using small numbers. This mechanism is called the 'decibel', or 'dB' for short. Note that decibels have no units.

This slide shows how to convert linear gain values to dB and vice versa.

This equation shows how to convert from a linear gain in volts per volt to decibels. For example, let's convert the closed loop gain of an op amp circuit from 100V/V to decibels.

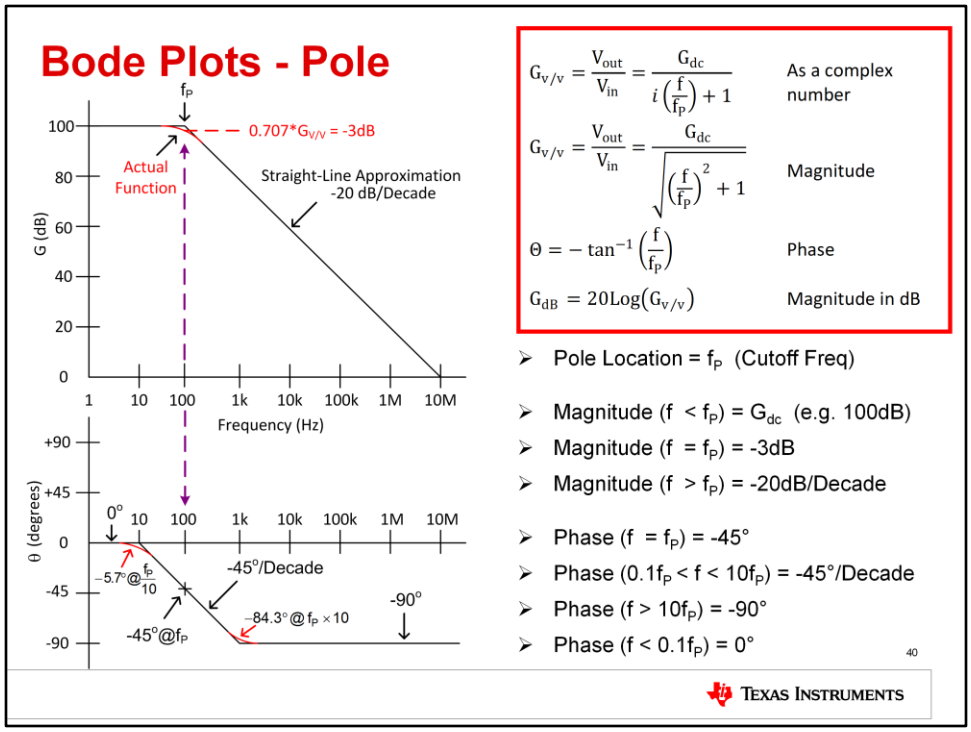
Substituting 100V/V for the linear gain in the given equation yields 40dB.

Similarly, given a gain in decibels we can convert it to a linear representation using this equation.

While the previous example may not seem like a significant improvement in representing large numbers, let's look at the open loop gain, or Aol, of the OPA188. At 1Hz, the open loop gain is 130dB, which equates to a linear gain of 3,162,277V/V.

At 2MHz the open loop gain is 0dB, which equates to a linear gain of 1V/V.

Ultimately we find it's much easier to represent such a large range of values using decibels instead of volts per volt.



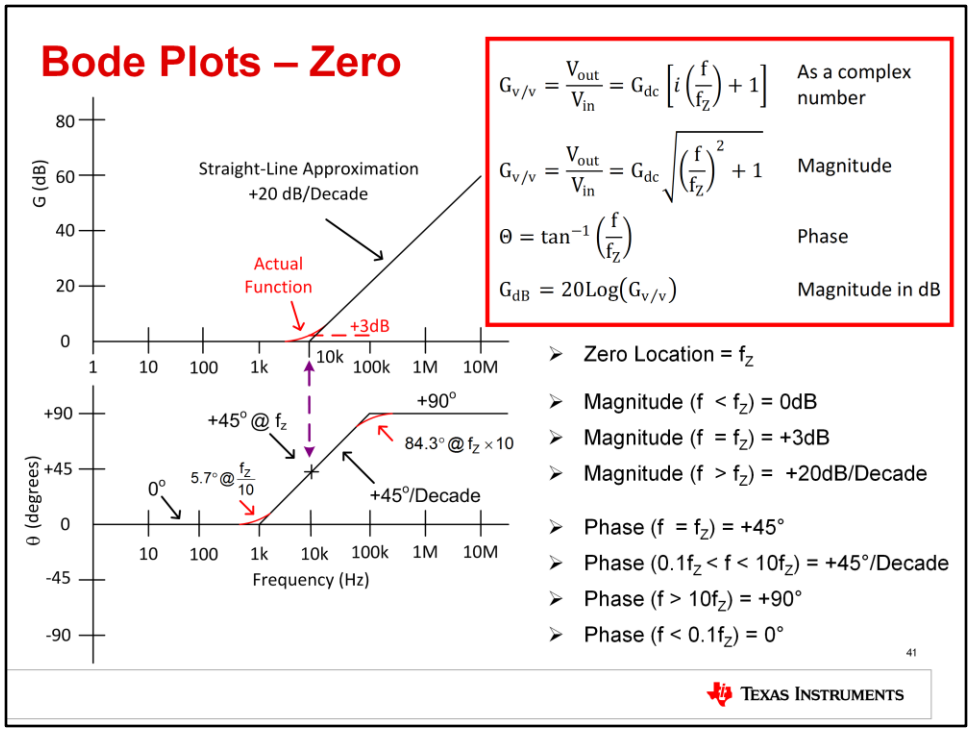
This slide illustrates the equations for a pole and its associated response. Later we will provide a real world circuit example for a pole. Looking at the equations, you can see that the first equation represents a pole as a complex number. Complex numbers have a real and imaginary part. For practical circuits the complex function is converted to a magnitude and phase. The second equation shows the magnitude and the third equation shows the phase. As discussed earlier 20*log base 10 of the linear gain yields the gain in decibels.

The graphs show the magnitude in dB as well as the phase in degrees. This type of plot is called a Bode plot. Notice that both the horizontal axis and vertical axis are logarithmic. Let's look at some key points on the bode plot. First, the pole frequency as denoted by f_P. For frequencies below f_P the gain is constant and is denoted G_{DC}. In other words, the gain at dc or zero frequency would be G_{DC}. In this example G_{DC} = 100dB. Also notice that the gain at f_P is attenuated by 3db, or is 0.707 times the dc gain. Finally, for frequencies greater than f_P, the magnitude plot rolls off at a rate of -20dB/decade.

Now let's consider the graph of phase shift vs. frequency. The phase shift at the pole frequency is -45 degrees. Phase begins to change one decade before the pole and stops changing one decade after the pole. In this region the slope is -45 degrees per decade. Considering frequencies that are lower

than one decade below the pole, the phase shift is 0 degrees. For frequencies greater than one decade beyond the pole the phase shift is -90 degrees.

Notice that bode plots and phase plots are drawn using straight line approximations. In reality the function will deviate from this approximation. For example, if you consider the points exactly one decade below and above the pole on the phase curve. The straight line approximation shows the value at these points to be 0 degrees and -90 degrees respectively. However, the actual function deviates slightly from the straight line approximation. In practice, simulation software can be used to obtain the actual values.



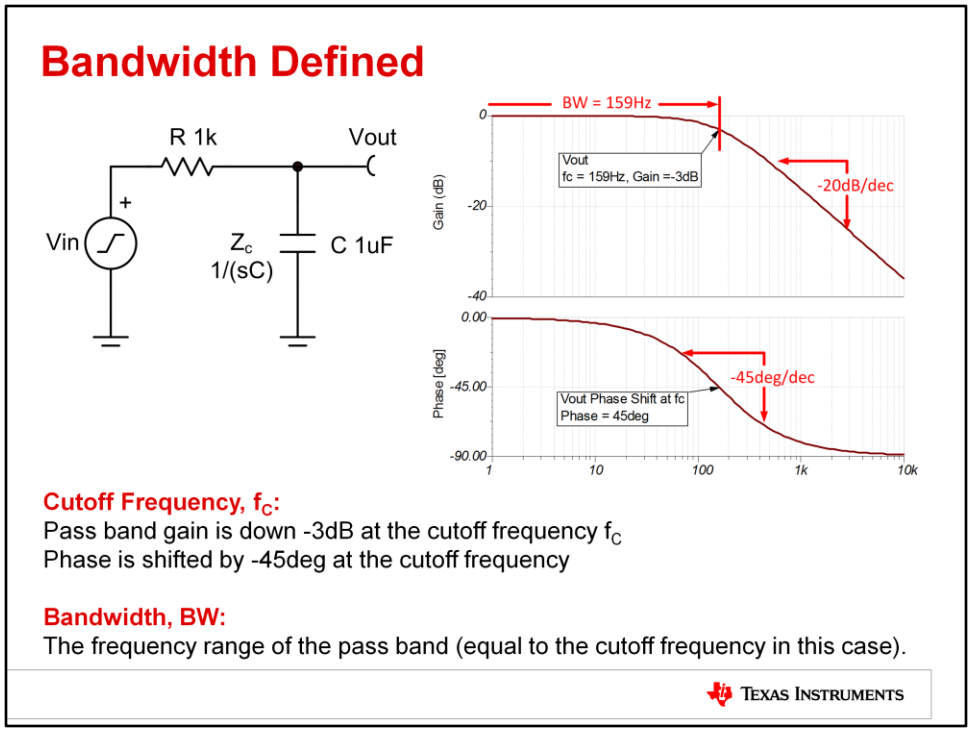
This slide illustrates the equations for a zero and its associated response. Looking at the equations, you can see that the first equation represents a zero as a complex number. Complex numbers have a real and imaginary part. For practical circuits the complex function is converted to a magnitude and phase. The second equation shows the magnitude and the third equation shows the phase. Taking 20 Log10 of the magnitude function gives the magnitude in dB.

The equations were used to generate the bode plot and phase plot. Let's look at some key points on the bode plot. First, the zero frequency is denoted f_Z. For frequencies below f_Z the gain is constant and is denoted G_{DC}. In this example G_{DC} = 0dB. Also notice that the gain at f_Z is at ***+3db***, or is 1.414 times the dc gain. Finally, for frequencies greater than f_Z, the magnitude plot increases at a rate of +20dB/decade.

Now let's consider the graph of phase shift vs. frequency. The phase shift at the zero frequency is +45 degrees. Phase begins to change one decade before the zero and stops changing one decade after the zero. In this region the slope is +45 degrees per decade. Considering frequencies that are lower than one decade below the zero, the phase shift is 0 degrees. For frequencies greater than one decade beyond the zero the phase shift is +90 degrees.

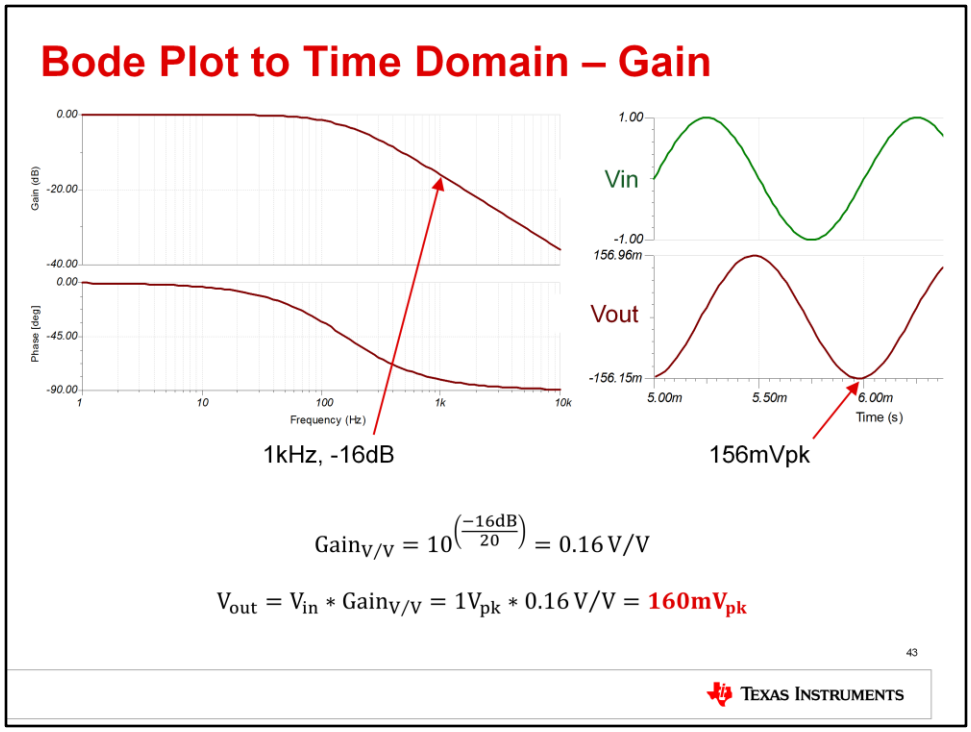
Up to this point we have looked at the mathematics behind frequency

response. Now we will look at connecting the mathematics to electrical circuits.

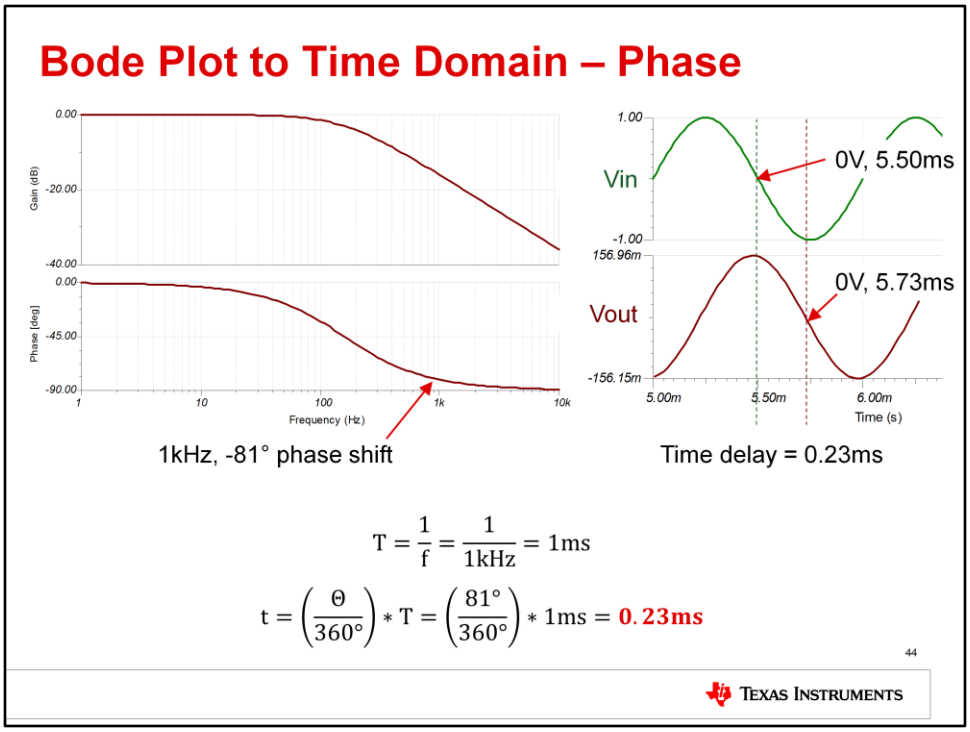


This figure shows the bode plot and the phase shift plot for a simple RC circuit. Recall that at dc or low frequencies a capacitor acts like an open. In this case the entire input signal is seen across the capacitor, so the gain is 1V/V or 0dB. Notice that the magnitude of the gain at the pole frequency is -3dB. Also notice that the phase at the pole frequency is -45 degrees. Furthermore, the phase shift begins about one decade before the pole and ends about one decade after the pole. Furthermore, the phase shift at very low frequencies is near zero degrees and at high frequencies the shift is nearly 90 degrees. Finally, notice that the gain decreases at a rate of -20dB/decade for frequencies above the pole frequency.

This circuit is a common building block and is called a low pass filter. The objective of this circuit is to pass low frequency signals and stop high frequency signals. For this reason, the pole frequency is often called the cutoff frequency, and denoted by fc. The idea is that all signals with frequency greater then the cutoff frequency are “cut off” or eliminated. In fact the high frequency signals are only attenuated and not fully eliminated. Another term associated with low pass filters is “bandwidth”. Bandwidth is simply the ***width*** of the pass-band, and in this case is synonymous with the cutoff frequency. In later videos we will discuss different types of filters. For some filters, such as a band pass filter, the bandwidth definition ***will*** include both a lower and upper cutoff frequency.



The bode gives information on the gain as well as the phase shift for a circuit. In this example we're going to calculate the peak output voltage of a 1Vp sinusoid at 1kHz. Given the amplitude and frequency of the input signal we can use the bode plot ***magnitude (Gain (dB))*** to determine the output signal amplitude. First, find the gain at 1kHz. In this example the gain is -16dB. Convert the gain from dB to a linear representation and multiply the input signal by the linear gain. In this example -16dB translates to 0.16V/V. Since the input is 1Vpk the output is 160mVpk. Notice that the time domain simulation peak output is very close to the expected value from the bode plot.



Here we will continue the example considering the phase shift in the time domain. Notice on the ***bode phase (Phase (deg))*** that the phase shift is -81degrees at 1kHz. On the time domain plot, you can see that the output signal is shifted to the right in time. This is called a phase shift or time delay. The calculation at the bottom of the page illustrates how you can convert the phase shift in degrees to expected time delay in seconds.

In this case, the phase shift is 81 degrees and the period of the 1kHz input is 1ms. The delay in seconds is calculated by dividing the phase shift by 360 degrees and multiplying by the period. As with the previous example, the calculated results match very well with simulation, and we see a time shift of 0.23ms.

Gain Bandwidth Product

PARAMETER		CONDITIONS	OPA827AI MIN	OPA827AI TYP	OPA827AI MAX	UNIT
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +1		22		MHz
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–)+3V ≤ V_O ≤ (V+)–3V, R_L = 1kΩ	120	126		dB

$GBW = Gain \cdot BW$

In this example, for any gain from 0dB to A_{OL}

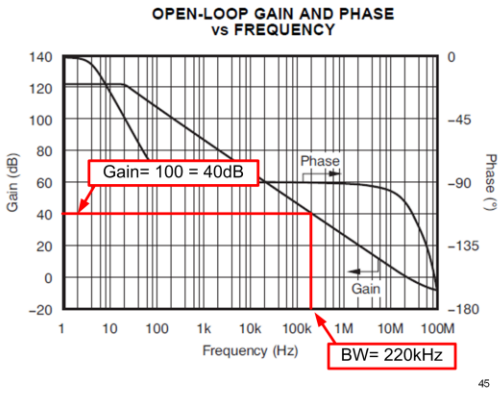
where
GBW -- Gain Bandwidth in Hz
Gain -- closed loop voltage gain
BW -- Bandwidth in Hz

For example

$Gain = 100\ V/V$

Closed Loop Bandwidth is calculated:

$$BW = \frac{GBW}{Gain} = \frac{22MHz}{100} = 220kHz$$



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TEXAS INSTRUMENTS

A simple approach to determining bandwidth is to use the gain-bandwidth product specification from an op amp data sheet.

The gain bandwidth product is literally the product of the linear gain and the bandwidth. Therefore, you can solve for one of the variables given the other two.

For example, let's calculate the bandwidth of a circuit that uses the OPA827 in a gain of 100V/V.

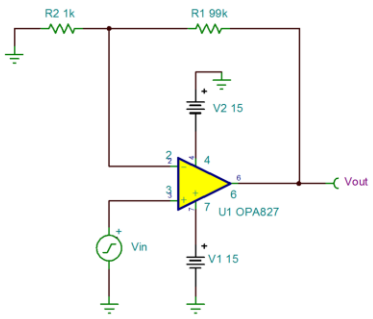
From the data sheet we see that the gain bandwidth product is 22MHz.

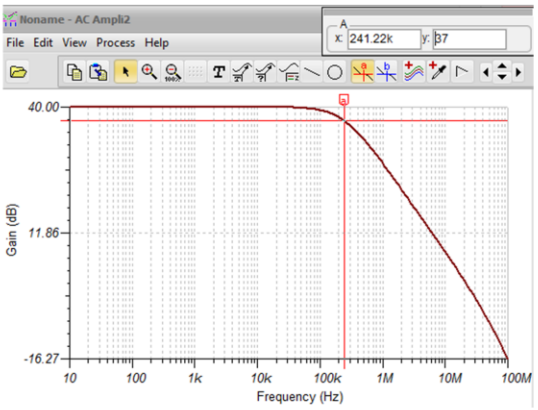
Solving the gain bandwidth equation for bandwidth tells us that the bandwidth is the gain bandwidth product divided by the linear gain. Dividing the OPA827 gain bandwidth product of 22MHz by the circuit gain of 100V/V yields a bandwidth of 220kHz.

This calculation is verified by looking at the OPA827 open loop gain curve from the data sheet. If we draw a horizontal line at the closed loop gain of 100V/V, or 40dB, until it intersects Aol we find the corresponding bandwidth is approximately 200kHz. Notice that solved graphically you may incorrectly interpret the bandwidth to be 200kHz, though by calculation we found it to be 220kHz.

It should be noted that the calculation approach to solving for bandwidth is only valid if the Aol curve decreases at a rate of ***-20dB/decade***. While this is true for most op amps, there are some that have a limited range where the gain bandwidth product is specified. Also, consider that the data sheet gives only the typical value for both the gain bandwidth product and the Aol curves. Generally, you can expect a variation of as much as ±30% from this value at room temperature and an additional error of ±30% over the specified temperature range. So, it is always advisable to include margin in your design when considering amplifier bandwidth.

Simulation Matches Calculation





Bandwidth (Calculated)	Bandwidth (Simulated)
220 kHz	241 kHz

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Let's now verify our bandwidth calculation with simulation. For the results to match, we must use the OPA827 in a non-inverting gain of 100V/V, or 40dB, like we did in the calculation on the last slide. If we run an AC transfer characteristic in TINA-TI, we see that the -3dB bandwidth, which occurs at 37dB since our DC signal gain is 40dB, is 241kHz. This matches well with our calculated bandwidth of 220kHz.

Dominant Pole

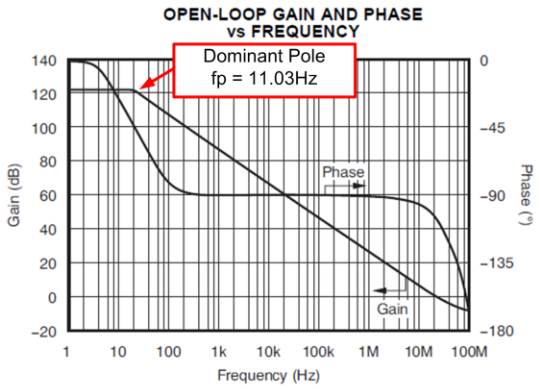
PARAMETER		CONDITIONS	OPA827AI MIN	OPA827AI TYP	OPA827AI MAX	UNIT
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +1		22		MHz
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–)+3V ≤ V_O ≤ (V+)–3V, R_L = 1kΩ	120	126		dB

$$\text{Dominant\_Pole} = \frac{GBW}{A_{OL}}$$

where
Dominant_Pole -- low frequency pole in Aol curve
GBW – Gain Bandwidth in Hz
BW -- Bandwidth in Hz

$$A_{OL} = 10^{\frac{126}{20}} = 1.995 \times 10^6 \text{ V/V}$$

$$\text{Dominant\_Pole} = \frac{GBW}{A_{OL}} = \frac{22\text{MHz}}{1.995 \times 10^6} = 11.03\text{Hz}$$



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TEXAS INSTRUMENTS

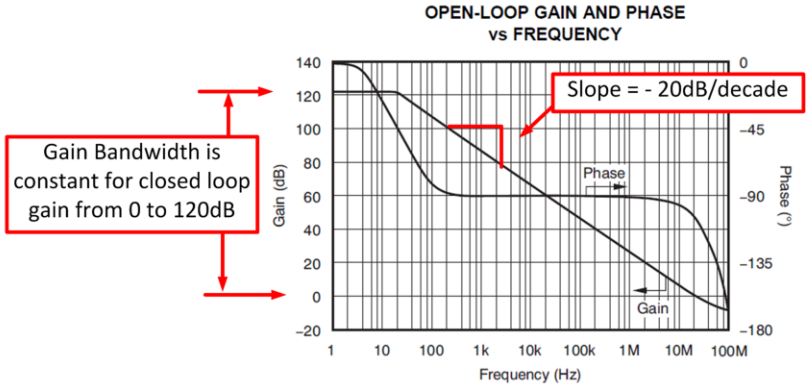
The dominant pole is the point on the Aol graph where Aol begins to roll off with frequency. This parameter is important when developing macromodels. The frequency of the pole can be estimated from the Aol curve, but a more accurate approach is to calculate it using this equation, where GBW is the gain bandwidth product and Avol is the open loop gain of the device.

Using the OPA827 as an example, we find the device has a gain bandwidth product of 22MHz and open loop gain of 126 decibels. We can convert 126dB to its linear representation using this equation.

Substituting 22MHz and 1.995 times 10 to the 6th for gain bandwidth and open loop gain, respectively, yields a dominate pole frequency of 11.03Hz. This calculation is consistent with the graph from the data sheet.

Constant Gain Bandwidth Product

PARAMETER		CONDITIONS	STANDARD GRADE OPA827AI			HIGH GRADE OPA827I[1][2]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW	G = +1		22			22		MHz



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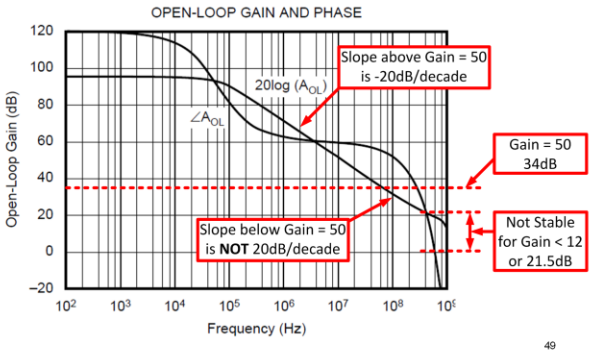
In this slide we further examine the OPA827 open loop gain curve. We see that the dc open loop gain is 120dB and remains constant until we reach the dominant pole. At frequencies greater than the dominant pole, the open loop gain decreases at a rate of -20dB per decade. Notice that for the OPA827 the slope of Aol is constant until we cross unity gain. Therefore the gain bandwidth product is constant for closed loop gains from 0 to 120 decibels.

While it is common to have open loop gain curves decrease at a constant rate of 20dB per decade, it is not always the case. For example, let's take a look at the high-speed OPA847.

Variable Gain Bandwidth Product

PARAMETER	CONDITIONS	OPA847ID, IDBV					
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/MAX
AC PERFORMANCE (see Figure 1)							
Closed-Loop Bandwidth	G = +12, R_G = 39.2Ω, V_O = 200mV_{PP}	600				MHz	typ
	G = +20, R_G = 39.2Ω, V_O = 200mV_{PP}	350	230	210	195	MHz	min
	G = +50, R_G = 39.2Ω, V_O = 200mV_{PP}	78	63	60	57	MHz	min
Gain Bandwidth Product (GBP)	G ≥ +50	3900	3100	3000	2800	MHz	min

Gain x Bandwidth =	12 x 600MHz =	7200MHz
Gain x Bandwidth =	20 x 350MHz =	7000MHz
Gain x Bandwidth =	50 x 78MHz =	3900MHz
Gain x Bandwidth =	100 x 39MHz =	3900MHz
Gain x Bandwidth =	500 x 7.8MHz =	3900MHz
Gain x Bandwidth =	1000 x 3.9MHz =	3900MHz



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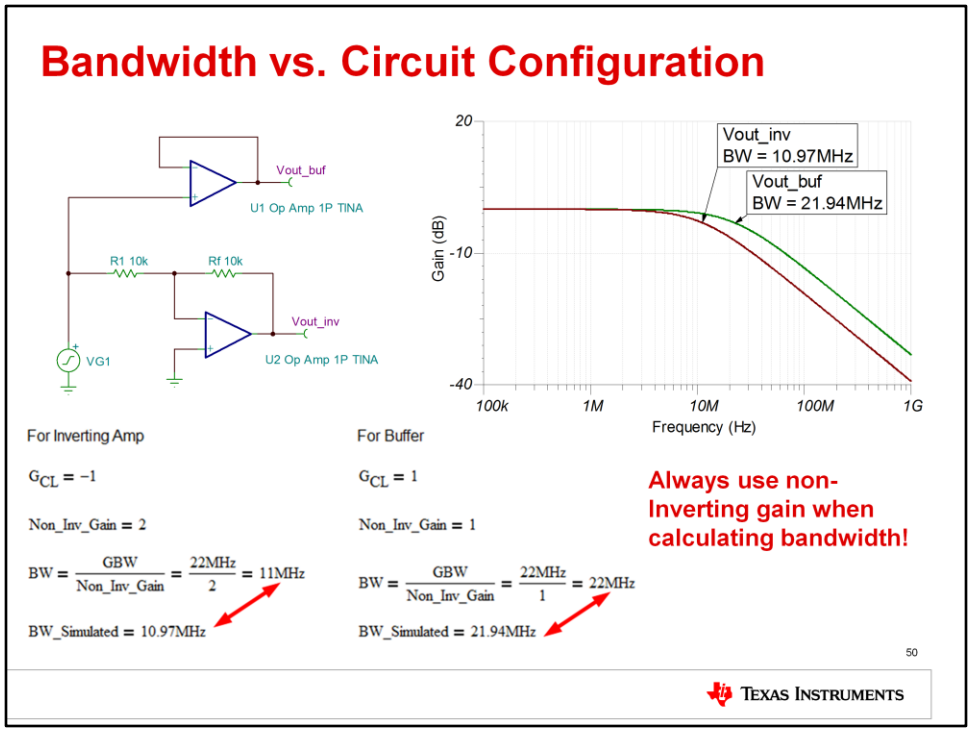
TEXAS INSTRUMENTS

This slide shows the Aol curve for the OPA847, whose gain bandwidth product is defined for only a portion of the Aol curve. In this case it's defined only for closed loop gains greater than 50V/V.

Looking at the open loop gain curve, we see that for gains greater than 50V/V, or 34dB, the slope of the Aol curve is -20dB/decade. Therefore the gain bandwidth product is equal to 3900MHz for all closed loop gains greater than 50V/V.

However, as the gain decreases below 50V/V, the slope of Aol changes. Therefore, there is no gain bandwidth product specified. Instead, the closed loop bandwidth for particular gains is specified. Also notice that for gains less than 12V/V the phase margin indicates that the device is not stable. The table illustrates how the product of the gain and bandwidth is not constant for gains less than 50V/V, but is constant for gains of 50 or greater.



Earlier we calculated closed loop bandwidth for a non-inverting configuration using the gain bandwidth product. You might be surprised to learn that the bandwidth calculation for the *inverting* configuration is calculated using the *non-inverting gain*. Note that the non-inverting gain is typically referred to as noise gain.

This example shows the same amplifier connected in both an inverting and non-inverting configuration. The inverting configuration has a gain of -1 and the non-inverting configuration has a gain of +1. Let's start by calculating the bandwidth for the non-inverting configuration. The bandwidth for the non-inverting amplifier U1 is calculated by taking the gain bandwidth product and dividing by the non-inverting gain. So, for this example, the bandwidth is 22MHz divided by 1 which is equal to 22MHz.

On the other hand, the bandwidth of the inverting amplifier, U2, is calculated using the *non-inverting gain*. The gain with respect to the non-inverting input is calculated as Rf/R1 +1, which is 2 in this example. So, the bandwidth of the inverting amplifier is 22MHz divided by 2 which is 11MHz. A common mistake is to consider the gain seen by the signal source rather than the noise gain for bandwidth calculations involving inverting amplifiers.

This example is simulated to prove that the hand calculations are correct. Notice that the simulation and hand calculation results are very close to each other. This

simulation uses a simple single pole amplifier model to illustrate the relationship between bandwidth and circuit configuration.

Bandwidth vs. I_Q

Op Amp	Typical GBW	Typical I_Q
OPA369	12kHz	0.8µA
OPA333	350kHz	17µA
OPA277	1MHz	790µA
OPA129	1MHz	1.2mA
OPA827	22MHz	4.8mA
OPA350	38MHz	5.2mA
OPA211	45MHz (Gain=1)	3.6mA
OPA835	51MHz (Gain=1)	250µA
OPA847	600MHz (Gain=12)	18.1mA

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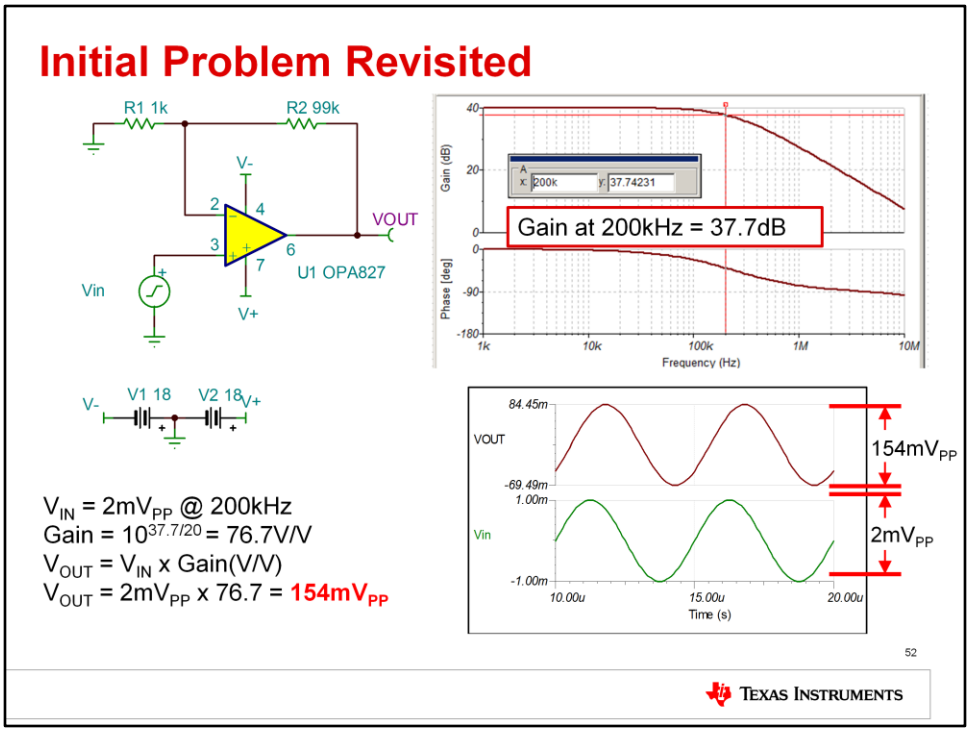
Finally, let's look at a number of op amps that depict a range of gain bandwidth products and their corresponding quiescent current, Iq.

In the slide we list Gain Bandwidth Products for different amplifiers that range from 12kHz to 600MHz. The OPA369, for example, is a very low bandwidth amplifier. This device is designed specifically to have very a low quiescent current of 0.8uA and is called a micro-power device. It is more common for amplifiers have bandwidth in the range of 1MHz like the OPA277. Some amplifiers like the OPA350 and OPA211 have wider bandwidth to facilitate driving A/D converters and for other wide bandwidth applications. For very high speed applications amplifiers like the OPA835 and OPA847 can be used. In general, the wider bandwidth op amps require more quiescent current. However, there are some exceptions , as displayed by the OPA835.



Let's return to our original problem, now that we understand the fundamentals of bandwidth. We have a non-inverting amplifier circuit with a closed-loop gain of 100V/V, or 40dB. The input is a 2mVpp sine wave at a frequency of 200kHz.

When we run an AC simulation of the circuit, we can see that at 200kHz, the closed-loop gain has dropped to only 37.7dB. If we convert 37.7dB to linear gain of 76.7V/V and multiply by our input signal amplitude of 2mVpp, we get an expected output of 154mVpp. This matches perfectly with our transient simulation on the bottom-right!

Multiple-Choice Quiz

- How will increasing the gain of an amplifier affect bandwidth?
  a) bandwidth will increase
  b) bandwidth will decrease
  c) bandwidth will not be affected

- Where is the dominant pole on an A_{OL} curve?
  a) at low frequencies (typically 1Hz to 100Hz)
  b) at high frequencies (typically near the unity gain bandwidth frequency)

Multiple-Choice Quiz

- How can you calculate bandwidth using the gain bandwidth product? **Note:** BW is closed loop bandwidth, GBW is gain bandwidth, and G_{CL} is closed loop gain.
  a) BW = GBW / G_{CL}
  b) BW = GBW * G_{CL}
  c) BW = G_{CL} / GBW

- What condition is required for the gain bandwidth product to be valid?
  a) A_{OL} curve roll off must be greater than 20dB/decade
  b) A_{OL} curve roll off must be equal to 20dB/decade
  c) the A_{OL} curve cannot have a dominant pole
  d) the amplifier must be bipolar

Multiple-Choice Quiz

- Different model amplifiers have different gain bandwidth products (GBW). Surveying many different models, you will see GBW vary from _____.
  a) 10Hz to 1kHz
  b) 100Hz to 1MHz
  c) 1MHz to 500MHz
  d) 10kHz to 500MHz

- Amplifiers with wide bandwidth generally have _____.
  a) lower I_Q than amplifiers with narrow bandwidth
  b) higher I_Q than amplifiers with narrow bandwidth
  c) low slew rate
  d) stability problems

Multiple-Choice Quiz

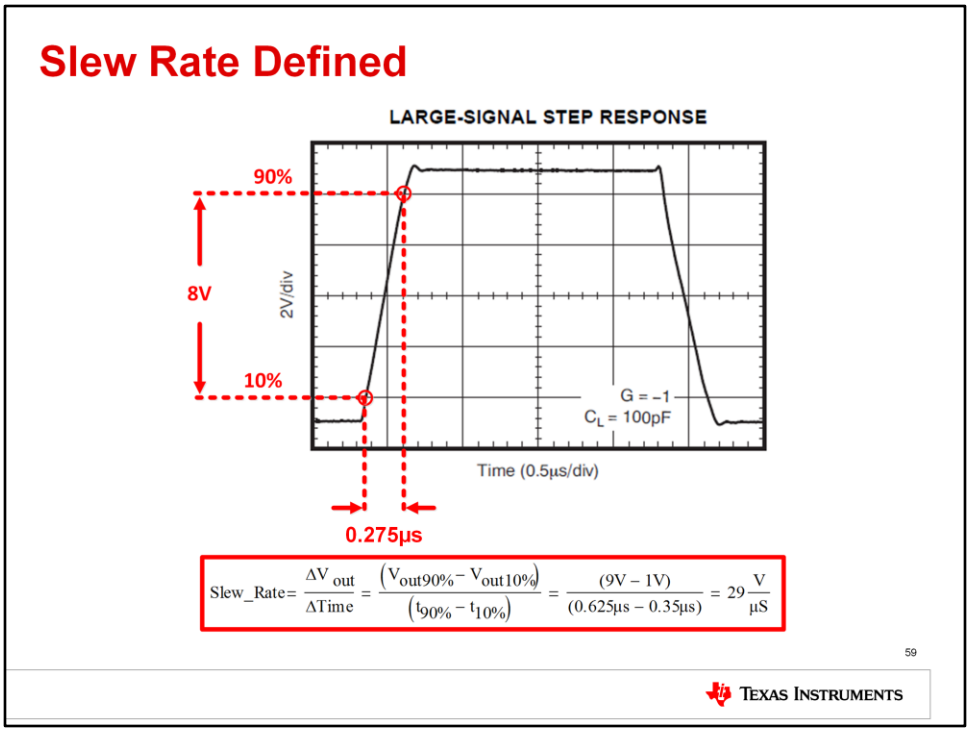
- What is the change in magnitude due to a pole at the pole frequency, f_P?
  a) -20dB
  b) -3dB
  c) +3dB
  d) +20dB

- What is the phase shift due to a zero at the zero frequency, f_Z?
  a) -90°
  b) -45°
  c) +45°
  d) +90°

Multiple-Choice Quiz

- Assume that an amplifier with a gain bandwidth product of 10MHz is used for both gain = +1 and gain = -1. What is the bandwidth for each configuration?
  a) bandwidth for both configurations is 10MHz
  b) bandwidth is 10MHz for gain = +1 and 5MHz for gain = -1
  c) bandwidth is 5MHz for gain = +1 and 10MHz for gain = -1
  d) none of the above

Hello, and welcome to the lecture for the TI Precision Lab discussing slew rate. In this lecture we'll go over the theory behind slew rate and compare the slew rate and current consumption of different TI amplifiers.



Slew rate is defined as the maximum rate of change of an op amp's output voltage and is given units of volts per microsecond. Slew rate is measured by applying a large signal step, such as 1V, to the input of the op amp, and measuring the rate of change from 10% to 90% of the output signal's amplitude.

The data sheet large-signal step response is an indication of the amplifiers slew rate. In this example, we calculate the slew rate to be about 29V/us. Again, the slew rate definition only considers the rate of change of the signal from 10% to 90%, which in this case is 1V to 9V.

Slew rate is a different specification than small-signal bandwidth, which considers differential input signals of ±100mV or less.

Capacitor Physics Review

- With constant current applied, the voltage across a capacitor changes linearly over time

$$i = C\frac{dV}{dt}$$

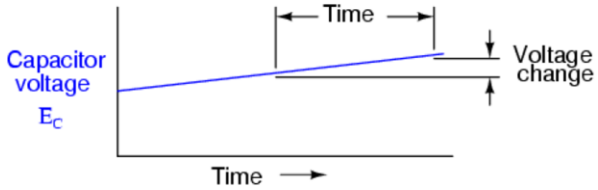
$$dV = \frac{i}{C} \cdot dt$$

$$V = \frac{i}{C} \cdot \int_0^t dt$$

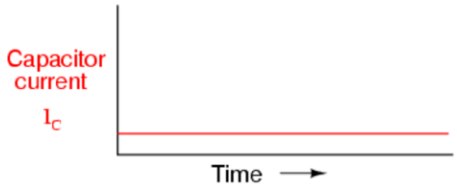
$$V = \frac{i}{C} \cdot t + Constant$$

This is in the form

$$y = mx + b$$



Potentiometer wiper moving slowly "up"



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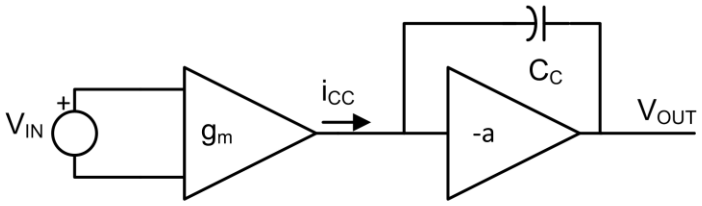
Before we get into an in-depth slew rate discussion, let's first review some basics.

The equation that defines how a capacitor works states that the current flow through a capacitor is equal to the capacitance times the derivative of voltage with respect to time. This behavior can also be interpreted to mean that if you have a constant current, then the voltage across the capacitor will rise linearly over time.

Slew Limit



- For slow moving or small signals $i_{CC} < i_{CC(max)}$
- For large, rapid moving signals $i_{CC} = i_{CC(max)}$
  - The output is slew rate limited
  - This is the fastest rate the output can change
  - The input is no longer a virtual short
  - Large input differential voltages are possible
  - i_{CC} is constant, so V_{OUT} increases linearly across capacitor C_C

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This is important with respect to slew rate of an amplifier. An amplifier has an internal g_M, or transconductance, stage which takes the input differential voltage and converts it to an output current, I_{CC}. I_{CC} flows into the next stage where it is used to charge C_C, which is called the Miller capacitance. If I_{CC} is a constant, then the voltage across C_C will rise linearly with time, just like we discussed on the previous slide.

For slow-moving signals, I_{CC} is less than some maximum value I_{CC_MAX}. This means that I_{CC} is able to change according to the differential input voltage without being limited. But for rapidly moving, large signals, I_{CC} reaches its maximum and becomes limited to some constant value. In this case the input to the amplifier will no longer be a virtual short, and therefore a differential voltage will develop across the input pins. Since I_{CC} is constant, V_{OUT} across the Miller capacitor C_C increases linearly over time. This is when the output of the amplifier is considered to be slew rate-limited, which is fastest that the output voltage can change.

Slew Rate of Different Amplifiers

Op amp	Slew Rate (typ)	I_Q (typ)
OPA369	0.005 V/µs	0.862 µA
OPA333	0.16 V/µs	17 µA
OPA277	0.8 V/µs	790 µA
OPA129	2.5 V/µs	1.2 mA
OPA350	22 V/µs	5.2 mA
OPA211	27 V/µs	3.6 mA
OPA827	28 V/µs	4.8 mA
OPA835	110 V/µs	250 µA
OPA847	850 V/µs	18.1 mA

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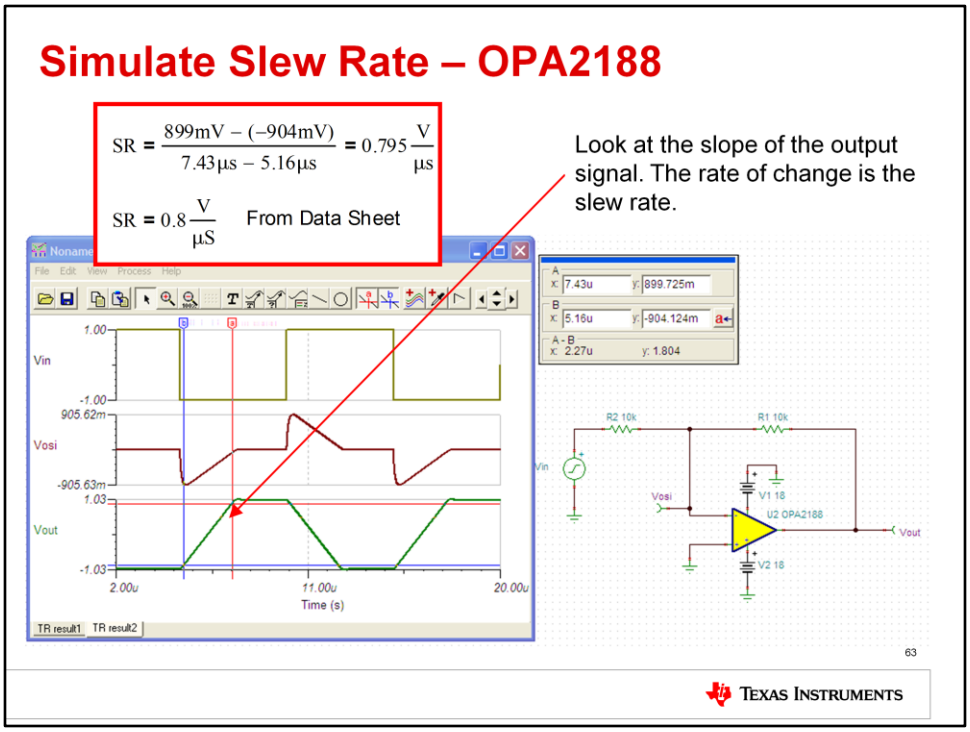
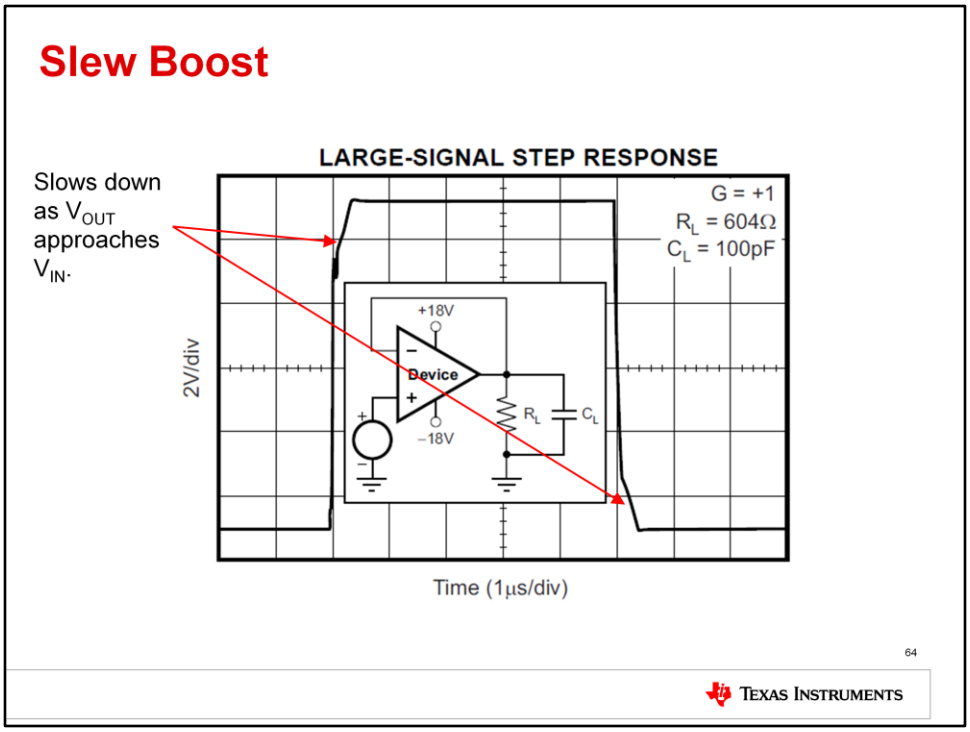
Here we compare the typical slew rate and quiescent current, or IQ, for different amplifiers.

On one end of the spectrum, we have the OPA369 which is a very low I_Q and low slew rate device. For 0.8µA of current we can achieve around 5mV/µs of slew. Compare that to the OPA847, which consumes 18.1mA of I_Q but can slew at 850V/µs. This shows us that amplifiers with higher slew rate, and therefore higher bandwidth, tend to have higher current consumption.

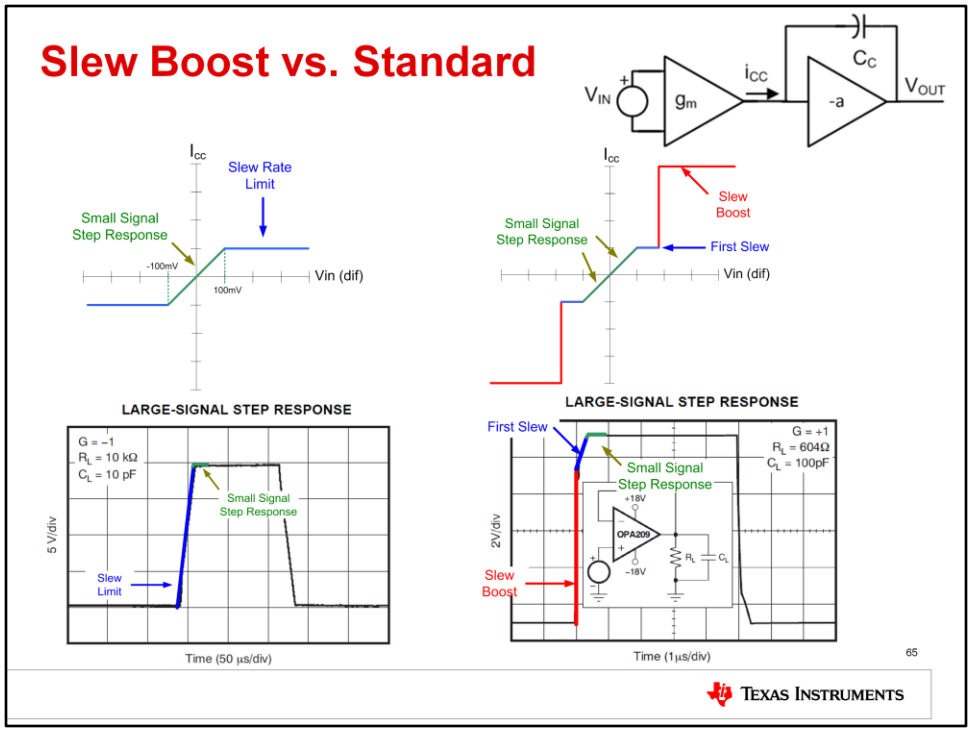


We can easily simulate slew rate using TINA-TI. Simply apply a step function to the input of the amplifier, which in this case is a ±1V square wave. You can see that when this input step is applied, the input offset voltage changes from 0V - which indicates a virtual short - to some other voltage, around 900mV in this case. Most importantly, the output voltage becomes slew rate-limited, shown as a constant ramp in voltage over time until finally reaching its true value. You can observe the input offset voltage moving linearly back to 0V as well.

Calculating the slew rate from this plot gives a result of 0.795V/µs. The data sheet for this device, the OPA2188, lists the slew rate as 0.8V/µs, indicating that the model accurately simulates the slew rate of the amplifier.

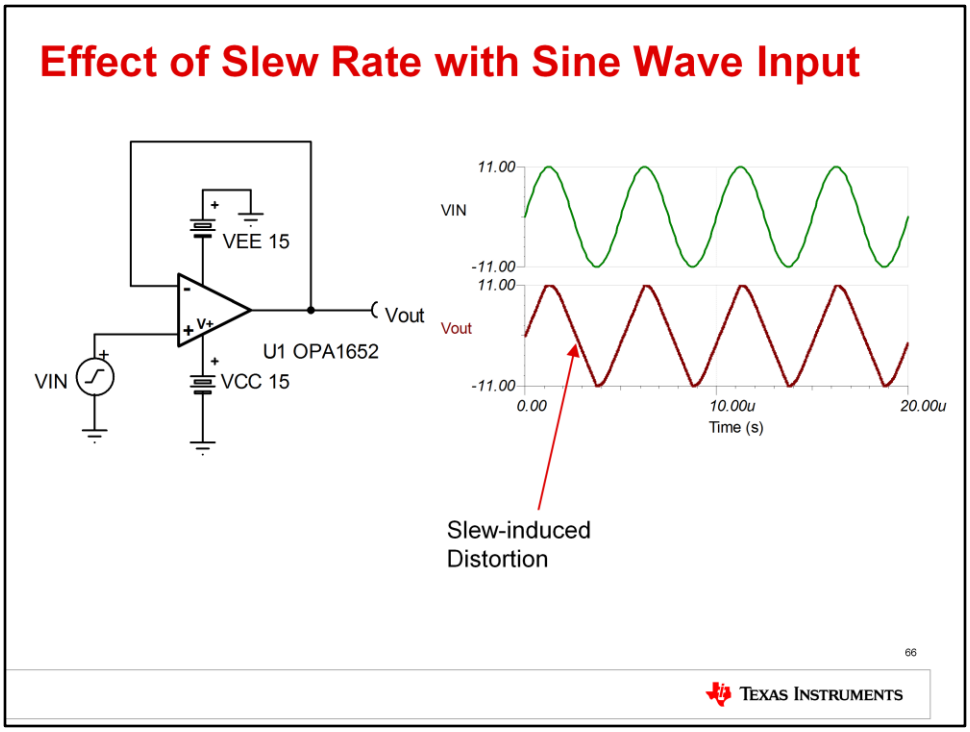


Some amplifiers include a “slew boost” circuit which allows for faster slew rates. An example of an amplifier with slew boost is shown in this large-signal step response plot. What happens is that the device has two different slew rates – an initial rate which is very fast, and a second, slower rate as the output settles to its final value. You may ask yourself, “why doesn’t the amplifier just have one slew rate which is always fast?” The reason is that with one, extremely fast slew rate, the output would have a large overshoot. When that overshoot occurred, the amplifier would try to compensate for this and the negative slew would kick in, resulting in a large negative overshoot. This behavior would continue, resulting in oscillation.

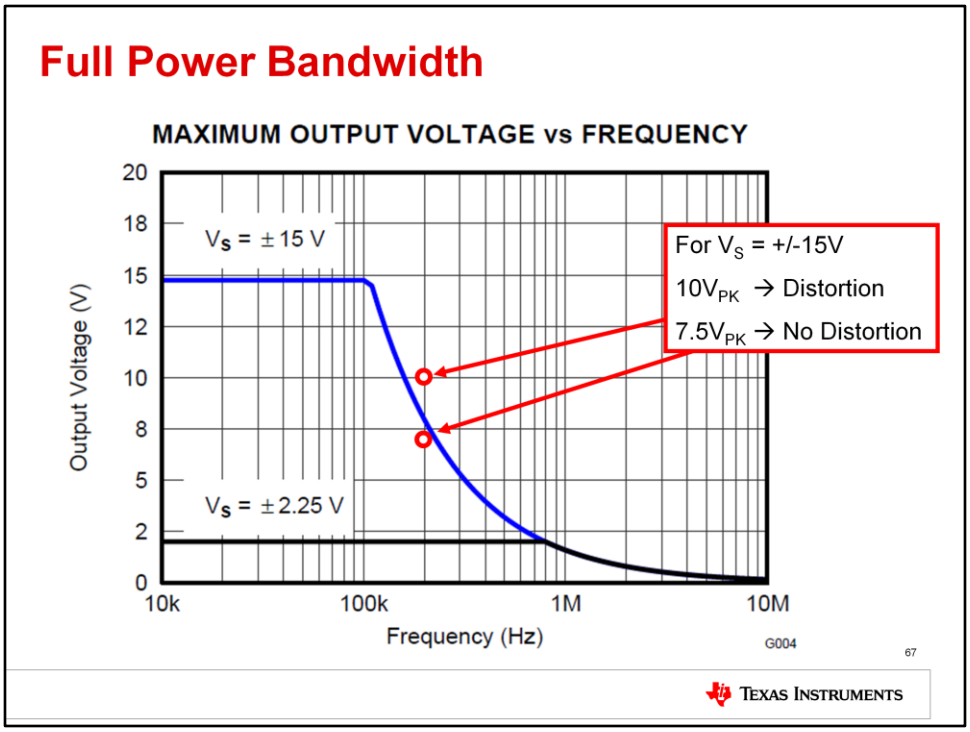


So how does this slew boost look compared to a standard amplifier? On the left hand side is the response of a standard amplifier. The green region shows the small-signal response (or differential input voltage greater than ±100mV), where the amplifier can linearly change the current flowing into the Miller capacitance. The blue region shows the large-signal response (or differential input voltage greater than ±100mV), where the amplifier reaches its slew rate limit and the current flow into the Miller capacitance is held constant..

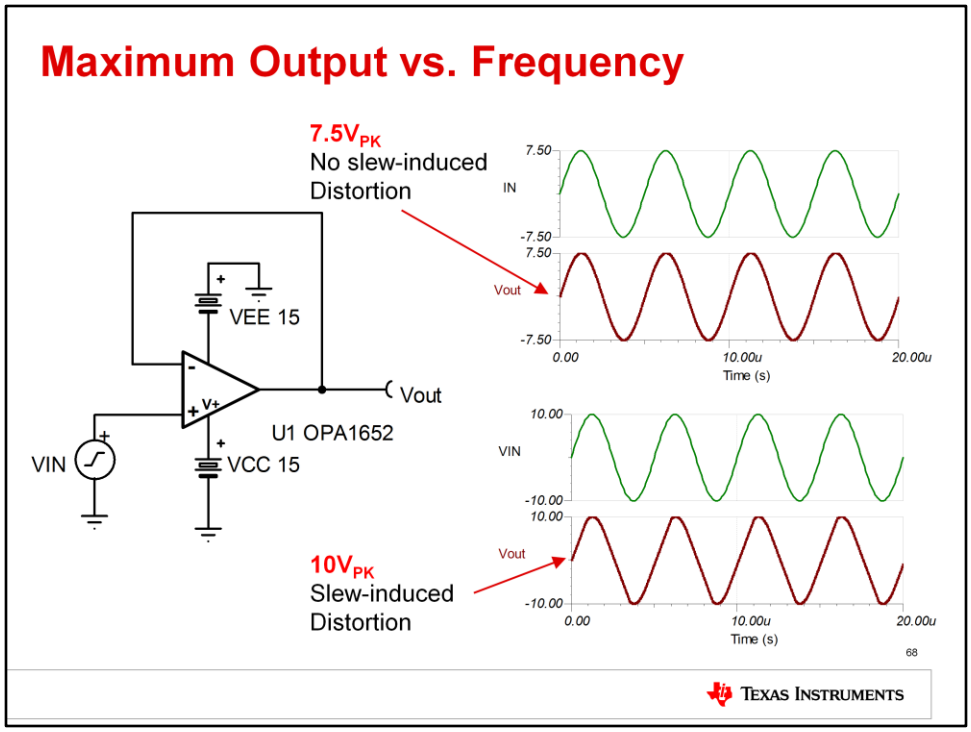
We have a similar situation for an amplifier with slew boost. There is still a small-signal response shown by the green region, but once the differential input voltage exceeds a certain value we reach the slew rate limit, indicated by the blue region, and eventually the slew boost, indicated by the red region. Therefore, when a large step function is applied to the input of the amplifier, the device will initially see a large differential input voltage and will be in Slew boost mode, allowing a large output current into the Miller capacitance and therefore a quickly-ramping output voltage. As the differential input voltage decreases the amplifier will move to its standard slew rate, and finally to its small-signal response once the input voltage becomes small enough. At this point the output will settle and the inputs of the amplifier will once again be a virtual short.



The slew rate of an op amp also impacts sinusoidal signals. If the op amp attempts to swing its output voltage past a certain frequency and amplitude which exceed the slew rate, the output will become distorted and will start to look more like a triangle wave. This limitation is called the full power bandwidth of the op amp.



The graph above shows the maximum output sinusoidal waveform that can be generated without slew-induced distortion. This example considers a 200kHz signal at both 7.5Vpk and 10Vpk. At 7.5Vpk, the output signal is under the curve and therefore will not be distorted by slew rate limitations. At 10Vpk, the output signal is above the curve and will be distorted by slew rate limits.



Let's simulate the conditions of the previous slide. With 7.5Vpk output, the response is sinusoidal with minimal distortion. However, with 10Vpk output, in a condition outside the full power bandwidth curve, the device is slew-rate limited and the output distorts.

Maximum Output vs. Frequency – Derived

$V_{out} = V_p \cdot \sin(\omega t)$

$\frac{d}{dt}(V_{out}) = \omega V_p \cdot \cos(\omega t)$ Rate of change.

Maximum happens a $\cos(\omega t)=1$

$Max\_Rate\_of\_Change = \omega V_p$

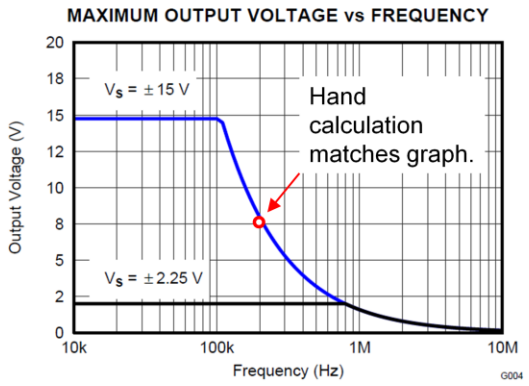
$SR = 2\pi \cdot V_p \cdot f$

$V_p = \frac{SR}{2\pi \cdot f}$

for OPA1652 example at 200kHz

$SR := 10\frac{V}{\mu s}$ $f := 200kHz$

$V_p := \frac{SR}{2\pi \cdot f} = 7.958V$



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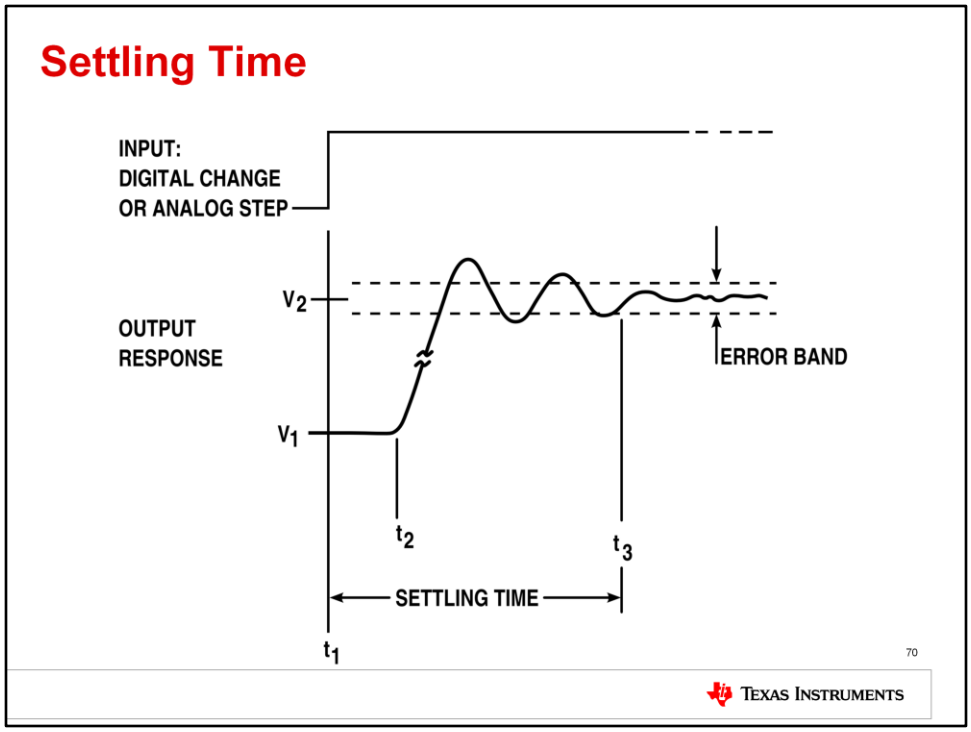
This slide illustrates that the maximum output vs. frequency curve can be derived with calculus. You can go through the math on your own, but the key point is that the final equation, Vpk = SR / (2 PI f) can be used if this curve is not available. The example shown in red confirms that the equation yields the same result as the curve.



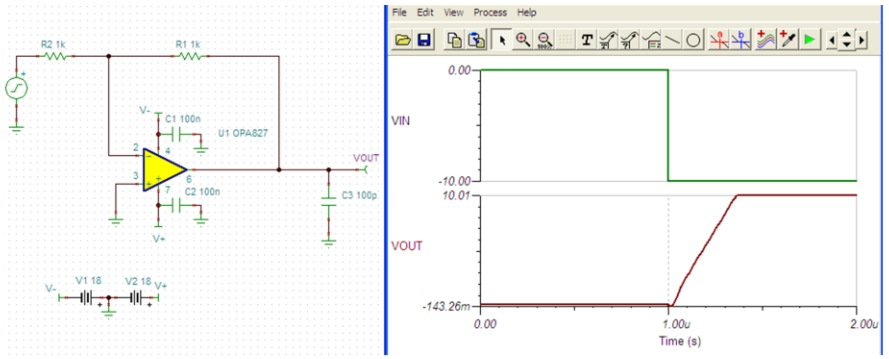
Let's now move on to discuss settling time.

Settling time is the time required for the amplifier's output to reach and stay within a certain error band after a large-signal step is applied to the input. The error band can either be specified in terms of percentage or number of LSBs (for an ADC with a specified number of bits).

Because the input is a large-signal step, the amplifier is in slew rate limit. The tighter the error band is (i.e. smaller error percentage), the longer the settling time will be. Capacitance, closed loop gain, and loading will also effect settling time.

Simulating Settling Time – OPA827

FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +1		22		MHz
Slew Rate	SR	G = –1	20	28		V/µs
Settling Time, ±0.01%	t_S	10V Step, G = –1, C_L = 100pF		550		ns



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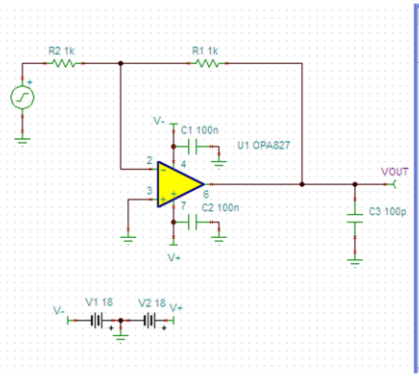
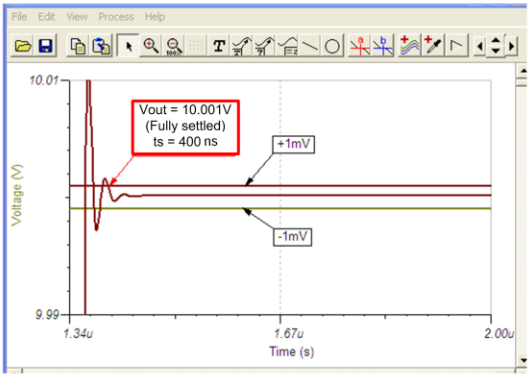
We can very easily simulate the settling time of an op-amp using TINA-TI's transient analysis function. In order to do this, it is important to closely follow the data sheet test conditions, such as the step size, gain configuration, and load capacitance.

In this case we are testing the OPA827 in a gain of -1, with a 10V step input and 100pF of load capacitance.

Simulating Settling Time – Large-signal





Data Sheet = 550ns

Simulated = 400ns

0.01% settling for a 10V signal

10V x 0.01% = 1mV

|Output – 10V| < 1mV

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The settling behavior, with some overshoot and damped oscillations, can really be seen once we zoom in on the plot. In this example, the output settles after an over shoot and one cycle of ringing, for a total settling time of 400ns. This is acceptably close to the typical data sheet value of 550ns.

Small-signal Rise Time

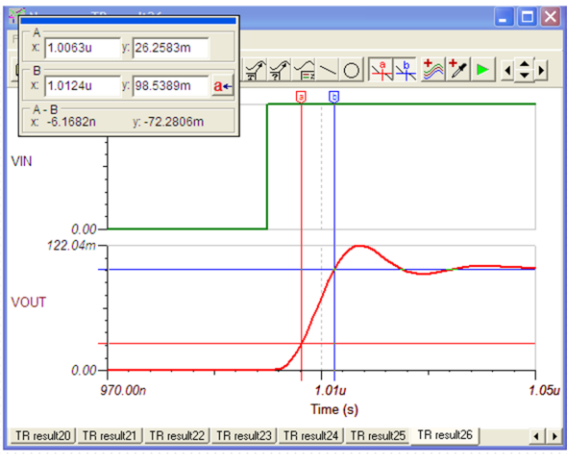
Rate of change of output:

- ΔV/ Δt = 72.3mV / 6.17ns
- ΔV/ Δt = 11.7V/µs
- Data sheet = 28V/µs

This is what you would expect with a real device! A small signal step will **not** put the amplifier into slew limit.

$$f_C = \frac{GBW}{G_{CL}}$$

$$t_R \cong \frac{0.35}{f_C}$$



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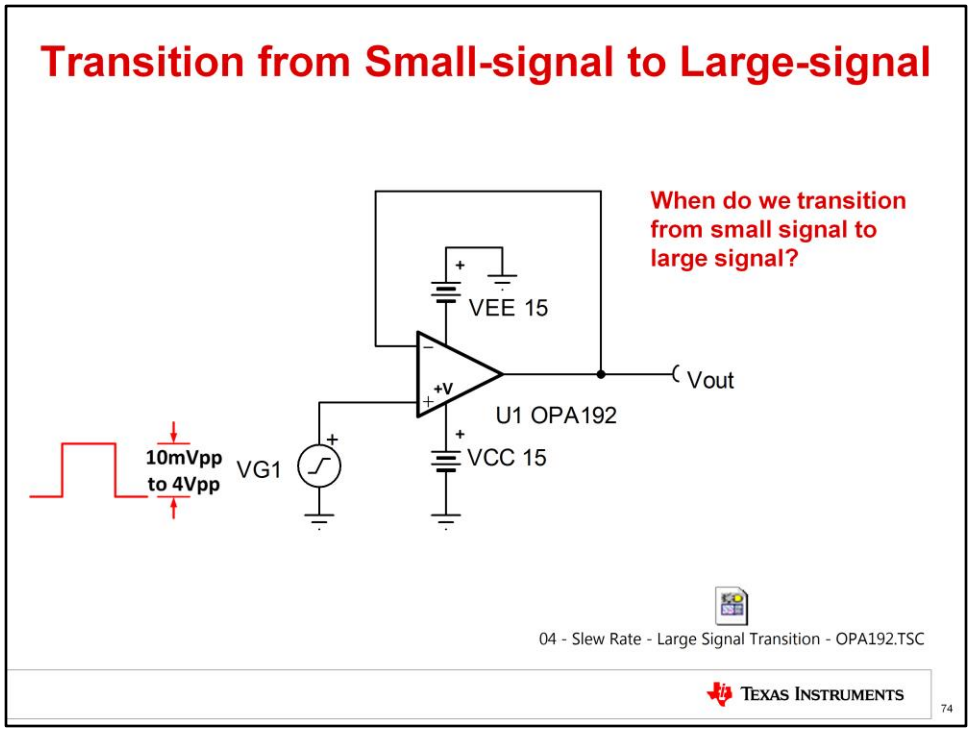
Here we observe the **small-signal** rise time of the same circuit, for purposes of comparison to the large-signal slew rate. Again, let's zoom in on the rising edge of the small signal step response. Measuring delta V over delta T from 10% to 90% of the output swing, me get a rise time of 11.7V/µs. Compare this to the data sheet slew rate value of 28V/µs – they're quite different!

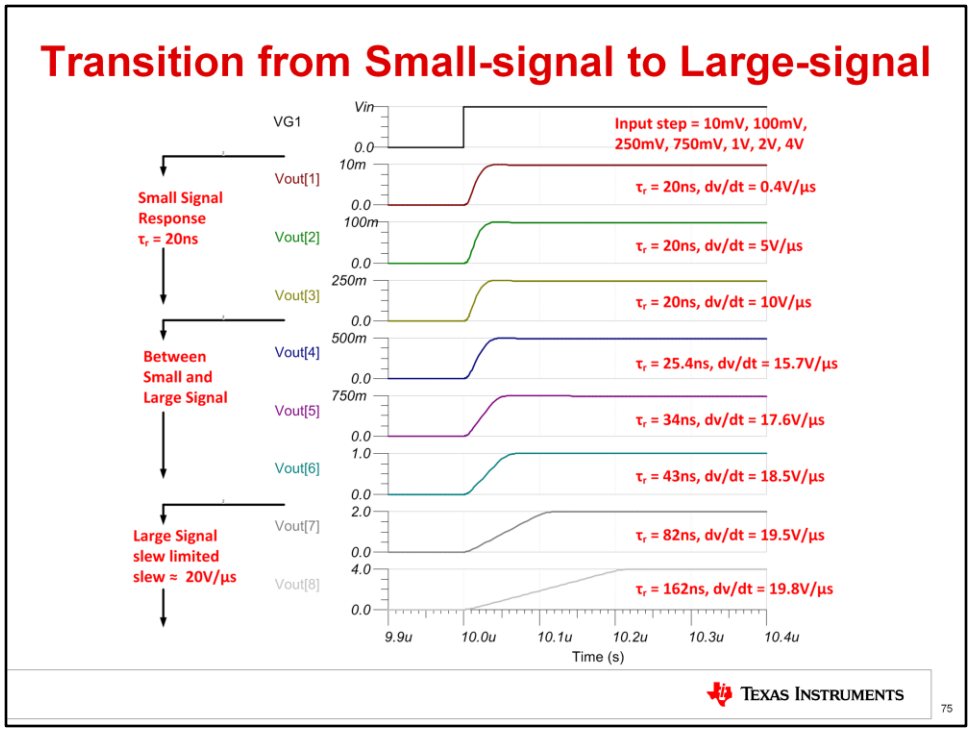
Where does the difference in this behavior come from? Well, as you may remember from earlier, a large-signal step input puts an op-amp in slew limit and therefore forces it outside of its normal linear operation. A small-signal step input, on the other hand, allows the op-amp to operate in its linear region and therefore the rise time is based on the op-amp's bandwidth.

The equation to calculate 10% to 90% rise time is given here. It is derived from the properties of a single-pole system.



An amplifier's small-signal or large-signal behavior, like most things in the real world, isn't fully black and white. The way in which a circuit operates is not always fully large-signal or small-signal. In fact, there's a gradual transition between these two operating conditions.

Here we have a simple op amp circuit configured as a non-inverting buffer. We'll apply a range of input steps, from 10mVpp to 4Vpp, and observe the output. A transient simulation done in TINA-TI will allow us to observe whether the circuit shows small-signal or large-signal behavior.



This figure illustrates the output of the non-inverting buffer circuit from the previous slide, versus different input step sizes.

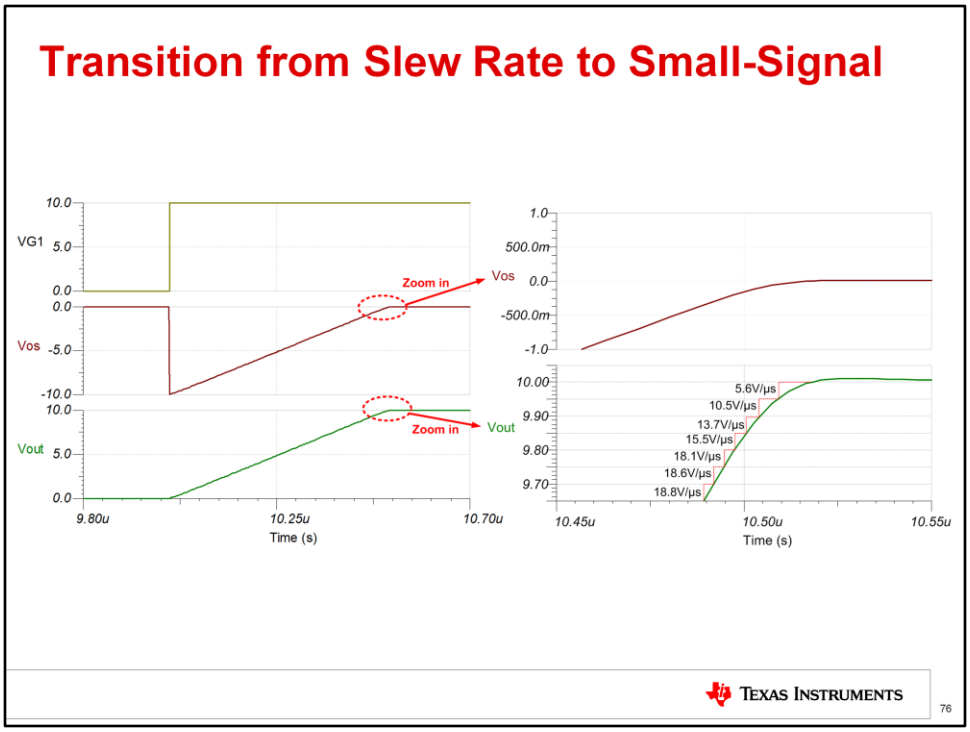
Notice that the output rise time is a constant 20ns for input steps of 10mV to 250mV. Because the rise time is constant, we know that the response is small-signal. The device in this example, the OPA192, has a slew rate of 20V/us. You can see that the rate of change for the small step response is lower than the slew rate. Also, notice that the output signal increases exponentially for the small signal response, as opposed to the linear increase for amplifiers that are slew rate-limited.

For input steps between 500mV and 1V, the amplifier is transitioning between small-signal and large-signal response. In this region the rise time is no longer constant; however, the amplifier is not yet at the full slew rate of 20V/us.

For input steps greater than 1V, the amplifier is slew rate-limited. You can see that the rate of change of the output signal is at the slew rate limit of about 20V/us. Also, notice that the output signal increases linearly in response to the input step.

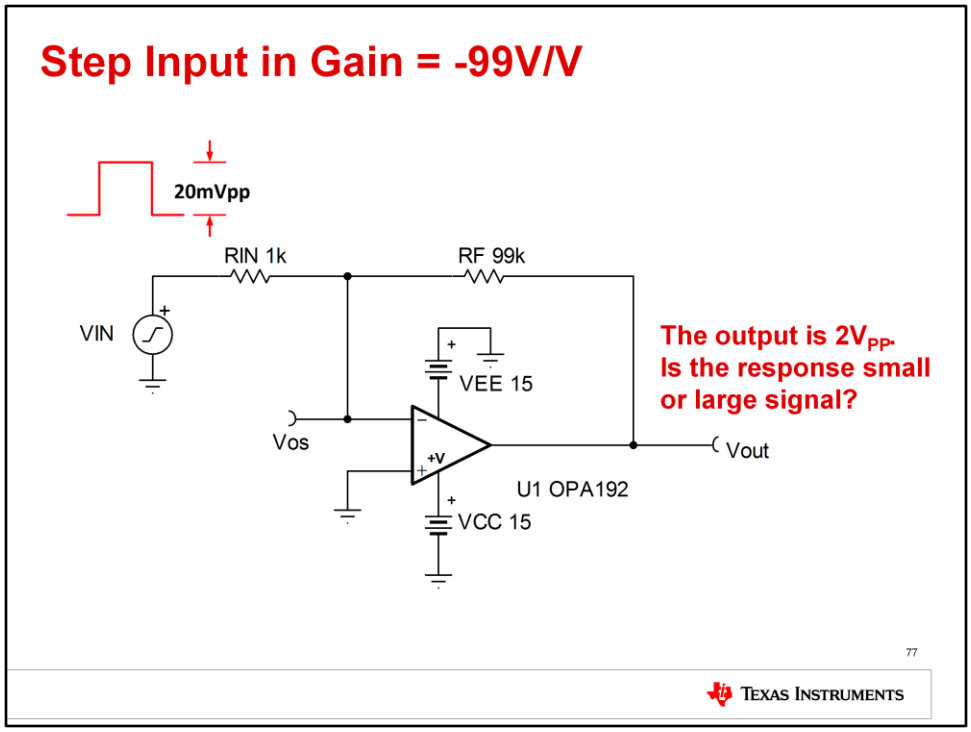
In this example, input signals less than 250mV caused a small signal response and signals greater than 1V caused a large signal response. However, this transition depends on the amplifier's design and technology. CMOS amplifiers tend to reach slew limit for signals greater than 100mV, and bipolar amplifiers can slew limit at even lower input voltages. Note that the industry standard for small signal response is a 100mV step, but in practice the actual limit may be lower.

Because of the way the output signal is scaled in this figure, it is possible to be tricked into thinking that the slew rate limited signal at the bottom of the figure is moving more slowly then the small signal response at the top of the figure. This is not the case, and the next slide will provide further clarification.



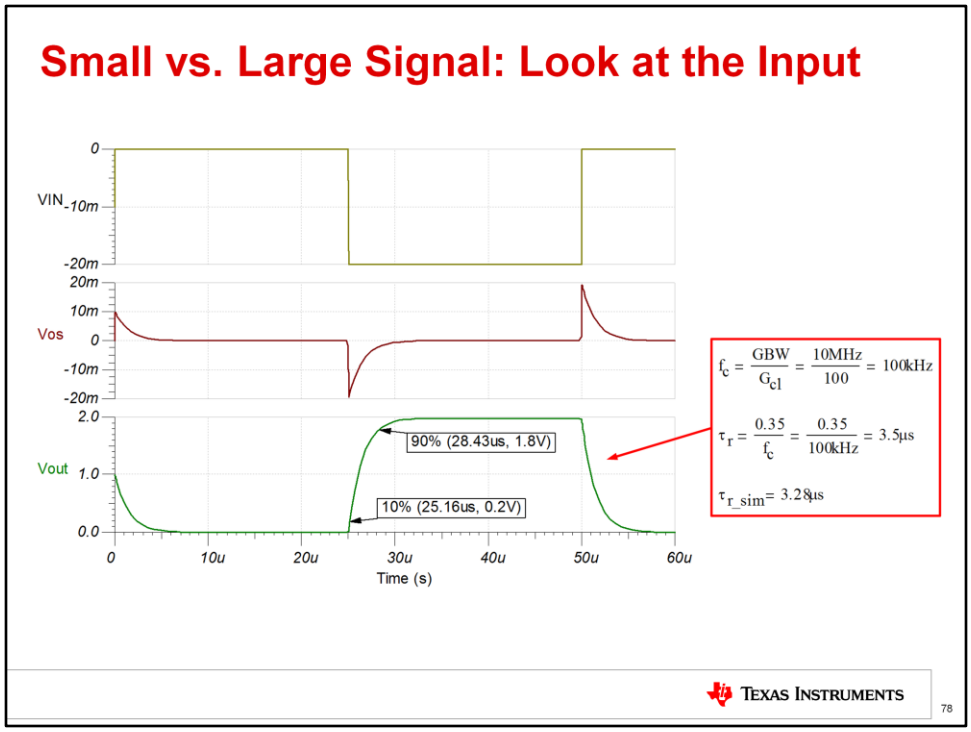
Let's take a closer look at the output of the non-inverting buffer circuit with a 10V step applied to the input.

In this case, the device is in slew-rate limit of 20V/us. However, when the signal approaches the final value of 10V, the op amp will transition to a small signal response. Zooming in on the last 300mV of the signal swing, you can see that the rate of change of the output decreases from approximately the slew rate, 20V/us, to a lower rate of change such as approximately 5V/us. Also, you can see that the shape of the output changes from the linear rise associated with slew rate limit, to the exponential behavior associated with small signal response.



Most of the examples discussed thus far have been basic buffer circuits, also called unity-gain followers. Now let's look at amplifiers with different closed loop gains in order to see the effect that closed loop gain has on output response.

Here we show an inverting amplifier circuit in a gain of -99V/V. The input is a small signal step of 20mVpp. Based on the gain, the output should be approximately 2Vpp. Does the output respond as a small signal or as a large signal?



This is the simulated output response of the circuit from the previous slide. Notice that the output signals rise and fall in an exponential way, which indicates a small-signal response. Also, if we use the small signal rise time formula from before, we can see that the calculated rise time of 3.5us is very close to the simulated rise time of 3.28us. Thus, the amplifier responds to the 20mV input step as a small signal, and we can conclude that the amplitude of the *input* signal determines the behavior of the op amp. The output signal amplitude does not determine whether the response is small or large signal.

Multiple-Choice Quiz

- When a constant current is applied to a capacitor, the voltage on the capacitor will _____.
  a) increase exponentially
  b) increase linearly
  c) remain constant
  d) oscillate

- Slew rate is defined as _____.
  a) the maximum rate of change of an input signal
  b) the maximum frequency that can be applied before attenuation
  c) the maximum rate of change of the output voltage
  d) the rate of current consumption of the amplifier

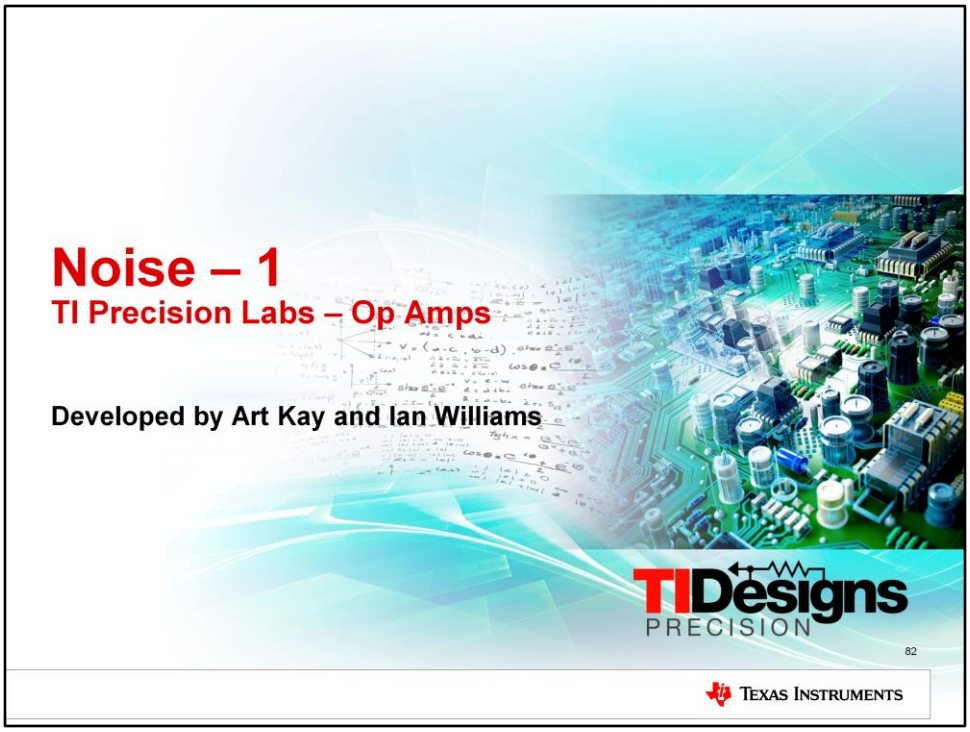
Multiple-Choice Quiz

- Settling time is the _____.
  a) Rise time from 10% to 90% of the output voltage
  b) Time starting from when the input step is applied until the output is within a specified error band
  c) time from the overshoot peak to the final dampened oscillation

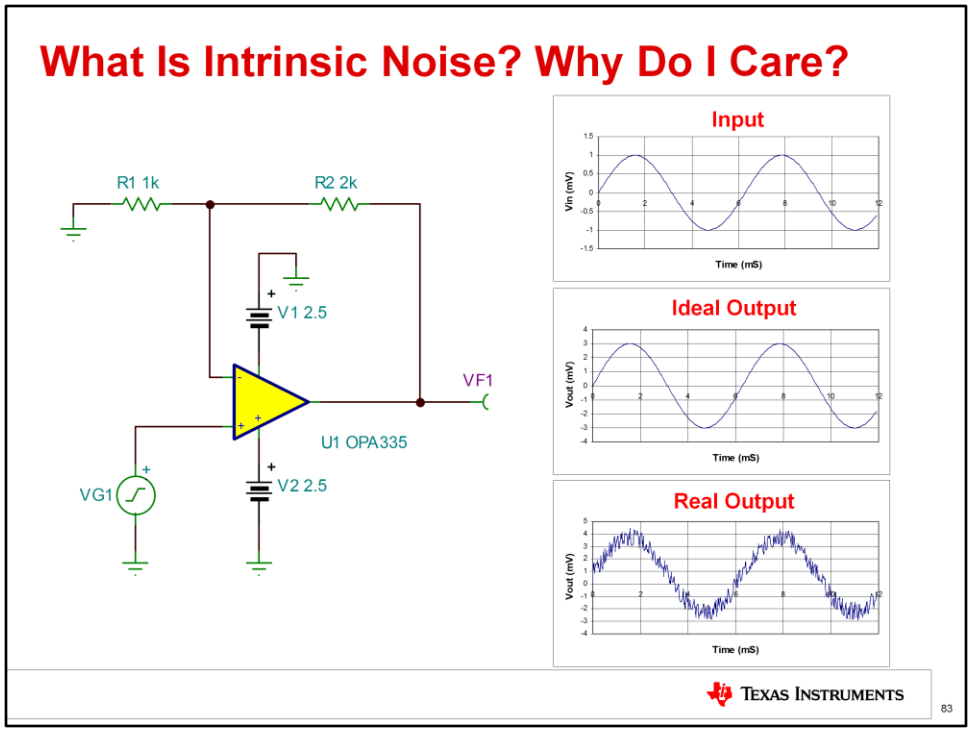
- Is settling time longer for a 0.1% or 0.01% error band?
  a) 0.1%
  b) 0.01%

Multiple-Choice Quiz

- Depending on the amplitude of the signal applied, an amplifier will exhibit a _____.
  a) small-signal response or slew-limited response
  b) small-signal response, slew-limited response, or transition between small-signal and slew limit
  c) phase shift
  d) stability limitation



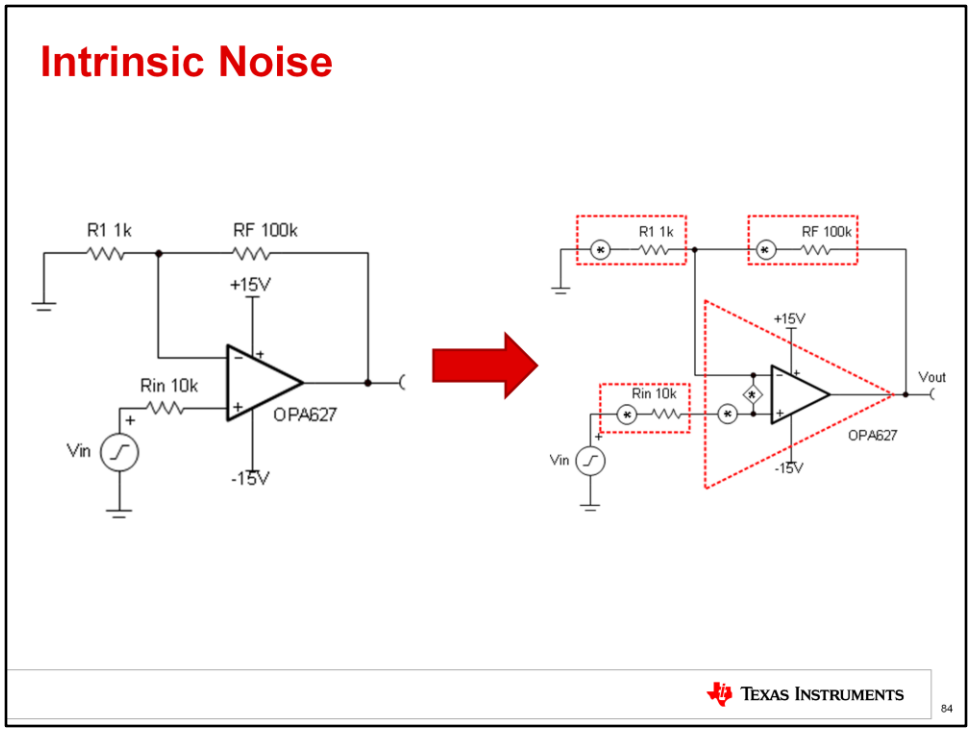
Hello, and welcome to the lecture for the TI Precision Labs discussing intrinsic op amp noise, part 1. In this lecture we'll show how to predict op amp noise with calculation and simulation, as well how to accurately measure noise.



Noise can be defined as an unwanted signal that combines with a desired signal to result in an error. In audio, for example, noise can be noticed as a hiss or popping sound. In a sensor system, noise can be an error in the measured sensor output, such as pressure or temperature.

Noise can be categorized into two basic groups: extrinsic and intrinsic. Extrinsic noise is noise produced from some external circuit or natural phenomena. For example, 60Hz power line noise and interference from mobile phones are common examples of extrinsic noise. Cosmic radiation is another example of a natural phenomenon that causes extrinsic noise. Intrinsic noise is caused by components within a circuit. Resistors and semiconductor devices generate noise, for example.

Intrinsic noise is very predictable, where as extrinsic noise is typically difficult to predict. In this noise lecture, we will focus on intrinsic noise. As we mentioned before, our discussion will focus on how to calculate, simulate, and measure noise. We will also discuss techniques for reducing noise.

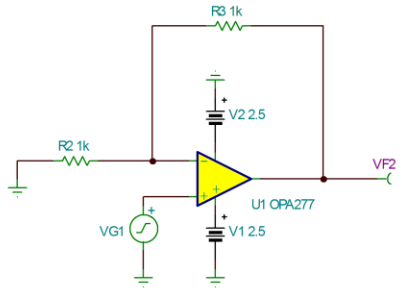


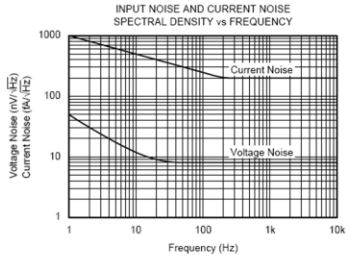
This slide illustrates how an amplifier circuit can be translated into a noise equivalent circuit.

Each resistor has a noise voltage source associated with it. The noise voltage source is denoted by a circle with an asterisk inside. The amplifier also has a noise voltage source and a noise current source. The noise current source is denoted by a diamond with an asterisk inside. The magnitude of the noise sources inside the amplifier is given in the amplifiers data sheet. The magnitude of the noise associated with the resistor is dependent on the resistance value and can be calculated.

We will soon learn how to combine the effects of all the noise sources to determine the total output noise. But first, lets look at some general categories of noise.

Noise Analysis for Simple Op-Amp Circuit





Noise Sources

- Op Amp Voltage Noise Sources
- Op Amp Current Noise Sources
- Resistor Noise Sources

Calculation Considerations

- Noise Gain
- Noise Bandwidth
- Convert Spectral Density to RMS
- Convert RMS to Peak-to-Peak

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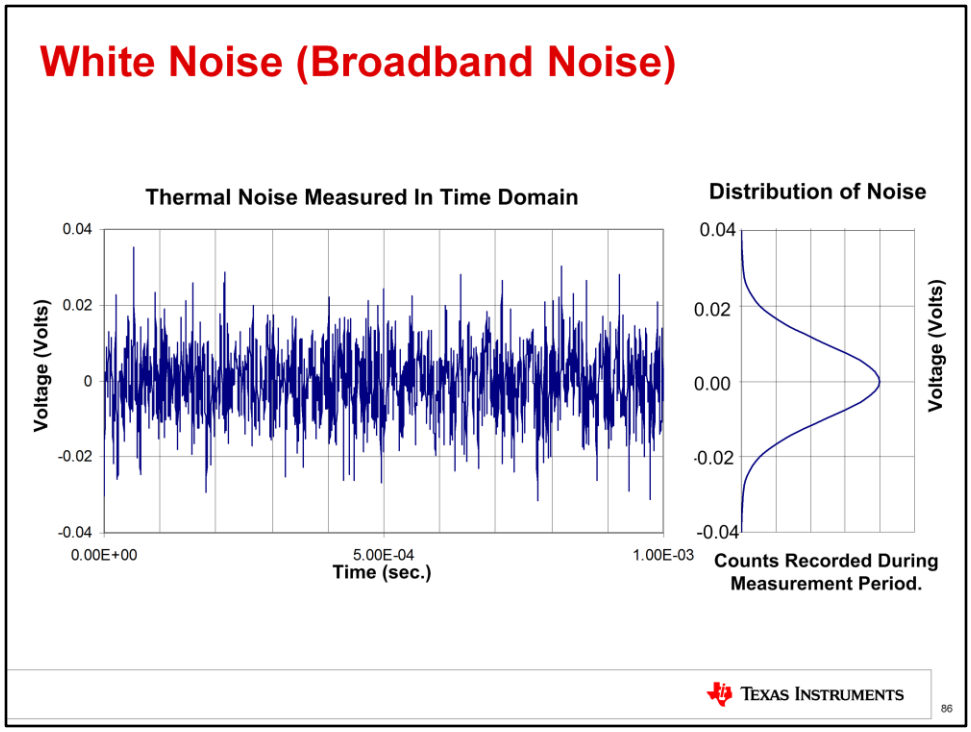
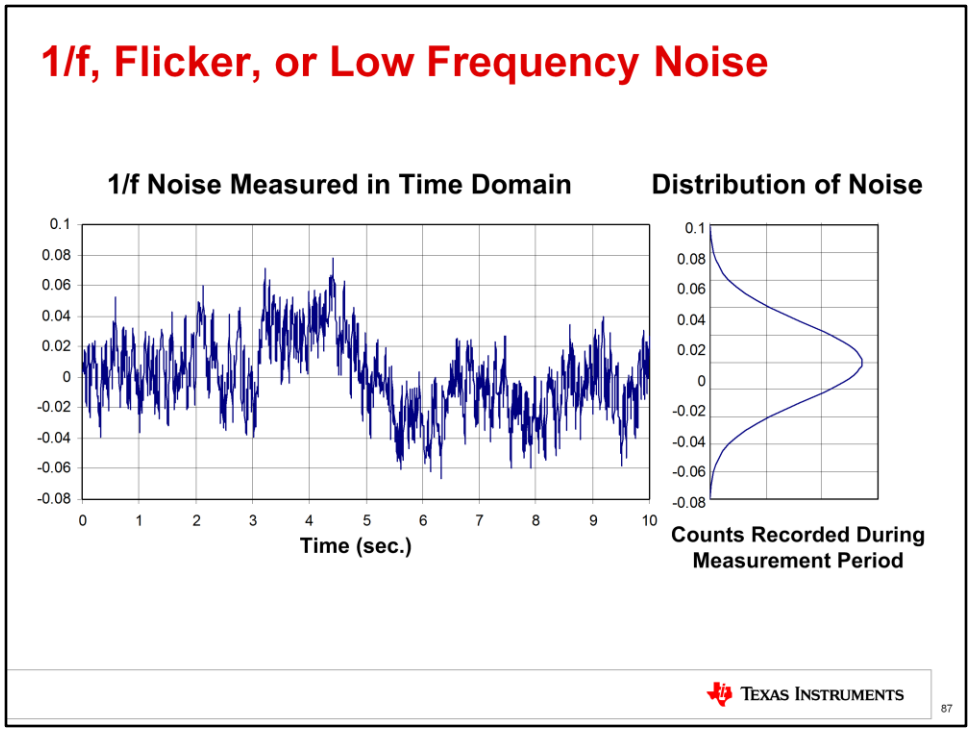
The noise analysis will involve looking at op amp noise voltage sources, op amp noise current sources, and resistor noise sources. The gain and bandwidth limitations of the op-amp will also effect the total noise calculation.

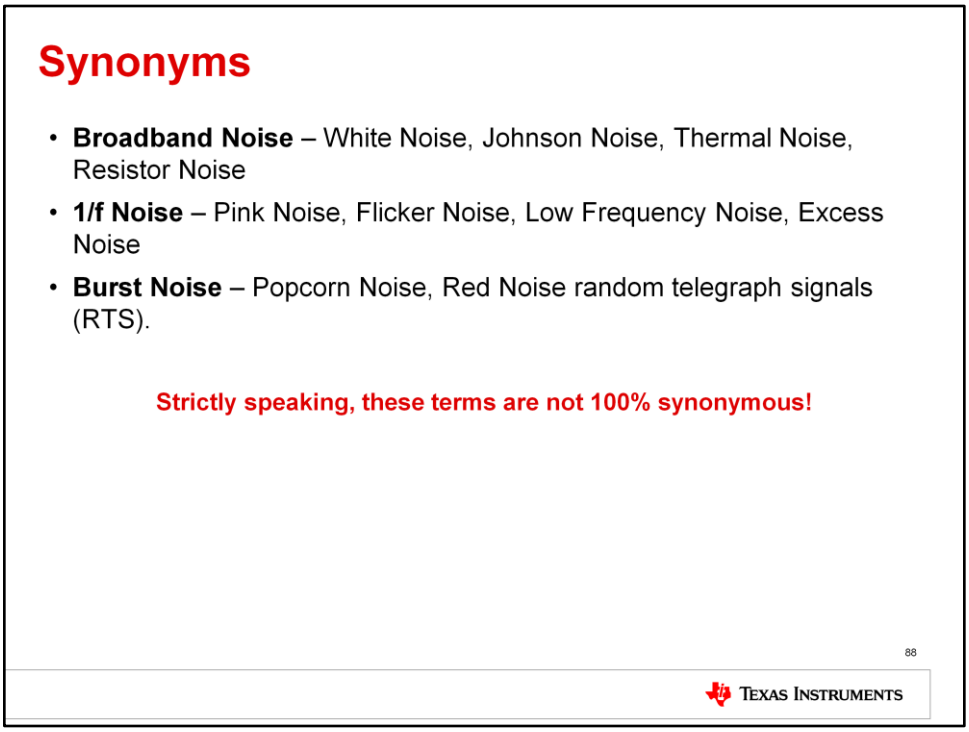


This slide shows the time domain waveform for white noise, also known as broadband noise. The time domain waveform is what you would see if you measured noise with an oscilloscope. Notice that the horizontal axis is 1ms, full scale. Taking the reciprocal of the full-scale time gives a frequency of 1kHz. In general, broadband noise is considered to be in the middle to high frequency range; that is, frequencies greater than 1kHz. In the next slide we'll consider lower frequency noise sources.

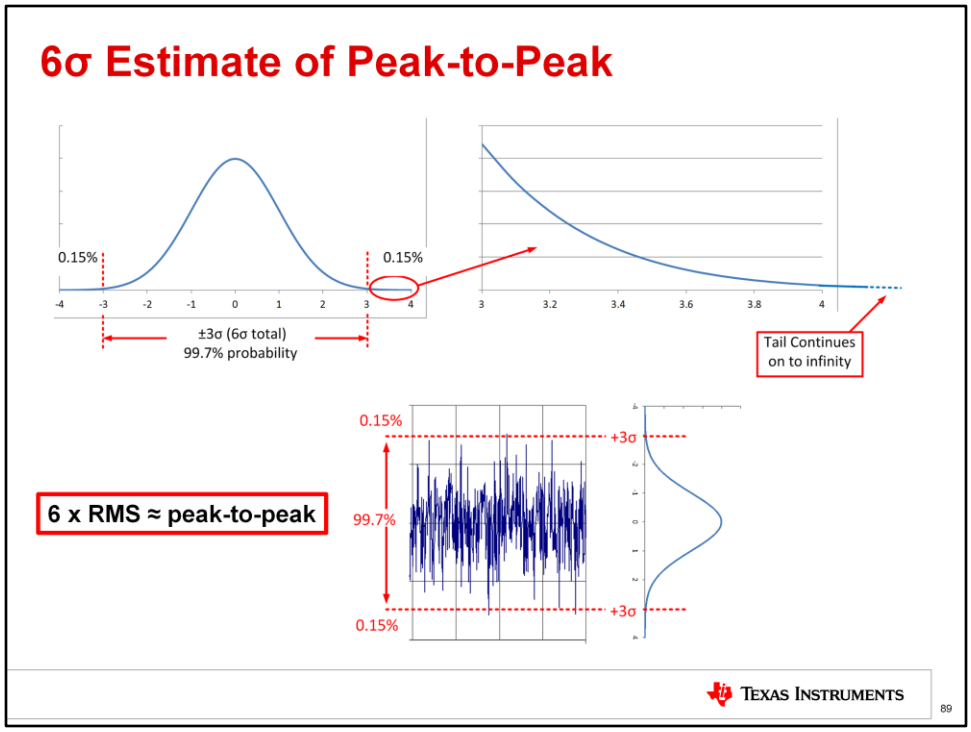
Also notice the statistical distribution to the right hand side of the slide. The distribution is Gaussian, with a mean value of 0V and the skirts of the distribution at approximately ±40mV. The distribution indicates that the probability of measuring noise near 0V is high, where as the probability of measuring noise near the skirts of the distribution is relatively low. Later we will see how the distribution can be used to estimate the peak-to-peak value of the noise signal.



Flicker noise, also known as 1/f or low frequency noise, is another category of noise. This slide shows the time domain waveform, as well as the statistical distribution for 1/f noise. The time domain waveform is what you would see if you measured noise with an oscilloscope. Notice that the horizontal axis is 10s full scale. Taking the reciprocal of the full scale time gives a frequency of 0.1Hz. In general, 1/f noise is considered to be in the low frequency range; that is, frequencies less than 1kHz.



As we have already seen, the various categories of noise have many synonyms. For example, broadband noise is also called white noise, Johnson noise, thermal noise, and resistor noise. It can become very confusing to engineers that are new to this subject when literature and presentations switch between these different terms.



Multiplying the rms noise by 6, or even 6.6, is a common estimate for peak-to-peak noise. Remember that noise has a Gaussian distribution. The Gaussian distribution tells us that there is a 99.7% probability that any reading in time is within the limits of +/- 3 standard deviation or 6 standard deviations total. This means that there is a finite probability of 0.3% that a noise reading will be outside of this limit. Sometimes 6.6 standard deviations is used, because the probability of noise being inside of the limits is increased to 99.9%. It is important to realize that the tails of the Gaussian distribution extend infinitely, so there is no number of standard deviations that will produce a 100% probability that all noise is inside of the bounds. Thus, 6 or 6.6. are used as good estimates. One final thing to keep in mind is that RMS and standard deviation are equivalent for noise signals with no mean value. This is generally true for the intrinsic noise that we are considering.

STDEV Relationship to Peak-to-Peak

Number of Standard Deviations	Percent chance of measuring voltage
2σ (same as ±1σ)	68.3%
3σ (same as ±1.5σ)	86.6%
4σ (same as ±2σ)	95.4%
5σ (same as ±2.5σ)	98.8%
6σ (same as ±3σ)	**99.7%**
6.6σ (same as ±3.3σ)	**99.9%**

Is standard deviation the same as RMS?

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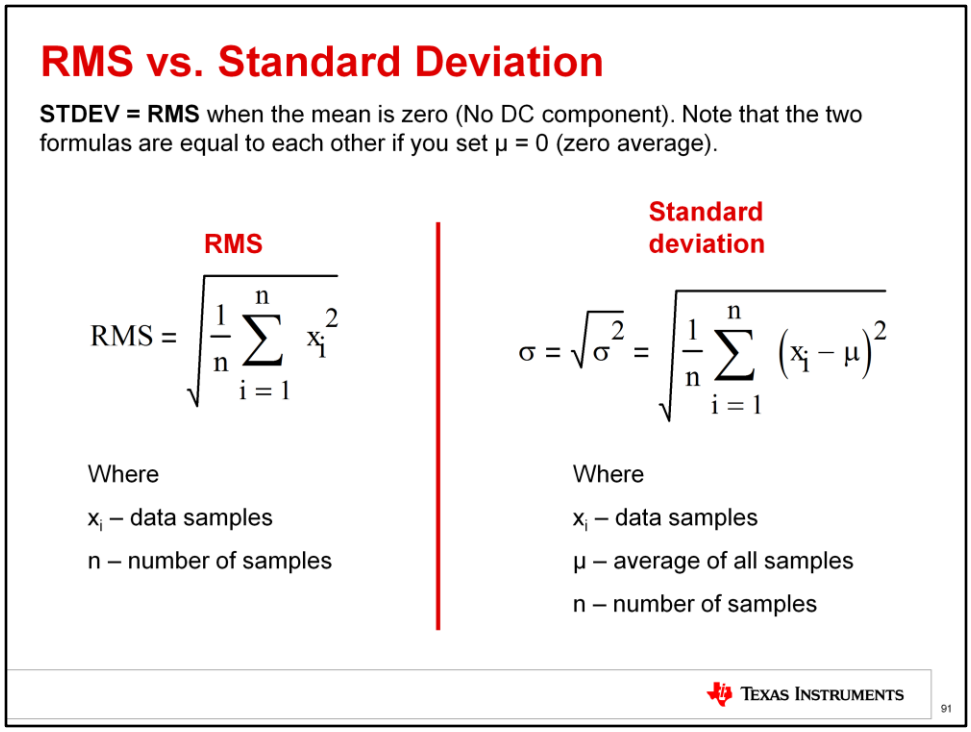
The table shown here relates the number of standard deviations to the probability that a measurement is bounded by this range. For example, there is a 68% chance that any instantaneous noise measurement will be in the range of 2σ, or ±1 standard deviation. 6σ and 6.6σ are common ways of estimating the peak-to-peak noise. In the case of 6σ, for example, there is a 99.7% chance that any instantaneous measurement will occur within that range. Thus, the chance that a noise reading is outside this limit at any instant in time is only 0.3%. The 0.3% probability is considered to be negligible, so 6σ is often used as an approximation for peak-to-peak noise.

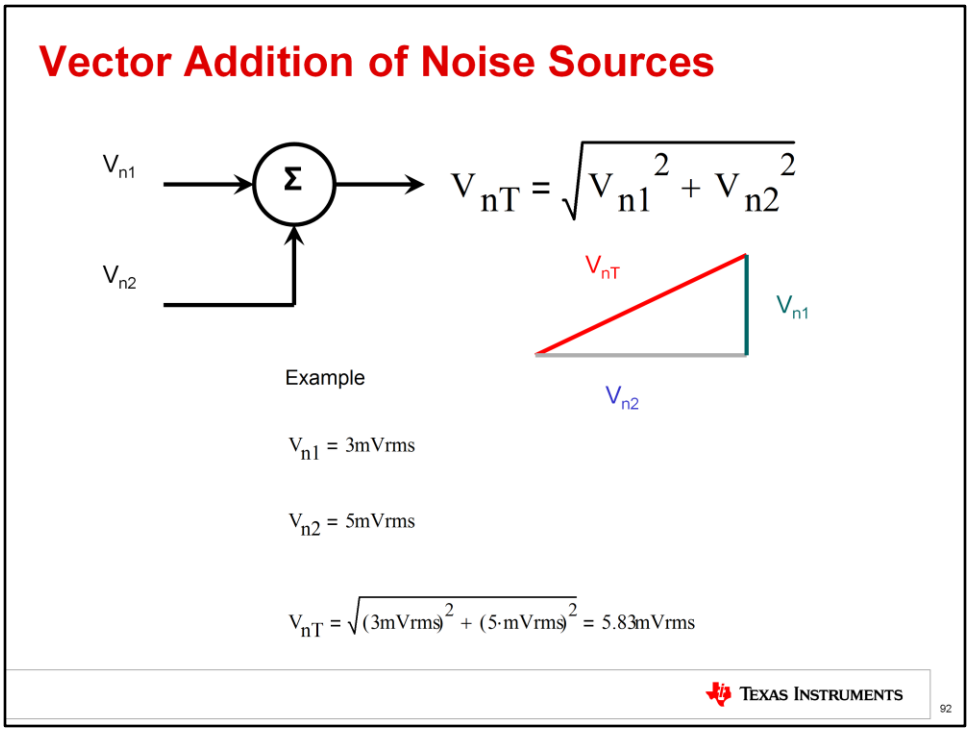
If you are familiar with noise analysis, you may have heard the terms standard deviation and RMS used interchangeably. This leads one to wonder, is RMS equivalent to standard deviation?



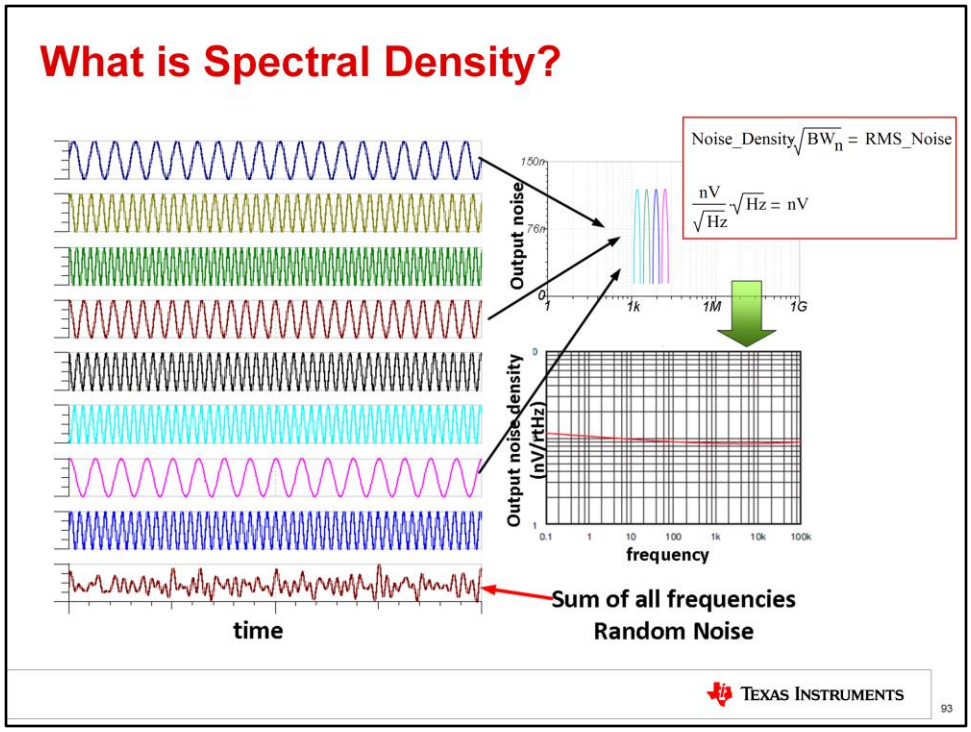
So, the question is does RMS = standard deviation?

The answer is both yes and no! If the signal has no DC offset, the answer is yes. This is the case for most noise signals. Notice that the equation for RMS and standard deviation are the same, except that the standard deviation equation subtracts out the average, or dc offset.

In the case where a signal has a DC offset, RMS will not be equal to the standard deviation. Fortunately, op-amp and resistor noise do not have a DC offset, so we can consider RMS to be equivalent to the standard deviation in these cases. Some extrinsic noise, such as digital switching noise, may not be symmetrical and thus will have a DC offset. It is important to note, however, that some instruments or simulation tools will report RMS noise including the offset term (AC + DC) and others will report RMS without the offset term (AC only).



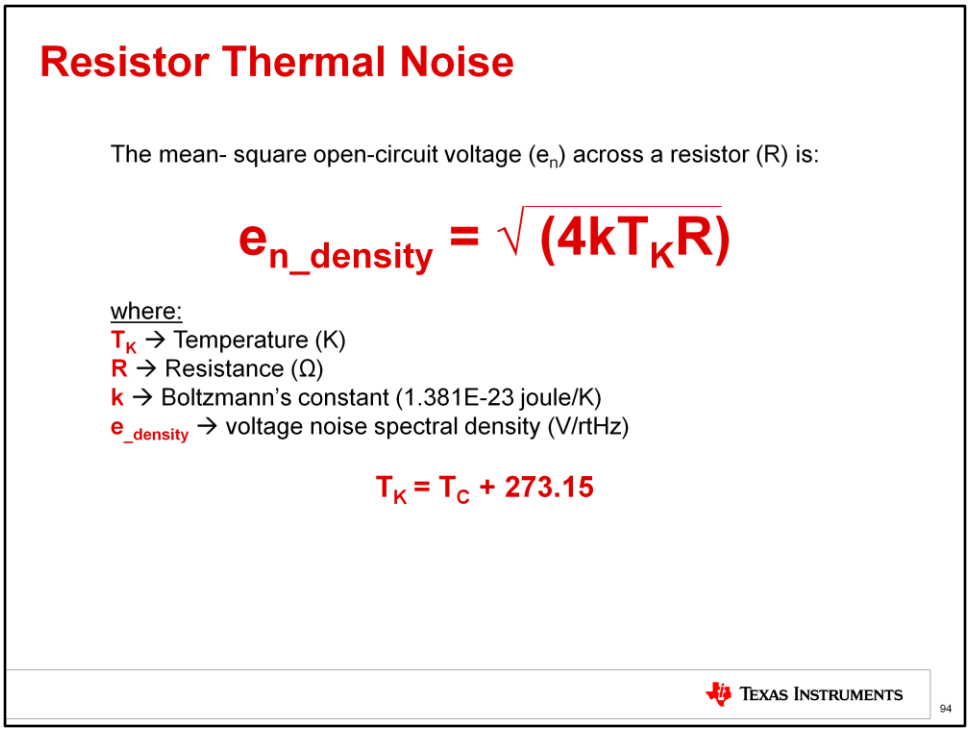
An important concept in nose analysis is adding noise values. Noise cannot be added algebraically, for example, 3+5=8. Noise must be added as a vector as shown here, where we take the square root of 3mVrms squared plus 5mVrms squared for a result of 5.83mVrms. It is important to note that this relationship applies only to uncorrelated ,random noise. If the noise source is correlated, a different formula applies.



Do you remember that white light is the combination of all colors? Well, white noise is the combination of all frequencies. This figure shows that when you add several signals of different frequencies together in the time domain, the result is a random looking signal. In the frequency domain, each one of these signals looks like an impulse. Combining an infinite number of these signals across all frequencies creates what is called a noise spectral density curve.

Voltage Noise Spectral Density is often a confusing parameter to engineers who are not familiar with noise analysis. Spectral density has units of nV per square root Hertz. Multiplying spectral density by the square root of the noise bandwidth gives the RMS noise as shown in the equation on the top right. Looking at the units in the equation, you can see how the square root Hertz cancels out.

The spectral density curve is the main amplifier specification used to describe an amplifier's noise characteristics. In this lecture we will use the spectral density curve extensively in noise calculations.

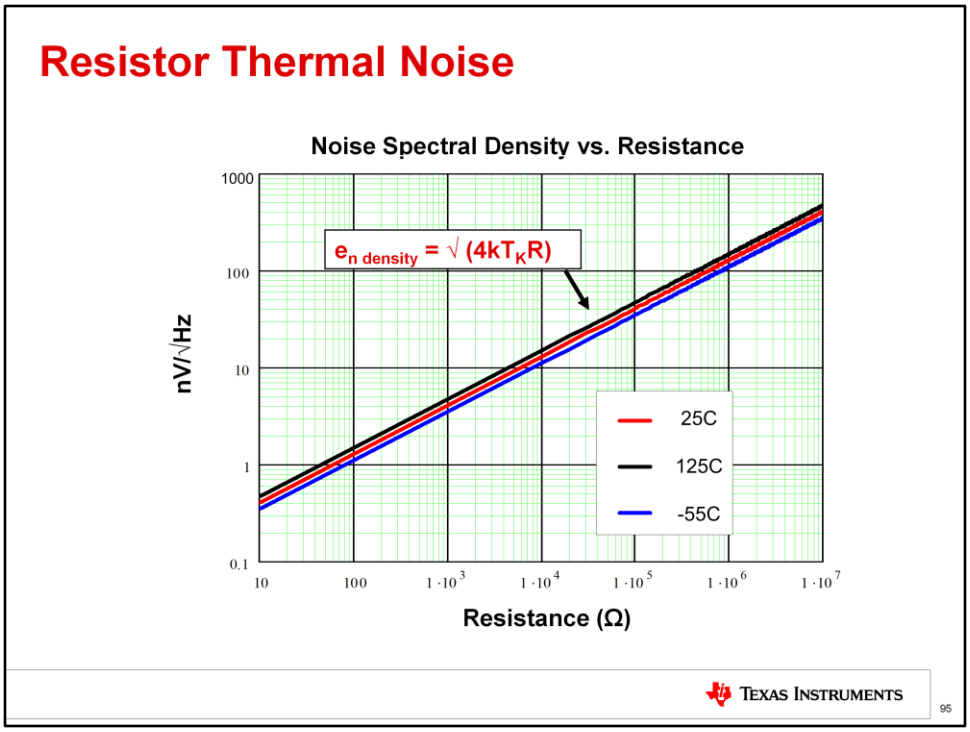


At this point we have introduced many of the fundamentals needed to understand noise.

This slide shows how to calculate the noise produced by a resistor. This noise is generated by the random motion of charges within the resistor.

The equation shown above gives the total RMS noise generated by a resistor. Notice that the equation requires the temperature in Kelvin, the resistance, the bandwidth, and Boltzmann's constant. Dividing both sides of the equation by the square root of the bandwidth yields the voltage spectral density equation.

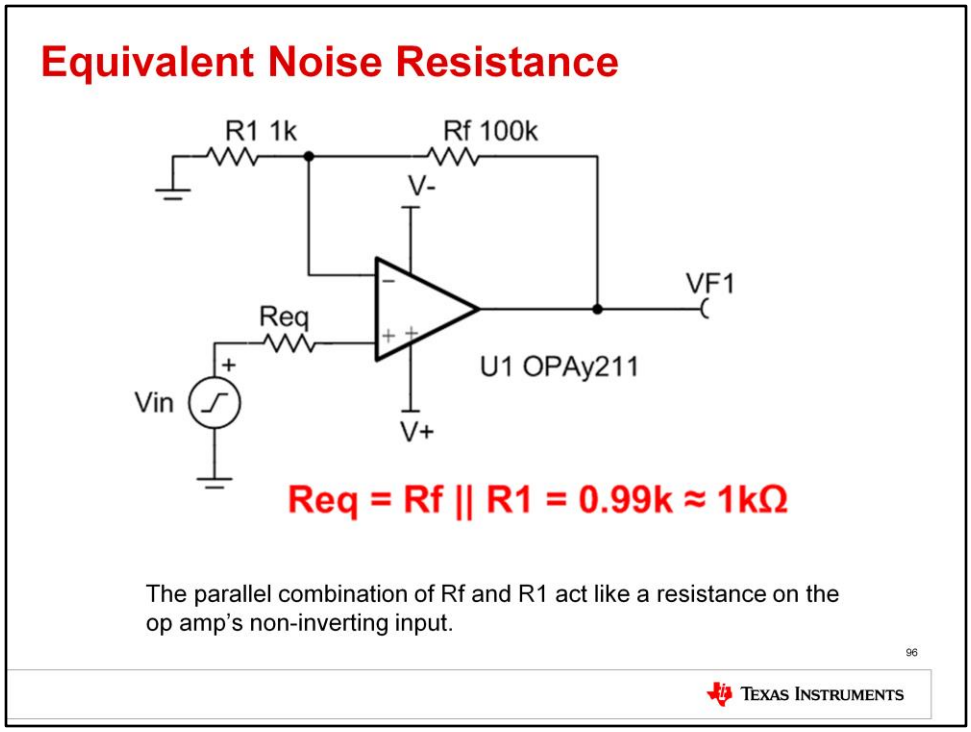
Remember that amplifiers' noise specifications are usually given in terms of spectral density. Determining the noise spectral density for a resistor is useful, because it allows for easy comparison of the noise generated by resistors and the noise generated by amplifiers.



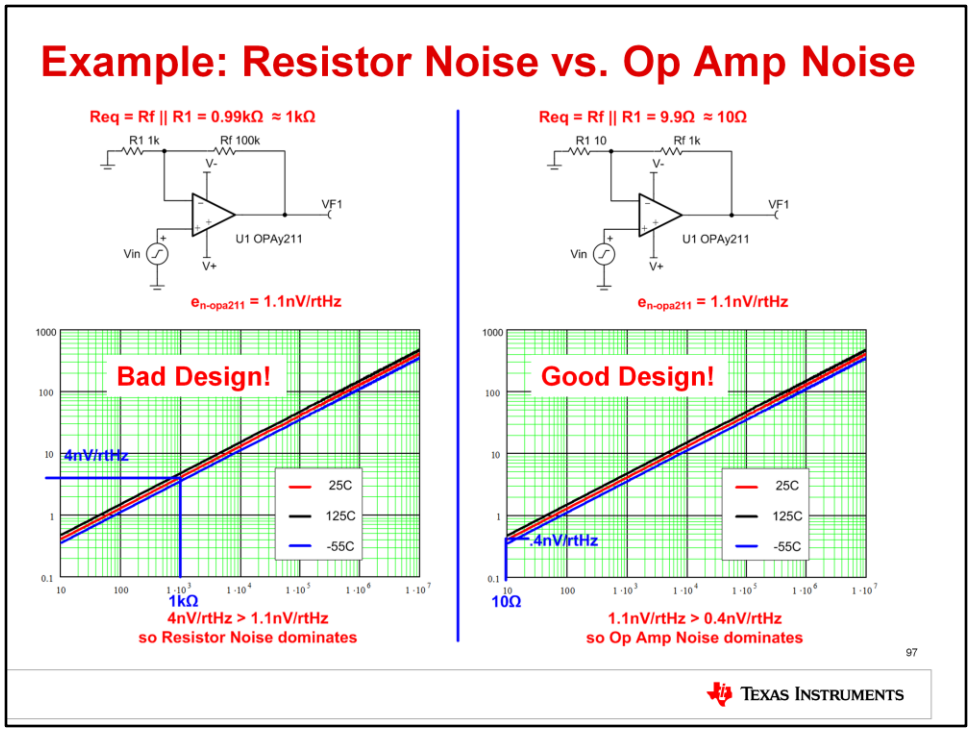
This plot was generated using the equation given in the last slide. Note that the equation was divided by the square root of bandwidth to give a spectral density, which is useful because it provides a quick way of comparing resistor noise to op-amp noise. Remember, most op-amps specify noise in nV/√(Hz).

A very low noise amplifier may have intrinsic noise of 1nV/√(Hz) noise. Comparing to this plot, 1nV/√(Hz) corresponds to a resistor value of approximately 70 ohms. Thus, for this example, op-amp you should try to use resistors of 70 ohms or less. For best performance, it's recommended for the amplifier in a circuit to generate more noise than the resistors. Low noise amplifiers can be expensive, and you would not want to pay extra for an expensive low noise amplifier and have resistor noise dominate the circuit's noise performance.

Neglecting resistor noise is a very common oversight of engineers who are new to noise analysis. For this reason, it is useful to have this chart available for quick reference.



For noise calculations, it is often necessary to calculate Req, the equivalent resistance seen by the input. The most common method for calculating Req is given here. The parallel combination of Rf and R1 act like a resistance on the op amp's non-inverting input, so Req in this example has a value of approximately 1k.



Let's compare resistor/thermal noise to op amp noise in two different circuits.

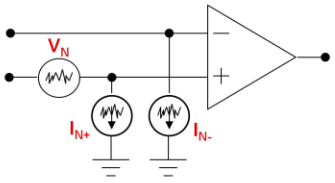
On the left, resistances of 1k and 100k are used. Req is roughly 1k, which according to the graph has a noise density of about 4nV/√Hz. This is greater than the noise density of the OPA211, so the circuit is dominated by resistor noise.

On the right, the same circuit but with resistances of 10 ohms and 1k are used. Req is now roughly 10 ohms, which has a noise density of about 0.4nV/√Hz. This is much less than the noise density of the OPA211, so the op amp noise dominates. This situation is most desirable for low-noise performance.

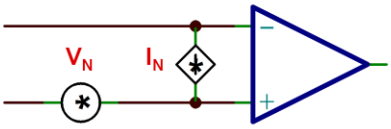
Op-Amp Noise Model

Noise Model

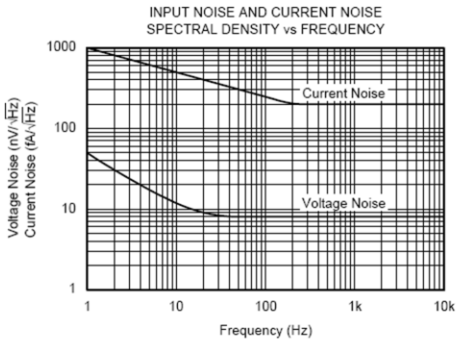
(I_{N+} and I_{N-} are uncorrelated)



Tina Simplified Model



OPA277 Data



TEXAS INSTRUMENTS

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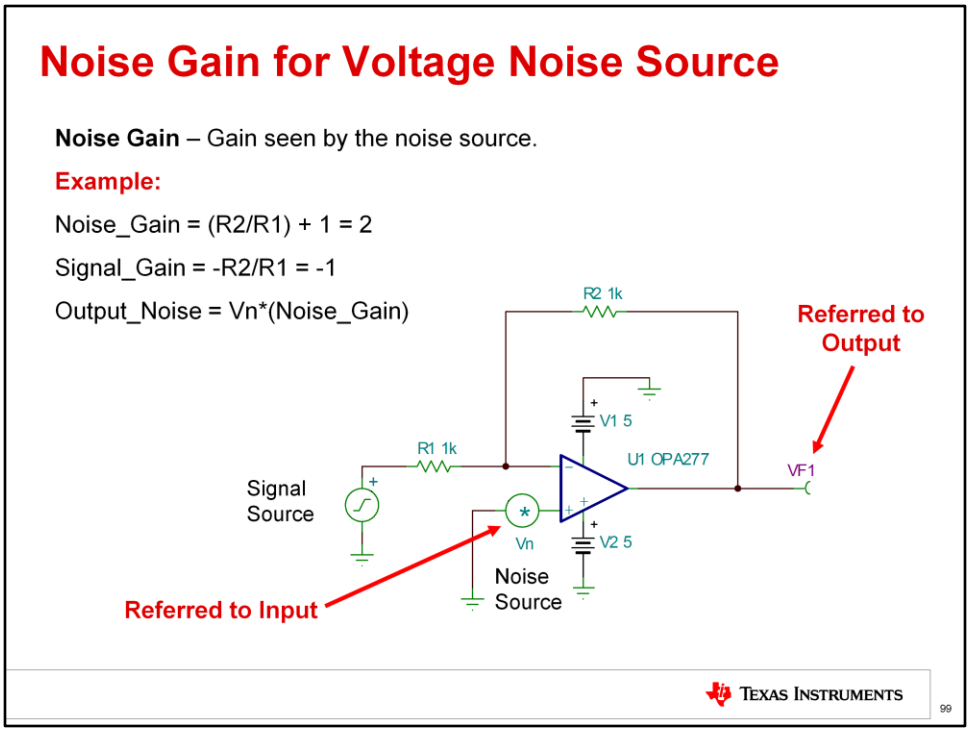
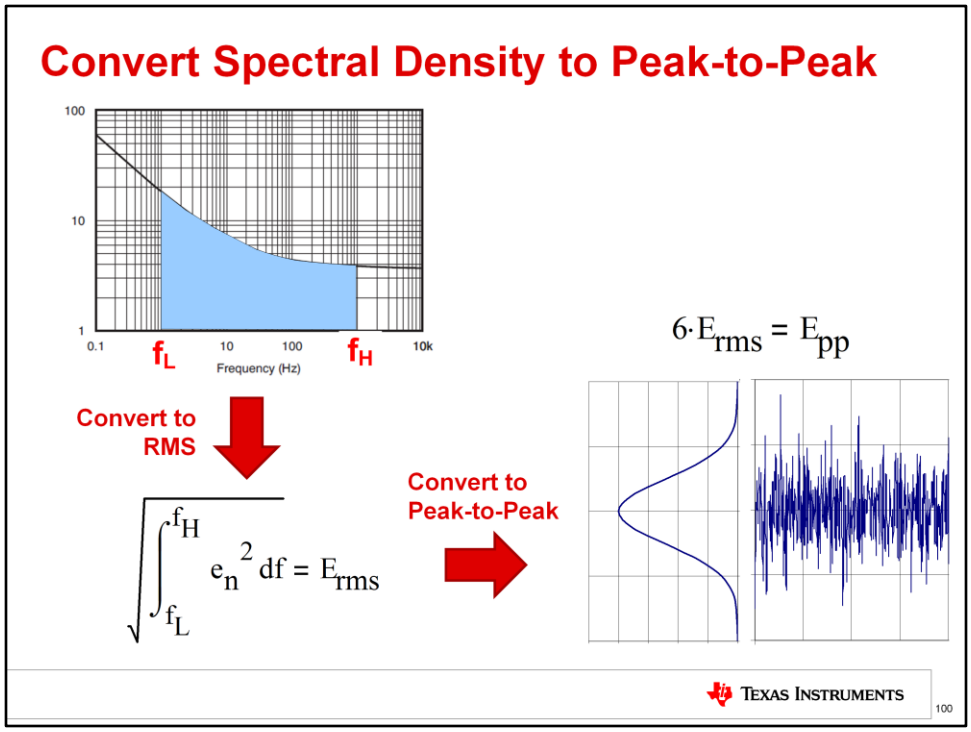
This slide show the typical op-amp noise model. In some cases, it is important to have two separate current noise sources, as shown in the upper left. In other cases, the simplified model with a single noise source between the inputs is adequate. The noise sources represent the spectral density curves. In the following lecture discussing noise, we will learn how to use the op amp noise model to predict the total peak-to-peak output noise for different amplifier configurations.



A key concept that we must understand before doing a noise analysis is **noise gain**. Noise gain is the gain seen by the noise voltage source, which is always on the non-inverting input of the amplifier. It can be different from the signal gain. The example above shows a circuit with a noise gain of 2 and a signal gain of -1. In other words, the circuit is an inverting amplifier with respect to the signal source, but a non-inverting amplifier to the noise voltage source.

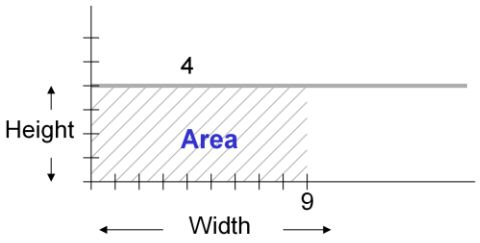


This slide summarizes the general procedure for converting voltage spectral density to RMS noise voltage, and for converting RMS to peak-to-peak voltage. To convert voltage spectral density to RMS, you must square the voltage spectral density, integrate across the desired bandwidth, and take the square root of the result. This is effectively integrating the power spectral density and taking the square root to convert back to voltage or current. Remember that $P = V^2 / R$ and $P = I^2 \times R$. We will discuss this in more detail soon.

Once the RMS noise voltage is calculated, it can be converted to peak-to-peak by multiplying by 6. The factor of 6 is a statistical estimate, representing ±3 standard deviations or 6σ, and there is a 0.3% chance that noise will exceed the peak-to-peak estimate at any instant in time.

Calculus Reminder

$$\int_0^9 4\,dx = 4 \cdot 9 = 36$$ Height x Width



Integral = Area under the curve

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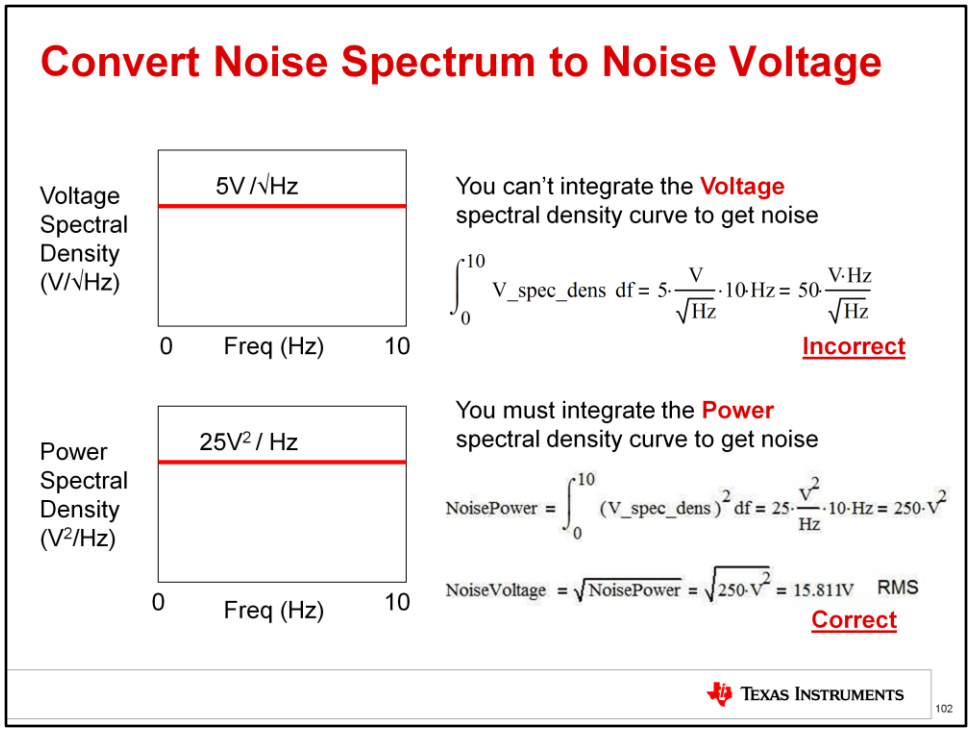
In order to gain a deeper understanding of the conversion from spectral density to RMS, we will need to use a little calculus. As a quick reminder, remember that the integral of a function is the area under its curve. The area of a rectangle is simply the width times the height, so the integral of a rectangle is also the width times the height. This simple fact will be useful in doing a dimensional analysis for noise.

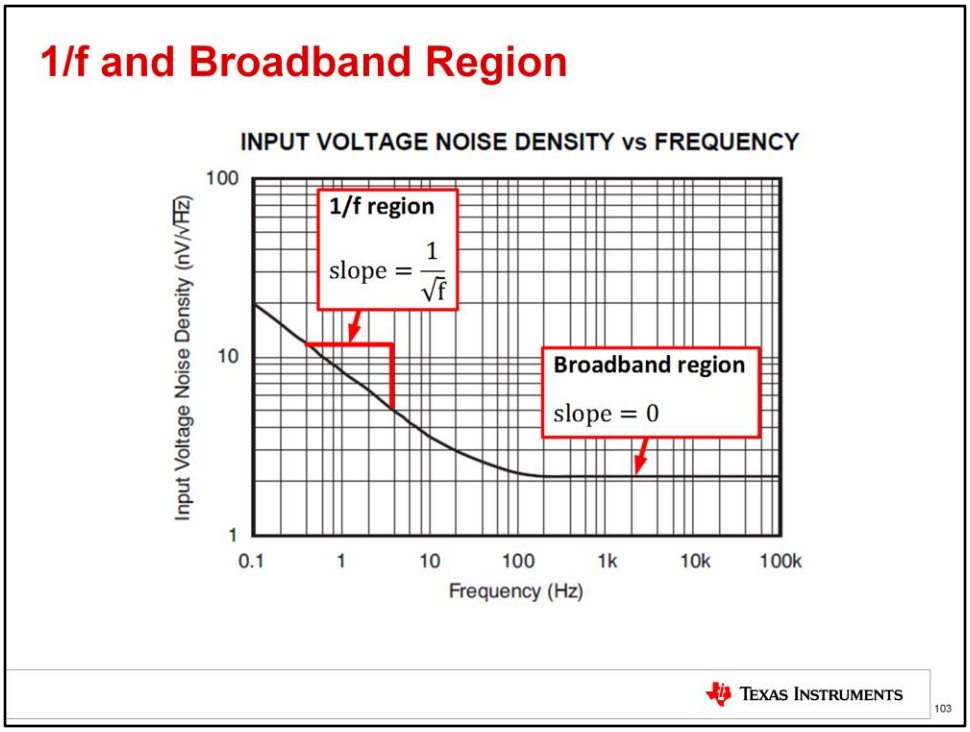


In this slide we will reiterate the method for converting from voltage spectral density to RMS voltage. A common misunderstanding with noise analysis is that total noise can be computed by integrating the **voltage** or **current** spectral density, when in fact you must integrate the **power** spectral density.

The example at the top of the slide shows what happens when integrating voltage spectral density. Remember from the previous slide that the integral of a rectangle is the width times the height, so in this case the result is 5 V/√Hz x 10Hz. Notice that the units for this example are very unusual, V*Hz / √Hz. In fact, the units should be Volts. The point is that through dimensional analysis you can see that integrating voltage spectral density directly is not the correct way to convert spectral density to rms.

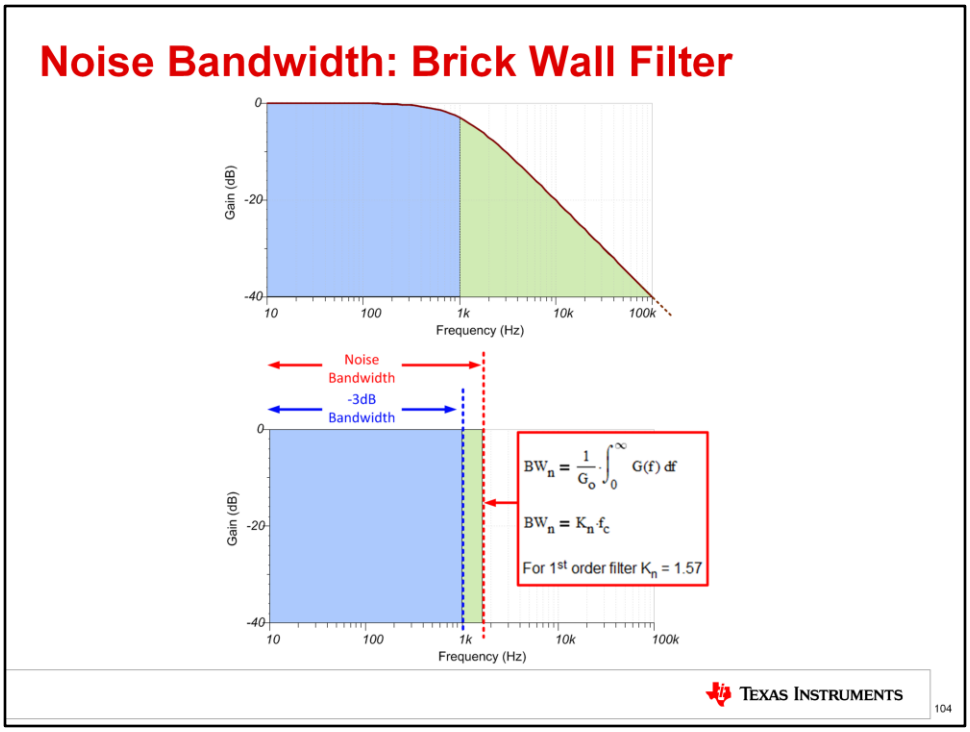
The example at the bottom, on the other hand, integrates power spectral density. Again, remember that that power is equal to V^2/R for voltage and I^2*R for current. When integrating power spectral density and taking the square root of the result, you get the correct units of Volts. Thus, when computing total noise, make sure to integrate the power spectrum.

Now that we understand how to properly integrate a spectral density curve, let's consider the different regions.



The spectral density curve has two regions: the 1/f region and the broadband region. 1/f noise occurs at low frequency, and has a slope of one divided by the square root of frequency for both voltage and current spectral density. Remember that power spectral density is voltage spectral density squared, so for power spectral density the slope of 1/f noise is equal to one divided by frequency. This is where it gets the name 1/f. Broadband, or white noise, has a flat spectral density.

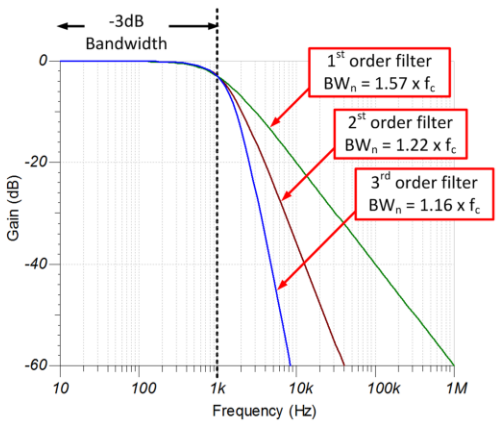
Let's take a closer look at 1/f noise.



Let's move on to the topic of noise bandwidth. As mentioned previously, the noise bandwidth of a real-world system has a low-pass filter response due to the circuit's inherent bandwidth limitations. The area under the skirt of the low pass response, shown in green, is added to the flat band response, shown in blue, to create a rectangle-shaped low pass filter. This rectangular filter, called a **brick wall** filter, has the same area as the low pass filter. It is called a brick wall because the stop band drops off vertically like a "brick wall". The point of doing this transformation is that a rectangle is easy to integrate so the noise calculations are greatly simplified.

Notice that the formula used to calculate the noise bandwidth involves calculus. In general, this formula is only needed once, and allows us to determine easy-to-use correction factors for different order filters. In this example, the formula was used to compute the correction factor of 1.57 for a 1st-order filter. On the following slide we will see correction factors for other order filters.

Noise Bandwidth: Brick Wall Factor



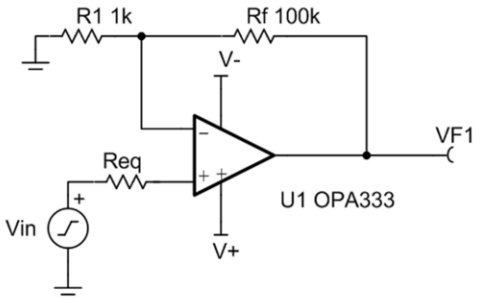
Noise Bandwidth

$BW_n = f_H * K_n$

Number of Poles	K_n Brickwall Correction Factor
1	1.57
2	1.22
3	1.16
4	1.13
5	1.12

This slide gives a table of brick wall correction factors that can be used to calculate noise bandwidth. To convert the -3dB bandwidth to the noise bandwidth, just multiply by the correction factor $\mathbf{K_n}$. Notice that the brick wall correction factor begins to approach one as the number of poles increases. This makes sense, since higher-order filters have a steeper roll-off, like a brick wall. One thing to consider is that gain peaking can affect the noise bandwidth, so in practical circuits the actual noise bandwidth may differ somewhat.

Noise Bandwidth Example



$$f_c = \frac{GBW}{Gain} = \frac{350kHz}{101} = 3.5kHz$$

$$BW_n = K_n \cdot f_c = 1.57 \cdot 3.5kHz = 5.5kHz$$

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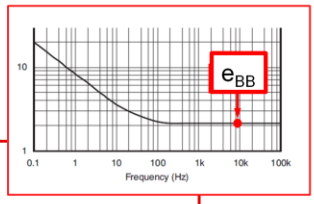
Let's calculate an example noise bandwidth for a simple circuit.

This circuit is in a non-inverting configuration and has gain of 101V/V. The gain bandwidth of the OPA333 is 350kHz, so we get a cutoff frequency or fc of 3.5kHz. Because there is no additional filtering on the circuit, it is only affected by the dominant pole of the op amp and therefore uses the K factor of 1.57 for a 1-pole system. This gives us a noise bandwidth of 5.5kHz.

Broadband Noise Equations



$$BW_n = K_n * f_H$$

Where:

BW_n	Noise bandwidth (bandwidth of brick wall filter)
K_n	Brick wall correction factor, includes the "skirt" of the low pass filter
f_H	-3dB upper cutoff frequency

$$E_{n_{BB}} = e_{BB}\sqrt{BW_n}$$

Where:

$E_{n_{BB}}$	Total RMS broadband noise
e_{BB}	Broadband voltage noise spectral density
BW_n	Noise bandwidth

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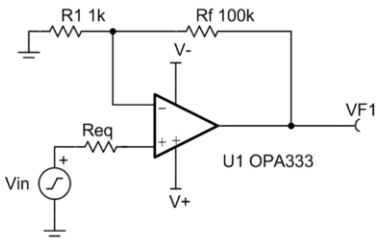
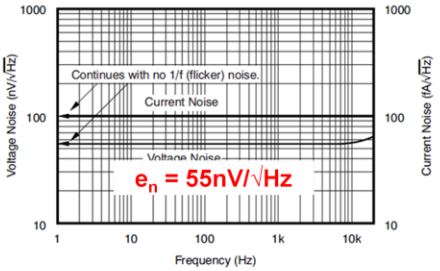
Now that we have the noise bandwidth relationship, we can use it to convert the op amp noise spectral density curve to RMS noise. The first equation given in this slide is the noise bandwidth equation that we have already discussed. Simply use the table on the previous slide to select the appropriate value for K_n and convert your signal bandwidth to noise bandwidth.

The second equation on this slide shows how to convert spectral density to RMS noise. The RMS noise, E_{n_BB}, is calculated by multiplying the broadband noise spectral density by the square root of the noise bandwidth. The value for the broadband spectral density can be read from the spectral density curve given in the op amp's data sheet. The relationship for converting noise spectral density to RMS noise is of key importance and should be memorized. It helps to remember the units when memorizing the formula. Spectral density in nV/√Hz is multiplied by the square root of noise bandwidth; the √Hz from both factors cancels so that RMS voltage has units of Volts.

Example: Calculating RMS Broadband Noise





$$f_c = \frac{GBW}{Gain} = \frac{350kHz}{101} = 3.5kHz$$

$$BW_n = K_n \cdot f_c = 1.57 \cdot 3.5kHz = 5.5kHz$$

$$E_n = e_n \cdot \sqrt{BW_n} = 55\frac{nV}{\sqrt{Hz}} \cdot \sqrt{5.5kHz} = 4\mu V \quad rms$$

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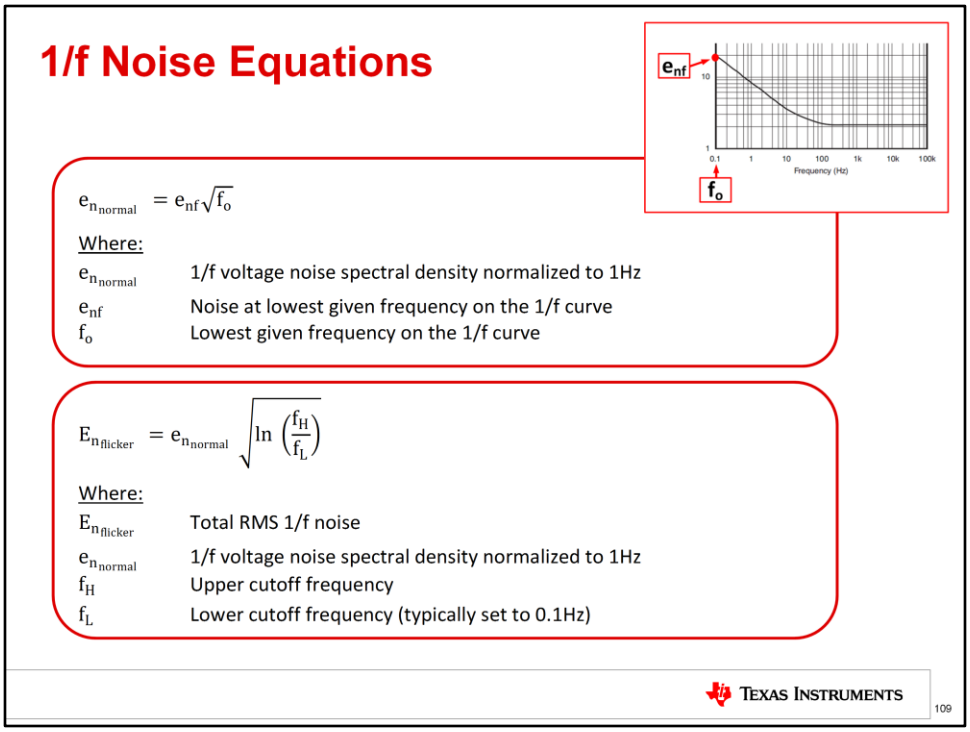
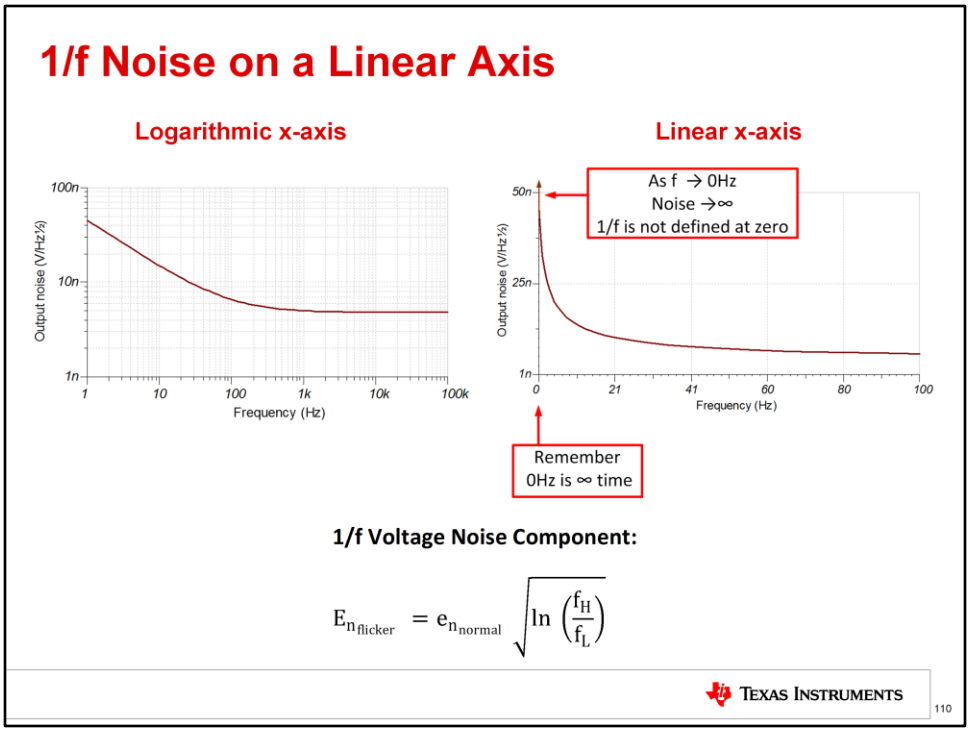
TEXAS INSTRUMENTS

Let's continue the example calculation and determine the RMS broadband noise. The noise bandwidth from before is 5.5kHz. We now take the OPA333 input voltage noise spectral density and multiply it by the square root of the noise bandwidth to get a result of 4uVrms.



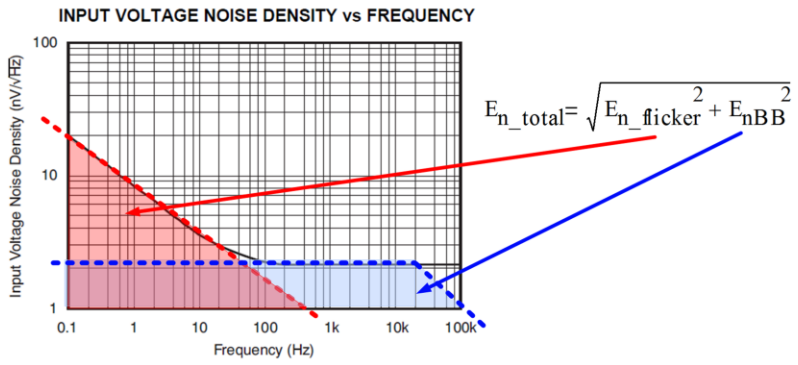
Let's move on to the 1/f noise equations. The first equation gives the 1/f noise normalized to 1Hz, given by e_{n_normal}. This means that we take a point on the 1/f curve and translate the spectral density to a level corresponding to what would be read at 1Hz. In general, it is best to choose e_{nf} at the lowest frequency possible, because this will ensure that 1/f is dominant.

The second equation computes the total RMS noise from the 1/f region. Notice that the equation uses the normalized 1/f noise from the previous equation as well as both the upper and lower cutoff frequency. It's easy to understand why the upper cutoff frequency is used, because it represents the same system bandwidth limitation as seen in broadband noise. But why do we need a lower cutoff frequency limitation?



Remember that we normally look at noise spectral density on a graph with a logarithmic x-axis. If we instead consider the spectral density curve with a linear x-axis, it becomes clear that noise increases to infinity at 0 Hz. The fact that noise is infinite at 0 Hz sounds alarming, until you consider that 0 Hz corresponds to infinite time. Infinite time is not practical to consider, so for practical considerations we use 0.1Hz for f_L, the lower cutoff frequency. 0.1Hz corresponds to 10 seconds. Later, we will take a deeper look into low frequency noise and the effect of observing noise over long time durations.

Combining 1/f and Broadband



In fact, if we consider both regions at the same time, you can see that the 1/f and broadband region both are present at all frequencies. At low frequencies, 1/f noise is dominant, but broadband noise is still present. At higher frequencies, the broadband noise is dominant, but 1/f is still present. To find the total combined noise, you must add the contribution of the two regions using the root sum of the squares.

Multiple-Choice Quiz

- Examples of intrinsic noise are ____.
  a) 60Hz pickup
  b) Capacitive coupling of digital signals
  c) Thermal noise from resistors
  d) Noise generated by op amps
  e) Both a and b are correct
  f) Both c and d are correct

- How do you convert rms to peak-to-peak?
  a) Noise_pp = 6 x (spectral density)
  b) Noise_pp = 6 x (Total rms noise)
  c) Noise_pp = 1.57 x BW
  d) Noise_pp = (spectral density) x (BW)

Multiple-Choice Quiz

- Why is it important to insure that noise generated by external resistors is small compared to the amplifier noise.
  a) Because resistor noise is dominated by temperature
  b) Because resistor noise increases with frequency
  c) Because low noise amplifiers are expensive compared to resistors.
  d) Because resistor noise is difficult to filter.

- When is current noise a problem?
  a) When the amplifier is heavily loaded
  b) When small resistors are used for feedback components.
  c) When large resistances are used for feedback components
  d) When the input source has large resistances.
  e) Both a and b
  f) Both c and d

Multiple-Choice Quiz

- Flicker noise is infinite at 0Hz. Why isn't this a problem in practical circuits?.

a) Time at 0Hz is infinite also. Infinite time is not practical.
b) Because flicker noise decreases at ultra low frequencies
c) Modern semiconductor devices do not have flicker noise
d) Low frequency filtering avoids this issue.

Problems

1. Two noise sources are in series (20mV rms, and 30mV rms). What is the total noise?

$$e_{n\_total} = \sqrt{e_{n1}^2 + e_{n2}^2} = \sqrt{(20\text{mV})^2 + (30\text{mV})^2} = 36\text{mVrms}$$

2. What is the thermal noise voltage spectral density for a 10kΩ resistor at 25C and at 125C?

$$T_n = 273 + 25 \qquad e_{n\_r} = \sqrt{4k_n \cdot T_n \cdot R_n} = \sqrt{4\left(1.38 \cdot 10^{-23}\,\frac{\text{J}}{\text{K}}\right) \cdot (298\text{K}) \cdot (10\text{k}\Omega)} = 12.8\,\frac{\text{nV}}{\sqrt{\text{Hz}}}$$

$$T_n = 273 + 125 \qquad e_{n\_r} = \sqrt{4k_n \cdot T_n \cdot R_n} = \sqrt{4\left(1.38 \cdot 10^{-23}\,\frac{\text{J}}{\text{K}}\right) \cdot (398\text{K}) \cdot (10\text{k}\Omega)} = 14.8\,\frac{\text{nV}}{\sqrt{\text{Hz}}}$$

Problems

3. What resistance would be required to generate 1nV/√Hz?

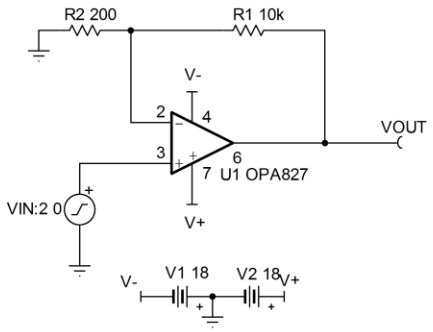
$$R_n = \frac{e_{n\_r}^2}{4 \cdot T_n \cdot k_n} = \frac{\left(1 \frac{nV}{\sqrt{Hz}}\right)^2}{4 \cdot (298K) \cdot \left(1.38 \cdot 10^{-23} \frac{J}{K}\right)} = 60.8\Omega$$

4. What is the rms voltage for a 10mVpp noise signal? Note: peak-to-peak translation to rms is always a statistical approximation. Remember that the noise is a Gaussian signal, so there is always a finite probability that a noise measurement will be on the far tail of the curve. The calculation below assumes that +/-3 standard deviations is sufficient for a peak-to-peak approximation.

$$\frac{10mVpp}{6} = 1.667mVrms$$

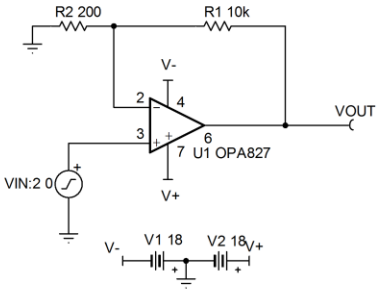
Problems

1. Find the total noise due to:
   a. Resistance
   b. Op amp broadband voltage noise
   c. Op amp 1/f voltage noise
   d. Op amp current noise
   e. Compute the total combined noise



Solutions

a. Resistance



$$k_n := 1.38 \cdot 10^{-23}$$

$$T_n := 273.15 + 25 = 298.15$$

$$R_n = \frac{R_f \cdot R_1}{R_f + R_1} = \frac{10k\Omega \cdot 200\Omega}{10k\Omega + 200\Omega} = 196\Omega$$

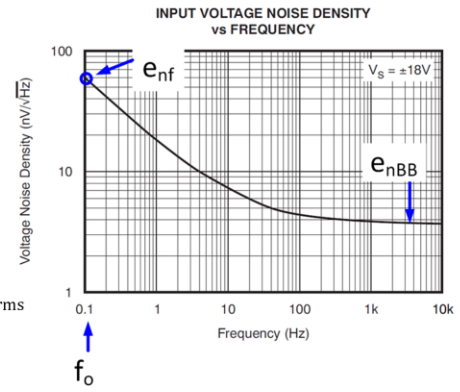
$$G_n = \frac{R_f}{R_1} + 1 = \frac{10k\Omega}{200\Omega} + 1 = 51$$

$$f_c = \frac{GBW}{G_n} = \frac{22MHz}{51} = 431kHz$$

$$BW_n = K_n \cdot f_c = (1.57) \cdot 431kHz = 677kHz$$

$$E_{n\_r} = \sqrt{4 \cdot k_n \cdot T_n \cdot R_n \cdot BW_n} = \sqrt{4 \cdot \left(1.38 \cdot 10^{-23}\right) \cdot (298.15) \cdot (196) \cdot \left(677 \times 10^{3}\right)} = 1.48\mu V$$

Solutions



b. Op amp broadband voltage noise

$$E_{nBB} = (e_{nBB})\sqrt{BW_n} = (3.8\,nV/\sqrt{Hz})\sqrt{(677kHz)} = 3.13\mu V\ rms$$

c. Op amp 1/f voltage noise

$$e_{n_{normal}} = e_{nf}\sqrt{f_o} = (60\,nV/\sqrt{Hz})\sqrt{0.1Hz} = 19nV$$

$$E_{n_{flicker}} = e_{n_{normal}}\sqrt{\ln\left(\frac{f_H}{f_L}\right)} = (19nV)\sqrt{\ln\left(\frac{677kHz}{0.1Hz}\right)} = 75.4nV\ rms$$

Solutions

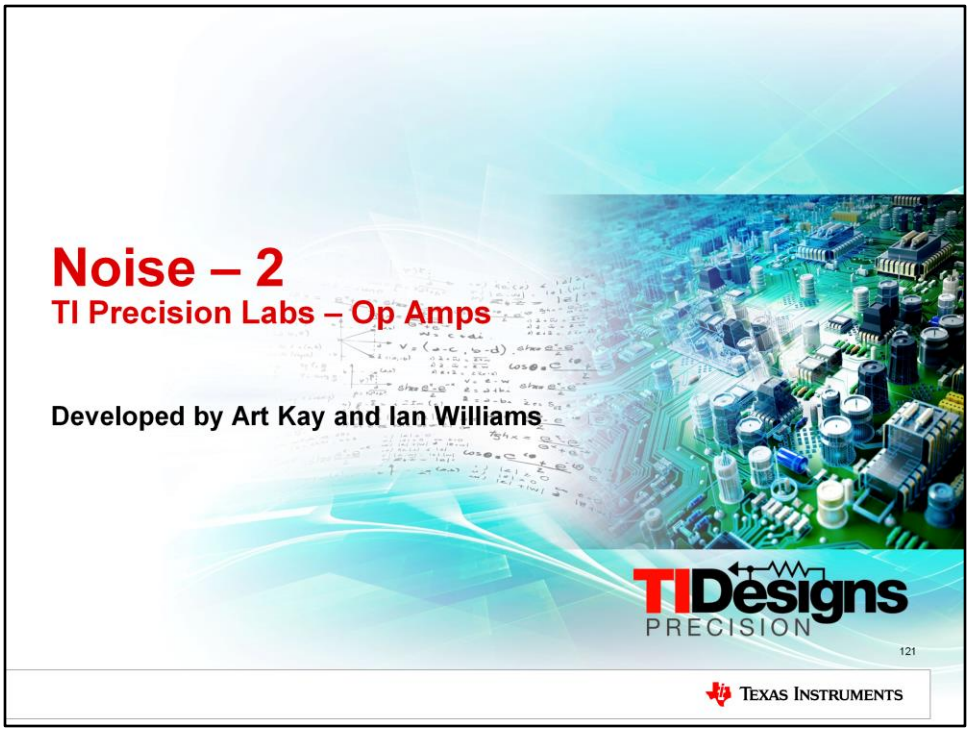
PARAMETER	CONDITIONS	OPA827AI			UNIT
		MIN	TYP	MAX	
Input Current Noise Density: f = 1kHz i_n	V_S = ±18V, V_{CM} = 0V		2.2		fA/√Hz

d. Op amp current noise

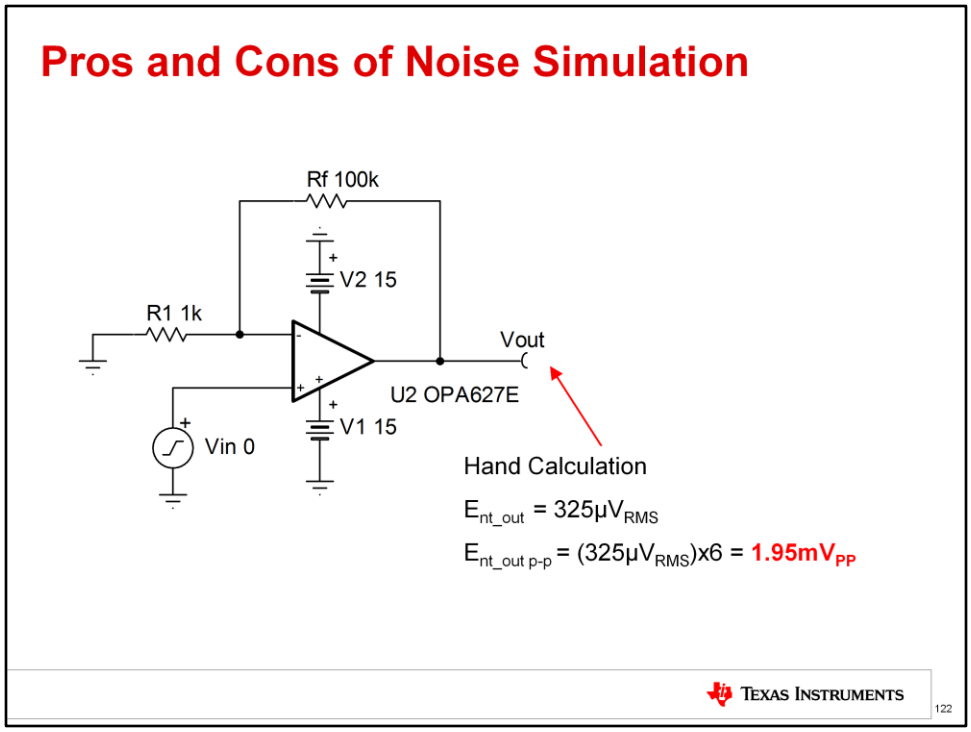
$$e_{ni} = R_{eq} \cdot i_n = (196\Omega)\left(2.2\,\text{fA}/\sqrt{\text{Hz}}\right) = 0.00043\,\text{nV}/\sqrt{\text{Hz}}$$
$$E_{ni} = e_{ni}\sqrt{BW_n} = \left(0.00043\,\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{677\text{kHz}} = 0.353\text{nV rms}$$

e. Total combined noise

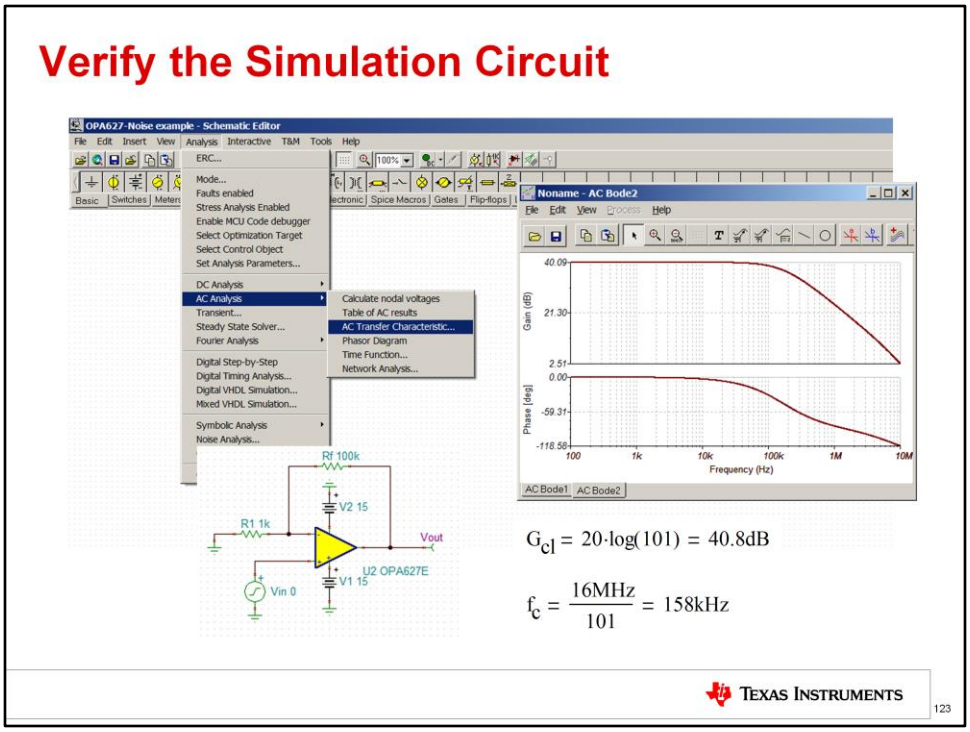
$$E_{n\_total} = \sqrt{E_{nr}{}^2 + E_{nBB}{}^2 + E_{nflicker}{}^2 + E_{ni}{}^2}$$
$$E_{n\_total\_in} = \sqrt{(1.48\mu\text{V})^2 + (3.13\mu\text{V})^2 + (75.4\text{nV})^2 + (0.353\text{nV})^2} = 3.48\mu\text{V rms}$$
$$E_{n\_total\_out} = G_n E_{n\_total\_in} = (51)(3.48\mu\text{V}) = 177\mu\text{V rms}$$
$$E_{n\_total\_out\_pp} = 6E_{n\_total\_out} = 6(177\mu\text{V}) = 1.07\text{mVpp}$$



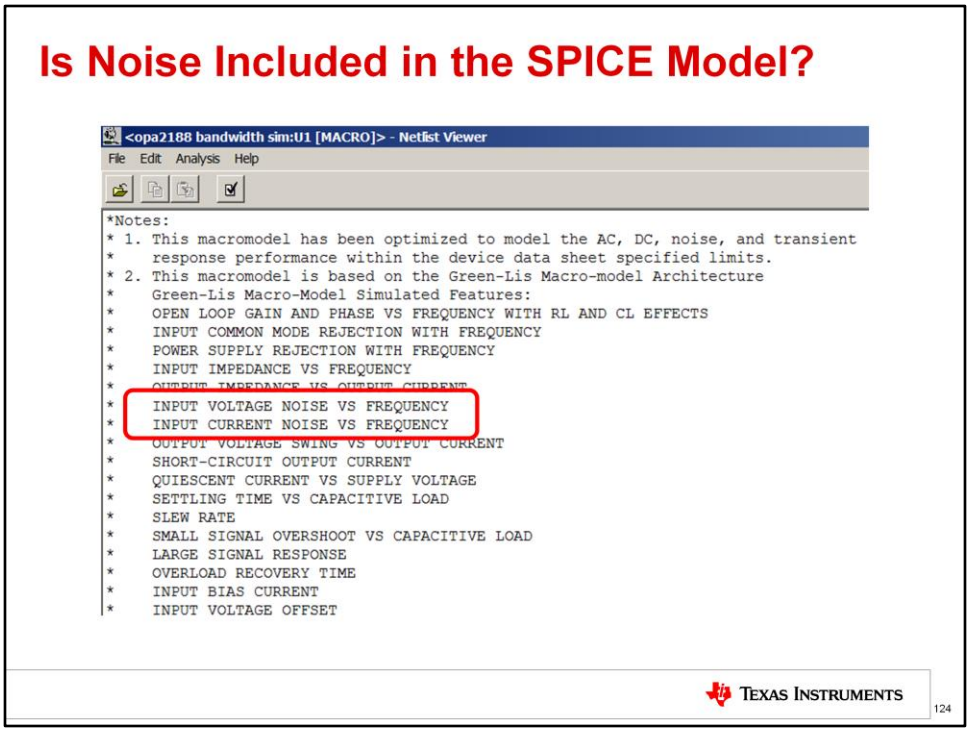
Hello, and welcome to the lecture for the TI Precision Labs discussing intrinsic op amp noise, part 2. In this lecture we'll discuss how to accurately simulate and measure noise.



Earlier in the workshop, we calculated the output noise for the OPA627 circuit shown on this slide. In this lecture we will learn how to solve the same problem using simulation. Using simulation to solve noise problems is much easer than hand calculations, so naturally some engineers choose to skip the hand calculations and rely only upon simulation. Don't fall into this trap! The hand calculations give useful insight into the dominant noise sources, which helps greatly when working to reduce noise. Furthermore, there may be an issue with the simulation that produces an erroneous result. On the other hand, having agreement between simulation and hand calculation gives you strong confidence that your answer is correct.

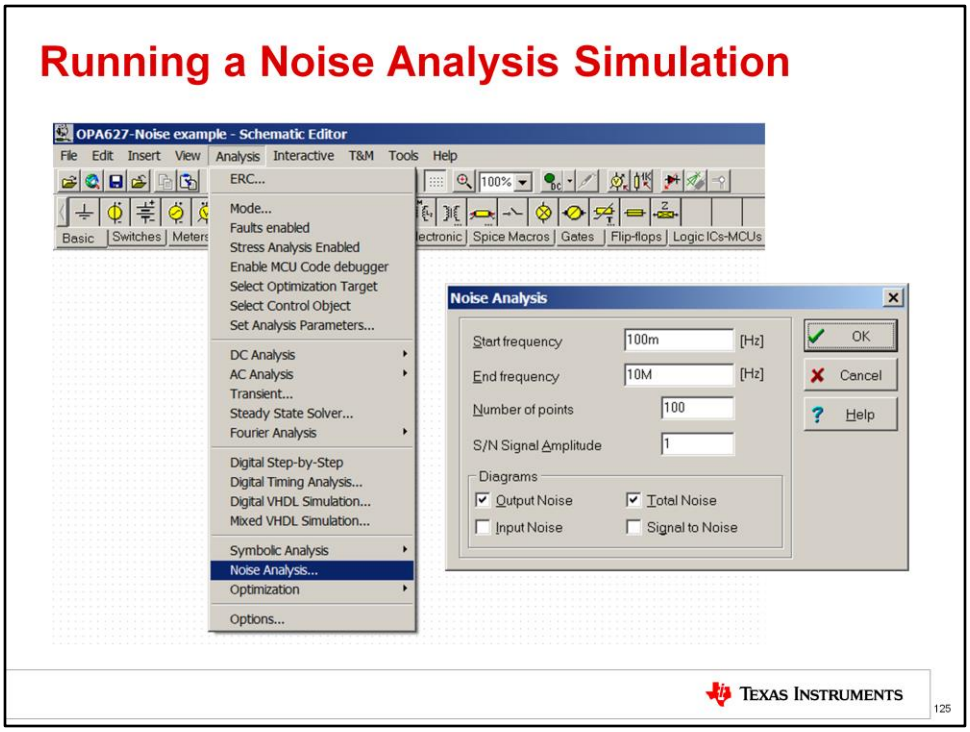


Before doing a noise simulation, you need to be verify that the circuit is connected properly. This is important because SPICE will not necessarily issue an error or warning if the circuit is miswired. Often, circuits that are miswired just give an incorrect noise simulation result, which can trick you into thinking that your system has really great noise performance. The easiest way to be confident that your circuit is connected correctly is to run an ac transfer characteristic. Refer to the lecture on Bandwidth for a review of how to run an ac transfer characteristic simulation. A very simple hand calculation for gain and bandwidth can confirm that the simulation circuit is working as intended.



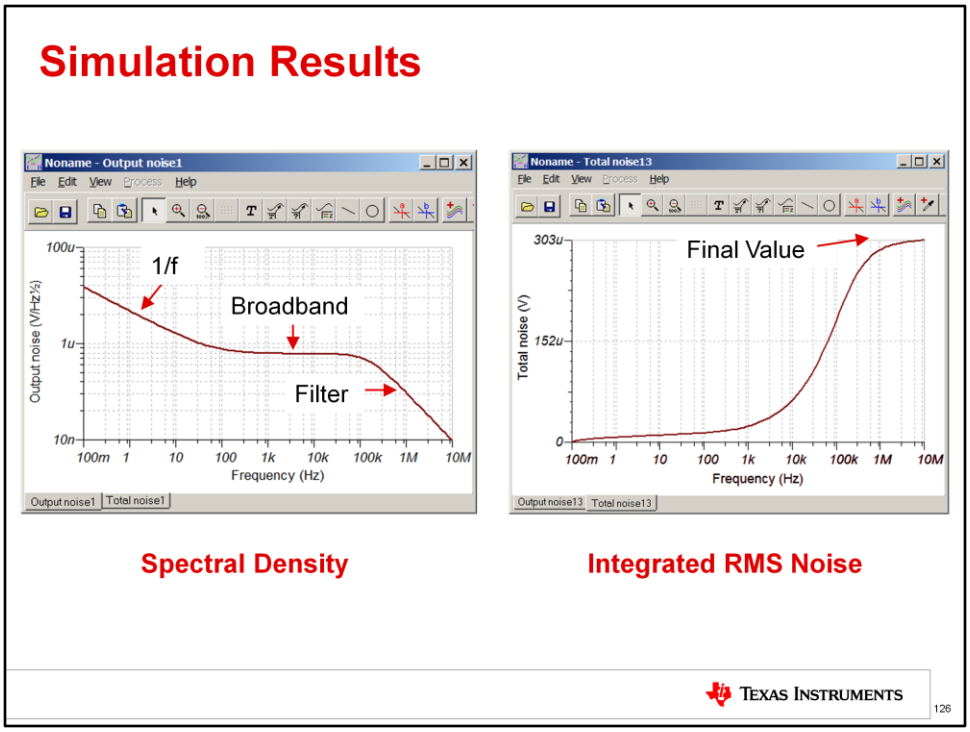
Another important thing to check before doing a simulation is if the op amp's SPICE model includes noise characteristics. If you double-click on Texas Instruments models in TINA-TI and click "Enter Macro," a net list viewer will open. The top of the net list on TI models includes a description of what is modeled. The key parameters to look for are **input voltage noise vs. frequency** and **input current noise vs. frequency**.

Other SPICE software packages will have similar net list viewers. It is important to be aware of the fact that not all SPICE models will model noise. In fact, this applies to other parameters as well. Always be aware of what your model covers, and always compare your simulated result to a hand calculation.



To run a noise analysis simulation in Tina SPICE, click “Analysis” in the menu bar, then click “Noise Analysis.” This brings up the “Noise Analysis” window. Enter the Start frequency and End frequency according to your application. In this example, we are analyzing the same circuit from the hand calculation in Noise 3. The bandwidth of this example circuit is 158kHz.

In general, it is good choose an end frequency that is one or two decades greater than the bandwidth of your circuit. This is done so that we can integrate the skirt of the low pass filter response. The start frequency is generally selected to be 0.1Hz, or 100mHz, so that the 1/f noise is included. The default number of points is 100. This is normally sufficient for most calculations, although you can add more points to improve accuracy. Select the “output noise” and “total noise” diagrams. **Output noise** is the noise spectral density measured at any meter or probe. If you have several meters placed on the simulation schematic, you will get one curve for each meter. The **Total noise** is the RMS noise integrated using the methods that were discussed previously. Let’s take a look at the results for this example.

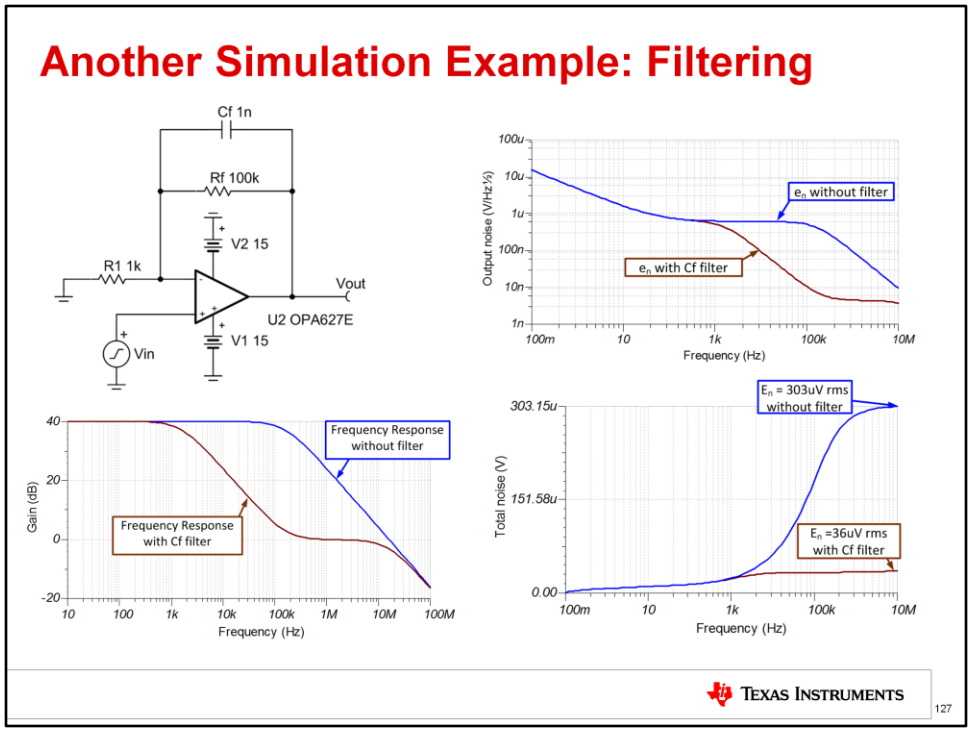


This slide shows the simulation results. The graph on the left is the spectral density plot, called "Output Noise" by TINA-TI. Note that the 1/f, broadband and filtered regions are clearly visible. The filtered region results purely from the op amp's inherent bandwidth limitations, since there is no filter on the circuit.

The graph on the right is the integrated RMS noise, called "Total Noise" by TINA-TI. This graph is calculated using the same equations introduced in the hand calculation section. That is, the voltage noise spectral density is squared, integrated across frequency, and the square root is taken on the result. The total noise plot shows the noise integrated up to a given frequency with a brick wall filter. For example, the noise integrated from 0.1Hz to 100kHz is about 152uV rms. Ultimately, the most important information that can be taken from this graph is the total noise across the circuit's entire bandwidth. For this example, the total noise across the entire bandwidth is about 303uV rms. Notice that the integrated noise converges to a final value. This occurs because the low pass filter response of the op amp limits the total noise. In general, you should look for the integrated noise curve to converge as in this example. If it does not converge you may have to increase the "End Frequency" in your simulation.

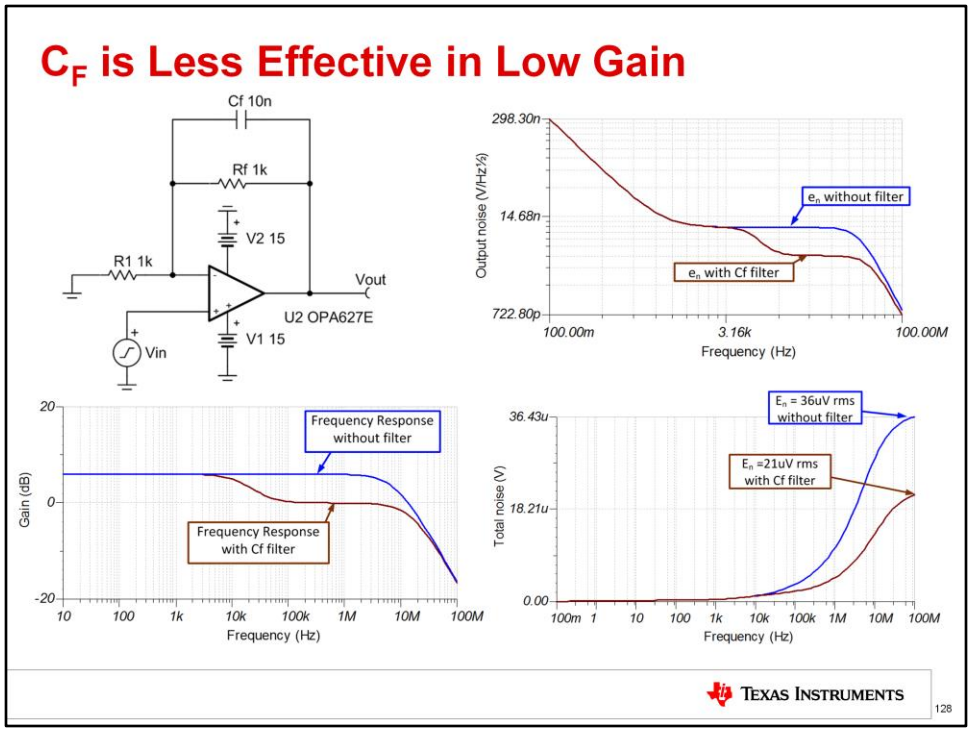
So, how does the simulation result compare with the hand calculations from earlier? The total noise from the hand calculation was 324uV rms and the simulation result is 303uV rms. This is very good agreement! In general, you **should** get good agreement

between calculation and simulation. However, there may be some differences from secondary effects in the model. If the difference between the model and hand calculation is greater than 20%, you should double check the simulation model and your hand calculations to find a discrepancy.



Now that we know how to do noise simulations let's try a few more examples. This example is the same circuit that we just simulated, except that a filter capacitor Cf of 1nF is added. This filter will decrease the impedance of the parallel combination of Rf and Cf at high frequencies. This causes the closed-loop gain to reduce with frequency, because the closed-loop gain is equal to the impedance of the feedback network divided by R1, +1. At some frequency the capacitor effectively becomes a short, which reduces the closed-loop gain to 1V/V or 0dB. The gain will remain at 0dB until the op amp's bandwidth limit causes the gain to further decrease further. Notice that this curve on the bottom left shows the effects with and without the filter. You can see that when the filter capacitor is acting like a short, the attenuation is about 40dB.

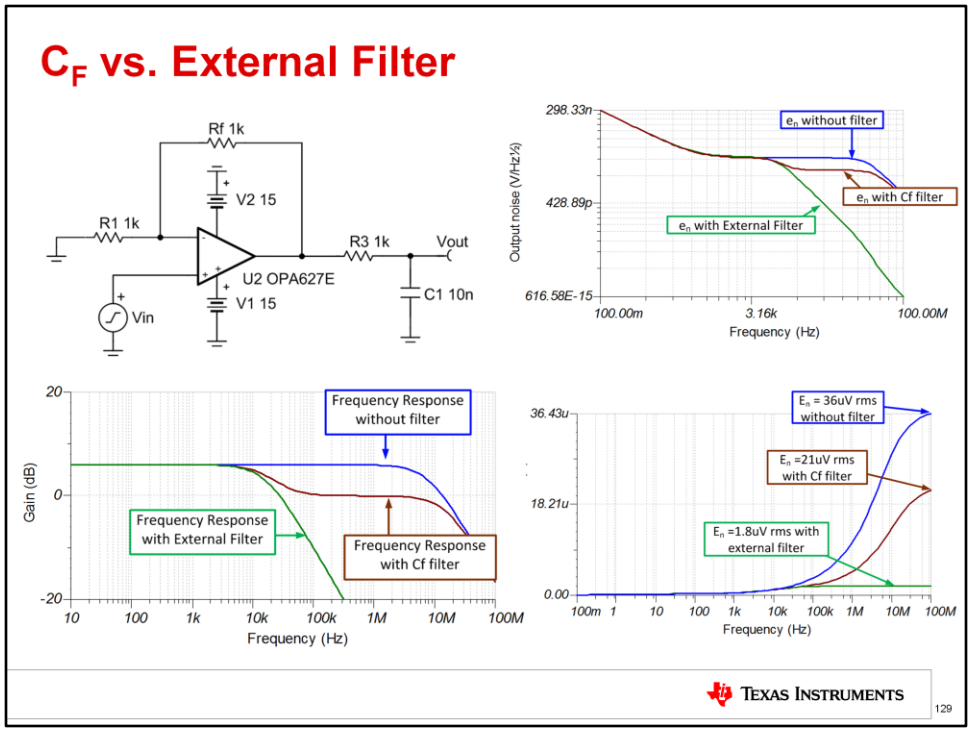
The output noise, or spectral density, curve, on the top right is simulated from the input noise spectral density multiplied by the circuit's gain vs. frequency. Thus, the filter attenuates the noise by about 40dB maximum. Finally, the integrated noise curve on the bottom right tells us that the total output noise is reduced from 303uV rms to about 36uV rms. The filter reduced noise by a factor of 8.5! As long as your application doesn't need the bandwidth, this is a very effective way to reduce noise. However, this method works best with amplifiers that have high gain. Let's consider an amplifier with lower gain.



In this example the closed-loop gain is 2V/V or 6dB. The filter behaves in the same way, except that the effective attenuation when the capacitor is acting like a short is only 6dB. In general, this type of filter will reduce the gain from the dc gain to a gain of 1V/V. Thus, this filter is most effective for circuits with high gain.

Looking at the spectral density curve on the top right, you can see the noise reduction from the filter occurs in the broadband region. Finally, the integrated noise curve on the bottom right with and without the filter shows that noise is reduced from 36 to 21uV. Noise is reduced by a factor of 1.7 for this circuit, but was reduced by a factor of 8.5 for the previous high- gain circuit!

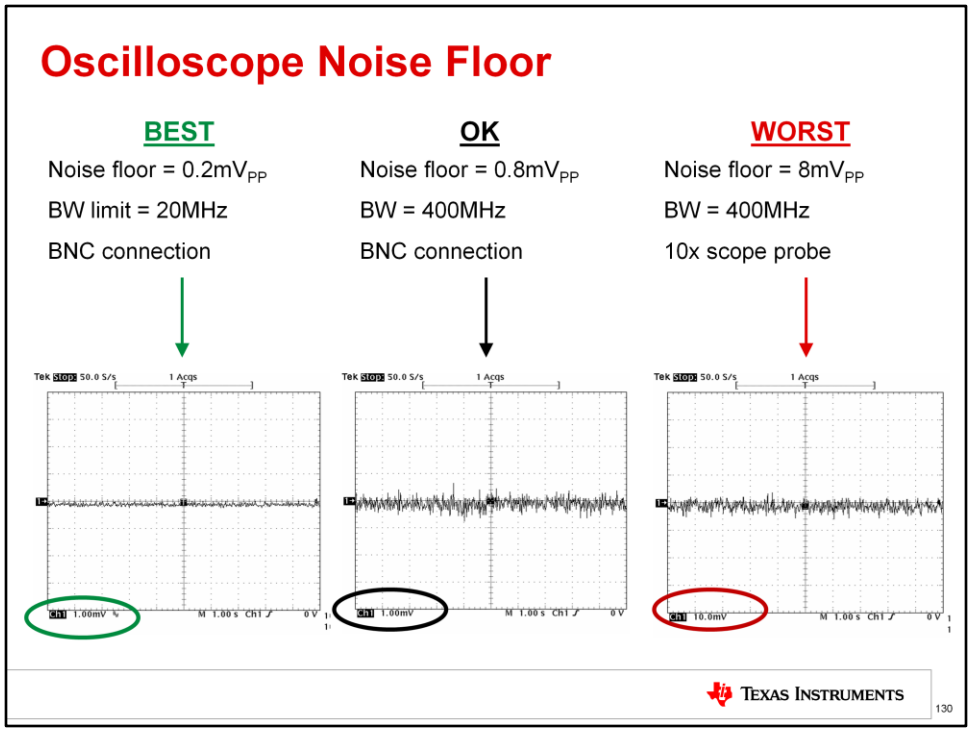
We can see from this example that the Cf filter is not as effective for low gain circuits. In this case, how do we properly filter noise from low gain circuits?



Using an external filter, which is a filter outside the op amp feedback loop, is the most effective way to reduce noise in circuits with low gain.

Looking at the gain vs. frequency curves on the bottom left, we see that the gain for the circuit with an external filter continuously rolls off, where as the gain for the circuit with the C_F filter reduces to 0dB and remains constant until the op amp roll-off region. The external filter provides significantly more attenuation than the Cf filter.

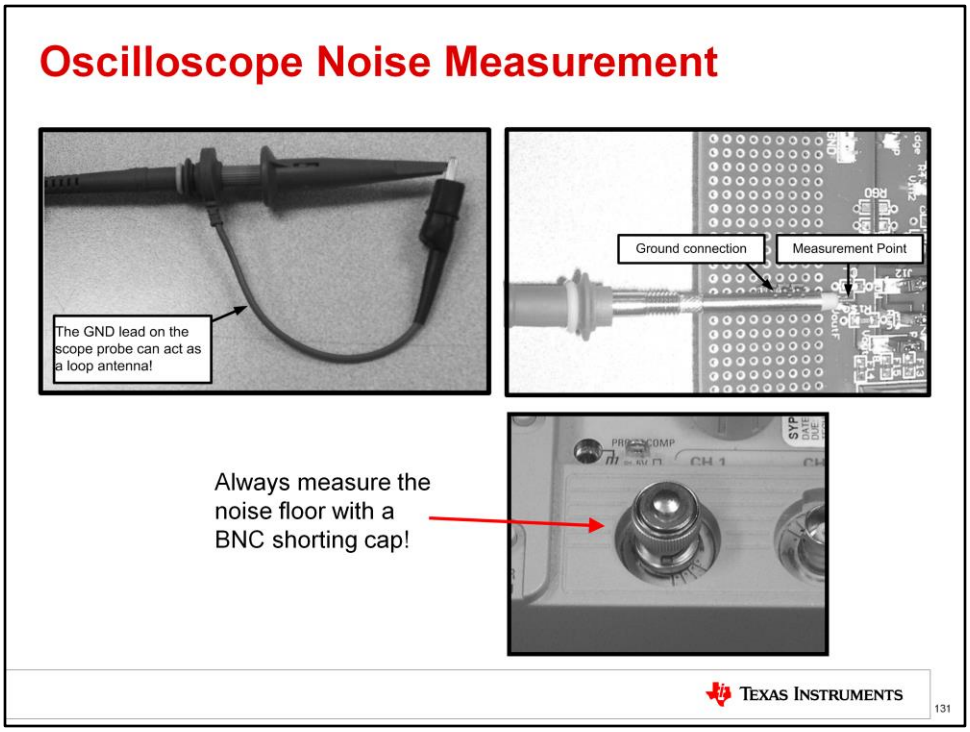
The benefit of the external filter is also clear when looking at the spectral density curve on the top right. Finally, the integrated noise curve on the bottom right compares the noise without the filter, with a Cf filter and with an external filter. The external filter reduces noise by a factor of 20! The only disadvantage to using the external filter is that the output impedance is now high as compared to the op amp output. This is ok if the next stage has a high input impedance; however, there will be significant errors for low impedance loads.



This slide shows a typical digitizing oscilloscope, measuring its noise floor in three different configurations. The worst configuration, shown on the right, has a noise floor of 8mVpp. In this case, a 10x scope probe is used and the scope bandwidth is set to the full 400MHz.

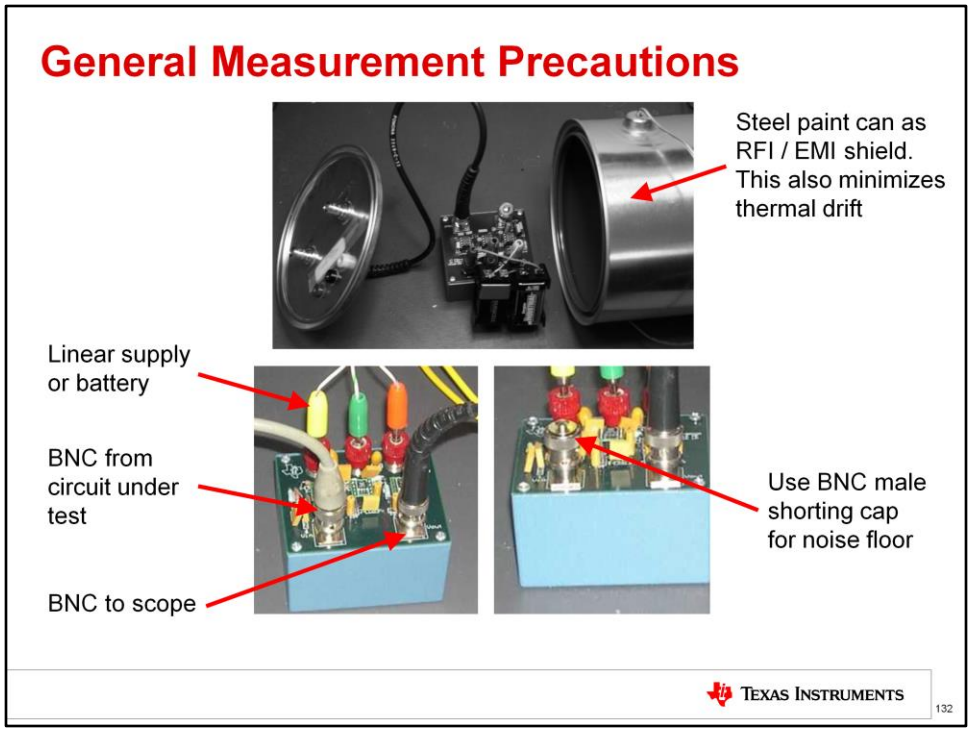
A significant improvement can be achieved by replacing the 10x scope probe with a direct BNC connection or 1x scope probe. Making this change effectively decreases the noise floor by a factor of 10, as shown in the center image. Notice that the vertical range changed from 10mV per division to 1mV per division.

The best noise floor occurs when a BNC connection is used along with the bandwidth limiting feature, as shown on the left. In this example, limiting the bandwidth to 20MHz reduces the noise from 0.8mV to 0.2mV or less.



This slide shows a few additional tips that can help improve the performance of your scope measurements. First, you should avoid using the scope probe's GND lead. It can act as a loop antenna and receive extrinsic noise, giving you errors in your measurements. If possible, remove the scope probe cap and use a direct GND connection (as shown on the top right). Note that the internal shaft on the scope probe is connected to ground. Also, it is important to always measure the noise floor of your scope. One way to do this is by using a shorting cap as shown in the figure on the bottom right. Another method is to short the end of your scope probe or measurement cable. However, as was mentioned previously, your cable or scope probe can act as an antenna. Using a shorting cap will tell you the noise floor of the scope without adding any noise pick-up on the cable. It may be useful to try both methods to determine if you are picking up noise on your cable.

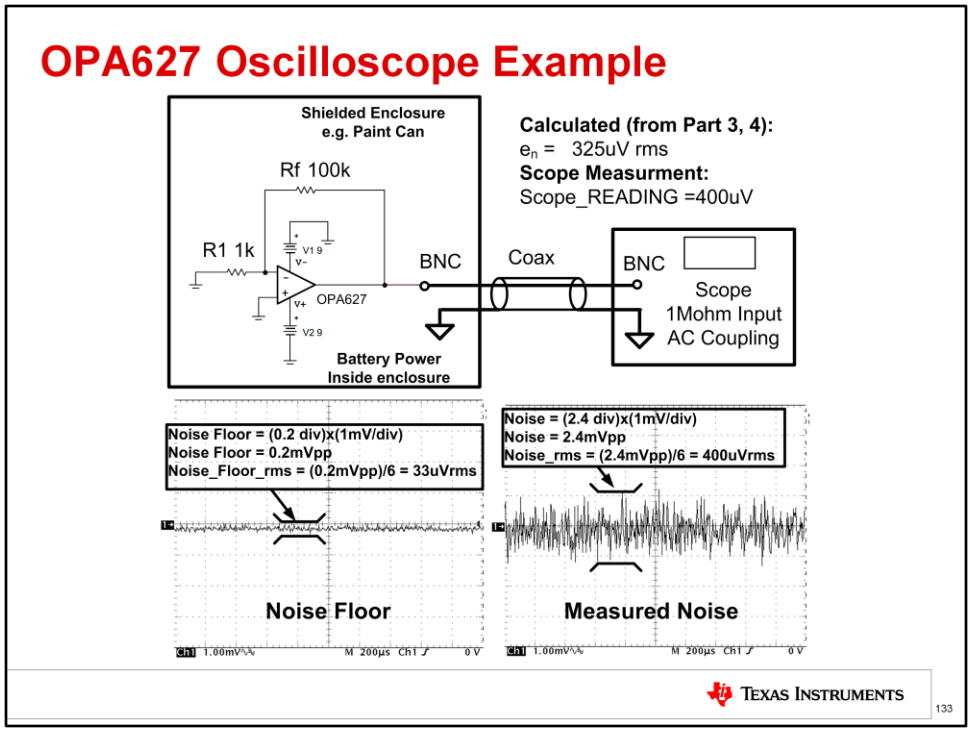
Once you have properly configured your oscilloscope, measuring noise is done by adjusting the time scale to match the bandwidth of your circuit. Later we will show an example measurement of the circuit that we did hand calculation and simulation for.



In addition to the proper configuration of oscilloscopes and spectrum analyzers, other aspects of your test setup can also have a huge impact on the quality of your noise measurement.

1. First, use a well shielded and grounded environment. Make sure that the shield is grounded, and any gaps in the shield are minimized. Copper and steel are good choices for shielding material. We often use a modified steel paint can as a shield for our noise circuits.
2. As mentioned before, if possible, make all circuit connections directly and with BNC cables.
3. Use batteries or linear power supplies in order to provide the lowest-noise power possible.
4. A BNC shorting cap is useful when measuring the noise floor. Don't leave un-terminated or floating inputs on your devices, as these will tend to pick up extrinsic noise.

Remember, the goal of this testing is to measure the intrinsic noise, so these precautions are focused on eliminating sources of extrinsic noise.

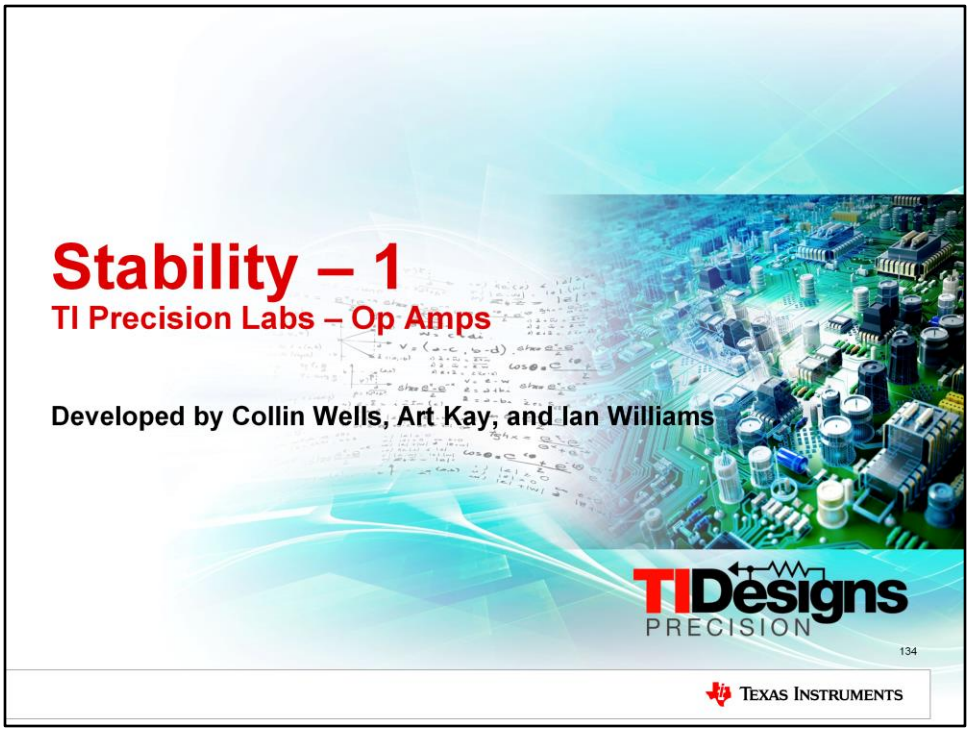


Let's now apply all of these real-world techniques to the OPA627 example circuit from our hand calculations and simulations. This circuit was connected directly to an oscilloscope with a BNC cable. As previously mentioned, the direct BNC connection is better than a 10x scope probe because the noise floor is ten times better.

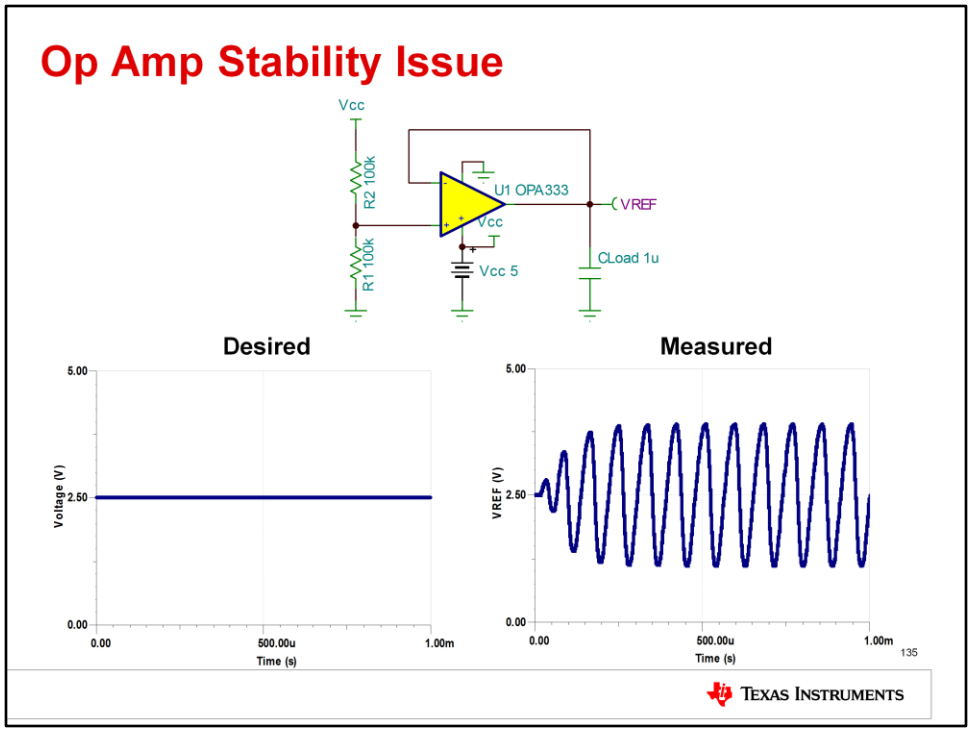
The measured output noise voltage was $400uV_{RMS}$ while the calculated result from earlier was $325uV_{RMS}$. There is some discrepancy in the measurement, which is typical for scope measurements. The discrepancy results from process variations in the device as well as measurement accuracy limitations of the test equipment. In general, the agreement between measured and calculated noise should be on the order of ±20%.

If the discrepancy is large, first confirm that the device is connected properly and is functional. Next, make sure that the equipment is configured properly. Always confirm that the system noise floor is low enough to allow for accurate results. Assuming that there are no functionality or equipment issues, the next thing to consider is extrinsic noise. Try improving the shielding environment. If you still see large discrepancies after thoroughly troubleshooting the circuit, you should try a noise measurement with a spectrum analyzer to get a deeper understanding of the system's noise characteristics. You may discover, for example, that switching noise at

a specific frequency is significantly affecting the noise.



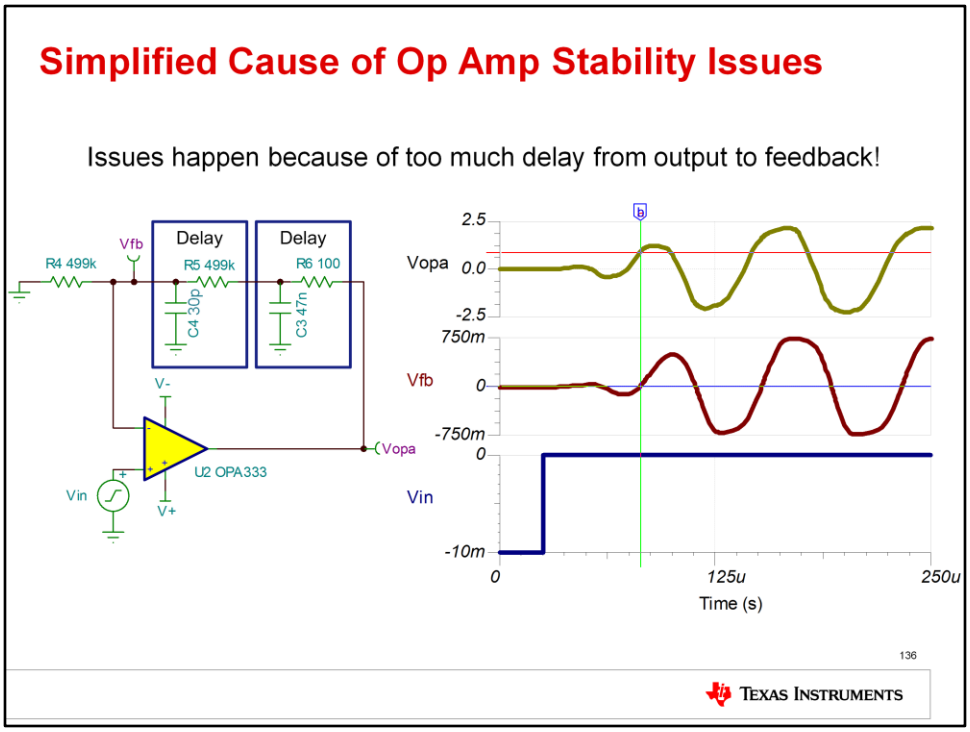
Hello, and welcome to part 1 of the TI Precision Labs lecture on op amp stability. In this lecture we will introduce the theory behind op amp stability and introduce the conditions for a circuit to be stable. We'll also show the common causes of op-amp stability issues, and how to identify these stability issues in the lab using standard test equipment.



Here is an example of what can happen if a circuit's stability is not verified before going to production. An op amp circuit that is unstable will have an unpredictable or unexpected output with poor transient performance. This typically results in large overshoots and ringing when changes occur on the input or load, but may also result in sustained oscillations. Often stability problems are caused by connecting a capacitor to the output or to the inverting input of the amplifier.

This op amp supply-splitter circuit was designed to deliver a constant 2.5 V dc output for the reference voltage in a system. However, the unstable design resulted in a sustained output oscillation, which has turned the DC reference voltage into a sine wave!

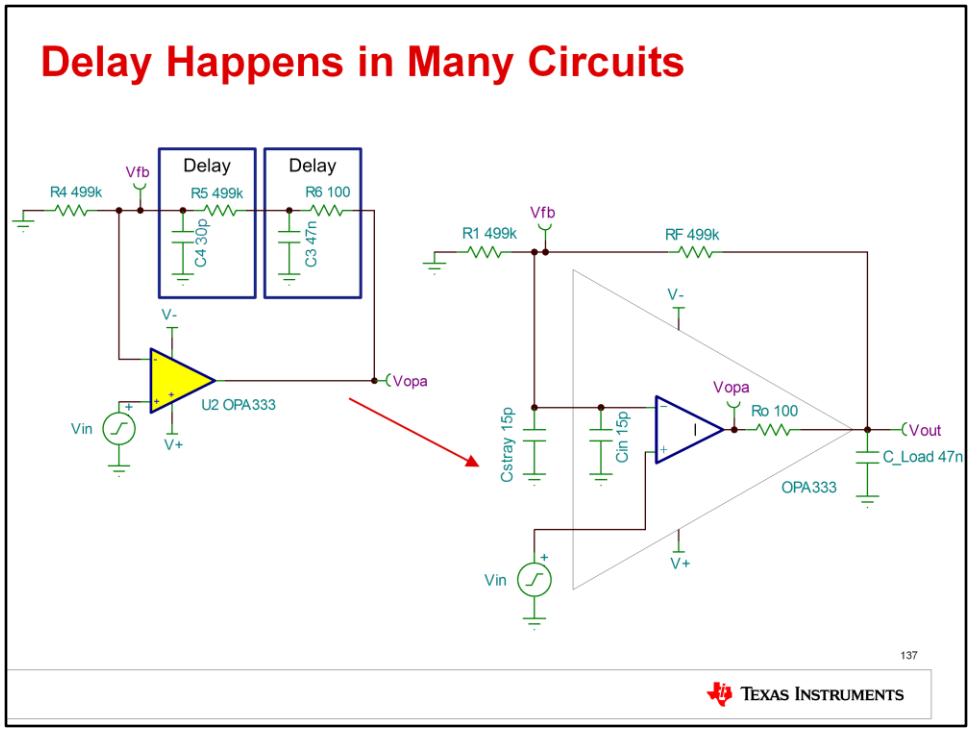
Even though this circuit is meant to operate with a dc input and output, transient disturbances on the input, power-supplies, or on the output may cause the amplifier to begin to oscillate. Therefore, we recommend checking every op amp circuit for stability regardless of the closed loop signal frequency of operation.



Too much delay between the amplifier output and the inverting feedback node is a straightforward way to visualize the root cause of op amp stability issues.

The effects of feedback delay are displayed in the example shown by observing the voltages at the amplifier output, Vopa, and inverting input, Vfb, when a step is applied to the input, Vin. When Vin changes, Vopa responds in an effort to set Vfb equal to Vin which will reestablish the “virtual short” between the inputs.

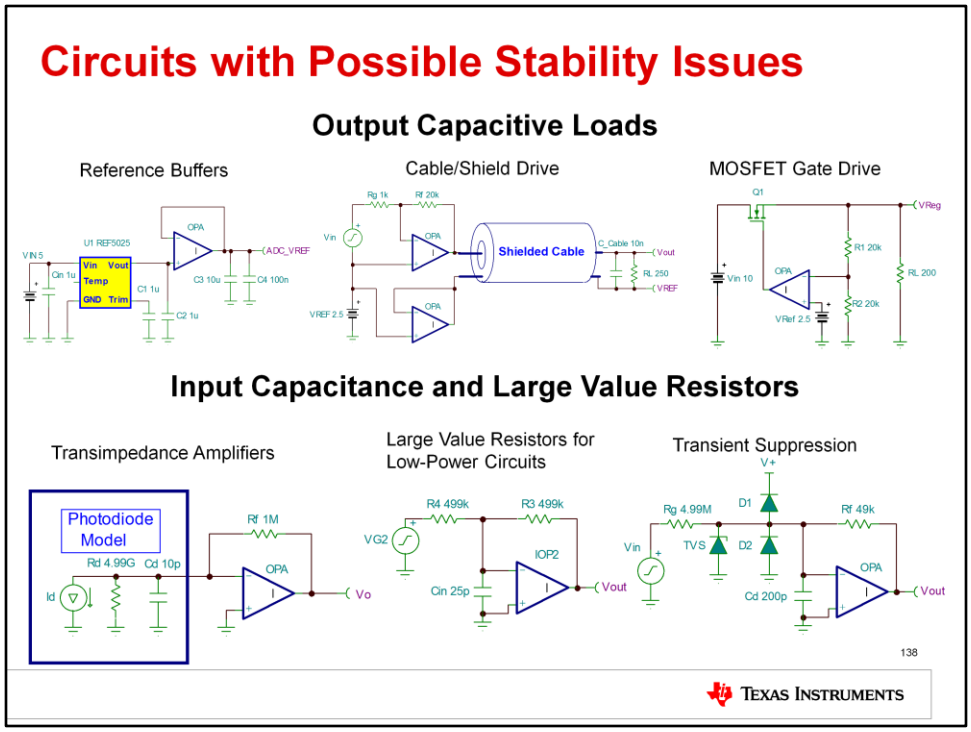
However, the feedback delay results in an erroneous voltage at Vopa by the time Vfb equals Vin. As a result Vfb continues to rise and overshoots the input voltage causing Vopa to reverse directions. Depending on the severity of the delay the output may settle, or may result in a sustained oscillation as shown here.



While the op amp circuit with the RC delay elements in the feedback path looks strange and unrealistic, many standard op amp circuits inadvertently create the same situation when external circuit components interact with non-ideal op-amp properties.

For example an op amp's open-loop output impedance, Ro, frequently interacts with the circuit load capacitance, Cload, to form a delay. Another delay is commonly formed when the feedback resistance, RF, interacts with the parallel combination of the op amp input capacitance, Cin, and any stray PCB capacitance.

The delay caused by either of these situations can result in stability issues if not properly taken into consideration..



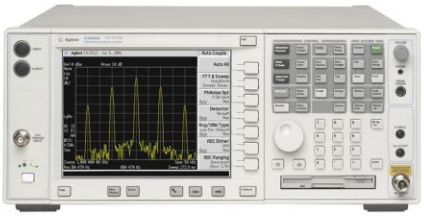
So, without further ado, here are the most common circuits and applications involved in op amp circuit stability issues. These circuits all create unwanted delay from the output to the feedback node and can be divided into two distinct groups based on the issue they cause in the op amp control loop.

The first, and most common group of circuits are those that disturb the open-loop gain of the amplifier circuit by presenting a capacitive load, either directly or due to parasitic elements, on the output of the amplifier. Examples of these circuits include voltage reference buffers, cable/shield drive circuits, and MOSFET drive circuits.

The second group of circuits disturb the feedback network of the amplifier circuit due to interaction between the input capacitance and large valued feedback resistors used in the circuit. Common examples of these circuits include transimpedance amplifiers, circuits designed for low-power operation, and circuits that feature transient suppression elements on the inverting input.

Identify Stability Issues in the Lab

- Suggested Tools:
  - Oscilloscope
  - Signal Generator
- Other Useful Tools:
  - Gain / Phase Analyzer
  - Network / Spectrum Analyzer



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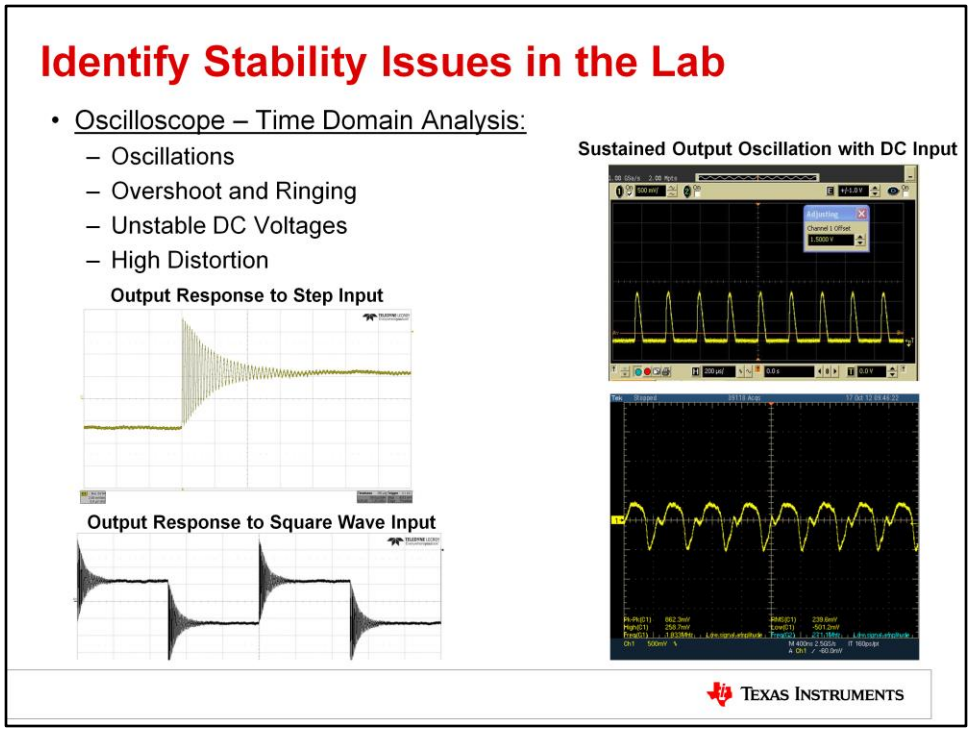
Although solving op amp stability issues takes practice and experience, identifying them in the lab is generally straightforward.

An input step signal generator and an oscilloscope are all that is required. The input step could come from a DAC that's already in the system or from an external function generator. If they are available, gain/phase analyzers and network/spectrum analyzers can also be used to help identify stability issues.



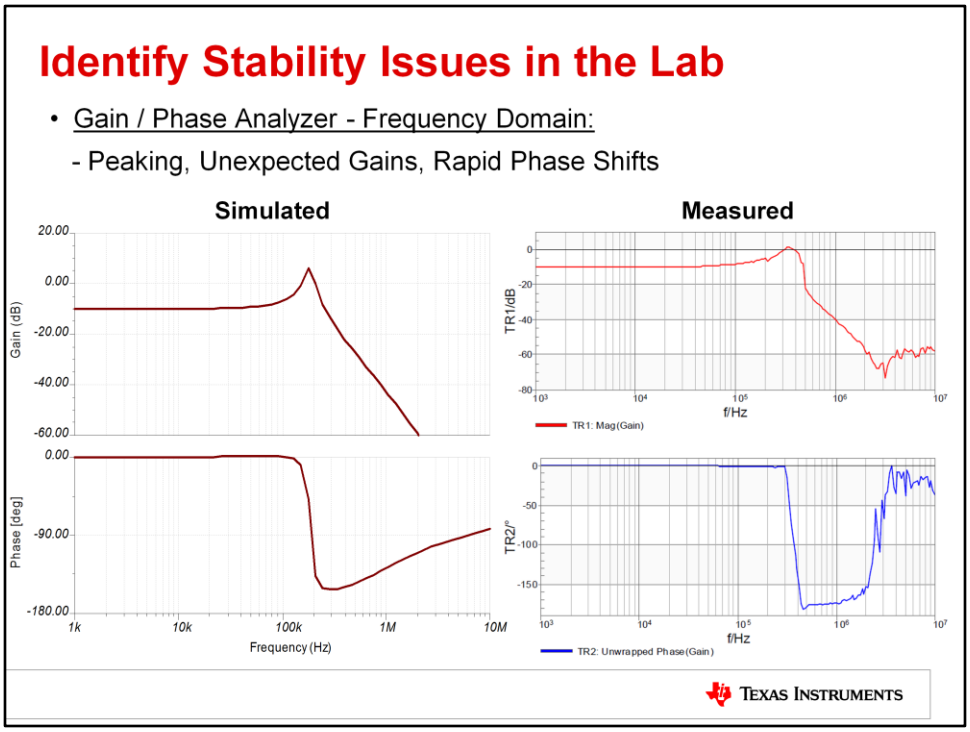
Here are some images of output signals from unstable circuits taken with common lab oscilloscopes.

A circuit with a dc output may look stable when first observed on an oscilloscope until the loop is disturbed when a small-signal step or square wave is applied to the input. An unstable circuit's output will overshoot the input signal and will then ring back and forth until the output settles out.

The magnitude of the overshoot and the duration of the ringing directly relate to the severity of the of stability issue. Circuits with minor stability issues may feature modest overshoots with minimal ringing. More severe stability issues will result in overshoots equal to or greater than the input signal with significant ringing as shown in these examples.

The most severe stability issues can result in sustained output oscillations without having to apply a signal to the input to disturb the loop. These circuits can produce a wide variety of strange looking output signals which may not always be pure sine-waves as possibly expected.

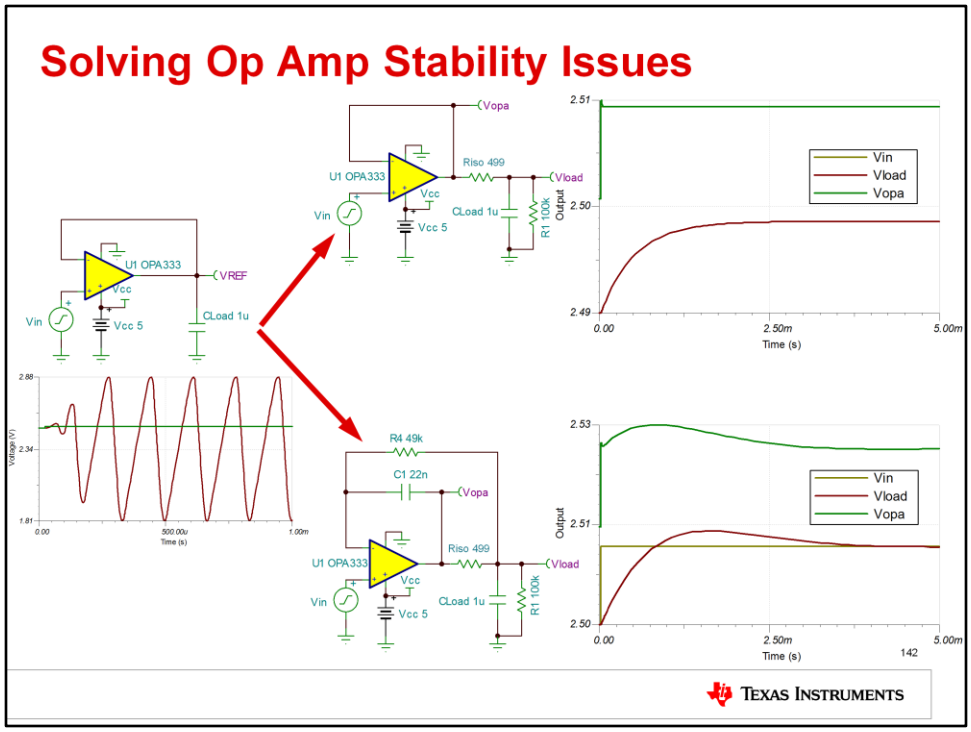
Although not featured here, unstable dc outputs and higher than expected distortion readings can be more subtle signs of a stability issue.



In addition to oscilloscopes, gain/phase analyzers can be used to measure the frequency response of a circuit which can also be used to identify stability issues. These results compare a circuit's simulated gain/phase response versus the measured response.

Gain peaking, rapid phase shifts in the frequency domain, or unexpected gains are all indicators of circuit stability issues.

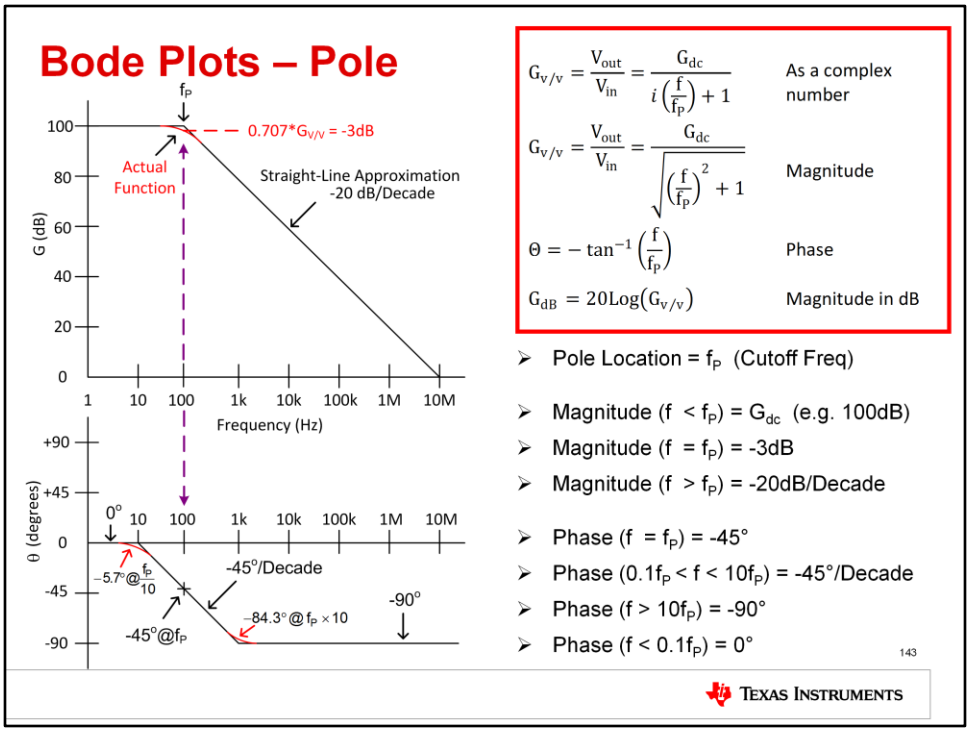
When trying to measure the gain and phase of an unstable circuit it is common for the measured response to appear jagged or not clean and may be difficult to measure over the full frequency range. Watch for those more subtle signs of stability as well.



Once a stability issue is identified, the next step is to solve it! There are several methods available, and the best method to use depends on the final application.

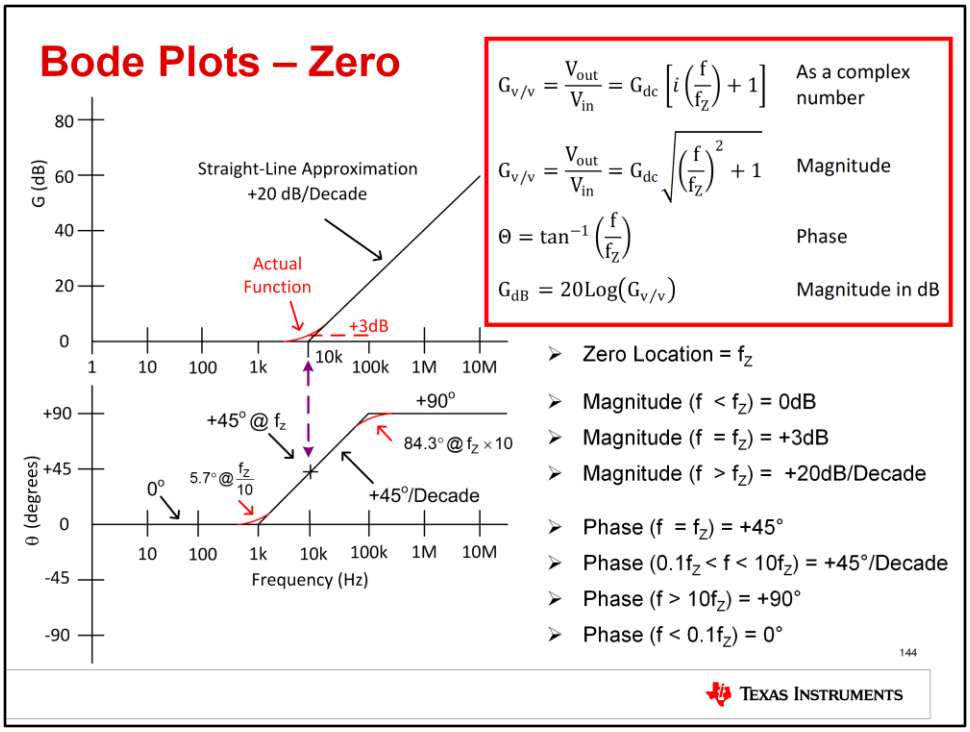
In this lecture, we'll introduce two of the more common techniques. The first technique uses an isolation resistor, Riso, to compensate the circuit at the expense of DC accuracy due to the voltage drop across Riso.
The second technique pulls Riso back into the feedback loop, allowing the op amp to eliminate the voltage drop across Riso at the expense of settling time.

We'll explore the different methods to stabilize circuits after we review the necessary theory to understand, simulate, and compensate a feedback network.



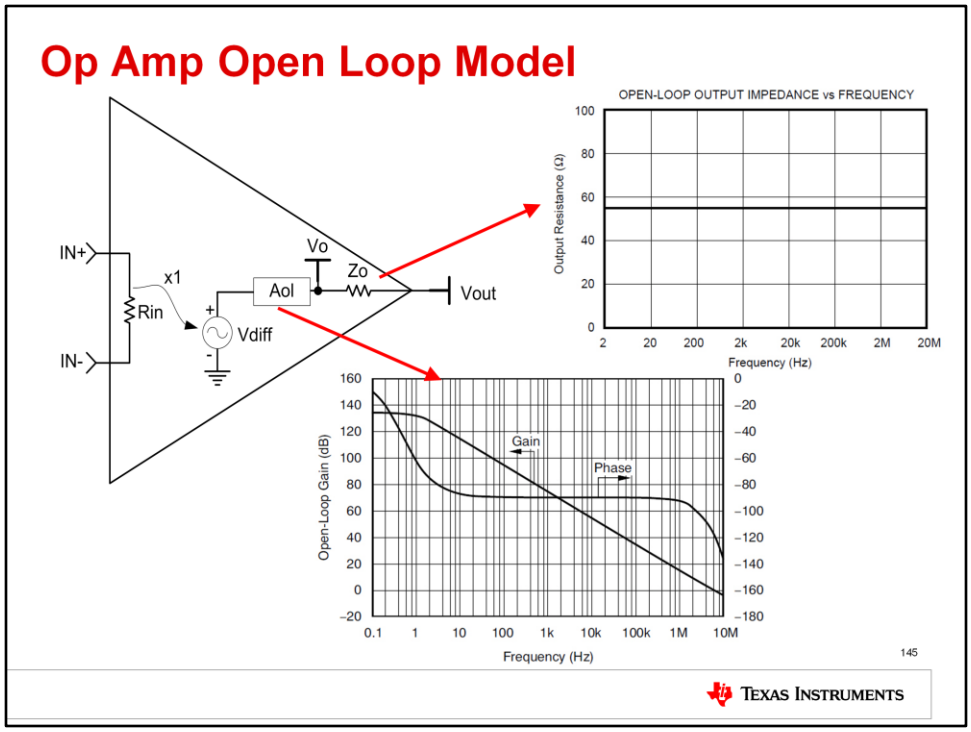
This slide is a review from the lecture on op amp bandwidth. It illustrates the equations for a pole and its associated magnitude and phase response on Bode plots. A pole causes a negative 20 dB/decade decrease in the slope of the magnitude response after the pole frequency, fp. The pole also causes a negative 90 degree phase shift in the phase response beginning roughly a decade before fp and ending roughly a decade afterwards.

At fp the magnitude response will have decreased by negative 3 dB, and the phase will have shifted by negative 45 degrees. While the pole results in a total phase shift of 90 degrees over about 2.5 decades, the phase shift is equal to negative 5.7 degrees a decade before fp and negative 84.3 degrees a decade after fp.



This slide, also from the op-amp bandwidth lecture, illustrates the equations for a zero and its associated magnitude and phase response on Bode plots. A zero causes a positive 20dB/decade increase in the slope of the magnitude response after the zero frequency, fz. The zero also causes a positive 90 degree phase shift in the phase response beginning roughly a decade before fz and ending roughly a decade afterwards.

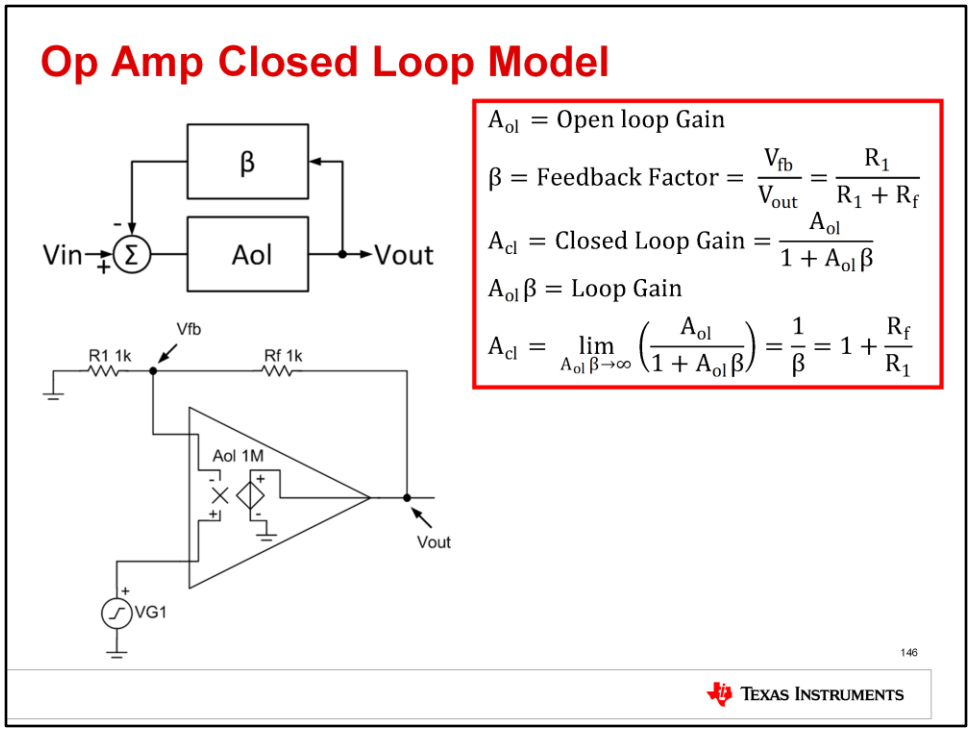
At fz the magnitude response has increased by plus 3 dB and the phase has shifted by positive 45 degrees. While the zero results in a total phase shift of positive 90 degrees over about 2.5 decades, the phase shift is equal to positive 5.7 degrees a decade before fz and positive 84.3 degrees a decade after fz.



It is helpful to use an intuitive model for the op amp when performing ac stability analysis because of the complexity of modern op amps. In this simplified "stability" model, the differential input voltage applied to the inputs is passed to the amplifier output stage where it passes through the amplifier open-loop gain, followed by the open-loop output impedance before it reaches the output terminal.

The open-loop gain, or Aol, of an op amp represents the maximum gain that can be applied over frequency to the differential voltage applied between the inputs of the device. Aol for an ideal amplifier is infinite and is not limited by frequency. Modern op amps can have open loop gains in excess of 1 million volts per volt, or 120dB at low frequencies and unity-gain bandwidths from 10's of kHz up to several GHz.

The open-loop output impedance, Zo, is a measure of the impedance of the open-loop output stage of the op amp. Zo should not be confused with the amplifier's closed-loop output impedance, Zout, which depends on Zo, Aol, and the circuit configuration. To keep the stability analysis focused on the basic concepts for this series, the behavior of the Zo will be viewed as a resistor over all frequencies of interest. In truth Zo canl vary widely over frequency for newer rail-to-rail output stages making stability analysis more difficult. Complex output impedance will be discussed in the advanced section at the end of this series after a firm understanding of analysis with resistive output impedance has been developed.



To control the large open-loop gain of modern amplifiers, negative feedback is required between the output of the amplifier and the inverting input. This is referred to as "closing the loop." In this circuit, the loop is closed with Rf and R1 which create a voltage divider, and therefore an attenuation, between the output and the inverting input. The ratio of the resistors determines the amount of the output that is fed back to the input which is defined as the feedback factor, or Beta, of the circuit.

Closing the loop results in a closed-loop gain, Acl, that is equal to Aol divided by 1 plus Aol multiplied by Beta. Aol multiplied by Beta is referred to as Loop-gain. When the loop-gain is large, the closed-loop gain formula can be simplified to equal 1/Beta. In this example 1/Beta equals 1+Rf/R1, which can be recognized as the gain of a non-inverting amplifier circuit.

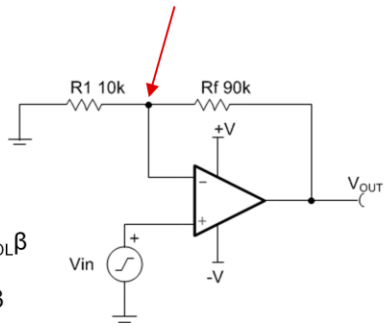
Closed-loop gain through negative feedback is a fundamental concept in amplifier circuit design and should be thoroughly understood. Let's review it again quickly. The amplifier will adjust it's output to equalize the two inputs establishing the virtual short between them. Therefore an attenuation from the output to the input, set by Beta, forces the output to be larger than the input by the inverse of Beta. This is how the ratio of the feedback resistors sets the closed-loop gain of the circuit. .

When is an Amplifier Unstable?

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180^0 relative to Vin



Phase Margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

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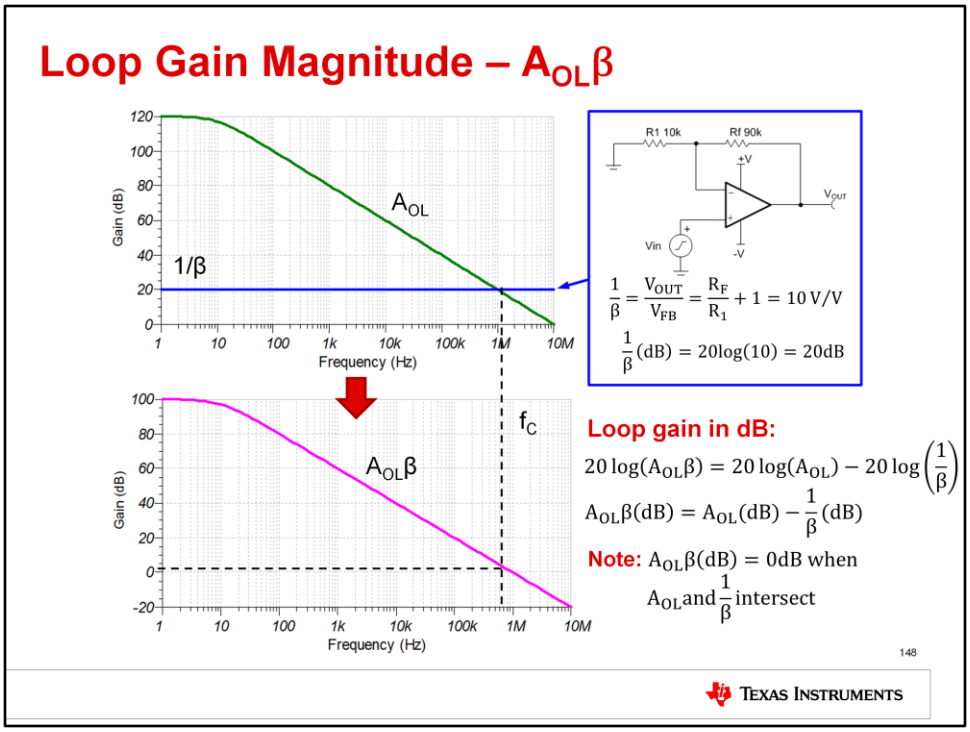
First, we must define when an amplifier is unstable. Looking back at the op amp closed-loop gain equation, we remember that Acl = Aol / 1+ AolB. Taking a closer look, we can see that if AolB, or the loop gain, equals -1, we get zero in the denominator and therefore Acl becomes undefined. This is the mathematical definition of instability. How can this happen in a real circuit?

Well, at some point in frequency AolB will equal 0dB, which is equal to 1V/V. If enough delay is introduced into the feedback path, the phase in the feedback network will shift 180 degrees relative to Vin. A 180 degree phase shift is equivalent to an inversion of the input, or -1. Therefore, when the gain of AolB = 0dB and the phase has shifted by 180 degrees, the result is AolB = -1.

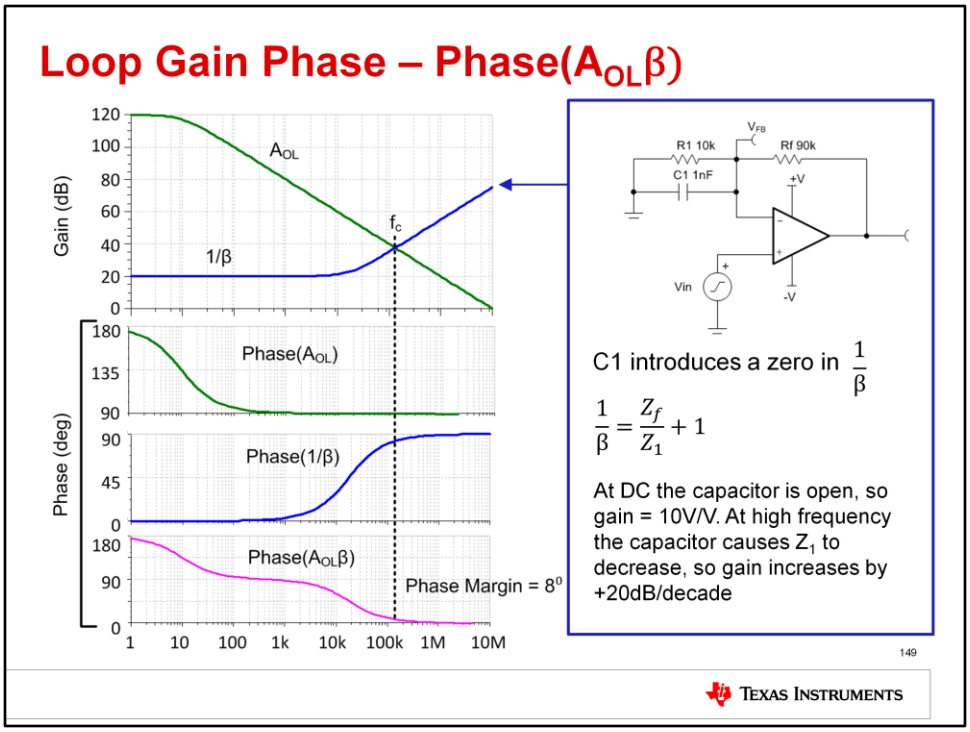
The term “Phase Margin” is used to define how close a circuit is to this condition. Phase margin is simply the phase of AolB at the frequency where AolB = 0dB. For example, 10 degrees of phase margin means that AolB has shifted by 170 degrees at the point where AolB = 0dB.

As you can see, loop gain or AolB is a key component of stability analysis. How can we observe loop gain?



Well, first we can consider the loop gain magnitude using a Bode plot. Using the same circuit as before, we have a gain of 10V/V, or 20dB, so 1/B is a constant 20dB over frequency. The circuit's Aol is also shown. To find the magnitude of AolB, we can simply subtract 1/B from Aol. This might not seem intuitive, but the mathematical relationship shown on the right side of the slide proves this using the properties of logarithms.

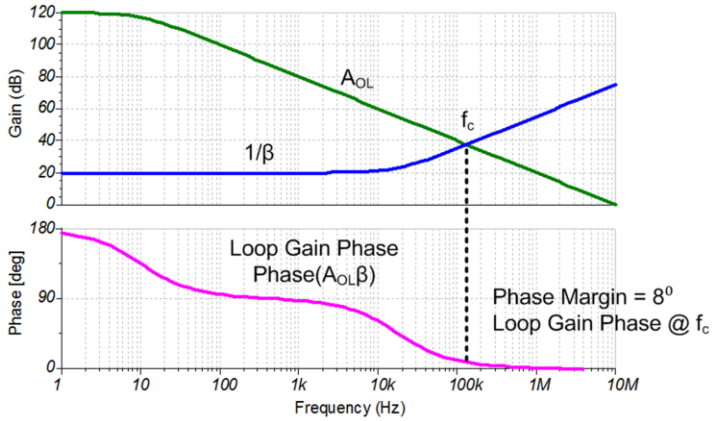
Remember in the last slide we stated that the phase margin is the loop gain phase at the frequency where AolB = 0. This frequency is called fc. This is also the frequency where Aol and 1/B intersect, which makes sense since the difference of two equal values is always zero.



To measure the phase margin, we need to know the loop gain phase, or phase of AolB, over frequency. Using the same log properties as before, we can simply subtract the phase of 1/B from the phase of Aol to get the phase of AolB.

In this example, a capacitor was added to the feedback network of the op amp circuit. At DC the capacitor is open, so the gain is the same as before at 10V/V. At some higher frequency, the capacitor causes the impedance of the combination of R1 and C1 to decrease, so the gain of the circuit increases by +20dB/decade. This can be seen from the zero in the 1/B plot. Looking at the phase, the 90° increase in the phase of 1/B creates a 90° decrease in the phase of AolB, so phase margin becomes very low at only 8°.

Phase Margin



Rule of thumb:
Phase margin > 45° is required for optimal stability!

Phase margin < 45° is considered "marginally stable."
This does not ensure a robust design over process variation.

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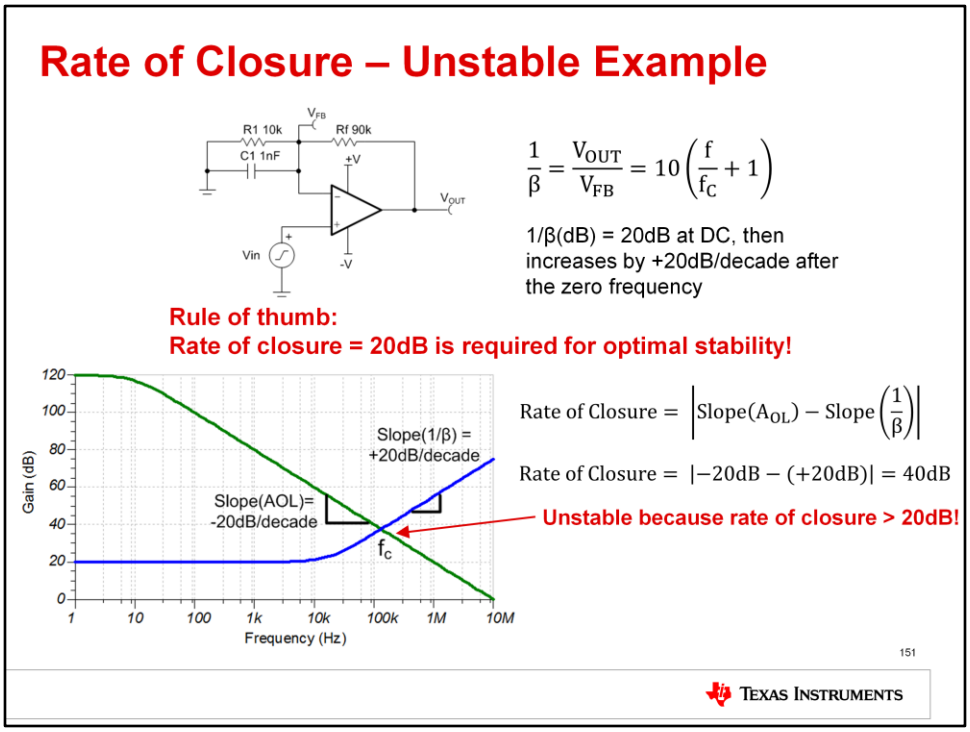
Now that we know how to observe phase margin, let's review what it's actually telling us. Remember that what we want is to avoid the condition where the loop gain, AolB, equals -1. That means we have a phase shift of 180 degrees at fc, or 0 degrees of phase margin. For optimal stability, we use a rule of thumb which states that a phase margin of 45 degrees or higher is required. While a circuit may work with phase margin less than 45 degrees, it is considered to be only marginally stable and will still show overshoot and ringing. Also keep in mind that different devices will have different characteristics due to process variation, temperature, component value tolerances, and other fluctuations, so for a robust design you should really meet the 45 degrees of phase margin minimum requirement.

That being said, phase margin isn't the only way to analyze stability. Another method exists which is simpler, and can actually give more information about what causes the stability problem in a circuit.



This method is called rate of closure analysis. To use this method, we only need to consider the gain plots of Aol and 1/B. These plots have well-defined slopes due to the poles and zeros in their transfer functions. By analyzing the rate of closure of Aol and 1/B at fC, the point where they intersect, we can quickly determine the stability of a circuit. The rule of thumb for this method is that the rate of closure at fc must equal 20dB for optimal stability.

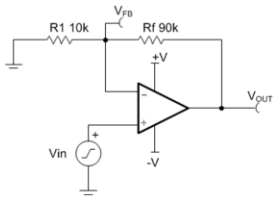
Let's use our same circuit example from earlier with a capacitor on the op amp negative input. That capacitor causes a zero in 1/B, which makes 1/B increase with a slope of 20dB/decade. The Aol curve of the op amp is decreasing at 20dB/decade due to the op amp's dominant pole. When they intersect at fc, the rate of closure is the absolute value of the slope of Aol minus the slope of 1/B, which works out to be 40dB. Since the rate of closure is greater than 20dB, we can conclude that the circuit is unstable.

Besides being quick and easy to check, the rate of closure method has another benefit of showing us what in the circuit is contributing to instability. In this example, the slope of Aol is normal, and we see only the effect of the op amp dominant pole. However, the rise in 1/B indicates a zero in the feedback network, so we can then take steps to compensate for it. Phase margin alone does not give us this information.

The rate of closure method works because the slopes of Aol and 1/B are linked to the

poles and zeroes in the circuit. A 20dB rate of closure means a circuit is only under the net influence of 1 pole, which means the phase margin is at least 45 degrees, enough for optimal stability.

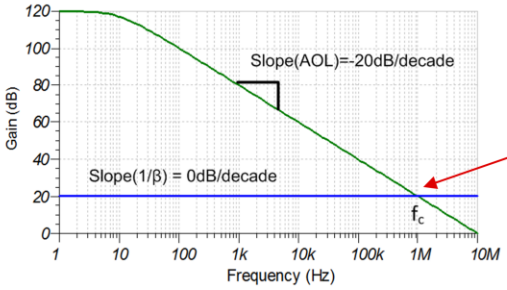
Rate of Closure – Stable Example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Rule of thumb:
Rate of closure = 20dB is required for optimal stability!



$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB!

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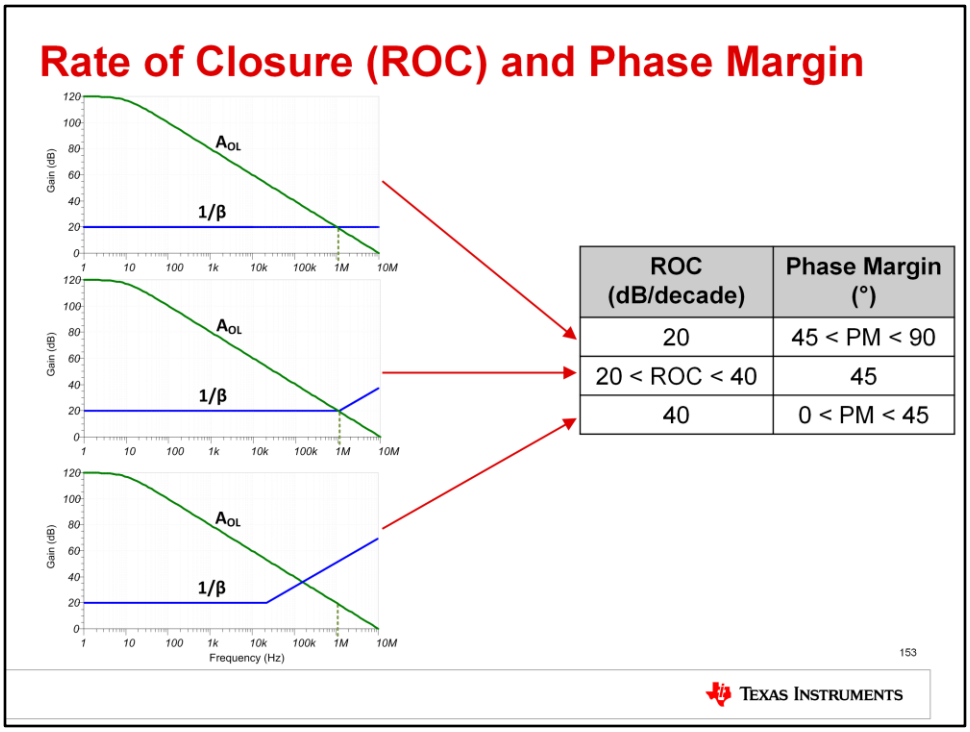
TEXAS INSTRUMENTS

We can also analyze this circuit from earlier in the lecture using the rate of closure method. In this case, there is no capacitor in the feedback network, so there is no zero and therefore no increase in 1/B. Aol is still decreasing with a slope of -20dB/decade as before. The rate of closure is now the absolute value of -20dB – 0dB, or 20dB. We can conclude that this circuit is stable.

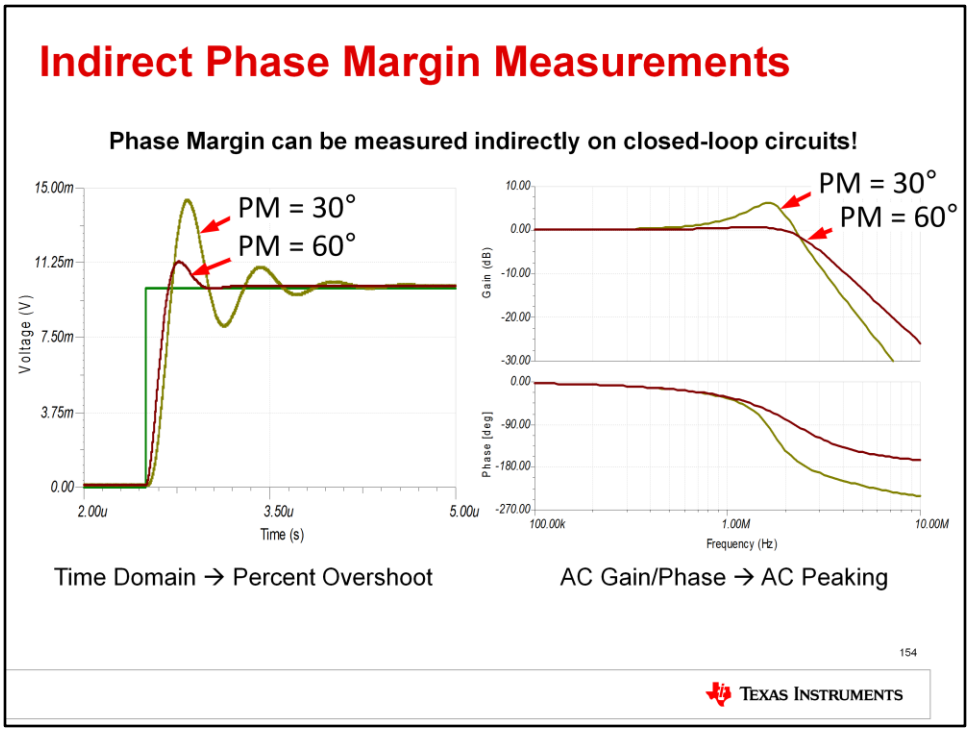


As shown in the previous slides, rate of closure and phase margin are closely connected. We can predict one value based on the other, and this slide gives three different examples of rate of closure and their corresponding phase margins.

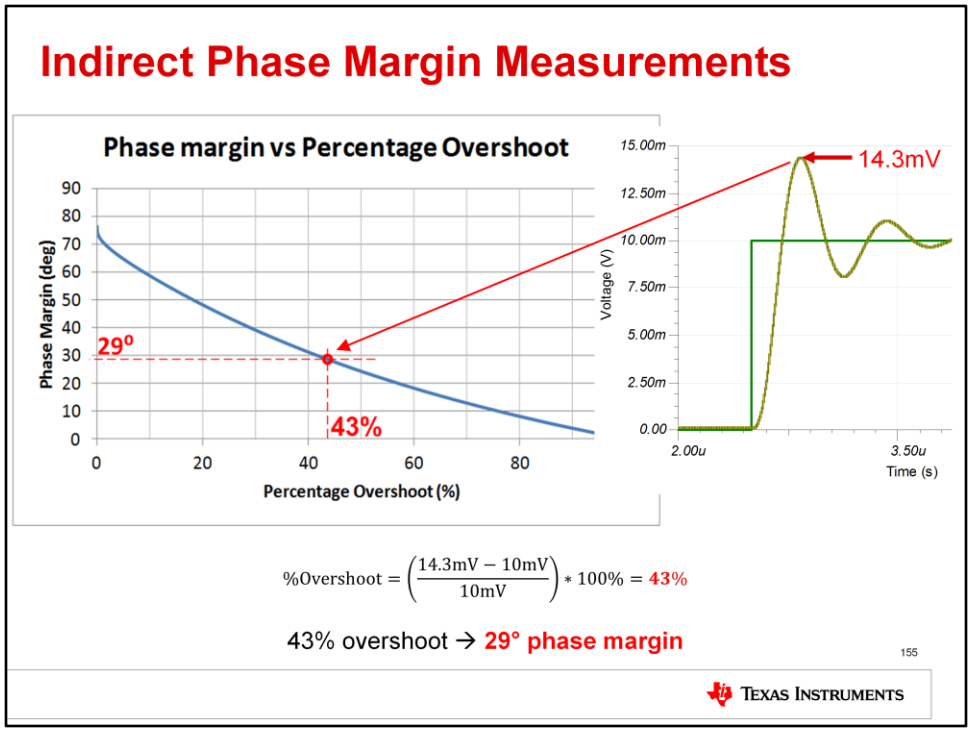
In the first case, we have a rate of closure of 20dB/decade, so the circuit is stable and we have between 45 and 90 degrees of phase margin. This is the best case.

In the second case, we have a zero in 1/B right at fc, so the rate of closure is beginning to change. At fc the rate of closure is somewhere between 20 and 40dB per decade, which corresponds to about 45 degrees of phase margin. Remember that a zero causes a total phase shift of 90 degrees, but 45 degrees of phase shift right at the zero frequency, so we get a total of 90 degrees of phase shift from the Aol dominant pole and 45 degrees of phase shift from the zero at fc. This leaves 45 degrees of phase margin.

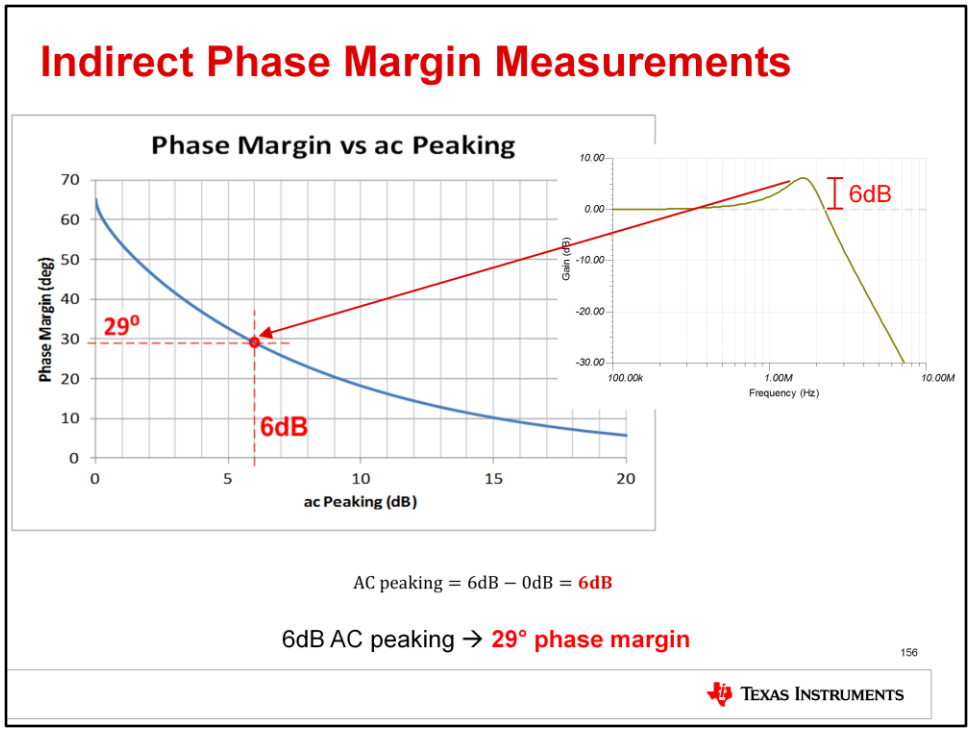
In the final case, we have a zero in 1/B well before fc, so the rate of closure is exactly 40dB/decade. This results in between zero and 45 degrees of phase margin.



Phase Margin can also be indirectly measured on closed-loop circuits in the time domain and in ac gain/phase measurements. In the time domain, we can observe phase margin based on the overshoot of an op amp's output relative to a small-signal step input. In the frequency domain, we can observe phase margin based on the maximum AC peaking in the circuit's transfer function compared to the DC gain.



In the time domain the percent overshoot to a step input can be used to indirectly calculate the phase margin. In this example, a 10mV step was applied. The output overshoot reached 14.3mV, or 4.3mV above the intended output. This corresponds to a percent overshoot of 43%. Using the phase margin vs. percentage overshoot plot, we can see that 43% of overshoot results in only 29 degrees of phase margin.



In AC Gain/Phase plots, the amount of ac peaking relative to the DC gain can be used to indirectly measure the phase margin of a circuit. In this example, the AC transfer function is peaking at 6dB, while the DC gain is 0dB. A total peaking of 6dB again results in 29 degrees of phase margin.

Multiple-Choice Quiz

- What are some possible signs of an unstable op amp circuit?
  a) oscillations
  b) large overshoot and ringing
  c) unpredictable or unexpected response
  d) all of the above

- Many common circuits inadvertently cause delay in the feedback network, resulting in stability issues.
  a) true
  b) false

Multiple-Choice Quiz

- Which of these is **not** a cause of amplifier instability?
  a) capacitance on the amplifier's output to GND
  b) capacitance on the amplifier's inverting input
  c) large value feedback resistors
  d) low valued resistors on the amplifier's output to GND

- Which common application is most likely to have a stability issue?
  a) photodiode transimpedance amplifier
  b) low-noise gain stage
  c) summing amplifier
  d) integrator

Multiple-Choice Quiz

- Amplifiers with stability problems are _____?
  a) only sensitive to transients on the input
  b) sensitive to transients on the input, output, and power supplies

- Amplifiers with DC inputs (eg. reference buffer) will **not** have stability issues.
  a) true
  b) false

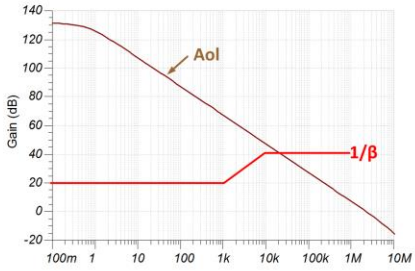
Multiple-Choice Quiz

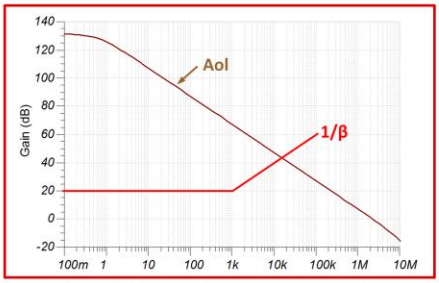
- Which of the following is a common method for stability testing?
  a) apply a sinusoidal input signal, monitor the amplifier output with an oscilloscope
  b) apply a square wave input signal, monitor the amplifier output with an oscilloscope
  c) apply a triangle wave input signal, monitor the amplifier output with an oscilloscope

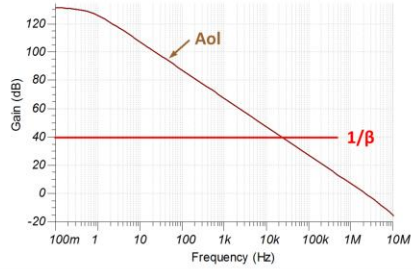
- Which of these is **not** a sign of stability issues in closed loop gain/phase analyzer measurements?
  a) steep magnitude roll-offs
  b) rapid phase shifts
  c) unexpected gains
  d) AC gain peaking

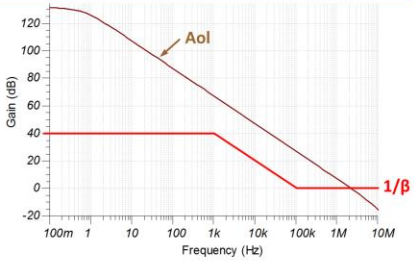
Quiz

- Which **one** of these A_{OL} and 1/β curves is **un**stable?









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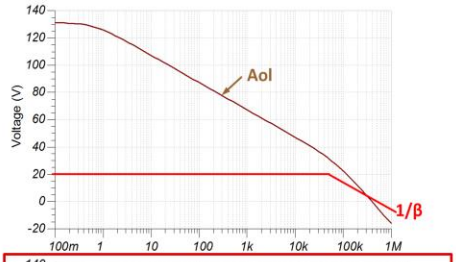
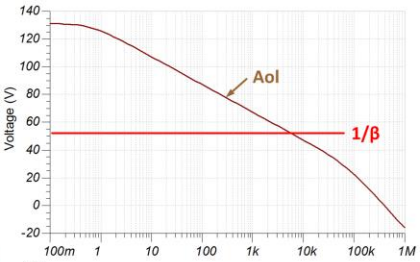
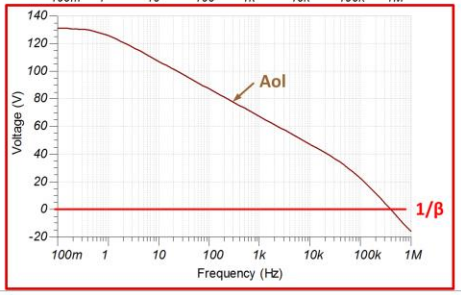
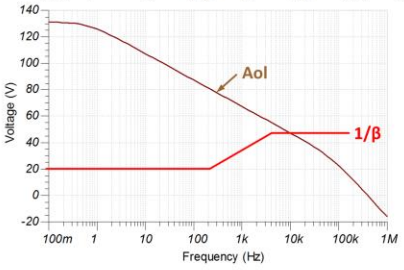
Quiz

- Which **one** of these A_{OL} and 1/β curves is **un**stable?









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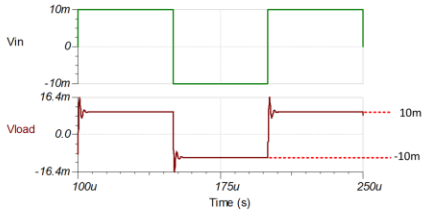
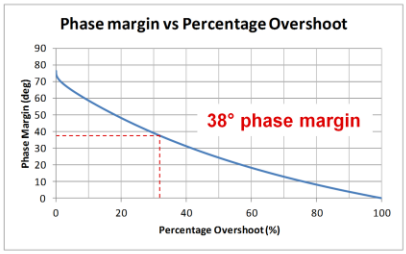
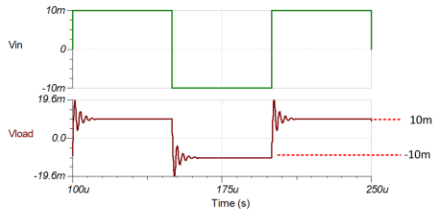
Quiz

- Find the phase margin of each system according to the % overshoot.

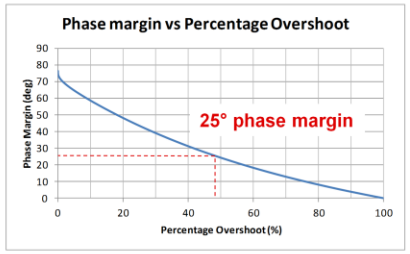


$$\%\text{Overshoot} = \left(\frac{16.4\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{32\%}$$



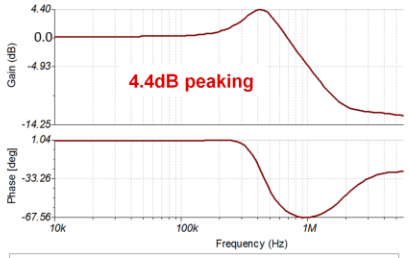


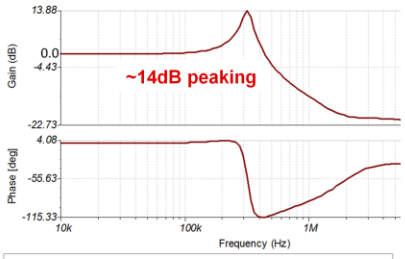
$$\%\text{Overshoot} = \left(\frac{19.6\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{48\%}$$

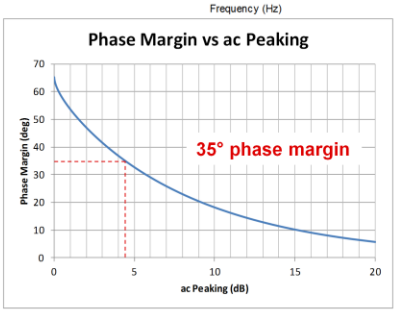


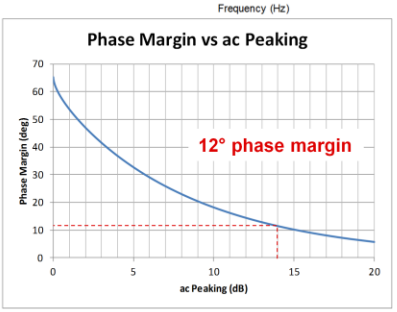
Quiz

- Find the phase margin of each system according to the AC peaking.









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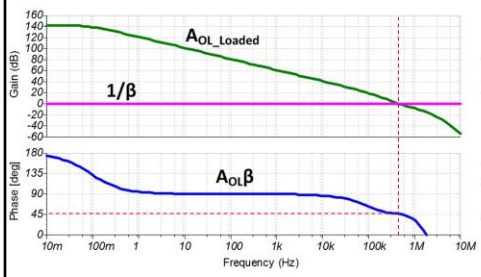
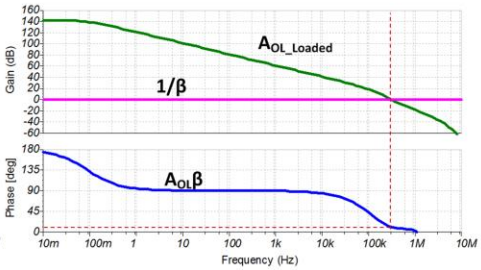
Quiz

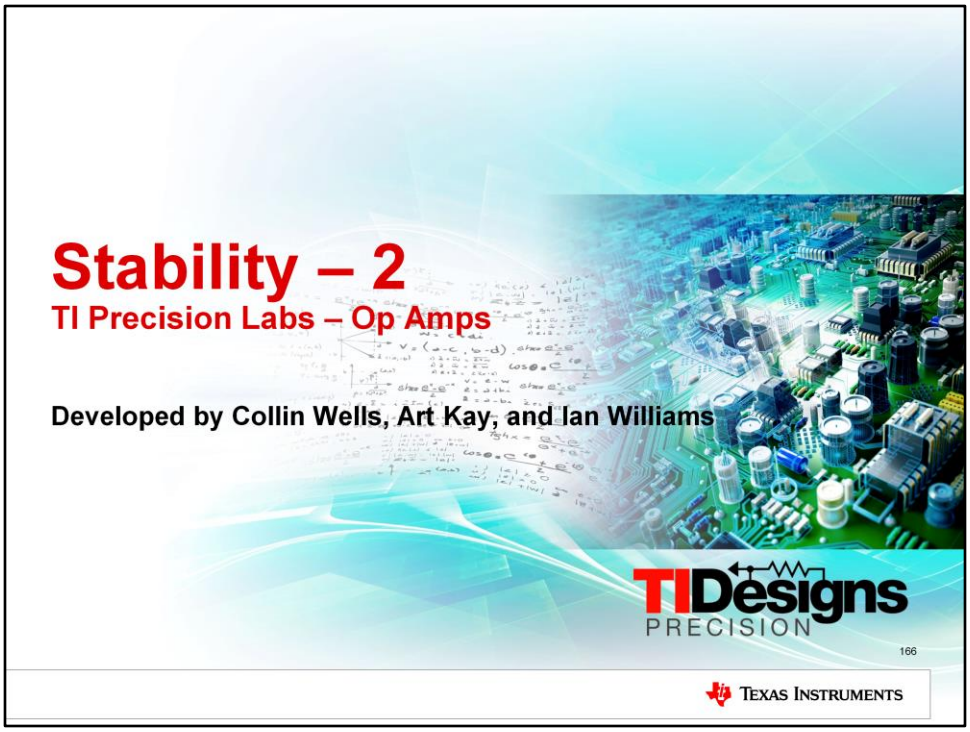
- Find the phase margin of each system according to the Bode plot.



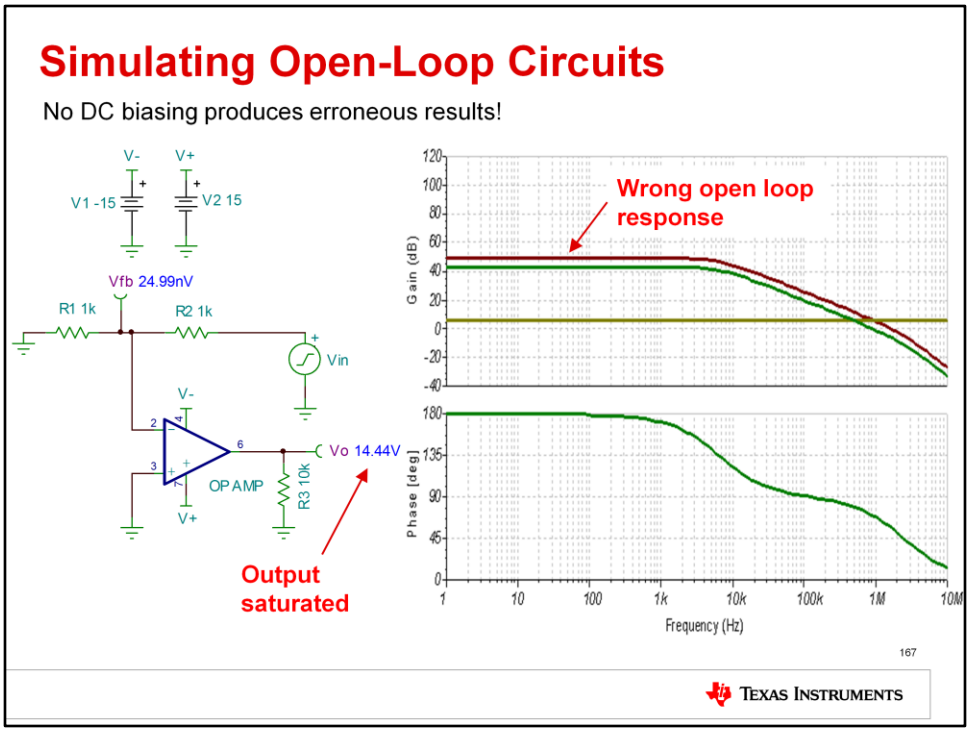
45° phase margin



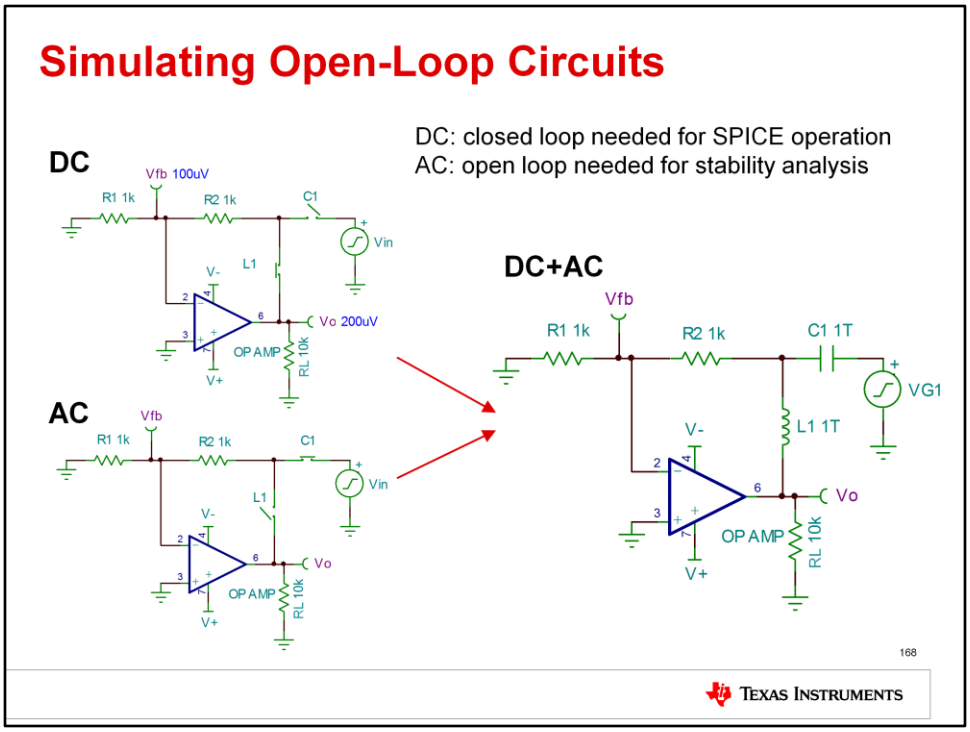
~15° phase margin



Hello, and welcome to part 2 of the TI Precision Lab lecture on op amp stability. In this lecture we'll show how to simulate circuit stability in SPICE, as well as show several methods for stabilizing circuits.

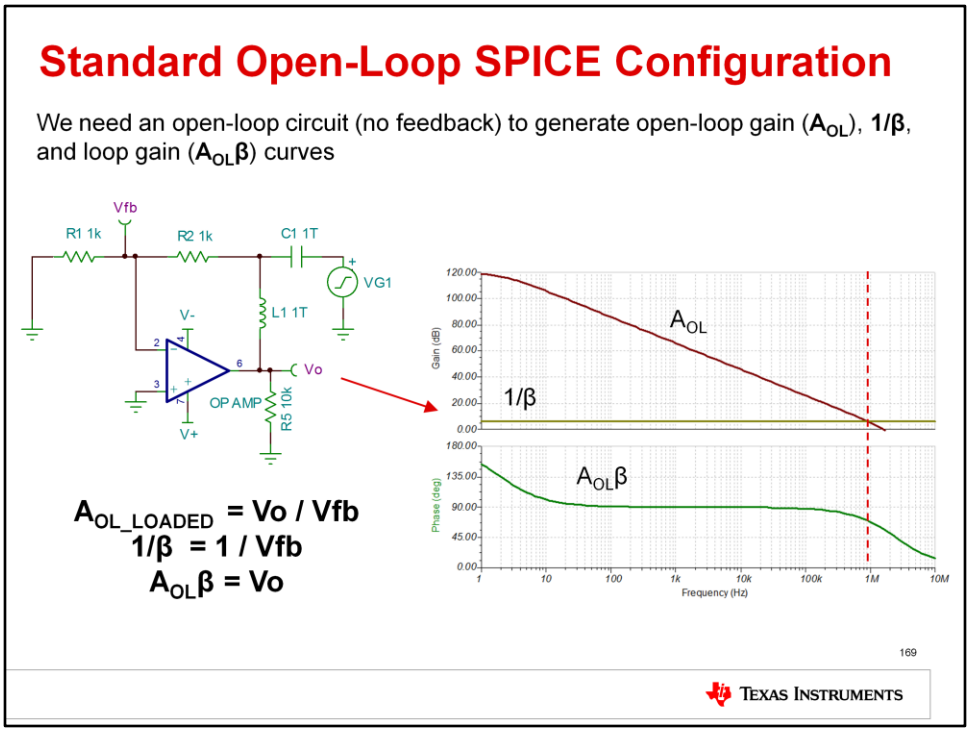


However, a circuit without feedback will not simulate properly because the output will go to one rail or the other. This causes incorrect Aol or output characteristics to be displayed. As shown here, the op-amp output is near the positive rail, resulting in an erroneously Aol curve.



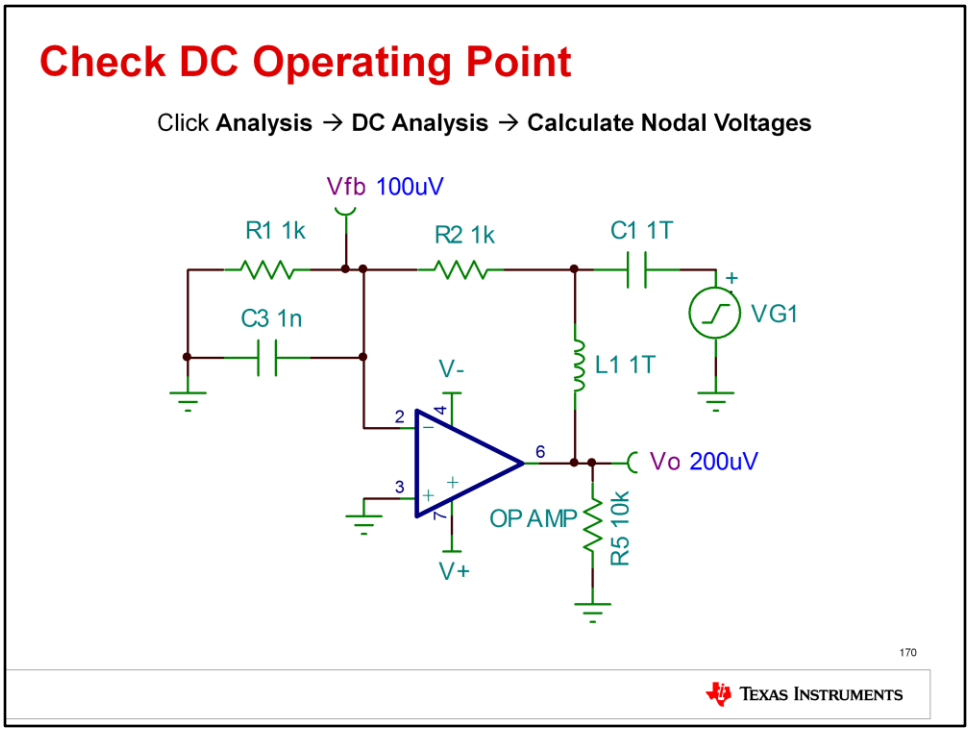
To correct for this, we need to do a simple manipulation of the circuit. SPICE simulators need a DC operating point in order for the models to converge properly, so a DC feedback path is required. This is equivalent to the circuit at the top left, where switch L1 is closed and switch C1 is open. At AC, we want the feedback loop to be open and apply a signal through the feedback network to determine the open-loop characteristics. This is equivalent to the circuit at the bottom left, where switch C1 is closed and switch L1 is open.

Thankfully, there's a straightforward way to do this in a circuit that meets both the DC and AC criteria. Switch L1 is replaced with a 1T inductor, and switch C1 is replaced with a 1TF capacitor. This gives us a DC operating point, where L1 acts like a short and C1 acts like an open, and at some very small AC frequency the inductor acts like an open circuit and C1 acts like a short, giving us the proper connections at AC as well.

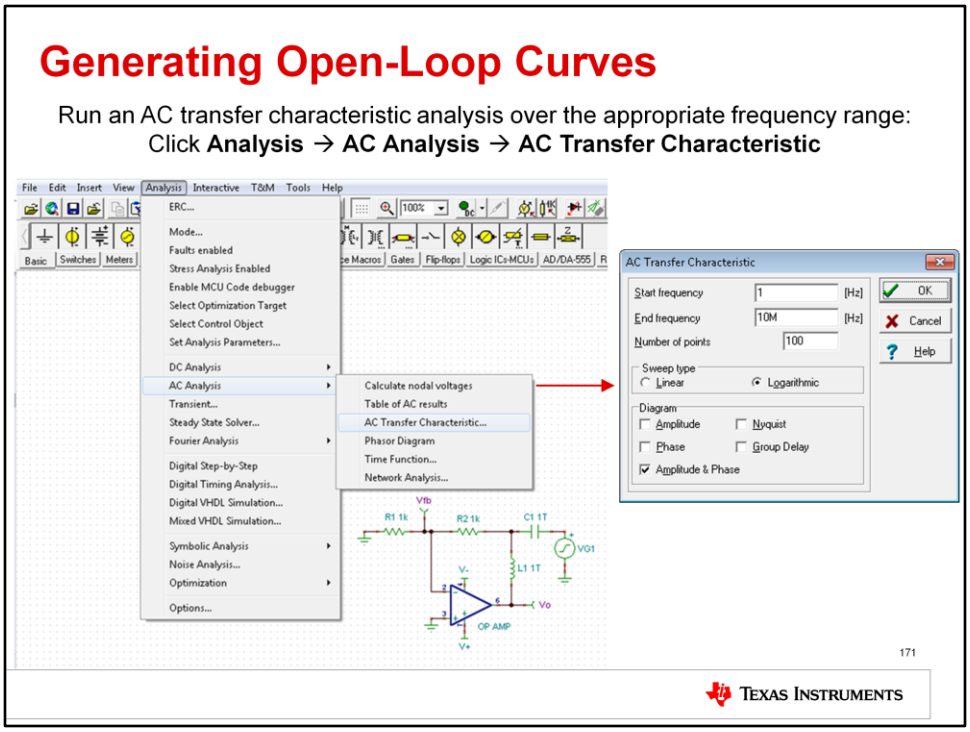


In order to successfully generate the open-loop curves to perform the rate-of-closure and phase margin analysis, the feedback loop of the op amp needs to be broken. Then, a small signal source can excite the high-impedance node of where the loop was broken and measurements can be taken at the input (Vfb) and output (Vo) to derive the desired curves.

With the op-amp feedback loop broken as shown here, the equations for generating the curves are as follows:
Aol_loaded = Vo/Vfb
1/B = 1/Vfb
Aol*B = Vo



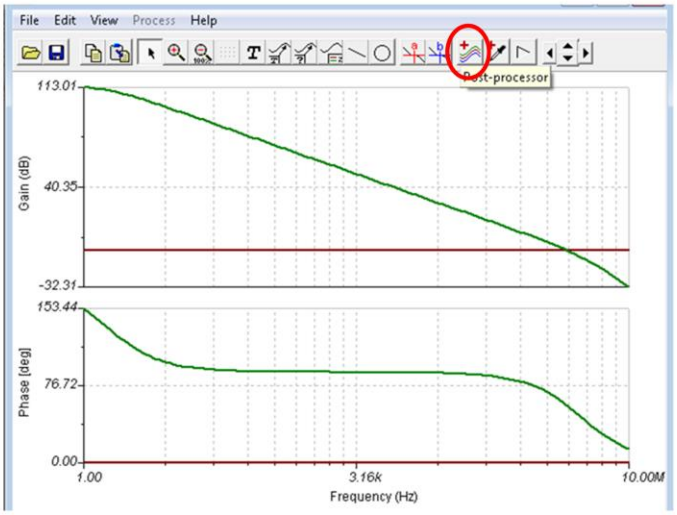
Before checking the AC behavior of the circuit, a quick check of the DC operating point should be done. Simply click Analysis, DC Analysis, and Calculate Nodal Voltages to do this. Vfb should show the input offset voltage, or Vos, of the op amp, while Vo will show Vos multiplied by the closed-loop gain.



Once you've verified the DC functionality of the circuit, perform an AC transfer characteristic analysis over the op-amp bandwidth. Click Analysis, AC Analysis, AC Transfer Characteristic to do this.

Generating Open-Loop Curves

Click the “Post-Processor” button to add the desired curves



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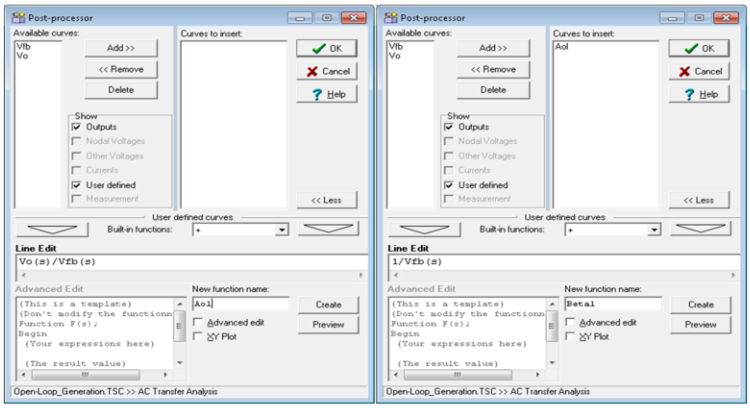
TINA by default will only display the curves which have markers, which in this example is Vo and Vfb. To add the desired curves for open-loop analysis, click the post-processor button in the result window.

Generating Open-Loop Curves

Perform math on the existing curves to create the new curves:

$$A_{OL} = Vo / Vfb$$
$$1/\beta = 1/Vfb$$
$$A_{OL}\beta = Vo$$



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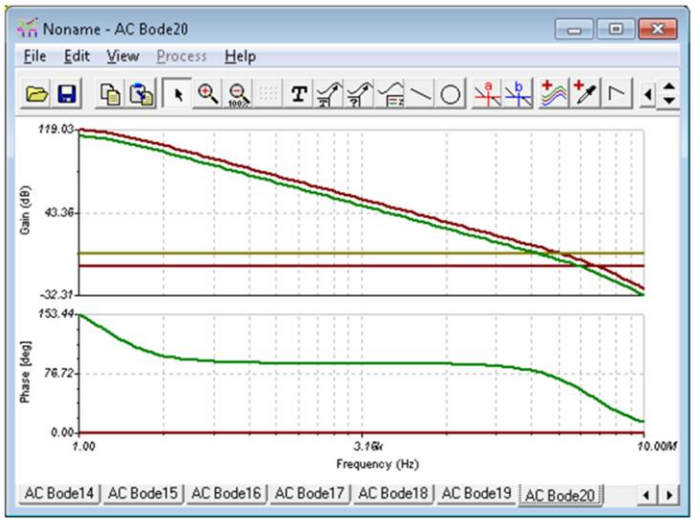
Write the proper equations for Aol and 1/β in the line editor, name them, and then create the curves. A new curve can be added for Aol*β, but since it equals “Vo” which is already displayed, this is not necessary.

Please note, the editor will not allow the entry in the “New Function Name” box to begin with a number or have special characters. Therefore “1/Beta”, or “1Beta” are not allowed. We recommend to use “Beta1” for the 1/Beta curve name.

Generating Open-Loop Curves

Unformatted results with all curves:



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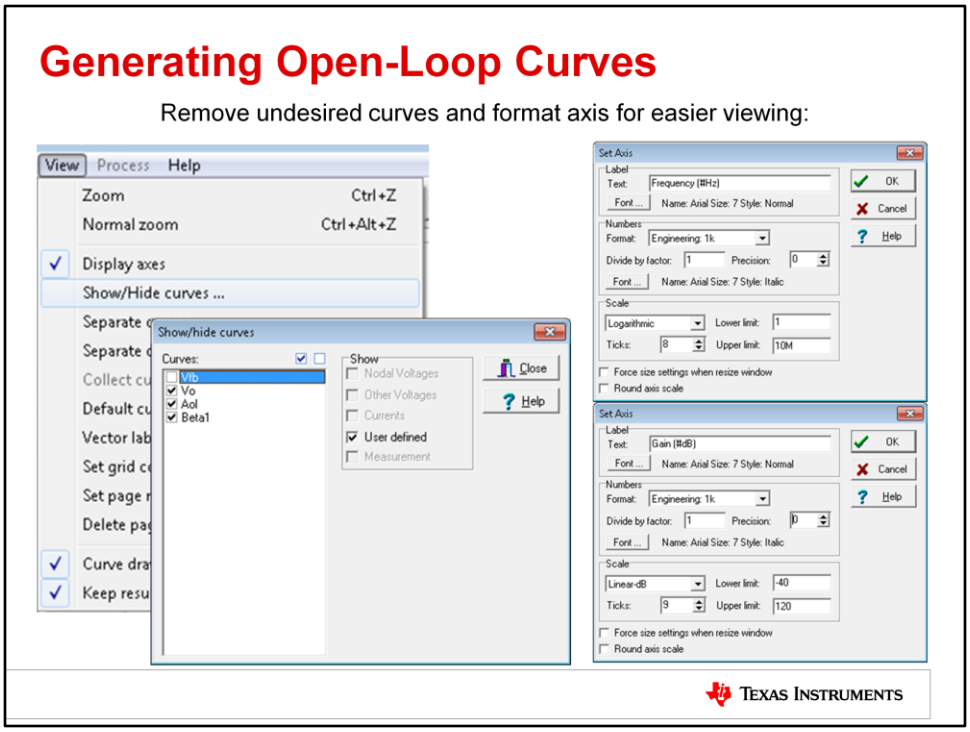
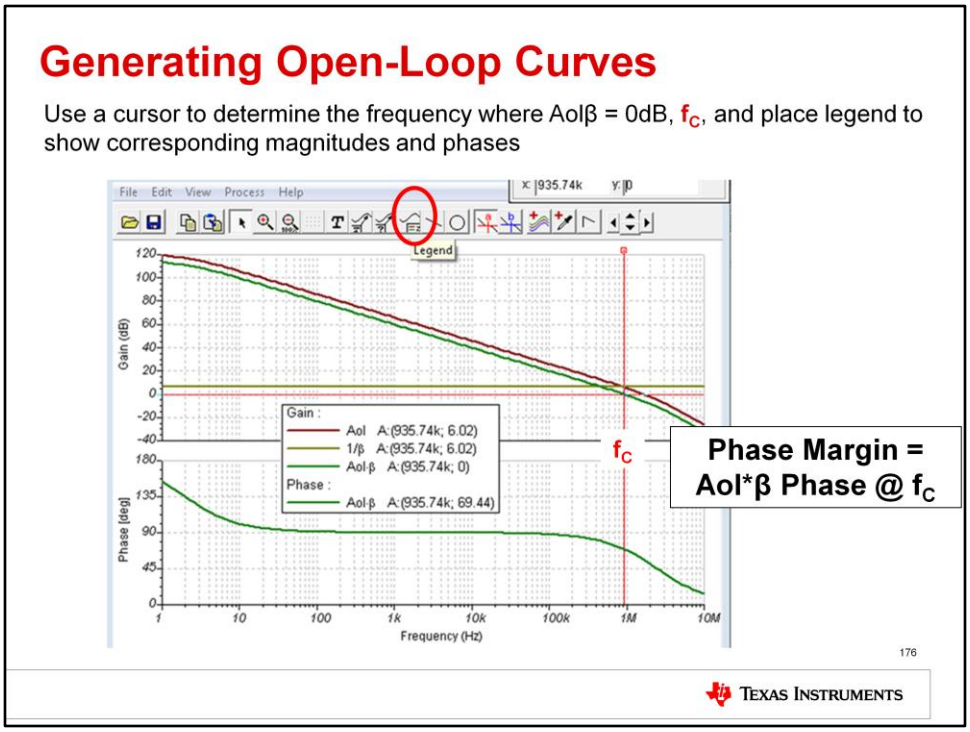
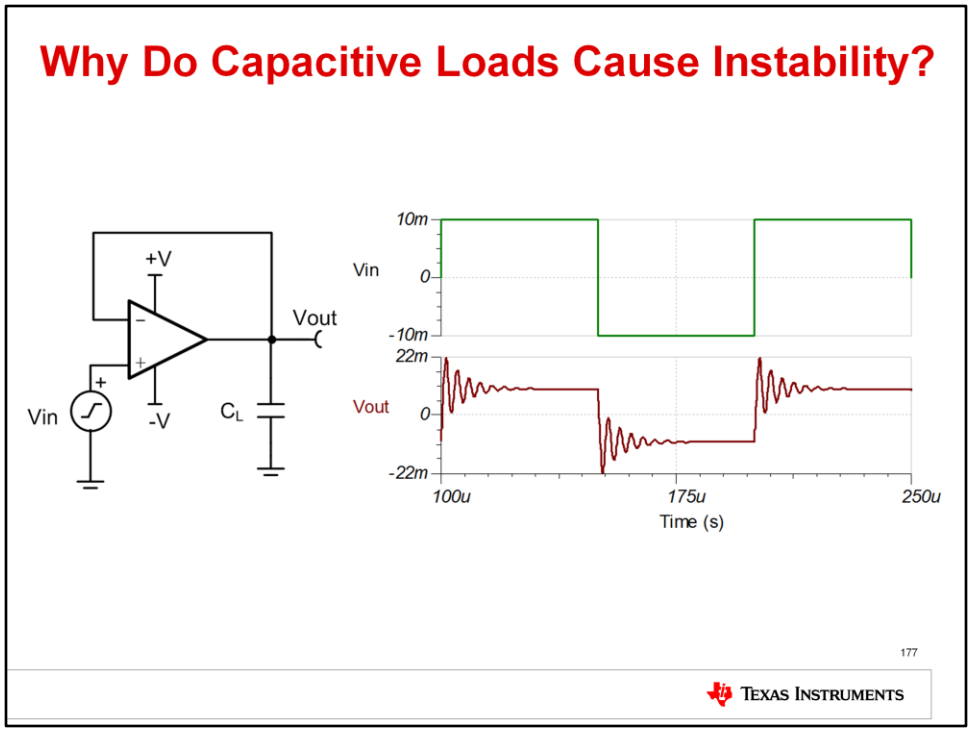
Here's what the results will look like with the new curves added. The next steps will format the results to make them easier to view.



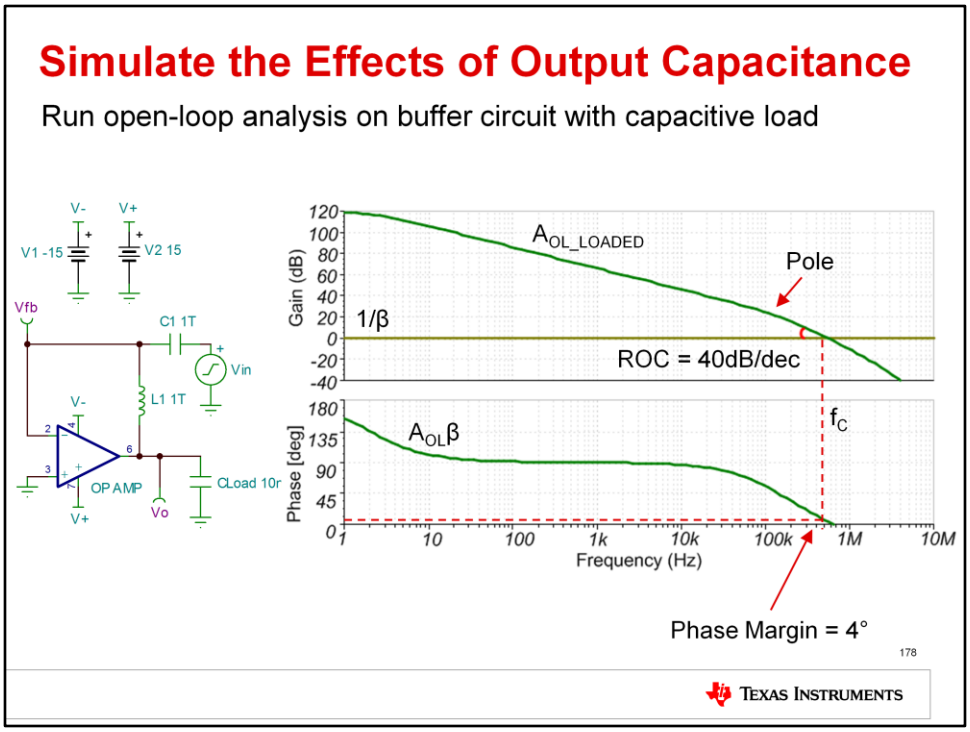
Click View, then Show/Hide curves. Select only the curves Vo, Aol, and Beta1. Then, double-click the x-axis and y-axis to bring up the “Set Axis” window. Change the x-axis to a logarithmic scale, 8 ticks, lower limit 1Hz, upper limit 10MHz. Change the y-axis to a linear-in-dB scale, 9 ticks, lower limit -40dB, upper limit 120dB.



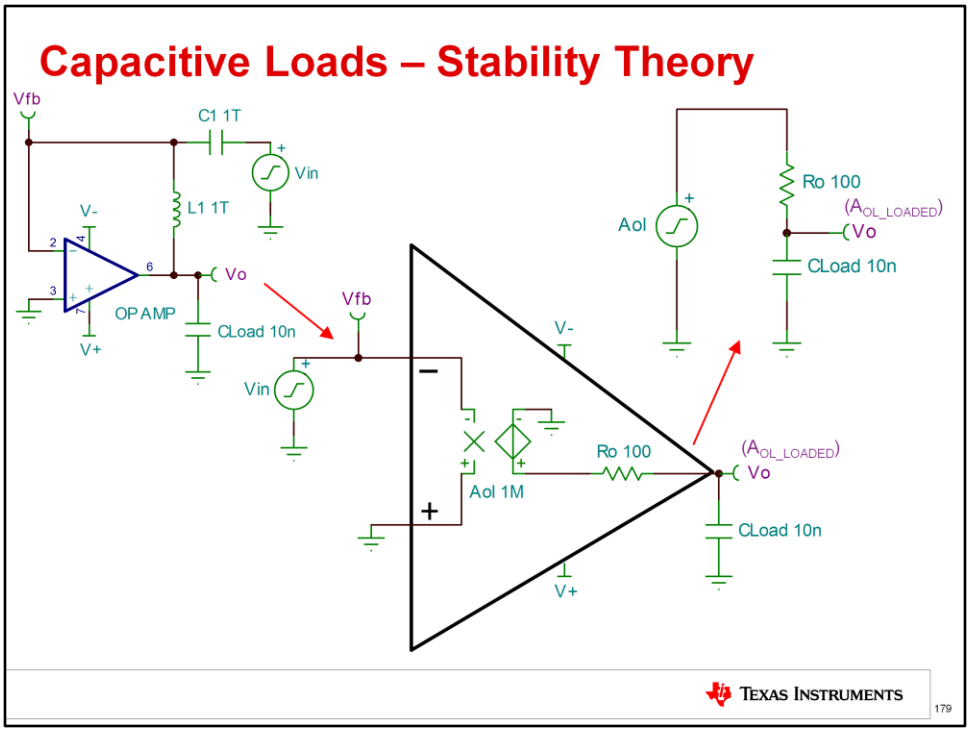
The final step is to measure the phase margin on the curves. The easiest method is to place a cursor on the Aol*β curve and then type "0" into the "y:" text box to set the cursor to the fc frequency. Then click the "Legend" button and place it on the screen, which will display the phase of Aol*β at fc. This is the phase margin.



We've told you earlier in the presentation, and you may have seen in your experience, that capacitive loads cause instability such as the overshoot and ringing shown on the right. Why does this happen? We'll explain why in this section of the lecture.

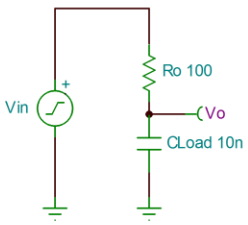


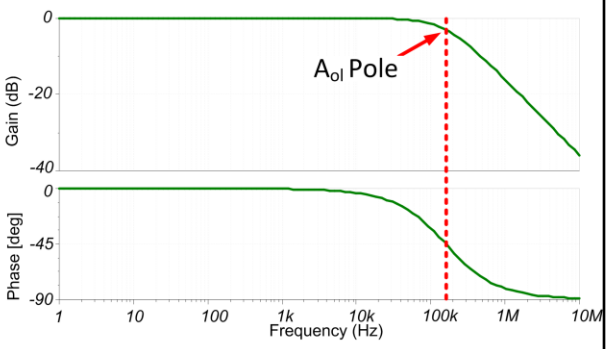
Using the steps shown previously, we ran an open-loop simulation on the circuit shown here with a 10nF capacitor on the op amp output. As the results show, the 10nF capacitive load results in a pole in the Aol curve which degrades the Aol*ß phase to only 4 degrees at fc. Let's examine why this happens.



If we take a look at a simplified representation of the open-loop circuit, we see that the input signal passes through the Aol gain block and then the series open-loop output impedance, Ro, before reaching the op amp output, Vo. With a capacitor, Cload, on Vo, the op amp loaded Aol curve is divided down by an RC voltage divider.

Capacitive Loads – Stability Theory

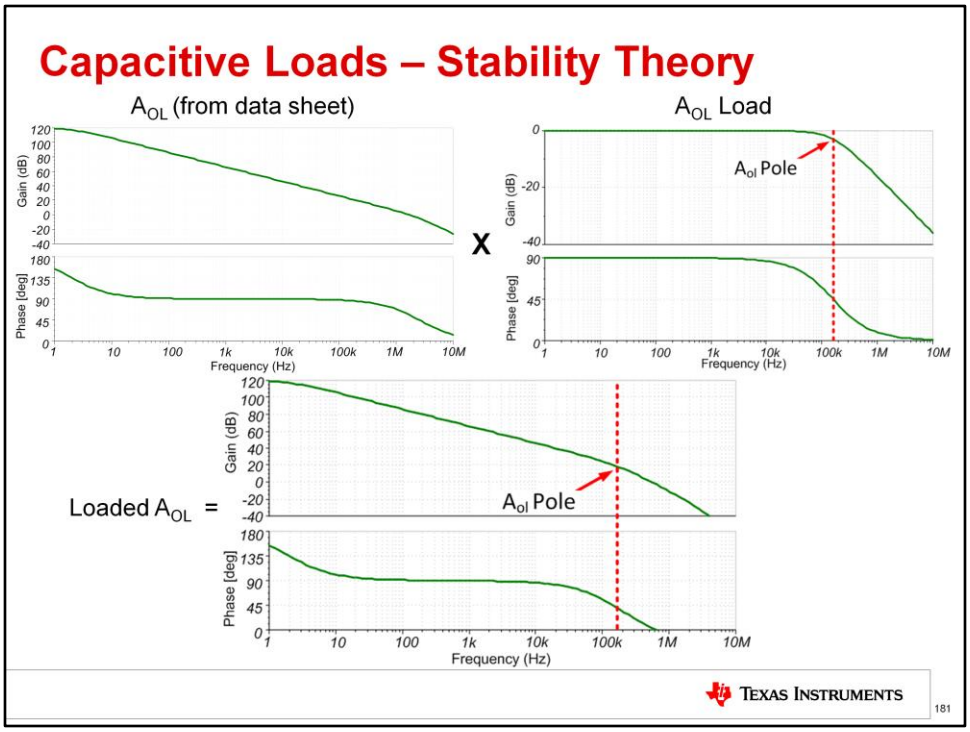




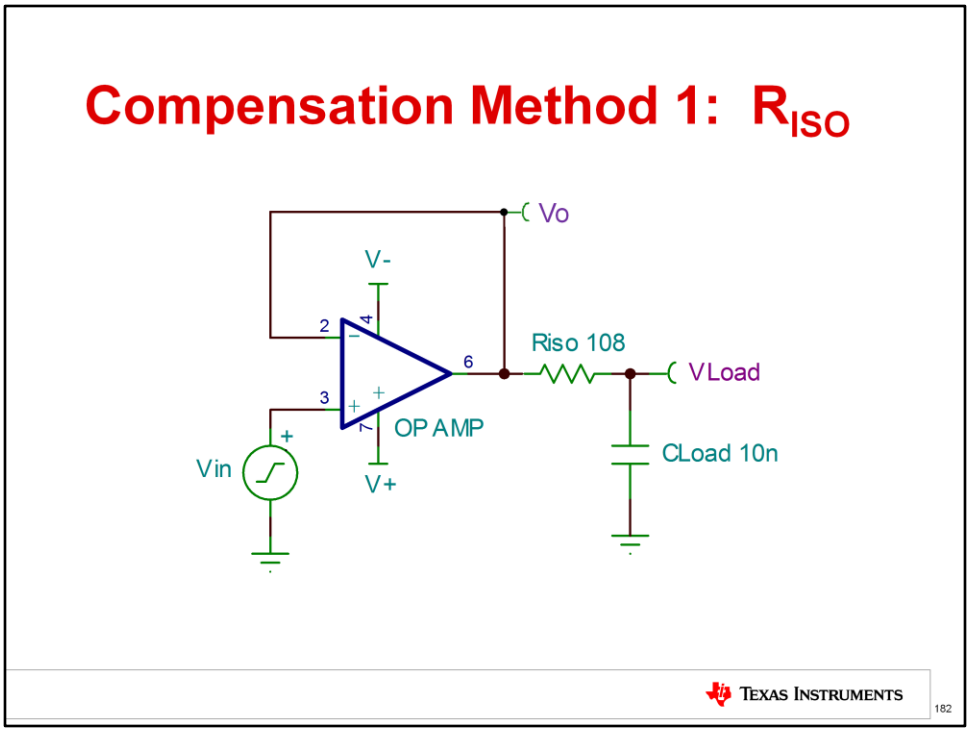
Transfer Function: $\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$

Pole Equation: $f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$

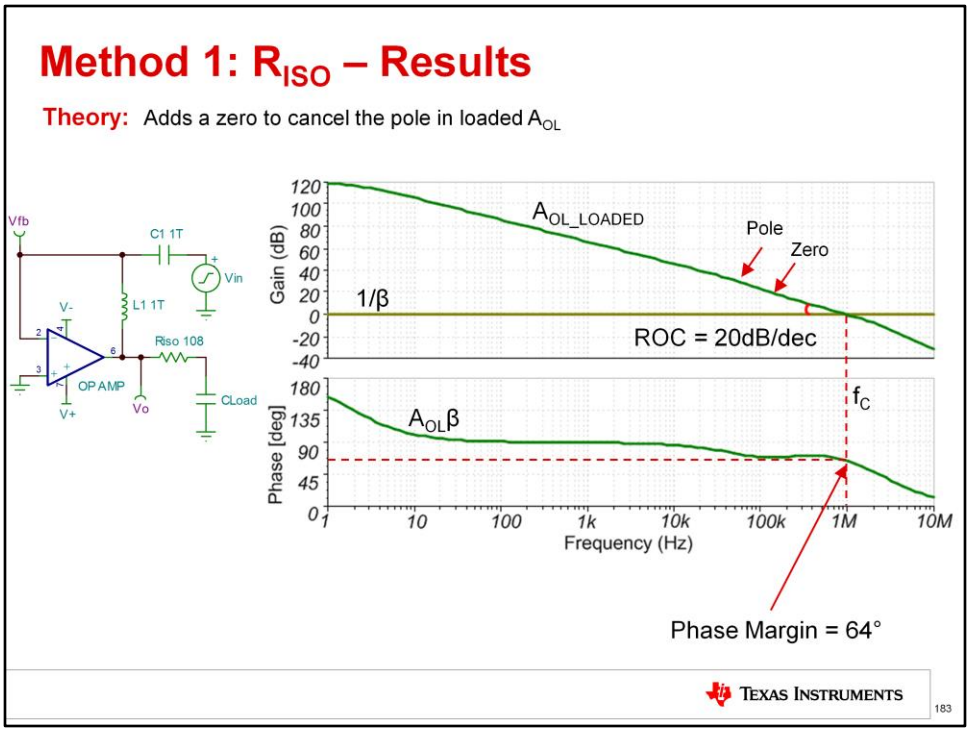
The AC transfer function of the equivalent load RC circuit has been plotted here. The pole location can be calculated from the transfer function and is shown at the bottom of the slide.



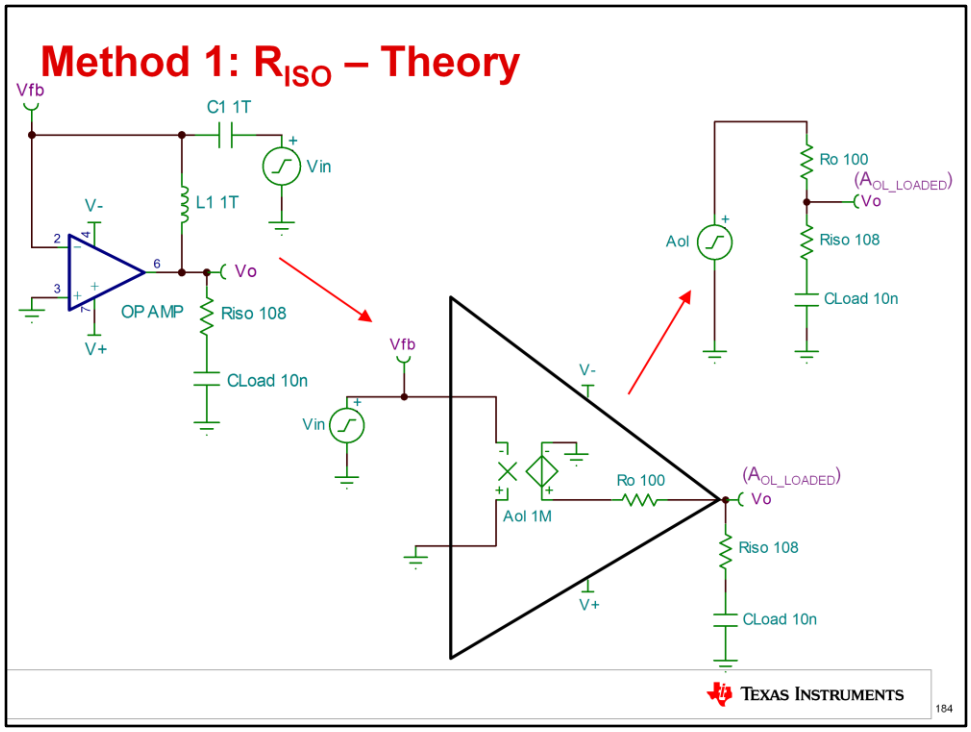
If the original op amp Aol curve and the Aol load curve are combined, the result is the loaded Aol curve shown on the bottom. As shown, the pole from the interaction of Ro and Cload causes a change to a -40dB/decade Aol magnitude slope and a degraded unity-gain phase margin.



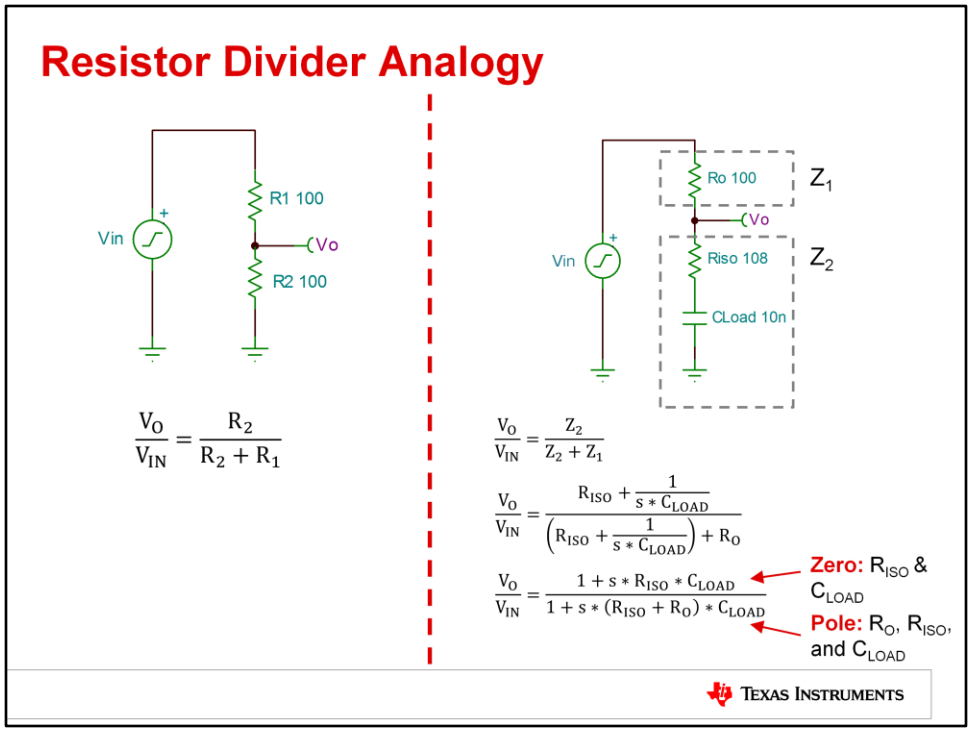
The Riso method is quite simple. It works by adding a zero to the Aol curve to cancel the pole from Ro and Cload.



Looking at the open-loop results from the “Riso” compensation method, a zero can be seen cancelling the pole from Riso and Cload. This results in a return to a 20dB/decade Aol slope and significantly improved phase margin.

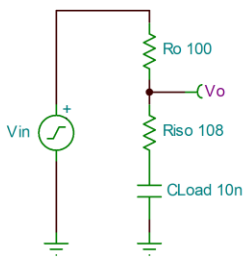


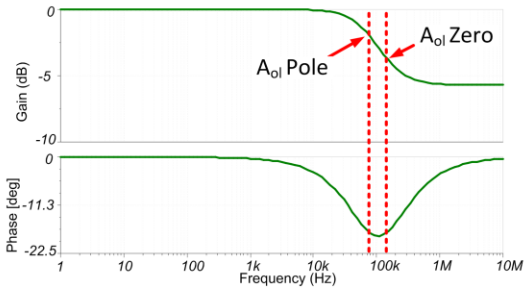
We can look at the Riso circuit the same way we looked at the original circuit. Here we see another voltage divider on the Aol output. This time there are two elements, Riso and Cload, on the bottom of the divider and Ro on the top leg of the divider.



We can still compare this circuit to a classic resistive voltage divider. Remember, the transfer function of a resistive voltage divider is the resistance of the bottom leg divided by the sum of both the top and bottom impedances. The same applies to the circuit with Ro, Riso, and Cload, as shown on the right. Ro makes up Z1, the impedance of the top leg, while the series combination of Riso and Cload make up Z2, the impedance of the bottom leg. The transfer function can be simplified to the form shown at the bottom-right. The numerator shows a zero dependent only on Riso and Cload, both external circuit components, while the denominator shows a pole dependent on Ro, Riso, and Cload.

Method 1: R_{ISO} – Theory



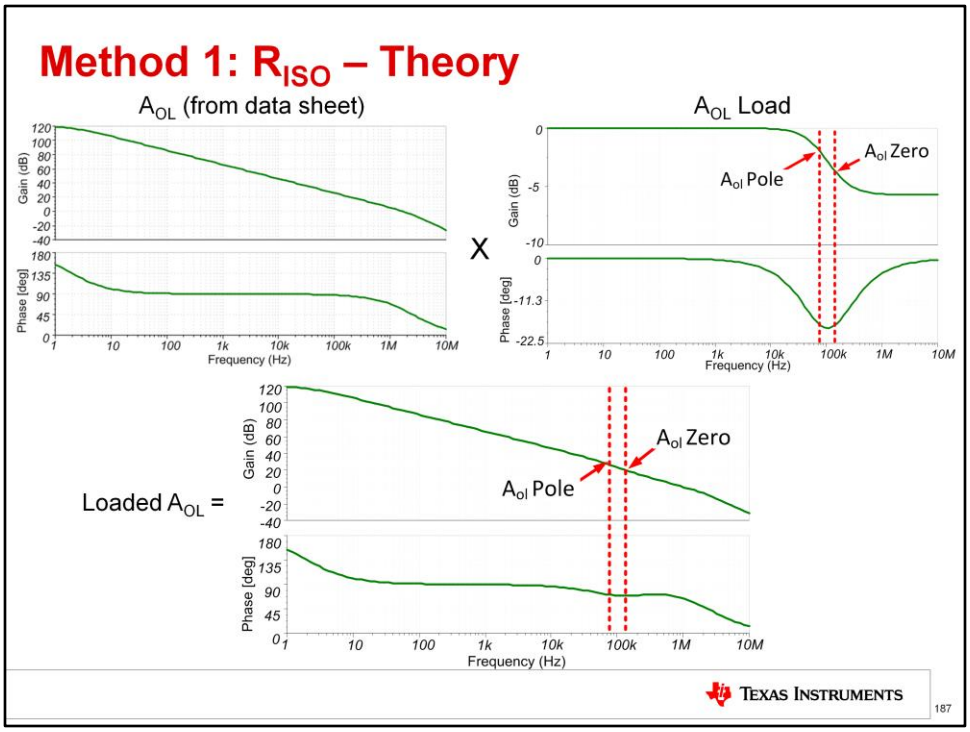


Transfer Function: $$\frac{V_o}{V_{in}}(s) = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_O + R_{ISO}) * C_{LOAD}}$$

Zero Equation: $$f_{ZERO} = \frac{1}{2 * \pi * R_{ISO} * C_{LOAD}}$$

Pole Equation: $$f_{POLE} = \frac{1}{2 * \pi * (R_O + R_{ISO}) * C_{LOAD}}$$

The resulting Laplace transfer function for this circuit is shown here. Again, with a single “s” term in both the numerator and denominator it is clear that there is now both a pole and a zero in the transfer function. The equations for the pole and zero frequency can be calculated from the transfer function. Plotting the AC transfer function, you can see that the positive phase shift from the zero cancels the negative phase shift from the pole, causing a net phase shift of zero degrees.



Adding the Aol and Aol load curves together as before, we can again see that the zero added by Riso cancels the pole in the Aol curve and restores the phase margin to an acceptable level for stability.

Method 1: R_{ISO} – Design

Design Steps:

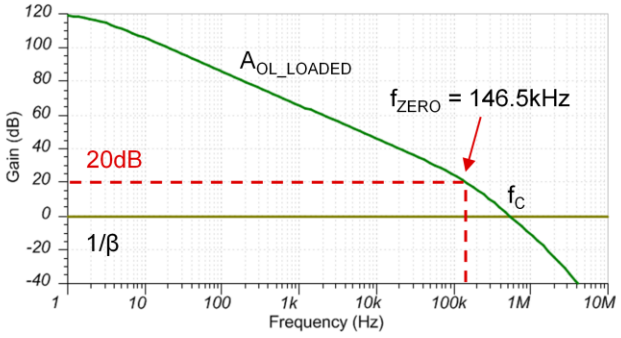
1.) Find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20 dB
2.) Calculate Riso to set the zero at f_{ZERO}
This will yield between 60° and 90° degrees of phase margin

R_{ISO} Equation:

$$R_{iso} = \frac{1}{2 * \pi * f_{ZERO} * C_{LOAD}}$$

$$R_{iso} = \frac{1}{2 * \pi * 146.5\text{kHz} * 10\text{nF}}$$

$$R_{iso} = \mathbf{108\Omega}$$



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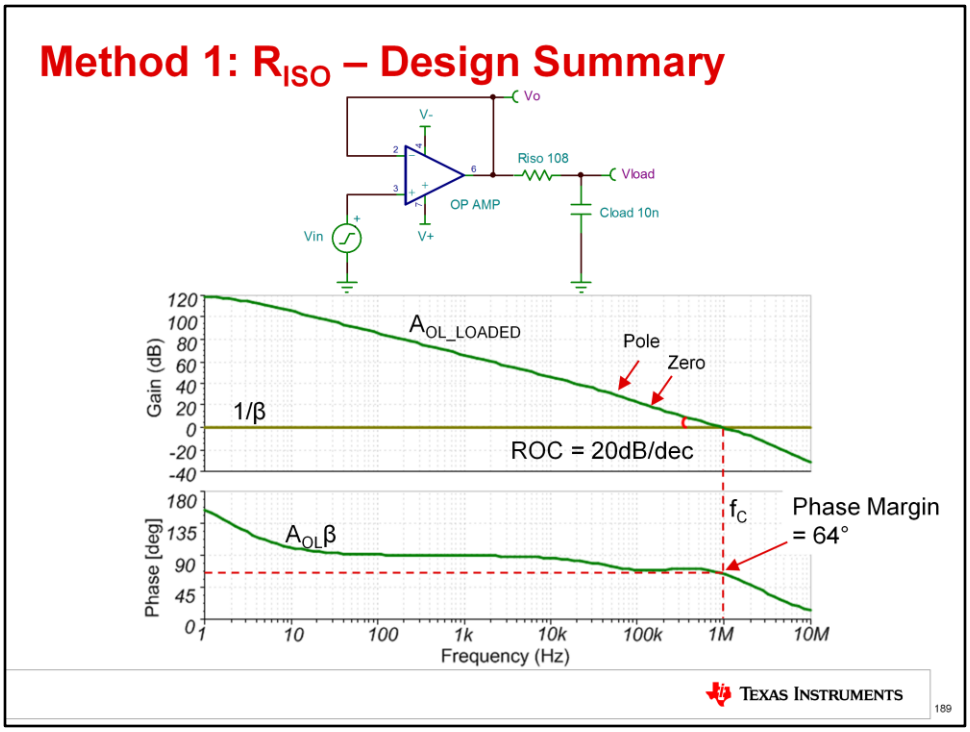
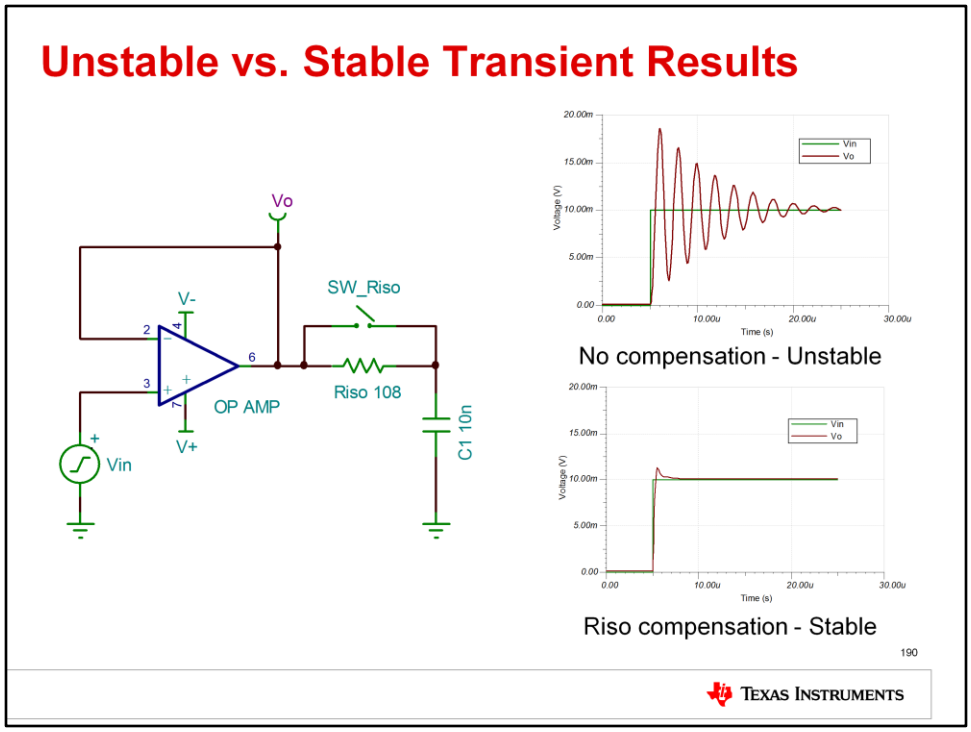
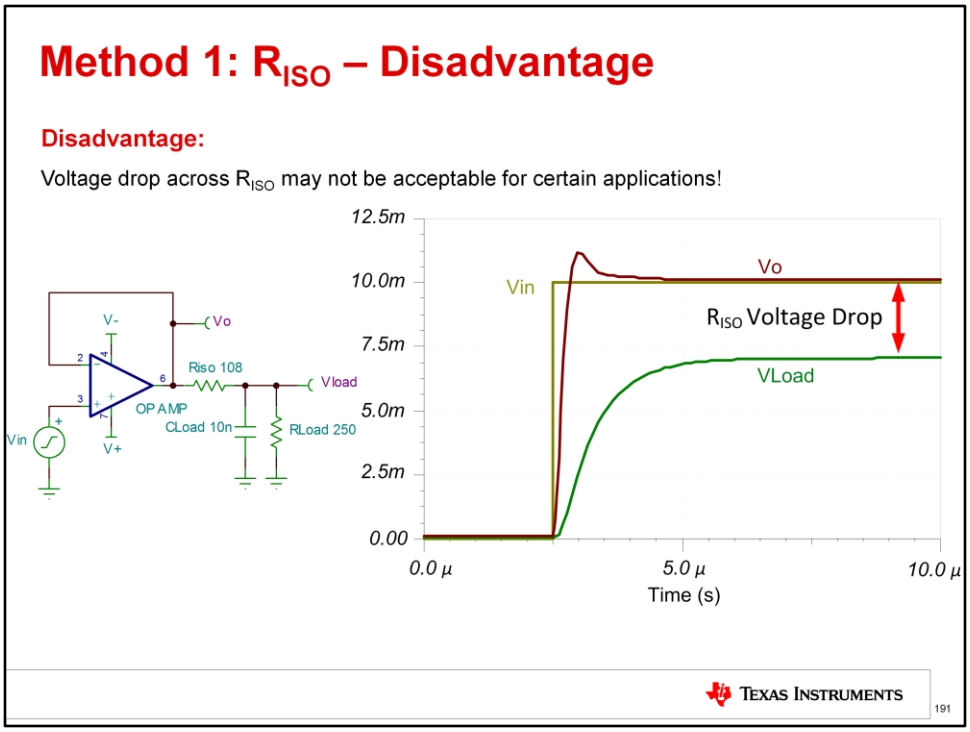
To design the Riso circuit for between 60 and 90 degrees of phase margin (depending on the op amp unity-gain phase margin and location of the Aol pole), first find the frequency where the Loaded Aol curve is equal to 20dB, f(Aol = 20dB). Using the Riso equations shown on the left and plugging in the values for Cload and f(Aol = 20dB), the Riso value is calculated to be 108 Ω in this example.



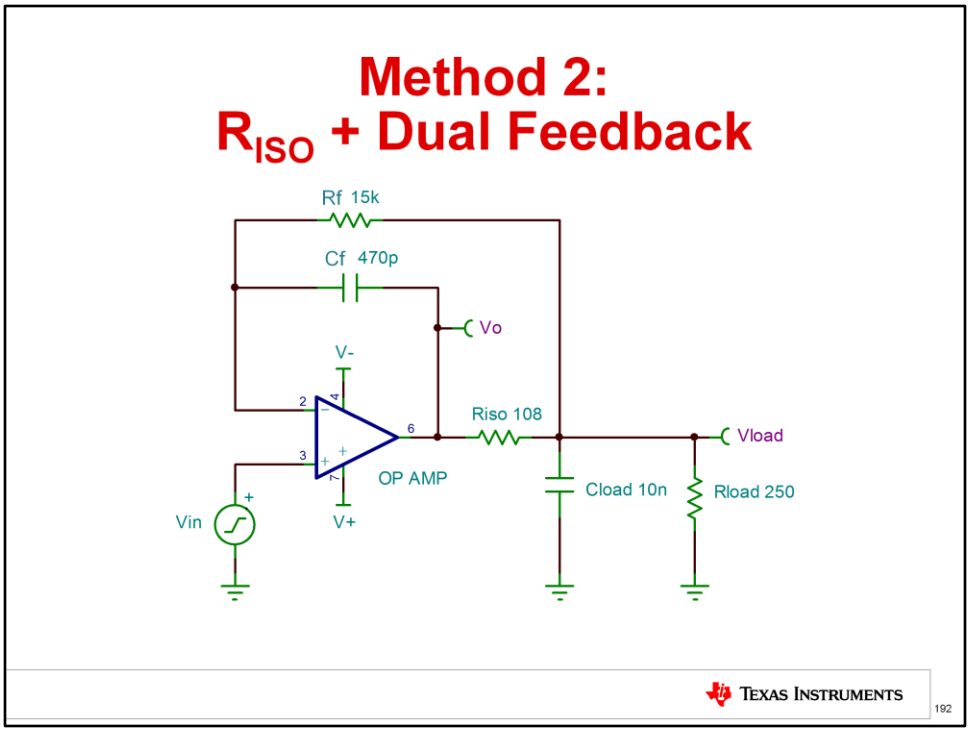
In summary, find the f(Aol = 20dB) frequency and set the zero there by calculating Riso. While the theory behind this is not shown here, if the zero frequency ends up greater than ~1.5 decades from the pole, the Riso value should be increased to prevent the Aol*ß phase from dipping too low in the loop. If Riso is equal to at least Ro/34, then the zero will be within 1.5 decades of the pole. If the circuit is not required to deliver larger output currents then consider increasing Riso to be equal to or larger than Ro and the circuit will be stable under basically all capacitive loads.



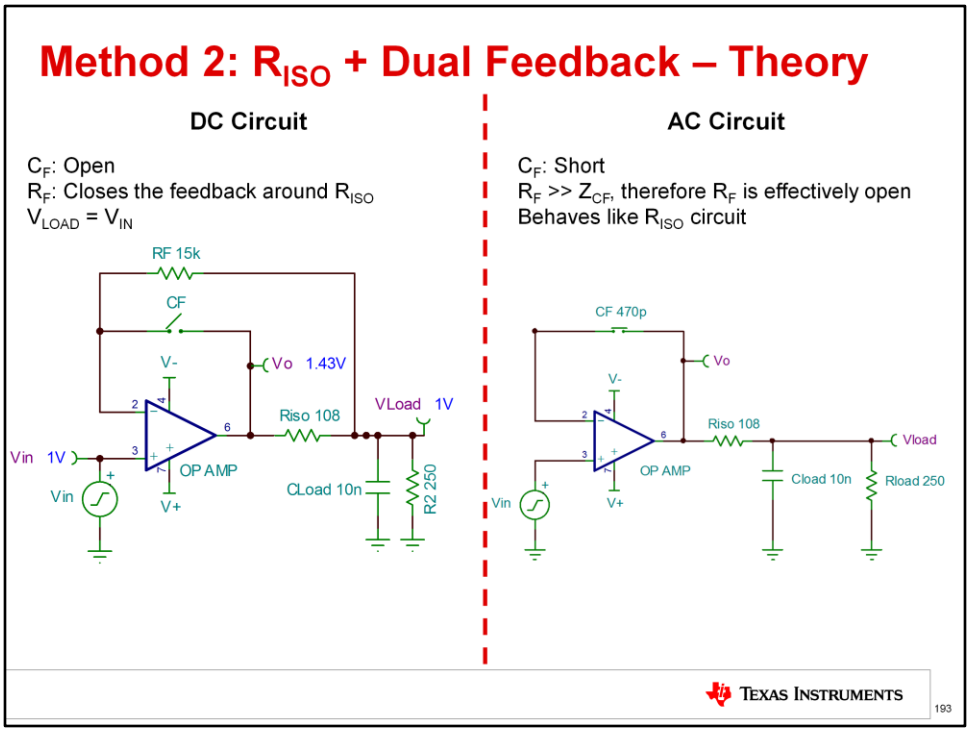
Comparing the transient response of the circuit both with and without Riso compensation, we can see the significant improvement by using Riso. Without Riso, the output of the circuit shows heavy overshoot and ringing.



While the Riso circuit is both simple to implement and design it has a big disadvantage in precision circuits. The voltage drop from Riso is dependent on the output current or output load, and may be significant compared to the desired signal. As shown here a 10mV signal has over 3mV (30%) of error due to a 250Ω output load.



A solution to the voltage drop problem from the Riso circuit is to implement the “Riso + Dual Feedback” circuit shown here.



The Riso + dual feedback circuit works by having an equivalent circuit at both DC and AC.

At DC, the feedback capacitor CF acts as an open circuit and RF closes the feedback loop around Riso. Since Riso is now in the op amp feedback loop, the op amp output will increase to overcome the Riso voltage drop such that the load voltage, Vload, is equal to Vin.

At AC frequencies, CF acts as a short. When this happens, RF can be thought of as an open-circuit because the impedance of CF, X_{CF}, will be much smaller than the impedance of RF. Therefore, at AC, this circuit looks effectively the same as the standard Riso circuit.

Method 2: R_{ISO} + Dual Feedback - Design

Design Steps:

1) Set R_{ISO} using Method 1: R_{ISO} techniques
2) Set R_F: $R_F \geq (R_{ISO} * 100)$
3) Set C_F: $\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$ lower values of C_F = faster settling, higher overshoot

Rule 3 ensures that the two feedback paths will never create a resonance that would cause instability

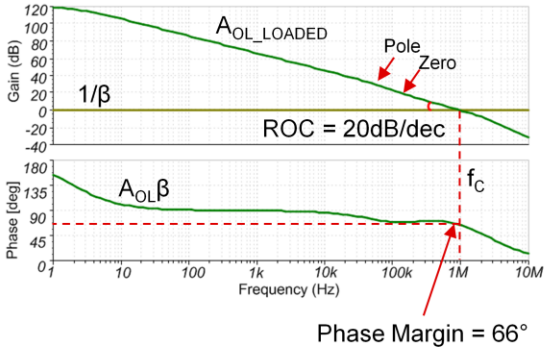
$R_{ISO} = 108\Omega$

$R_F \geq R_{ISO} * 100$

$R_F \geq 10.8k\Omega$

$$\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$$

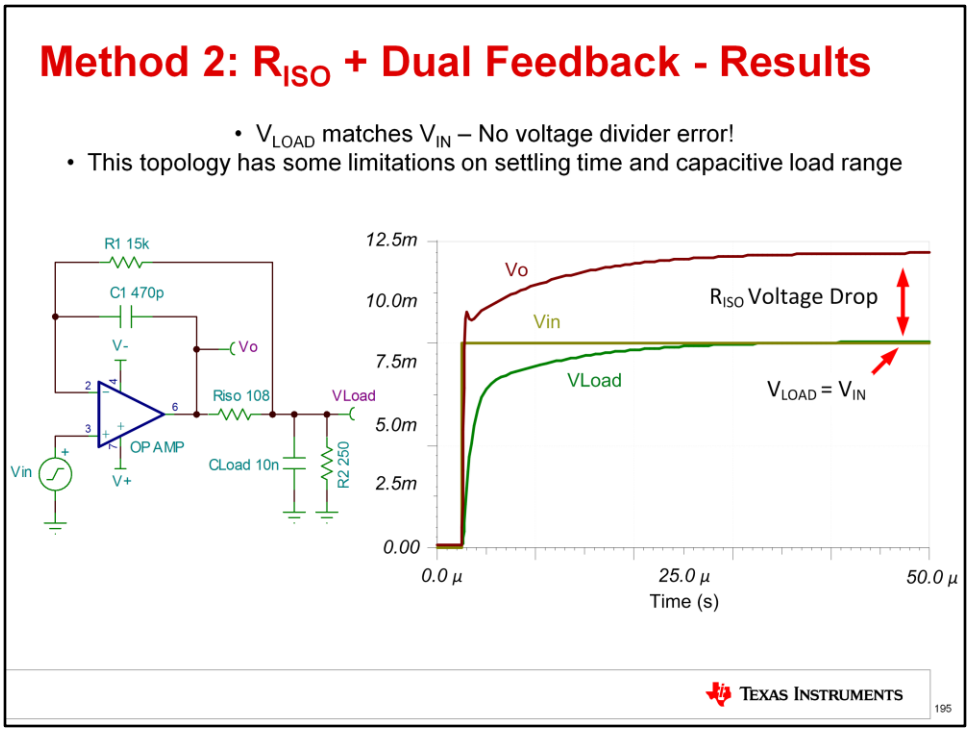
420pF ≤ C_F ≤ 720pF



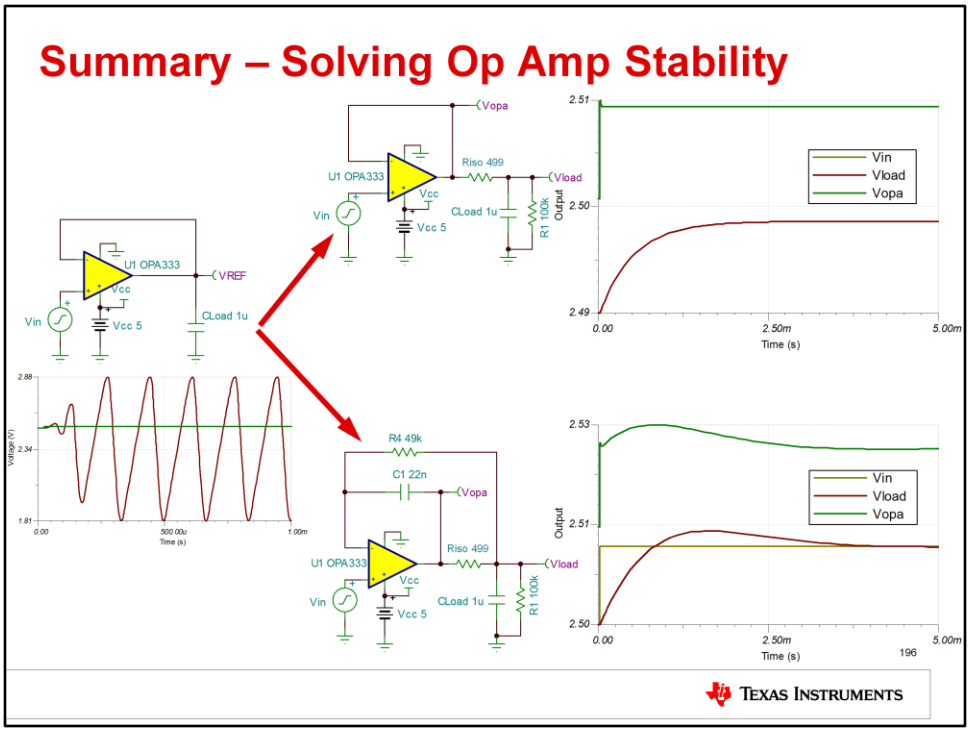
The first design step in this circuit is to select Riso. The same method that was used to select Riso in “Method 1: Riso” is used here, and Riso is selected to produce a zero in the Aol curve at f(Aol = 20dB).

Then, RF can be selected to any value greater than 100*Riso in order to prevent interactions with Riso.

The last step is to select a value of CF in the range shown. Using this range ensures that the two feedback paths, Rf and Cf, will never create a resonance that would cause instability. Smaller values for CF will result in faster settling time, at the expense of overshoot for certain load ranges.



The results show that the output and load voltage arrive at the final level without excessive overshoot or ringing, indicating a stable system. The increase in Vo to overcome the voltage drop from Riso can also be clearly seen here.



In summary, this presentation explained how to simulate the open-loop behavior of op amp circuits, and continued by showing how to use that information to stabilize circuits. Two methods were introduced, the Riso method which is simple and effective but sacrifices DC accuracy, and the Riso + dual feedback method which has good DC accuracy, but longer settling time and less flexibility. Keep in mind that these two stability lectures barely scratch the surface of op amp stability. Don't hesitate to reach out to your op amp experts for assistance with solving your stability questions!

That concludes the lecture manual – thank you for your time!

Changes

- Page 62-slew rate internal op amp diagram. Change iout to icc
- Page 61: added integration
- Page 5 – changed histogram to more closely match stdev = typical
- Page 97 – added example of Req
- Page 98 – added res noise vs. op amp noise
- Page 107 – added noise bandwidth example
- Page 109 added rms noise example
- Page 60 edited time at bottom of diagram from 0.25us to 0.275us
- Page 66 – added little figure of internal op amp slew in corner of slide
- Page 28 – changed Vsd=.9 to Vsat=0.1
- Page 17-changed bias current example to use Req method as opposed to nodal analysis
- Page 187-187 Fixed equations in stability part 2
- Page 194 – added annimation

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