Application Note

Thermal Analysis of the DVF Package of the TMCS1143

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ABSTRACT

The rapid increase in power density and reduction of PCB copper volume in modern electrified systems create a demanding thermal environment for in-package Hall-effect current sensors such as the TMCS114x series. This paper presents a comprehensive thermal analysis of the DVF package used in the TMCS1143 sensor. Two complementary characterization approaches are investigated: (1) a traditional current-based method that derives junction temperature from a curve-of-best-fit to steady-state current-temperature data, and (2) an alternative method that directly monitors ambient and lead-frame temperatures using the isolated temperature-sensor IC ISOTMP35R. Results show that, beyond low-current operation, power dissipated in the lead frame quickly dominates over quiescent silicon power, causing the conventional JEDEC model to underestimate junction temperature. A linear relationship between lead-frame temperature rise and junction temperature at higher power is observed, yielding an effective thermal resistance of approximately 5°C/W that remains consistent across the tested temperature range for the TMCS143 evaluation module.

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Trademarks

1 Introduction

Current measurement systems are experiencing rapid adoption as global electrification accelerates. These systems serve critical functions including feedback control, overcurrent protection, GaN FET zero-crossing detection, and advanced monitoring applications. In parallel, power density continues to be of chief importance, with solutions for various products chasing increasingly smaller footprints with each generation. This combination of trends creates a challenging thermal environment: as power density increases, component density rises, printed circuit board copper content decreases because of shrinkage, and ambient temperatures increase from cumulative heat generation. Accurately determining the maximum safe operating limits for semiconductor devices has become essential for reliable system design.

This paper examines the behavior of junction temperature in the DVF package used for the TMCS114x product series across multiple reference frames. For a characterization of junction temperature, the paper presents both a traditional current-based approach through curve of best fit, and alternative characterization methods examining the superposition of the power generated by the part itself as well as the power produced in the lead frame. Current remains the typical value provided to end users for defining safe operating areas, but its applicability varies significantly based on board construction. However, the current-based approach continues to dominate industry standards. If a design maintains steady-state operation at the maximum current specification, thermal considerations can typically be deprioritized from a reliability perspective.

As an alternative approach, this paper characterizes junction temperature through direct measurement of ambient temperature and lead frame temperature. This is accomplished by examining both heat sources internal to the device: the quiescent power of the silicon itself, as well as the power developed in the lead frame. This is accomplished using the ISOTMP35R reinforced isolated temperature sensor integrated circuit. The ISOTMP35R integrates an isolation barrier with a 5kVRMS withstand voltage and combines an analog temperature sensor featuring a 10mV/°C slope across the operating range of −40°C to 150°C. While still tested to the original layout of the standard TMCS family evaluation modules, this approach provides the user an application based approach for more granular monitoring and control of the junction temperature. This paper examines both the traditional current-based methodology via best fit curve, and the alternative junction temperature characterization approach.

2 Motivation and Discussion

Thermal Operating Limits and Design Constraints

In-package Hall effect devices operate at a maximum ambient temperature of 125°C, while the die junction withstands temperatures up to 165°C. The higher junction rating is necessary because internal power dissipation from the sensed current generates additional heat, even at the device maximum ambient operating point. Designers typically have limited thermal data to 125°C maximum ambient specification and standard JEDEC thermal metrics. To achieve the specified maximum current at this ambient temperature, the PCB layout must replicate both the copper volume and weight of the device evaluation module or test fixture. This requirement presents a practical challenge: evaluation boards are typically oversized relative to real-world applications to demonstrate peak device performance. Evaluation modules for Hall effect sensors often differ significantly from standard JEDEC reference boards used to characterize thermal parameters. These differences introduce deviations in thermal metrics when applied to actual designs.

Factors Affecting True Maximum Current Capability

Thermal management of current in in-package Hall sensors involves several interdependent factors:

- *Lead frame resistance (and shape)*: Variation in lead frame resistance across manufacturing lots directly affects internal power dissipation. Because of different design choices and optimizations across IC manufacturers, this parameter is often not uniform across multi-sourced devices. Choice of fused vs. non-fused lead frame varieties can also affect this value, with fused lead frame options typically performing better at higher current values.
- *PCB copper characteristics*: The copper weight, layer count, and trace volume on the PCB input side significantly influence thermal extraction. These factors determine how effectively heat flows away from the device.
- *External thermal hardware*: Lugs, heat sinks, copper cabling, and the thermal profiles of these components all contribute to the overall thermal path. When these components are not optimized, the components generate additional heat.
- *Cable thermal exposure*: For cables connecting current through the device inputs, the fraction exposed to the elevated thermal environment versus ambient conditions outside that environment affects total heat dissipation.
- *Ambient operating temperature*: The baseline temperature before any current flows establishes the starting point for junction temperature rise.\

JEDEC Thermal Model and The Application to Hall Sensors

The JEDEC thermal model, characterized by R_{θ} parameters, is the industry standard for estimating device temperature points. The most used parameter is $R_{\theta JA}$, which relates ambient temperature to die junction temperature. This parameter simplifies junction temperature estimation: a single ambient temperature measurement allows straightforward calculation of junction temperature under typical conditions. The JEDEC standard characterizes these parameters for a specific reference PCB layout, and any deviation from that layout introduces error in the calculated thermal response.

A critical limitation exists when applying standard JEDEC thermal models to in-package Hall sensors. The JEDEC characterization assumes that die quiescent current dissipation is the dominant heat source in the model. For Hall sensors at high currents, this assumption breaks down: the lead frame power dissipation becomes the primary heat-generating element, and quiescent current contribution becomes negligible by comparison. This shift in dominant heat source causes the thermal response to shift from the standard JEDEC model at high currents.

This behavior is not permanent, and the thermal coefficient will move as power varies in the IC. As current decreases and lead frame power dissipation reduces, the die thermal contribution gradually increases in relative importance. At zero current (quiescent operation), the thermal model converges back to a value more in line with the original JEDEC characterization, like how offset error dominates at low signal levels in an amplifier.

3 Method

For this experiment, a TMCS1143EVM was modified to include the ISOTMP35R sensor in multiple locations for the purposes of gradient measurement and evaluation of options to successfully recreate desired temperatures in application. In addition, a single TMP118 sensor mounted to flex cable was utilized and was affixed via Capton tape directly to the lead frame of the TMCS1143 under examination. The motivation of these multiple sensors is to examine various placements in the application and look for the sensor which most closely follows the lead frame temperature tracked via the TMP118. Figure 3-1 andFigure 3-2 below show an Altium rendered 3D drawing of the printed circuit board top and bottom layers, respectively, whileFigure 3-3 shows the placement of the TMP118 on the lead frame.

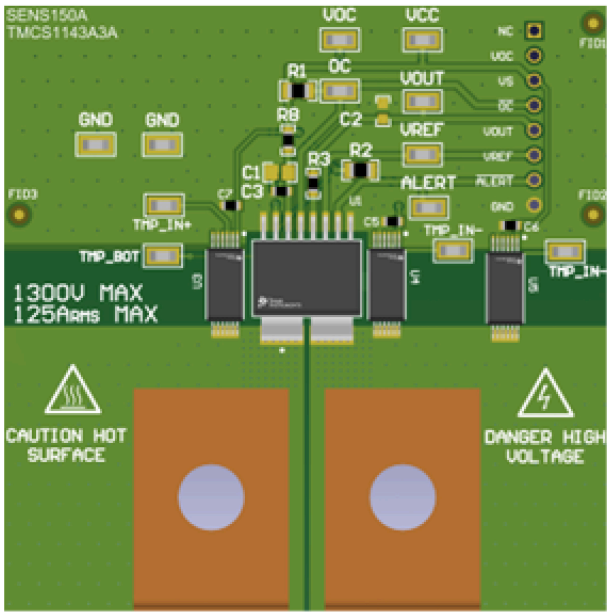

Figure 3-1. Modified TMCS1143EVM, Top View

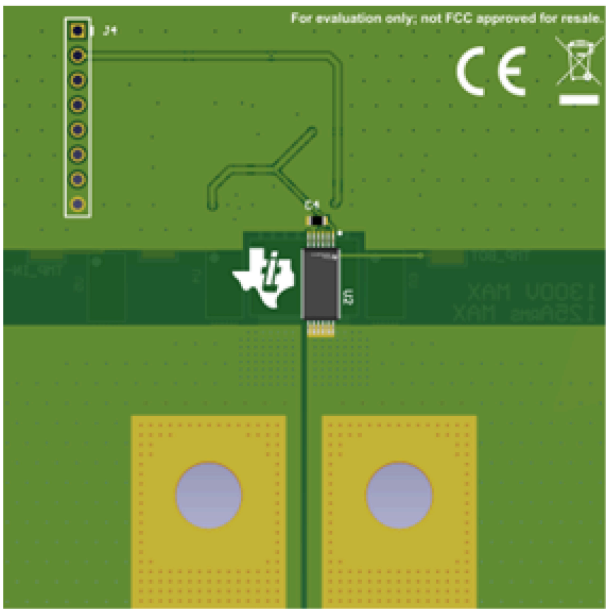

Figure 3-2. Modified TMCS1143EVM, Bottom View

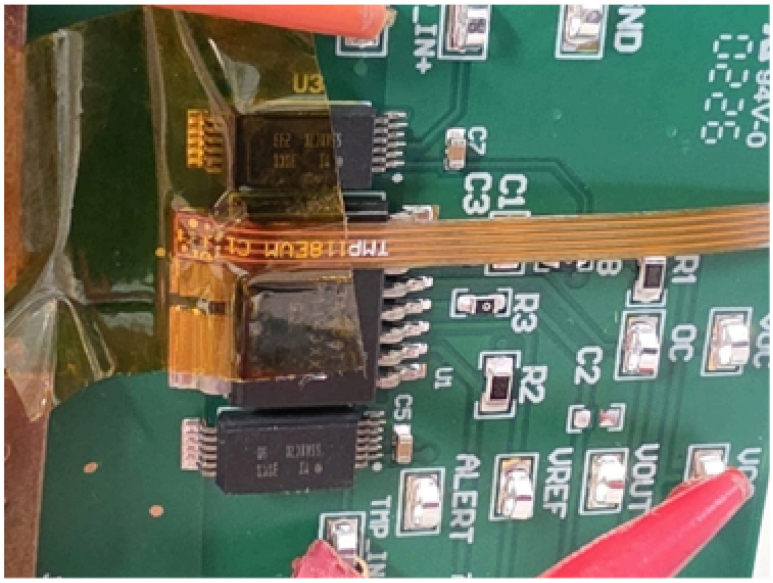

Figure 3-3. TMP118 Flex Cable Placement on PCB

For the current delivery, two Keysight N7971A supplies were utilized in parallel in load sharing mode to create a single supply capable of generating up to 200A of current. Approximately 4ft of 2AWG EastPenn welding cable was implemented for each side of IN+ and IN-, and were run from the mutual output point of the supplies and terminated via Amphenol's 8mm RADSOK quick disconnect system. A second smaller cable set of approximately 1ft (also 2AWG) were then interfaced with the RADSOK set, and terminated to the board inputs via Penn Union SLU125 lugs with standard stainless steel hardware. Each of the ISOTMP35's were measured via Keysight 34401A DMMs in slow 6-digit mode to help noise average measurements. All examinations were performed at either the ambient lab temperature, or in a Test Equity 115A oven at 125°C. This oven was calibrated to ±1°C. It should be noted that the welding cable utilized here is rated to 105°C, and thermal contributions at elevated temperature from these cables likely derated the full potential of the device to some margin in the 125°C, but were chosen for cable flexibility in the system, as this was required for cable management. A system block diagram of this setup is given in Figure 3-4. Junction temperature was measured via internal validation tools through a TI-SCB interfaced with the device to place the device into an internal test mode.

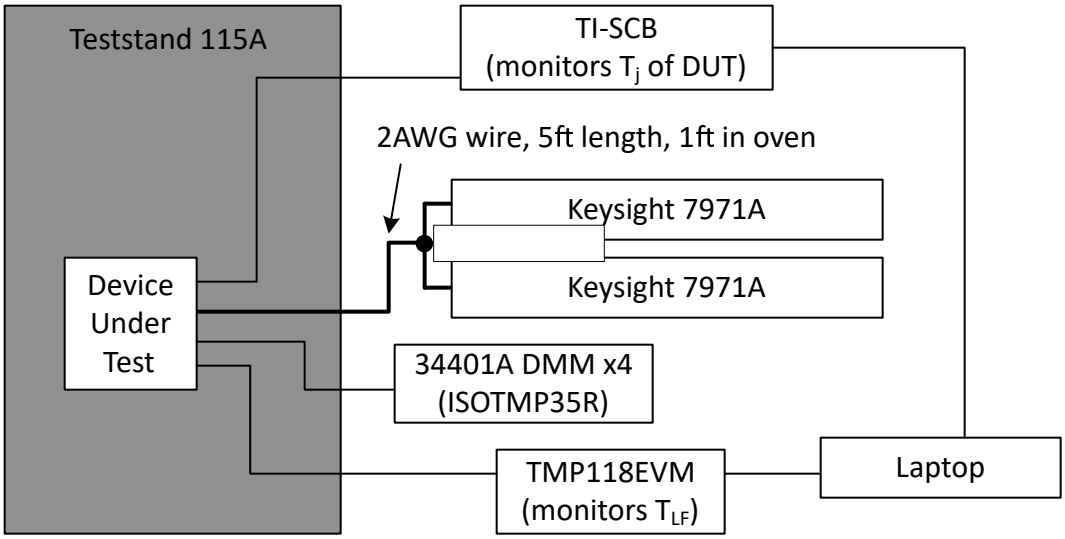

Figure 3-4. Experiment System Block Diagram

4 Results

For each experiment, 3 individual devices were run, and then their results were averaged to provide a typical response for each data point. The results for the room temperature examination are shown in Table 4-1, and the results for the 125°C examination are shown in Table 4-2. Note that the bolded values denote data captures for the TMP118 that are outside of the recommended range in its respective datasheet. While the TMP118 is accurate to ±0.4°C up to 125°C, it was accepted that these measurements may contain additional error above this margin of accuracy. For the ISOTMP35R's, IN+ denotes the sensor adjacent to the TMCS1143 on the IN+ polygon (U3), IN- denotes the device adjacent to the TMCS1143 on the IN- polygon (U4), BOT denotes the device placed beneath the TMCS1143 on the IN+ polygon (U2), and REF denotes the sensor placed on the IN- polygon at a distance from the TMCS1143 (U5).

Table 4-1. Results for Room Temperature Current Sweep

	Current (A)													
	0	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**110**	**125**	**137.33**
ISOTMP35R, IN+	23.51	23.74	24.75	27.11	29.89	33.76	38.39	44.17	50.94	59.27	68.43	79.39	99.07	115.08
ISOTMP35R, IN-	23.70	23.96	25.00	27.42	30.26	34.22	38.83	44.73	51.40	59.85	69.00	80.15	99.57	116.25
ISOTMP35R, BOT	23.64	23.95	24.91	27.42	31.16	35.73	41.18	48.10	56.10	65.92	76.99	90.26	114.08	136.27
ISOTMP35R, REF	23.58	23.76	24.83	27.07	28.85	32.03	35.66	40.36	45.49	52.13	59.07	67.56	81.88	93.46
TMP118 (°C)	24.04	24.39	25.56	28.23	31.47	35.83	41.49	48.02	56.12	64.59	75.85	89.42	113.19	138.41
JUNCTION, TJ (°C)	26.73	27.08	28.56	31.95	35.66	41.02	47.81	55.92	65.48	77.35	91.07	107.34	136.62	164.37
LF Resistance (µΩ)	270	270	270	270	270	270	270	270	270	270	270	270	270	270
LF Power (W)	0	0.027	0.108	0.243	0.432	0.675	0.972	1.323	1.728	2.187	2.7	3.267	4.219	5.092
Power from IQ (W)	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036
Total Power (W)	0.036	0.063	0.144	0.279	0.468	0.711	1.008	1.359	1.764	2.223	2.736	3.303	4.255	5.062

Table 4-2. Results for 125°C Temperature Current Sweep

	Current (A)									
	0	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**85.667**
ISOTMP35R, IN+	121.95	122.22	122.85	124.24	126.19	128.85	132.11	136.11	140.82	143.49
ISOTMP35R, IN-	122.08	122.39	123.27	124.80	127.06	129.83	133.42	137.80	142.99	145.91
ISOTMP35R, BOT	121.97	122.35	123.41	125.26	127.71	131.41	135.78	141.13	147.46	151.09
ISOTMP35R, REF	122.21	122.41	122.92	123.96	125.30	127.21	129.52	132.36	135.71	137.55
TMP118 (°C)	122.79	123.15	124.20	125.98	128.62	132.15	136.51	141.96	148.42	152.02
JUNCTION, TJ (°C)	125.35	125.86	127.34	129.83	133.37	138.15	144.07	151.31	160.00	165.02
LF Resistance (µΩ)	365	365	365	365	365	365	365	365	365	365
LF Power (W)	0	0.0365	0.146	0.3285	0.584	0.9125	1.314	1.7885	2.336	2.679
Power from IQ (W)	0.0363	0.0363	0.0363	0.0363	0.0363	0.0363	0.0363	0.0363	0.0363	0.0363
Total Power (W)	0.036	0.073	0.182	0.365	0.620	0.949	1.350	1.825	2.372	2.715

Examination of the Junction via Current Delivered

The first way junction temperature can be analyzed is through the examination of current over time. For this method, transients of the thermal equation are somewhat ignored, and the steady state values of current are examined against a curve of best fit.Figure 4-1 below demonstrates the thermal effects of various current step responses for a number of current magnitudes is shown in. Note that for most current steps within the range of the TMCS114x, thermal transients are mostly within convergence after 20 minutes.

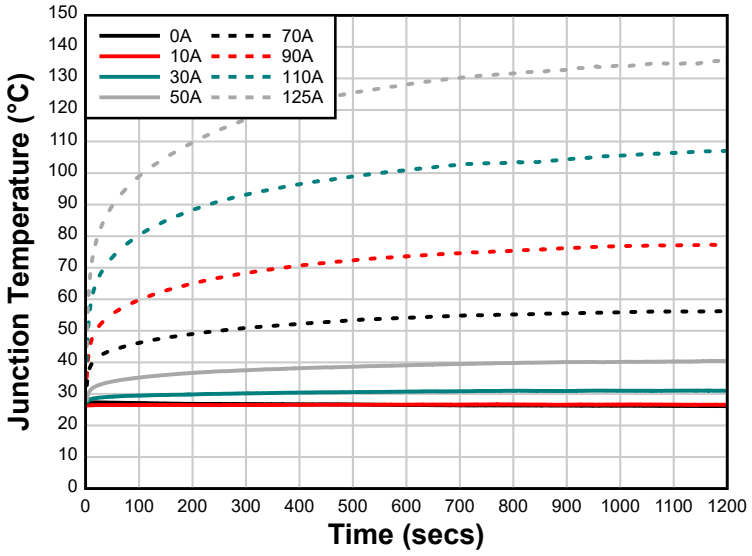

Figure 4-1. Junction Temperature vs. Time for DVF Package on TMCS1143EVM

For each of these curves, once thermal steady state is achieved, the DC value of the internal junction temperature was recorded and plotted in Figure 4-2. A 2nd order curve of best fit (COBF) is also calculated and given in the plot, which allows the designer to easily track typical junction temperature, provided their layout profile is within reason to that of the TMCS1143EVM. This process was also repeated for 125°C, and those results are shown in Figure 4-3.

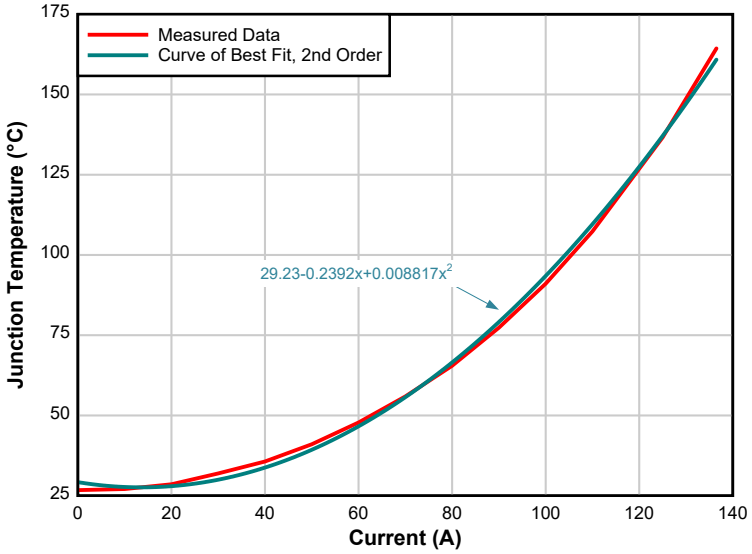

Figure 4-2. Typical Junction Temperature for TMCS114x with COBF, T_A = 25°C

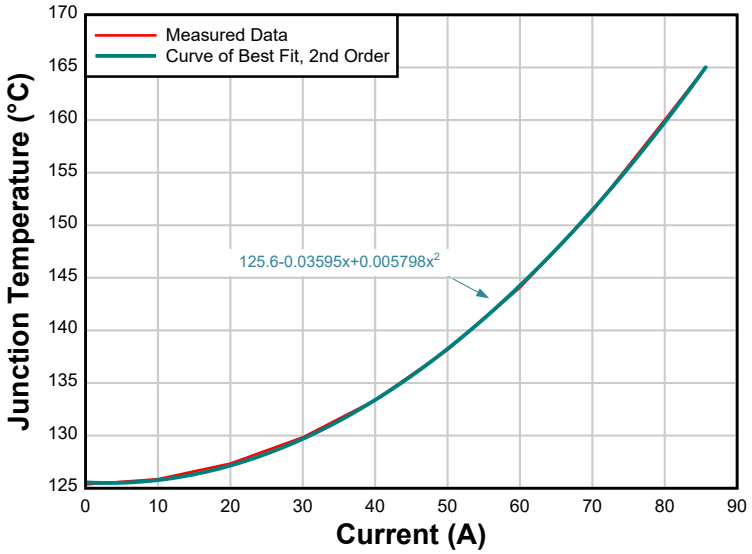

Figure 4-3. Typical Junction Temperature for TMCS114x with COBF, T_A = 125°C

An in depth look at this method with additional data plots for both DVG and DVF packages is also delivered in Thermal Analysis of the TMCS1123 Hall-Effect Current Sensor .

Examination of the Junction via Ambient and Lead Frame Conditions

With the measurements captured in Section 4, everything needed to analyze the thermal transfer characteristics between the junction and either ambient temperature or the lead frame can be executed. From the stance of input power, we have two signatures we need to analyze: the quiescent current of the part, and the power developed on the lead frame.

The power delivered from the quiescent current will be relatively static in nature. However, this value can change either with variance to the supply voltage, or the distribution of I_Q given in the datasheet**.** The tabular values in Tables 1 and 2 are calculated values, based on the provided 3.3V supply, and the typical value of 11mA of I_Q given in the datasheet.

The power delivered from the lead frame must also be adjusted. For the room temperature test, the standard value of 270μΩ is utilized across all values of current. For the 125°case, however, the input conductor resistance temperature drift must also be accounted for, adding an additional 95 μΩ to the resistance for a total of 365 μΩ at the elevated temperature. For each of these values, power developed in the lead frame is then calculated by the standard formula of

$$P_{LF} = I_{LF} \times R \quad (1)$$

These values were summed and applied to the standard JEDEC model to observe how the value of the coefficient changes as additional power is generated in the lead frame. Figure 4-4 shows the observations of the junction against measured ambient temperature, calculated by the equation

$$T_J = T_A + R_{\theta JA} \times \left(P_{LF} + P_{IQ}\right) \quad (2)$$

and Figure 4-5 shows the observations of the junction against the measured lead frame, utilizing the equation

$$T_J = T_{LF} + R_{\theta JLF} \times \left(P_{LF} + P_{IQ}\right) \quad (3)$$

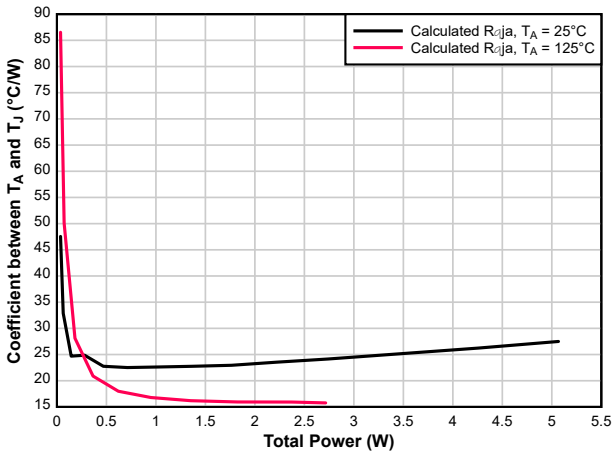

Figure 4-4. Calculated $R_{\theta JA}$ vs. Total Power, 25°C and 125°C

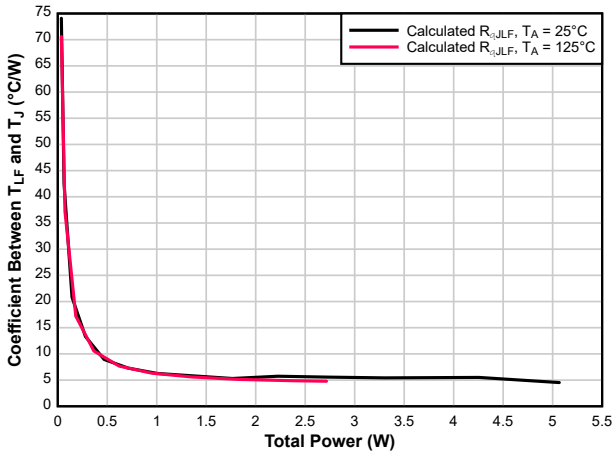

Figure 4-5. Calculated $R_{\theta JLF}$ vs. Total Power, 25°C and 125°C

It can be observed that for both gradients, the predicted behavior emerges: at a value of around 1W of total dissipation, the system converges to a new linear set of values consistent with a majority of the power being generated in the lead frame, and for values less than 1W, the coefficient loses linearity, and exhibits an inverse relationship. This is due to the leadframes delivered power no longer being large enough in magnitude to neglect the static power produced by the quiescent current. It can be observed that as power produced in the leadframe tends toward zero, for the ambient curves, the coefficient asymptotically converges to a value relatively similar in nature to that of the original $R_{\theta JA}$ **.** The differences in the separate coefficients is attributed to location: the power from I_Q is generated in the silicon itself, and therefore has a much more drastic effect on the junction over that of the heat from the leadframe, which sits physically farther away in the package.

For the ambient curve, it is observed that while both 25°C and 125°C curves converge to relatively static value, they do not converge together. This is likely due to the complex nature of ambient temperature here, and the simplistic approach of using the standard laboratory temperature for room temperature experiments. Micro-level changes to the actual ambient temperature in proximity to the part due to its own self-heating likely complicate this problem.

The far more interesting curve from these measurements is the correlation of coefficient between the lead frame and the junction temperature. In both 25°C and 125°C cases, the yielded curve is nearly identical, converging to an average value of 5°C/W for the evaluation module. This independence in the temperature demonstrates that, should the designer be able to accurately measure the lead frame temperature, then the junction temperature should be able to be estimated independent of ambient temperature. Examining the results across the various ISOTMP35's utilized during the process, the device populated on the bottom of the board shows that, in nearly all cases, leadframe measurement can be measured accurately to within 1.5°C, as shown in Figure 4-6.

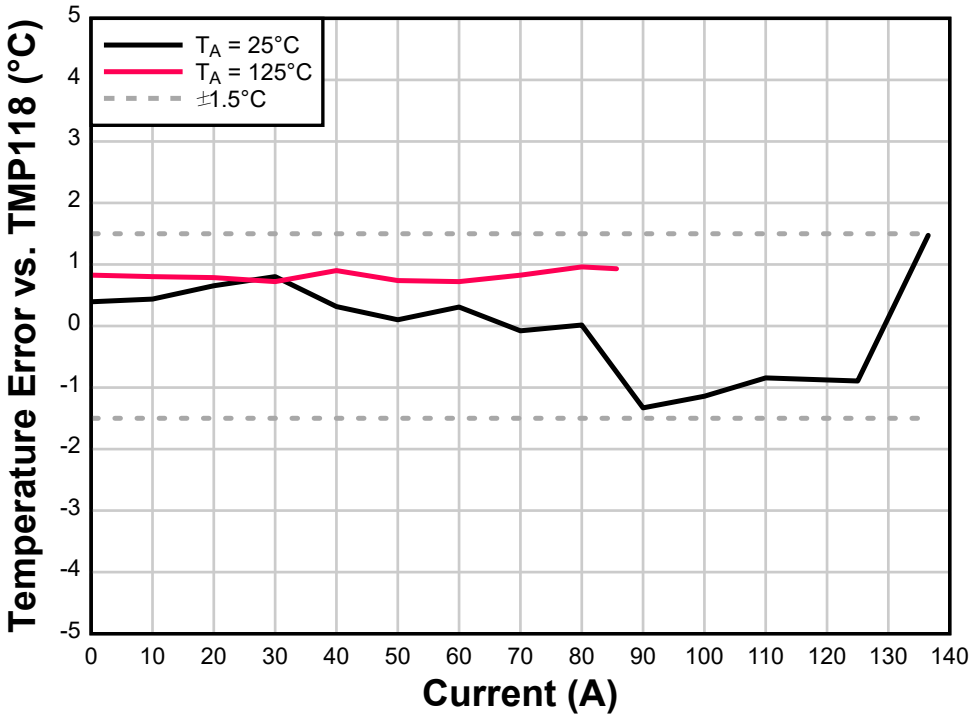

Figure 4-6. ISOTMP35R vs. Lead Frame Reference Temperature Error over Current Range

5 Summary

The rapid rise in power density and the concomitant shrinkage of PCB copper volume have created a demanding thermal environment for in-package Hall-effect current sensors such as the TMCS114x series. While the traditional JEDEC-based $R_{\theta ja}$ model provides a convenient first-order estimate of junction temperature, it assumes that die quiescent power is the dominant heat source. The measurements in this paper demonstrate that, at the currents typical for these devices, power dissipated in the lead frame quickly overtakes quiescent dissipation and fundamentally changes the thermal response. Consequently, reliance on a single ambient-temperature measurement can lead to significant errors when the layout or copper distribution deviates from the reference board used to generate the JEDEC parameters.

By directly monitoring the lead-frame temperature with an isolated temperature-sensor IC such as ISOTMP35R, a robust alternative method for estimating junction temperature can be achieved. The data shows a linear relationship between lead-frame temperature rise and junction temperature with an effective thermal resistance of approximately **5 °C/W**, a value that remains consistent across both room-temperature (25 °C) and elevated-temperature (125 °C) environments.

Overall, the study validates that a lead-frame-centric thermal model, supported by direct temperature measurement offers a more accurate and design-friendly approach for assessing safe operating limits of TMCS114x Hall-effect sensors in high-density power applications. Future work could extend this methodology to other package types, alternate volumes and weights of copper polygons, and explore active thermal-compensation techniques that leverage the measured lead-frame temperature for dynamic current-limit enforcement.

6 References

1. Texas Instruments, *Semiconductor and IC Package Thermal Metrics*, application note.
2. Texas Instruments, *Thermal Analysis of the TMCS1123 Hall-Effect Current Sensor*, application note.

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Last updated 10/2025