Application Brief

Top Design Questions about Ground-Level Translators

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Introduction

This application brief reviews common design questions related to ground-level translators. The goal of this document is to improve overall understanding of how these devices operate in real-world systems.

What are the differences between ground-level translators and digital isolators?

Digital isolators are a galvanic-based solution optimized for high-voltage systems that provide several safety features, such as high CMTI, EMC robustness, and regulatory certifications. While essential for device protection, this level of isolation is generally unnecessary when simply translating digital signals between different ground potentials. Ground-level translators (TXG product family) were developed to bridge the gap in separating DC and AC ground offsets while providing a reduced solution size and improved switching performance. Ground-level translators and digital isolators serve different purposes depending on system requirements such as isolation, size, speed and leakage performance.Table 1 lists the differences between the two devices.

Table 1. Differences between Ground-Level Translators and Digital Isolators

	Ground-Level Translators	Digital Isolators
GNDA to GNDB Difference	80V	3kVrms
Galvanic Barrier	No	Yes
GNDA to GNDB Leakage (VCC to GND Shorted)	70nA	<1nA
Size (4-Channel)	4mm^2	29.4mm^2
Propagation Delay (3.3V)	5.8ns	18.5ns
Ch-Ch Skew (3.3V)	0.35ns	4.7ns
Data Rate	>250Mbps	100Mbps
Level Shifting Capability	1.71 to 5.5V	1.71 to 1.89V and 2.2 to 5.5V
Operating Temperature	-40C to 125C	-40C to 125C
CMTI	1kV/us	100kV/us
Certification (UL, VDE, Surge)	No	Yes
EMC (EFT, RI, IEC-ESD)	No	Yes

Can a negative PWM signal be generated from a positive PWM signal?

A negative PWM signal can be generated using a ground-level translator if the system includes a negative supply rail. To prevent device damage, the voltage difference between VCC and GND must remain within the recommended operating conditions.

In Figure 1, VCC and GND for both the A-port and B-port fall within allowable limits. As a result, the output toggles between VCCB and GNDB, which in this case corresponds to 0V and -4V.

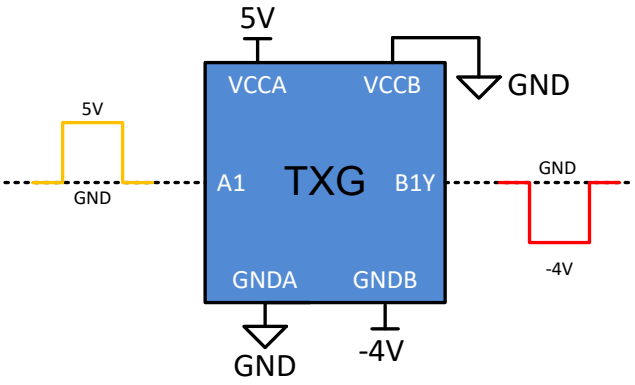

Figure 1. TXG Outputting Negative PWM Signal

Using the same conditions on TXG8041, the output waveform (pink) toggles between GND and -4V as seen in Figure 2

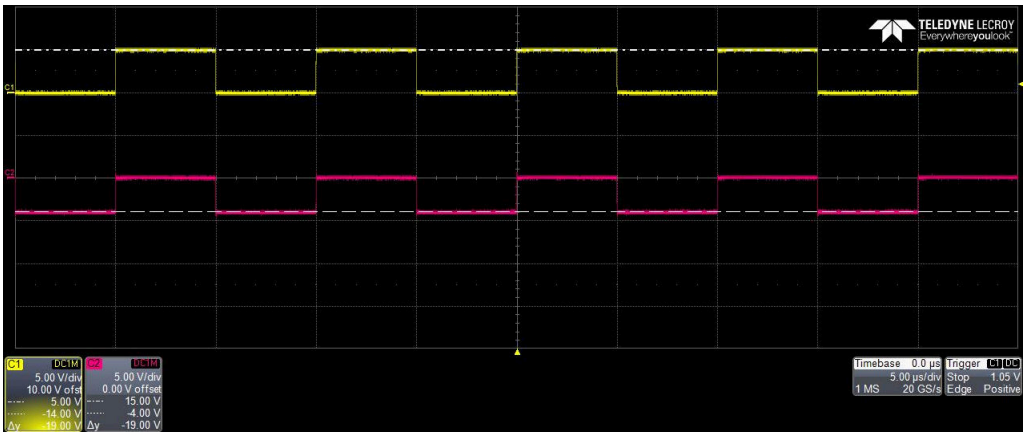

Figure 2. Waveform Capture of Negative PWM Signal

Is DC ground shifting possible when both supplies are connected together?

Ground shifting requires the voltage supplies to be separated and to remain within the recommended operating conditions.

In Figure 3 (a), GNDB shifts by -5V due to parasitic effects while A-side remains within the device limits. However, B-side exceeds its supply-to-ground absolute maximum rating. To avoid this condition, TI recommends that both supplies and their respective grounds remain separated from each other as shown on Figure 3 (b).

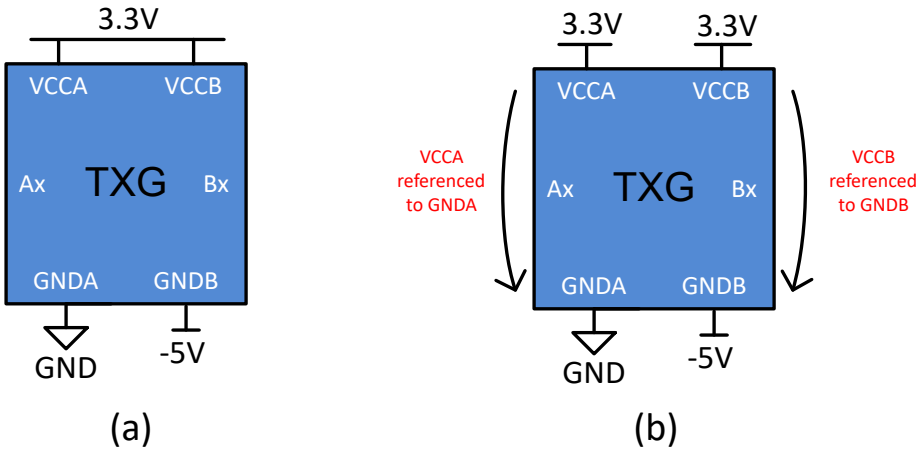

Figure 3. Incorrect Setup (a), Supplies and respective ground remain separated (b)

Can TXG be used as a simple level translator and buffer?

The TXG product family can be used as a standard level translator (VCCA > VCCB or VCCA < VCCB) or in a buffer configuration when VCCA equals VCCB.

If ground shifting is not required but high data rate and low output skew are important, GNDA and GNDB can be tied together.

If ground shifting is required, VCCA/GNDA and VCCB/GNDB must remain separated, as shown in Figure 4.

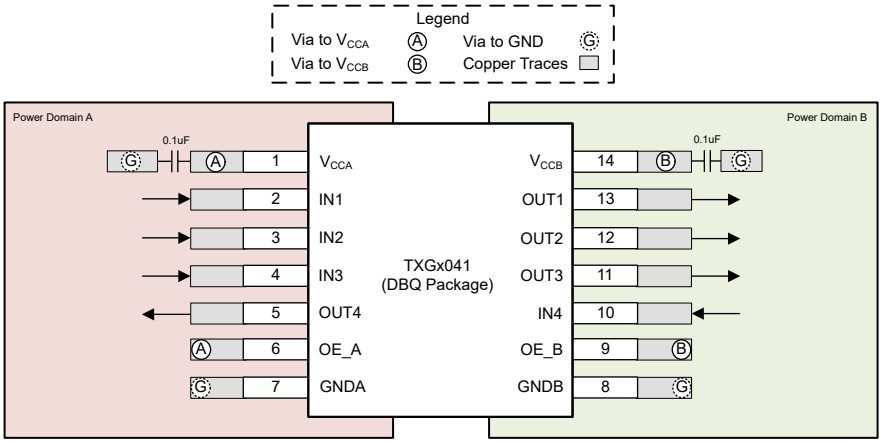

Figure 4. Separated Power Domains on TXG

What is the leakage between two grounds?

The leakage between two grounds is specified in the Electrical Characteristics section in the device datasheet.

Table 2 shows the ground-to-ground leakage values of TXG1041

Table 2. Ground-to-Ground Leakage

Test Condition	VCCA	VCCB	TYP
All channels combined (VCC and GND shorted)	1.71V - 5.5V	1.71V - 5.5V	28nA
All channels combined (VCC both sides are powered on and inputs are all low)	1.71V - 5.5V	1.71V - 5.5V	28nA
All channels combined (VCC both sides are powered on and inputs are all high)	1.71V - 5.5V	1.71V - 5.5V	33nA

How far apart can two systems be when using ground-level translator devices?

Open-Drain Architecture

For I2C applications, the allowable distance between systems is primarily limited by total bus capacitance. The I2C specification limits bus capacitance to 400pF for Standard and Fast Mode, and 500pF for Fast mode Plus. These same limitations apply when using devices such as TXG8122-Q1.

Total bus capacitance is determined by two main factors:

1. **Input Capacitance** - Each SDA and SLC pin contributes ~5pF. While this is minimal for a single device, the total input capacitance increases as additional peripherals are added to the bus.
2. **Cable Capacitance** - A common rule of thumb is approximately 1pF per centimeter of cable length. Under Standard Mode operation, this limits cable lengths to approximately four meters (13 feet).

To support higher capacitive loads, TI recommends TXG8122-Q1 Side 2 (SDA2 and SCL2) with all other I2C peripherals

Push-Pull Architecture

For push-pull architectures such as SPI, the allowable distance depends on the output drive capability of the signal source.

For example, if the microcontroller (signal source) has a high output drive strength, the ground-level translator does not need to be placed next to the source. Instead, the translator may be placed closer to the receiver.

If the microcontroller has limited output capability, TI recommends placing the ground-level translator close to the driver. This allows the translator to use the output drive capability to re-drive the signal over longer distances.

Can unused input pins be left floating on ground-level translators?

For standard logic and level translator devices, it is not recommended to leave input pins floating. Unused inputs should instead be tied to a defined logic level, either VCC or GND, to prevent unintended switching and excess in-rush current.

However, push-pull versions of ground-level translators feature an integrated pull-down resistor on each input pin (typically 5MΩ). As a result, unused input pins do not need to be externally tied to a defined logic level. The internal pull-down resistor forces the input to a logic low-state, which in turn drives a logic low level at the corresponding output.

Conclusion

This document went over the top design questions that have been received to date. If additional clarification is needed or if new questions arise, submit a thread on the TI E2E™ Community forum. As frequently asked questions are received, this document is updated accordingly.

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