

4222143/A 08/2015

NOTES:

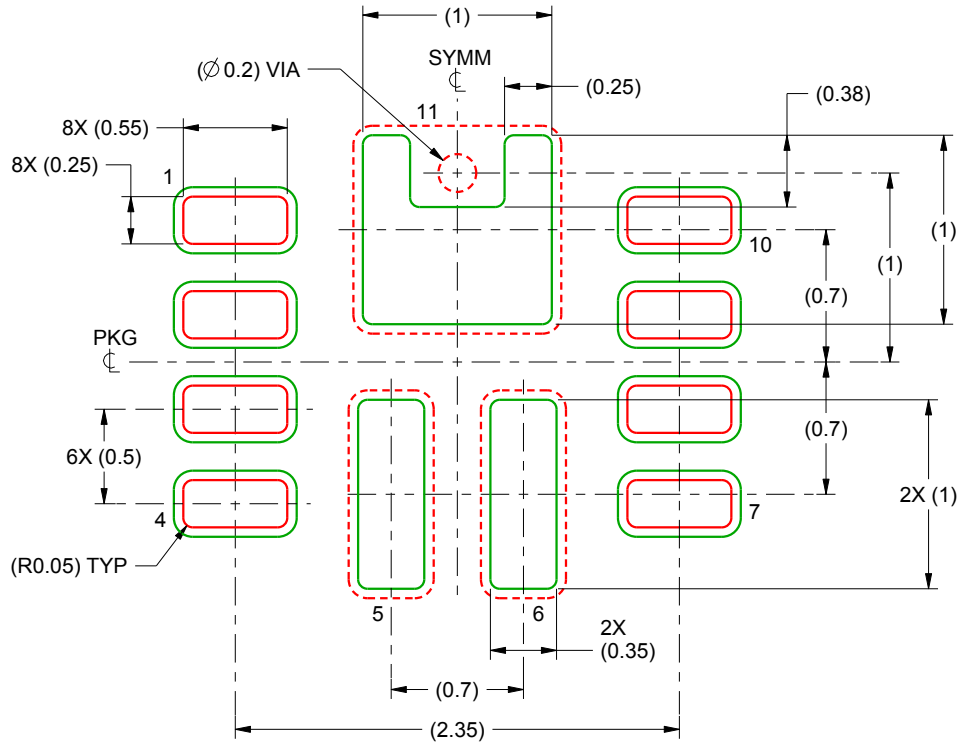
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

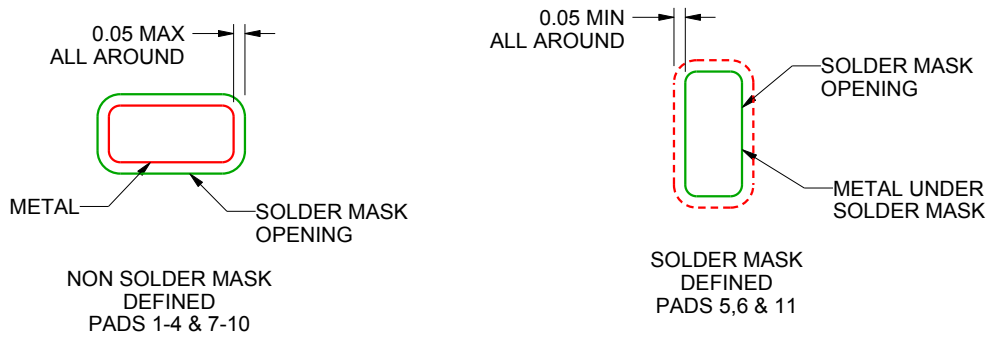
RNR0011A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

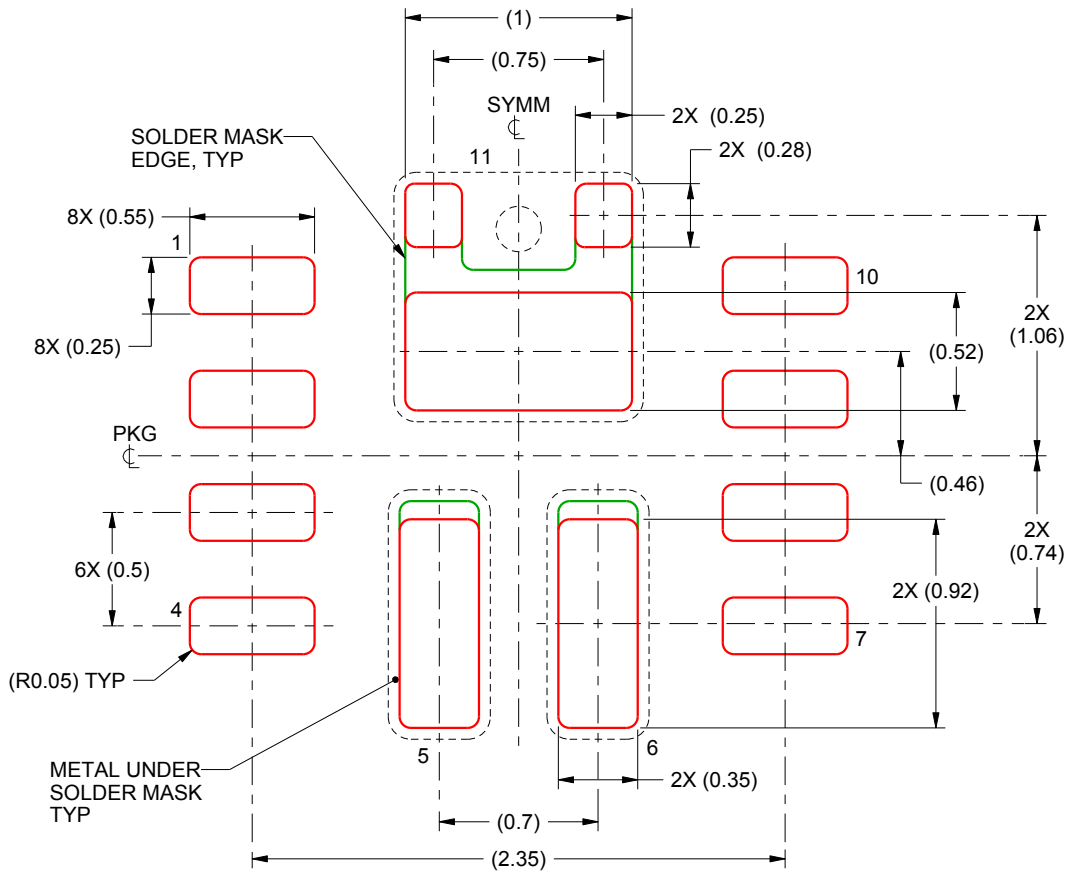
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RNR0011A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 PADS 5 & 6: 90% - PAD 11: 79%
 SCALE:30X

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NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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