TI Designs：TIDEP-01002
成本经优化的数字仪表组汽车参考设计 (DCARD)，配备 Jacinto™ 汽车处理器

说明

Jacinto™基于 DRA71x 的数字仪表组汽车参考设计 (DCARD) 是一种用于可重构数字仪表组系统的成本优化型设计。DCARD 是一种完整的自包含式 6 层 PCB 设计，可在 1920 × 720 分辨率的显示器上实现 60fps 数字仪表组解决方案，同时可优化整体系统物料清单 (BOM)。该设计面向 多种应用， 例如：可重构数字仪表组、具有动态图形的混合仪表组、抬头显示以及驾驶员识别和监控。

资源

TIDEP-01002	设计文件夹
DRA71x 信息娱乐 应用处理器	产品文件夹
DS90C189-Q1	产品文件夹
TAS2505	产品文件夹
TCAN1043-Q1	产品文件夹
DP83TC811R-Q1	产品文件夹

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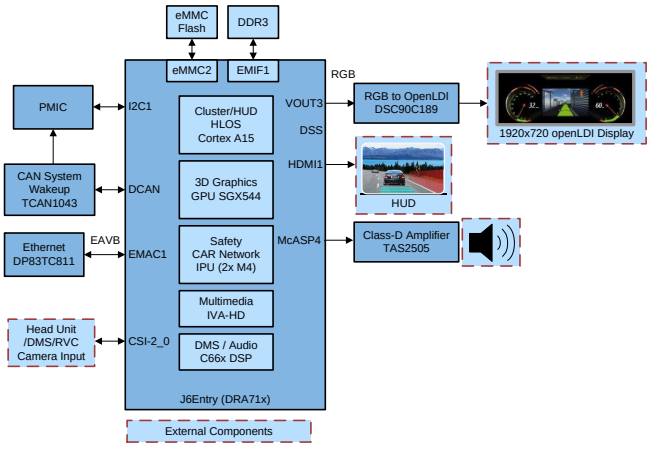
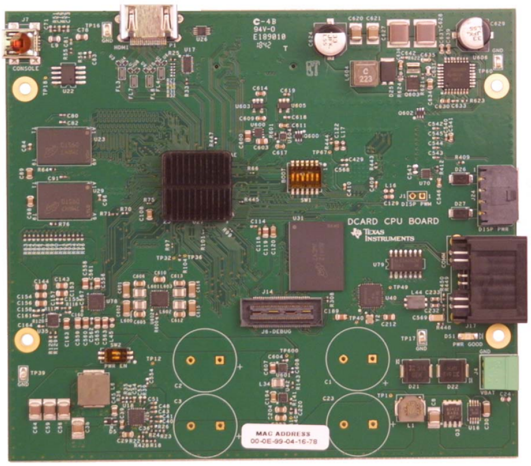
特性

- 采用 Jacinto™ DRA71x 汽车处理器在 1920 × 720 分辨率的仪表组显示器上渲染和驱动 60fps 仪表组图形
- 经优化的 德州仪器 (TI)™电源管理解决方案（包括 LM87523 和 LM5141）
- 使用 DSC90C189 串行器支持 OpenLDI 仪表组显示
- 使用 TAS2505 D 类放大器支持单区音频输出
- 采用 TCAN1043 CAN 收发器从 CAN 唤醒
- 利用 DP83TC811 Phy 支持以太网
- 采用 CSI-2 摄像头输入进行后视或驾驶员监控摄像头的集成
- 通过 HDMI 接口次级显示输出实现 HUD 集成
- 采用 6 层 PCB 设计最大限度缩减系统 BOM

应用

- 可重构的数字仪表组
- 具有动态图形的混合仪表组
- 抬头显示
- 驾驶员监控和识别





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1 System Description

The Jacinto™ DRA71x-based digital cluster automotive reference design (DCARD) is a cost-optimized design for reconfigurable digital cluster systems. DCARD is a complete and self-contained 6-layer PCB design to enable 60 fps digital cluster solutions on 1920 × 720 resolution displays while optimizing overall system BOM. DCARD also supports single zone audio output for warning chimes, wake-up from CAN, and Ethernet connectivity. Additional functionality can be added based on end-product requirements. For example, camera input is available to integrate rear-view camera or driver monitoring and second display output can be used to drive heads-up-display (HUD). System power management is optimized to minimize overall system BOM for reconfigurable digital cluster use-case. This design targets applications such as reconfigurable digital cluster, hybrid clusters with active graphics, heads-up display, and driver identification and monitoring.

2 System Overview

2.1 Block Diagram

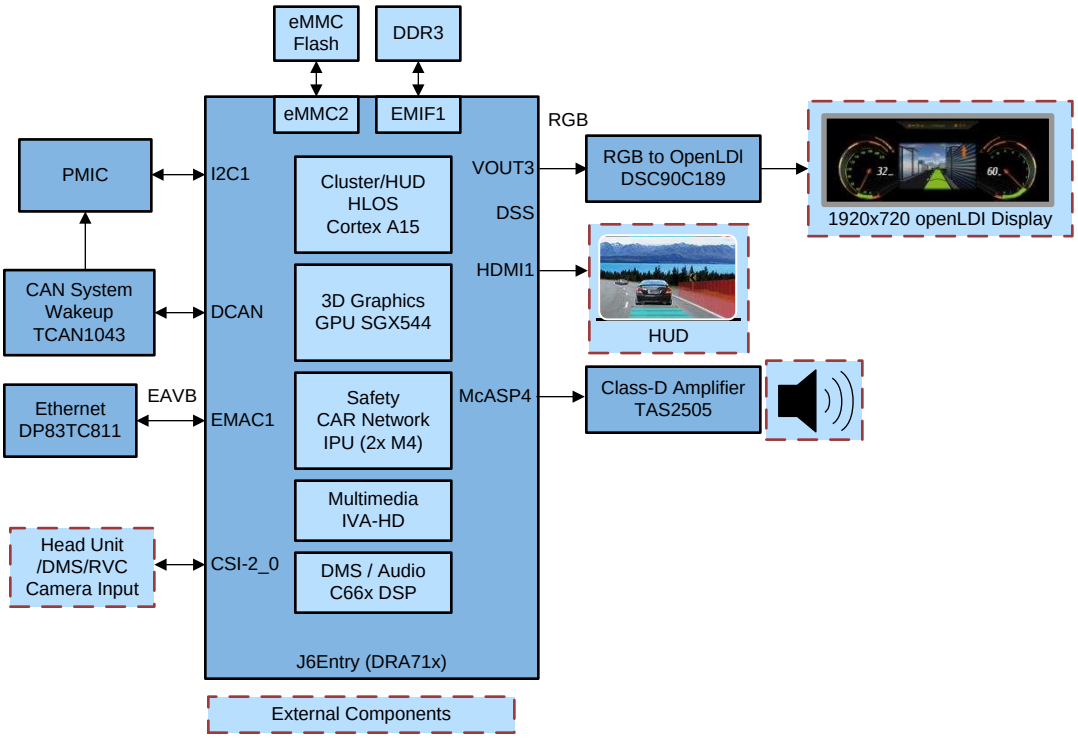

图 **1. TIDEP-01002 Block Diagram**

2.2 Design Considerations

2.2.1 DRA71x Automotive Processor

This reference design uses the DRA71x automotive processor to render 3D cluster graphics at 60 fps and to drive the 1920 × 720 digital cluster display. It handles all the peripheral inputs and to deliver the outputs to the respected ports. The DRA71x automotive processor also integrates C66x DSP that can be used to integrate driver monitoring and identification functionality. The device features a simplified power supply rail mapping, which enables lower cost PMIC solutions.

2.2.2 Power Architecture

This reference design has optimized power architecture. The input to the design can be a 12-V power source similar to a car battery. Details of power stages are illustrated in the following figures.

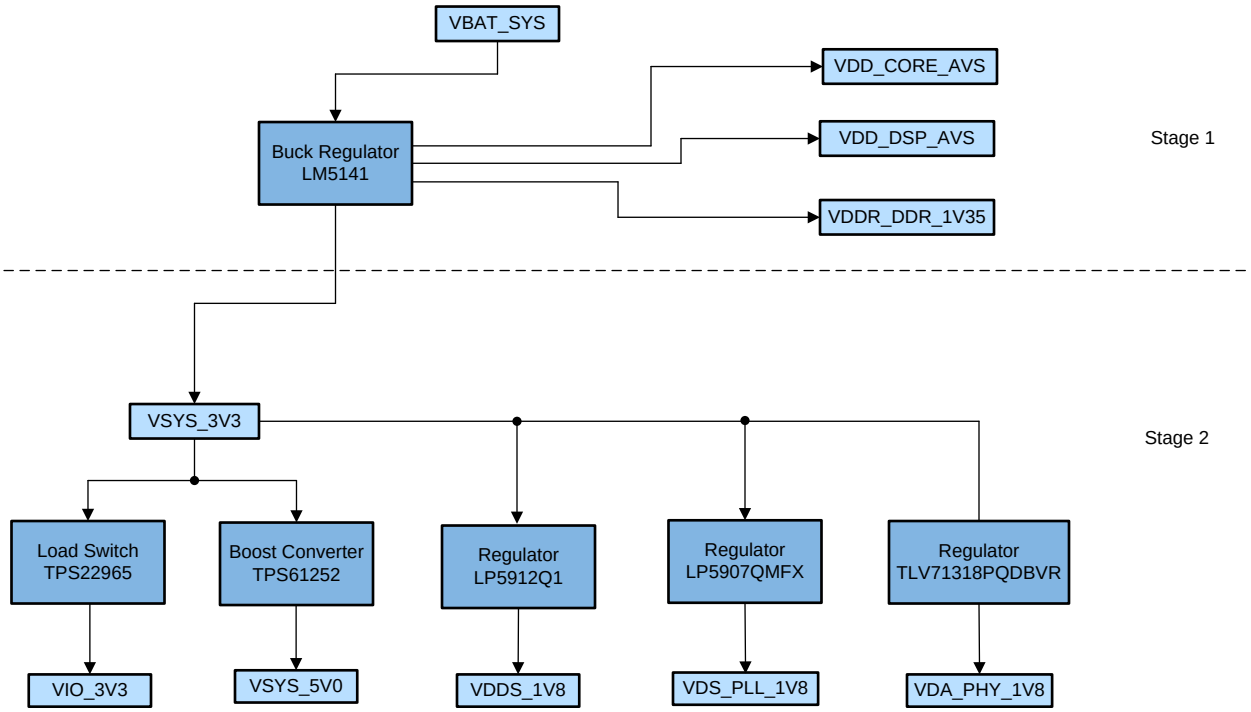

图 2. Stage1 and Stage 2 Power Infrastructure Block Diagram

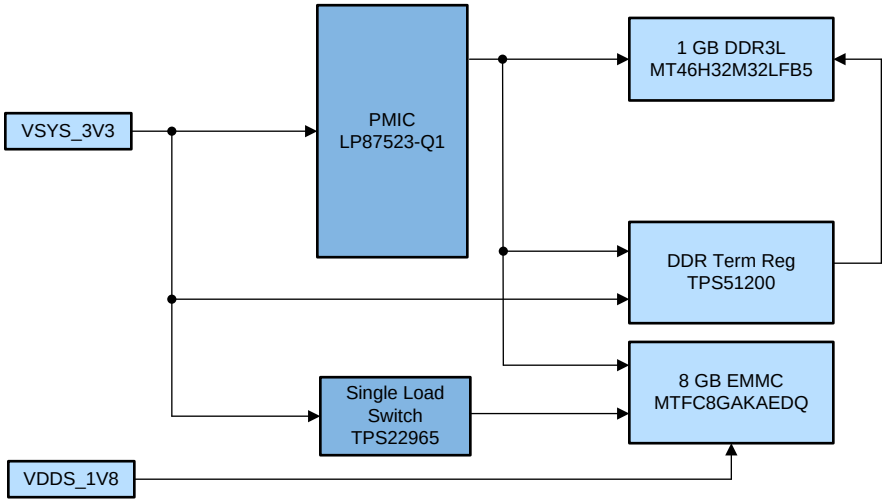

图 3. Memory Power Block Diagram

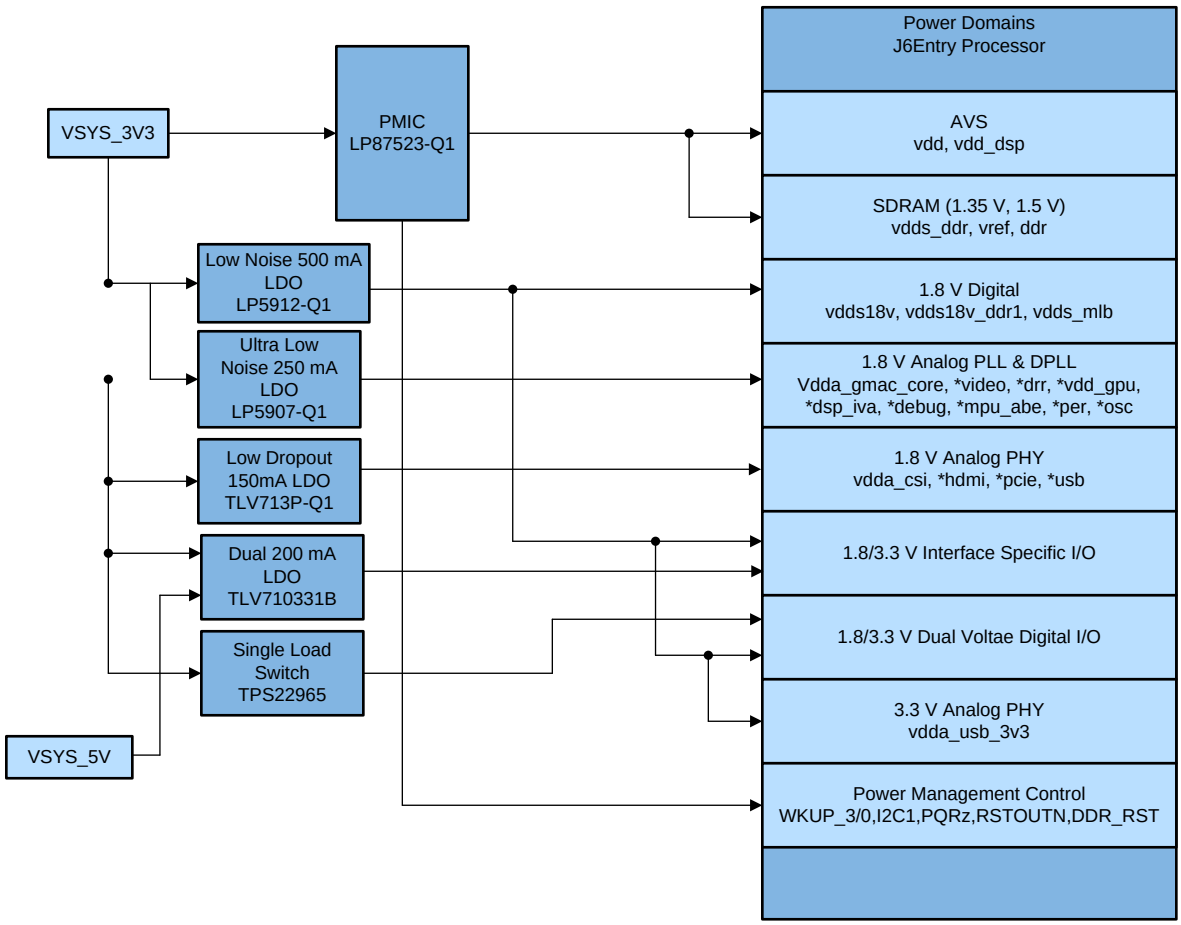

图 4. Processor Power Block Diagram

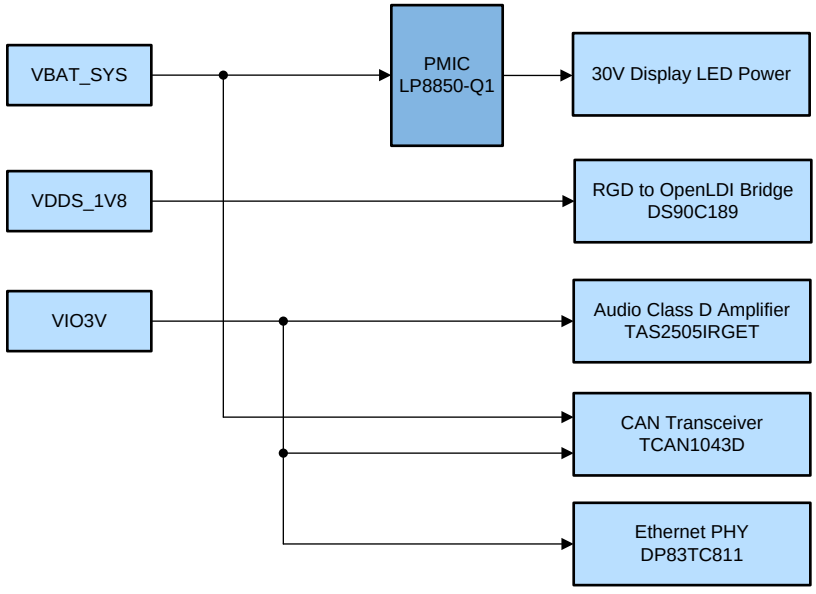

图 5. Active Power Block Diagram

2.2.3 Display

This reference design supports dual display output: cluster display and HUD display. Cluster display is a 1920 × 720 OpenLDI LCD display, and the DRA71x automotive processor renders 60 fps cluster graphics. An optional HUD output is available through an HDMI interface.

2.2.4 Class-D Audio Amplifier

This reference design supports single zone audio output for warning chimes with a TAS2005 Class-D amplifier. The TAS2505 device is a low-power digital input speaker amp with support for 24-bit digital I2S data mono playback. The outputs are placed on the design to connect speakers.

2.2.5 OpenLDI Serializer

This reference design uses a DSC90C189 serializer to convert RGB output from the DRA71x automotive processor to dual OpenLDI output to drive the cluster display at 1920 × 720 resolution. The DS90C189-Q1 is a low-power bridge for automotive applications that reduces the size of the RGB interface between the host application processor and the display.

2.2.6 CAN

This reference design supports CAN interface using a TCAN1043. This reference design also enables wake-up from CAN and Wake Input using a TCAN1043 Transceiver.

2.2.7 Ethernet

Ethernet interface is supported on this reference design to enable content from other subsystems such as navigation content from a head-unit to be displayed on the cluster display. A DP83TC811R-Q1 Ethernet Phy is used to interface with the DRA71x automotive processor where content sent over the Ethernet interface is processed.

3 Highlighted Products

This reference design features the following TI™ devices. Refer to the corresponding data sheets for additional information.

- DRA71x Infotainment Applications Processor
- DS90C189-Q1
- TAS2505
- TCAN1043-Q1
- DP83TC811R-Q1

3.1 DRA71x Infotainment Applications Processor

The DRA71x architecture is designed to deliver high-performance concurrences for automotive applications in a cost-effective solution, which provides full scalability from the Jacinto™ DRA7x family of infotainment processors including graphics, voice, HDMI, multimedia, and smartphone projection mode capabilities.

Programmability is provided by a single-core Arm® Cortex®-A15 RISC CPU with Neon extensions and a TI™ C66x VLIW floating-point DSP core. The Arm® processor allows developers to keep control functions separate from other algorithms programmed on the DSP and coprocessors, which reduces the complexity of the system software.

- Video, image, and graphics processing support:
  - Full-HD video (1920p × 1080p, 60 fps)
  - Multiple video input and video output – 2D and 3D graphics
- Arm® Cortex®-A15 microprocessor subsystem
- C66x floating-point VLIW DSP
- DDR3/DDR3L memory interface (EMIF) module

3.2 DS90C189-Q1 Dual Pixel FPD-Link (LVDS) Serializer

The DS90C189-Q1 is a low-power bridge for automotive applications that reduces the size of the RGB interface between the host GPU and the Display.

- AEC-Q100 Qualified for Automotive Applications
- 150 mW Typical Power Consumption at 185 MHz (SIDO mode)
- Drives QXGA and WQXGA Class Displays
- Two Operating Modes:
  - Single Pixel In, Single Pixel Out (SISO): 105 MHz Maximum
  - Single Pixel In, Dual Pixel Out (SIDO): 185 MHz Maximum
- Supports 24-Bit RGB
- 64-Pin VQFN Package (small 9 mm × 9 mm × 0.9 mm)

3.3 TAS2505 Class-D Amplifier

The TAS2505 device is a low-power digital input speaker amp with support for 24-bit digital I2S data mono playback.

- Digital Input Mono Speaker Amp
- Supports 8-kHz to 96-kHz Sample Rates
- Mono Class-D BTL Speaker Driver (2 W into 4 Ω or 1.7 W into 8 Ω)
- Mono Headphone Driver
- Two Single-Ended Inputs With Output Mixing and Level Control
- Embedded Power-On-Reset
- Integrated LDO
- Programmable Digital Audio Processing Blocks for Bass Boost, Treble, EQ With up to Six Biquads for Playback
- 24-Pin VQFN Package (4 mm × 4 mm)

3.4 TCAN1043-Q1 CAN Transceiver with CAN FD and Wake Input

The TCAN1043xx-Q1 meets the physical layer requirements of the ISO 11898–2 (2016) High-Speed Controller Area Network (CAN) specification providing an interface between the CAN bus and the CAN protocol controller. These devices support both classical CAN and CAN FD up to 2 megabits per second (Mbps).

- AEC Q100: Qualified for Automotive Applications
- Meets the Requirements of the ISO 11898-2 (2016)
- Three Operating Modes:
  - Normal Mode
  - Standby Mode with INH Output and Local and Remote Wake up Request
  - Low-Power Sleep Mode with INH Output and Local and Remote Wake up Request

3.5 DP83TC811-Q1 Automotive Ethernet PHY

The DP83TC811-Q1 is a single-port automotive Ethernet PHY compliant to IEEE802.3bw. The device provides all physical layer functions required to transmit and receive data over single twisted-pair cables. Additionally, the DP83TC811-Q1 provides flexibility to connect to a MAC through a standard MII, RMII, RGMII, and SGMII.

- Qualified for automotive applications
- Low active power: 3.3 V VDDA/VDDIO
- Configurable I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- Power saving features

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware

Front and back views of DCARD hardware are shown in 图 6 and 图 7.

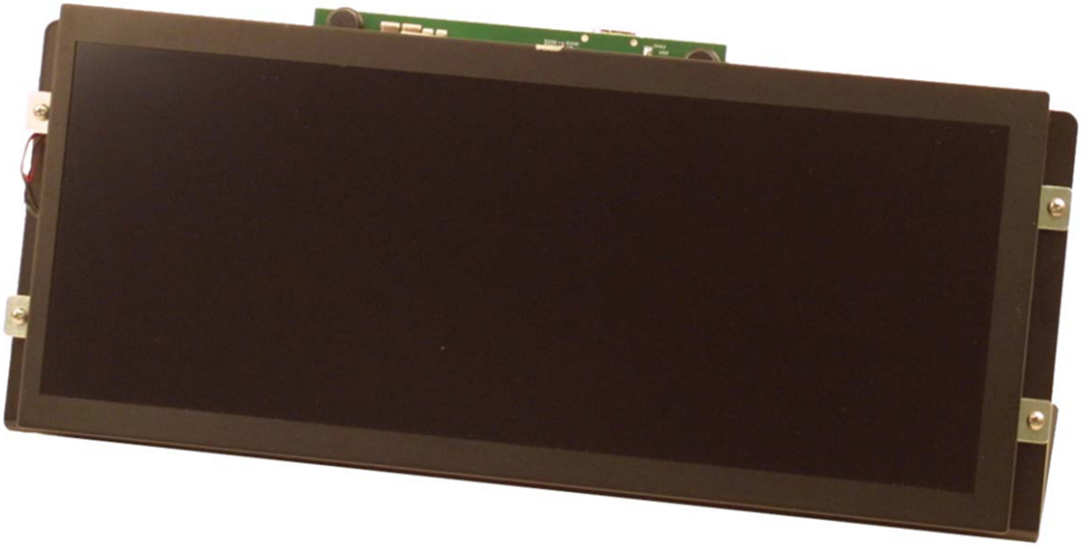

图 **6. DCARD Front View**

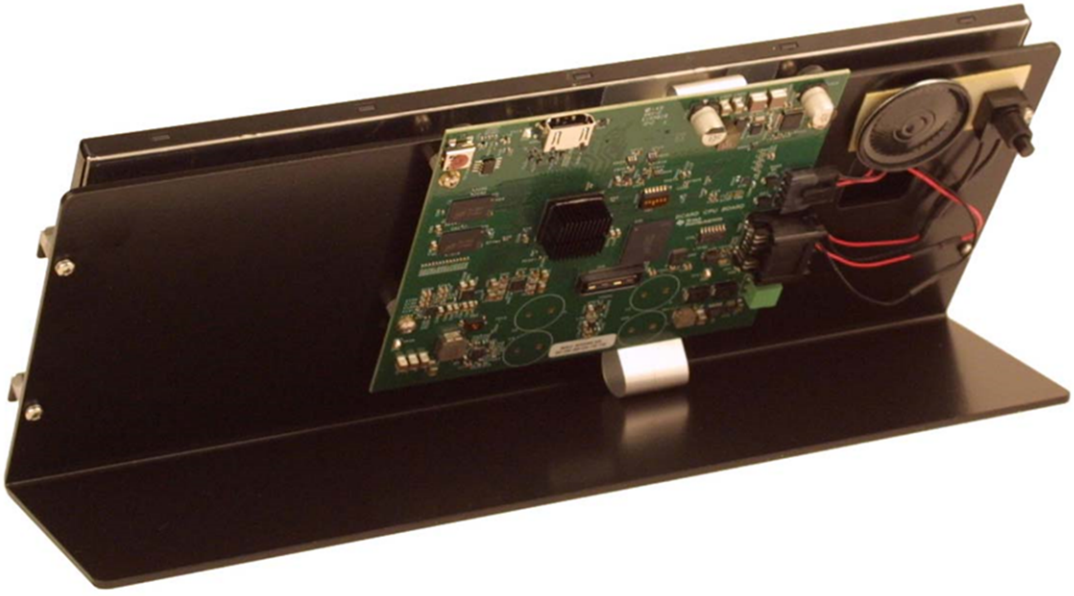

图 **7. DCARD Back View**

4.1.1 Interfaces

图 8 shows and 表 1 describes the DCARD interfaces.

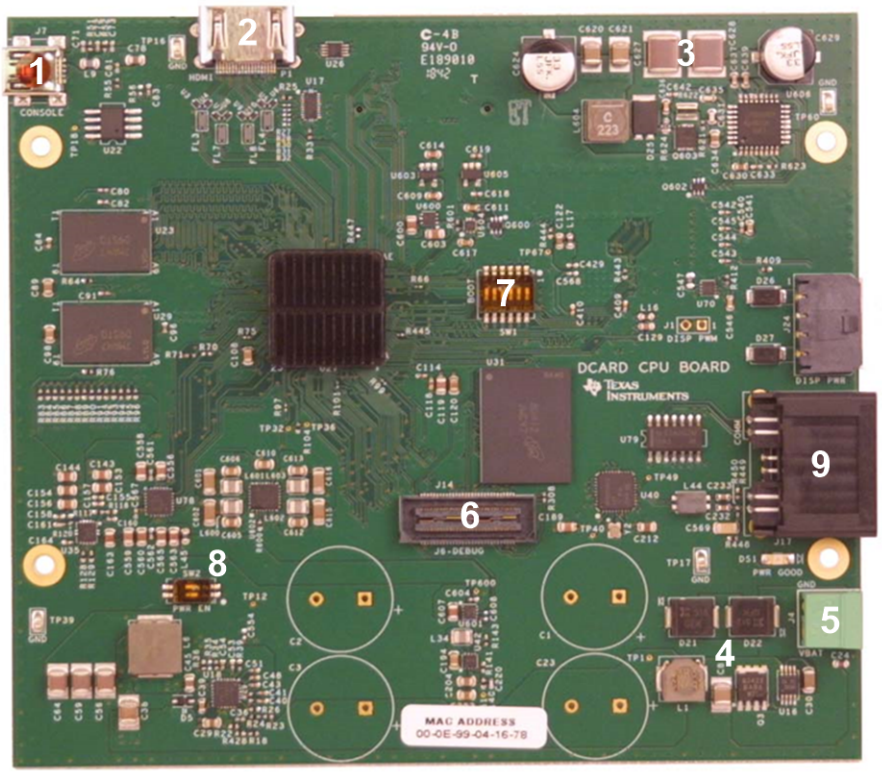

图 **8. DCARD Interfaces**

表 **1. DCARD Interfaces**

Legend	Description
1	USB-UART Terminal Console, J7
2	HDMI Connector
3	Cluster Display output
4	Power Cable (12 V, 5A)
5	LED Indicating Power Supply is Stable
6	JTAG Connector
7	Boot Switch, SW1
8	Wake/Power Mode Switch, SW2
9	Connector for Can and Audio output

4.1.2 Power

A variable power supply or 12-V power adaptor must be used to power the reference design.

4.1.3 Wakeup/Power – DCAN

DCARD supports various power-up options selected with switch SW2 (see 图 8).

- Bypass mode:
  - CAN wake-up is bypassed and DCARD is powered with 12V supply
- CAN Wake Up mode:
  - CAN wakeup through CAN transceiver is activated and power to DCARD is controlled through CAN transceiver
  - In this mode, DCARD will power-up for first time when 12V is applied. However, application processor is expected to put DCAN transceiver in the standby mode, which in turn will power off DCARD. After that, wake-up activity will be controlled by CAN bus. When there is an activity on CAN bus, CAN transceiver wakes up the system and powers DCARD.

4.1.4 Display

- CDTech 12.3 inch, 1920 × 720 screen mounted to PCB Board
- HDMI to support HUD integration

4.1.5 Memory and Flash

- 2 GB of DDR3 (MT46H32M32LFB5-5)
- eMMC Flash, 8 GB v5.1 compliance, HS-400 (MTFC8GAKAEDQ-AIT)

4.1.6 Debug

- JTAG Support
- UART-over-USB for terminal access. USB to serial FTDI chip.

4.1.7 Boot Mode Settings

Boot mode on DCARD is set using the boot switch (SW1) as shown in 图 9. See 图 8 for location.

- For SD boot, set SW1 to 0x110111
- For eMMC boot, set SW1 to 0x111111

图 **9. Boot Mode Switch SW1 Settings**

4.2 Software

Please contact Texas Instruments™ to see the latest cluster software demo package run on DCARD.

4.3 Testing and Results

Successful load of cluster demonstration software on the DCARD setup.

图 **10. Testing**

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDEP-01002.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP-01002.

5.3 Layout Prints

To download the layer plots, see the design files at TIDEP-01002.

5.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDEP-01002.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDEP-01002.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP-01002.

6 Related Documentation

1. Texas Instruments, *DRA72x (SR2.0, SR1.0), DRA71x (SR2.1, SR2.0) SoC for Automotive Infotainment Technical Reference Manual*
2. Texas Instruments, *DRA71x Infotainment Applications Processor Data Sheet*

6.1 商标

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