

DLP472TP 0.47 4K UHD 数字微镜器件

1 特性

- 0.47 英寸对角线微镜阵列
 - 4K UHD (3840 × 2160) 显示分辨率
 - 5.4µm 微镜间距
 - ±17° 微镜倾斜度 (相对于平坦表面)
 - 底部照明
- SubLVDS 输入数据总线
- 支持 4K UHD (60Hz)
- 支持 1080p (高达 240Hz)
- 由 DLPC8445 显示控制器、DLPA3085 电源管理 IC (PMIC) 和 LED 驱动器支持 LED 正常运行

2 应用

- 移动智能电视
- 移动投影仪
- 数字标牌

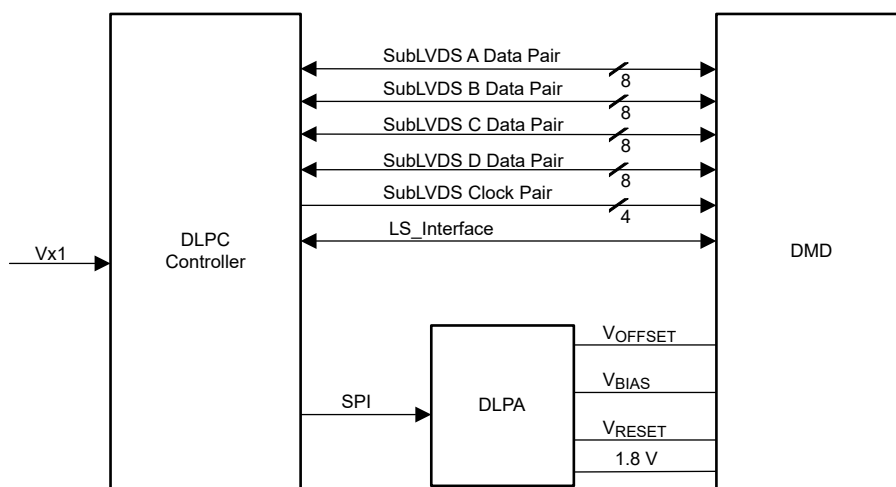
3 说明

DLP472TP 数字微镜器件 (DMD) 是一款数控微机电系统 (MEMS) 空间光调制器 (SLM)，可用于实现高亮的 4K UHD 显示系统。TI DLP® 产品 0.47 英寸 4K UHD 芯片组包括 DLP472TP DMD、DLPC8445 显示控制器、DLPA3085 PMIC 和 LED 驱动器。芯片组的外形紧凑，为体型小巧的 4K 超高清显示器提供完整的系统解决方案。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸
DLP472TP	FQY (166)	24.50mm × 11.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用

ADVANCE INFORMATION

4 器件和文档支持

4.1 第三方产品免责声明

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4.2 器件支持

4.2.1 器件命名规则

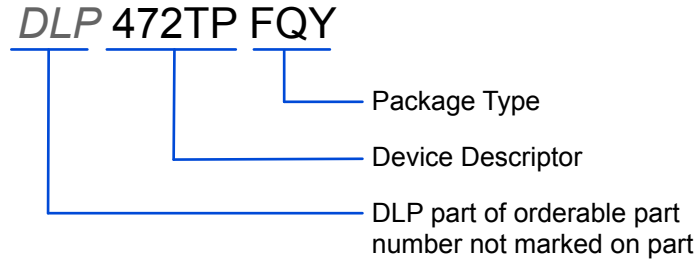


图 4-1. 器件型号说明

4.2.2 器件标识

器件标识包括人类可读的信息和二维矩阵码。图 4-2 说明了可供人类读取的信息，其中包括 GHJJJK 472TPFQY 这一清晰可辨的字符串。GHJJJK 是批次追踪代码，472TPFQY 则是器件标识。

示例：GHJJJK DLP472TPFQY

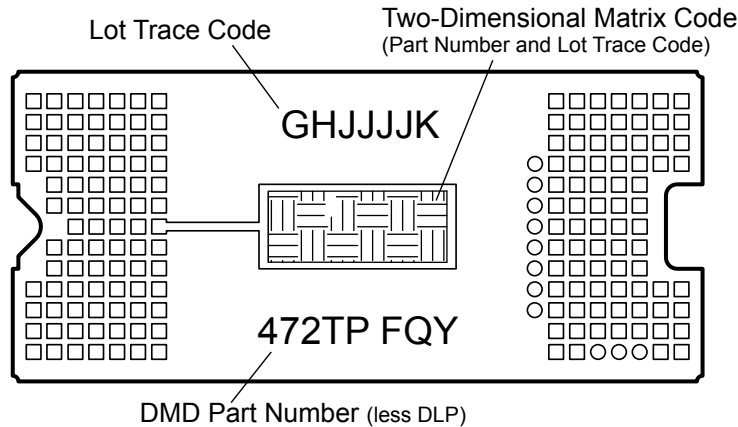


图 4-2. DMD 标识位置

4.3 文档支持

4.3.1 相关文档

以下文档包含与该 DMD 一起使用的芯片组元件相关的更多信息。

- [DLPC8445 高分辨率控制器数据表](#)
- [DLPA3085 PMIC 和高电流 LED 驱动器 IC 数据表](#)

4.4 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

4.5 商标

DLP® is a registered trademark of Texas Instruments.

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4.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

4.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

5 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

日期	修订版本	注释
May 2024	*	初始发行版

6 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP472TPFQY	Active	Production	CLGA (FQY) 174	80 JEDEC TRAY (5+1)	In-Work	NIAU	N/A for Pkg Type	0 to 70	
DLP472TPFQY.B	Active	Production	CLGA (FQY) 174	80 JEDEC TRAY (5+1)	In-Work	NIAU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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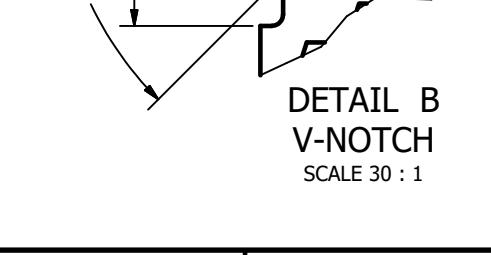
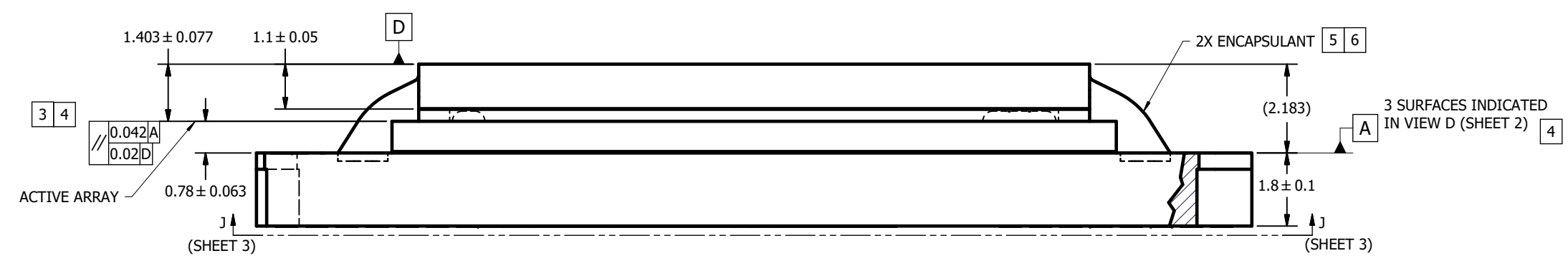
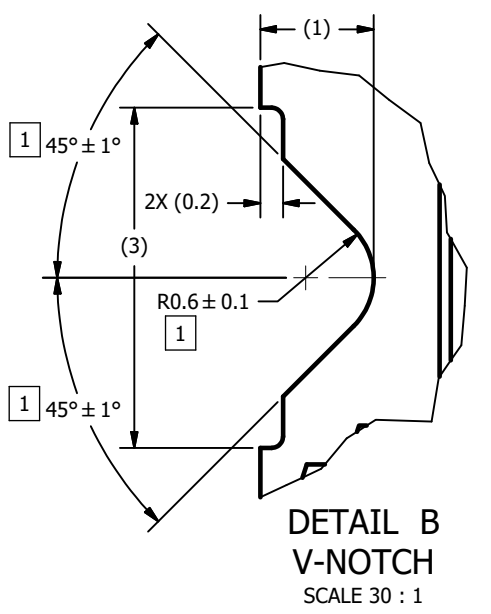
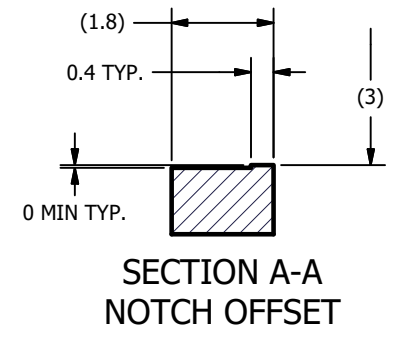
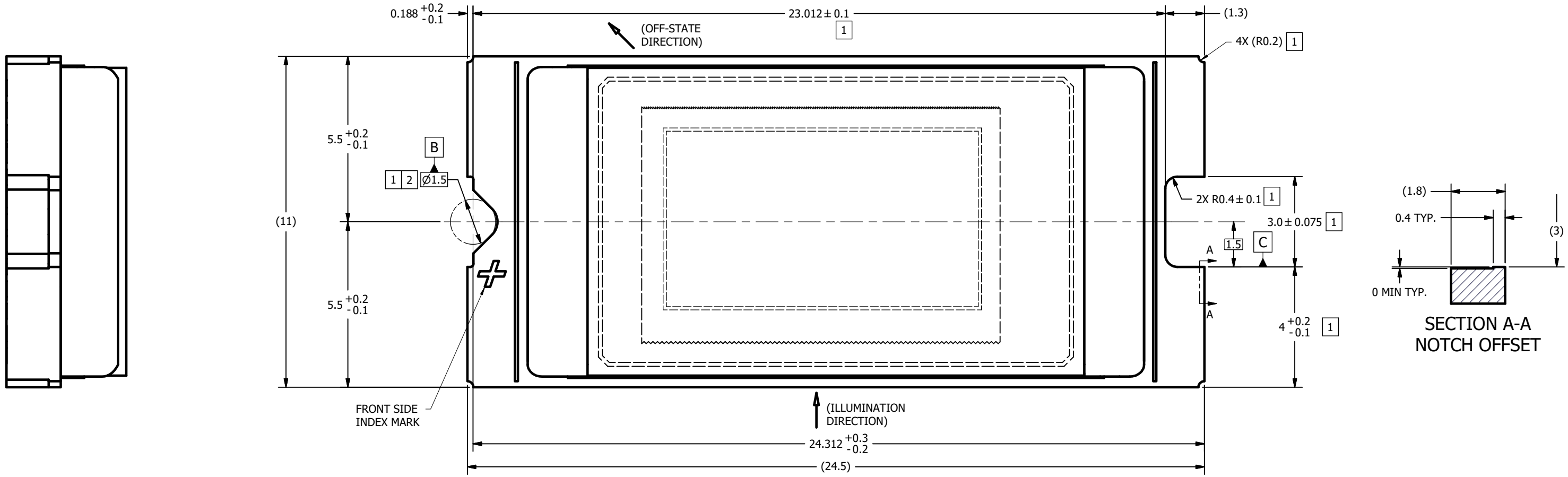
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REVISIONS		DATE	BY
REV	DESCRIPTION		
A	ECO 2202674: INITIAL RELEASE	12/22/22	HG

NOTES UNLESS OTHERWISE SPECIFIED:

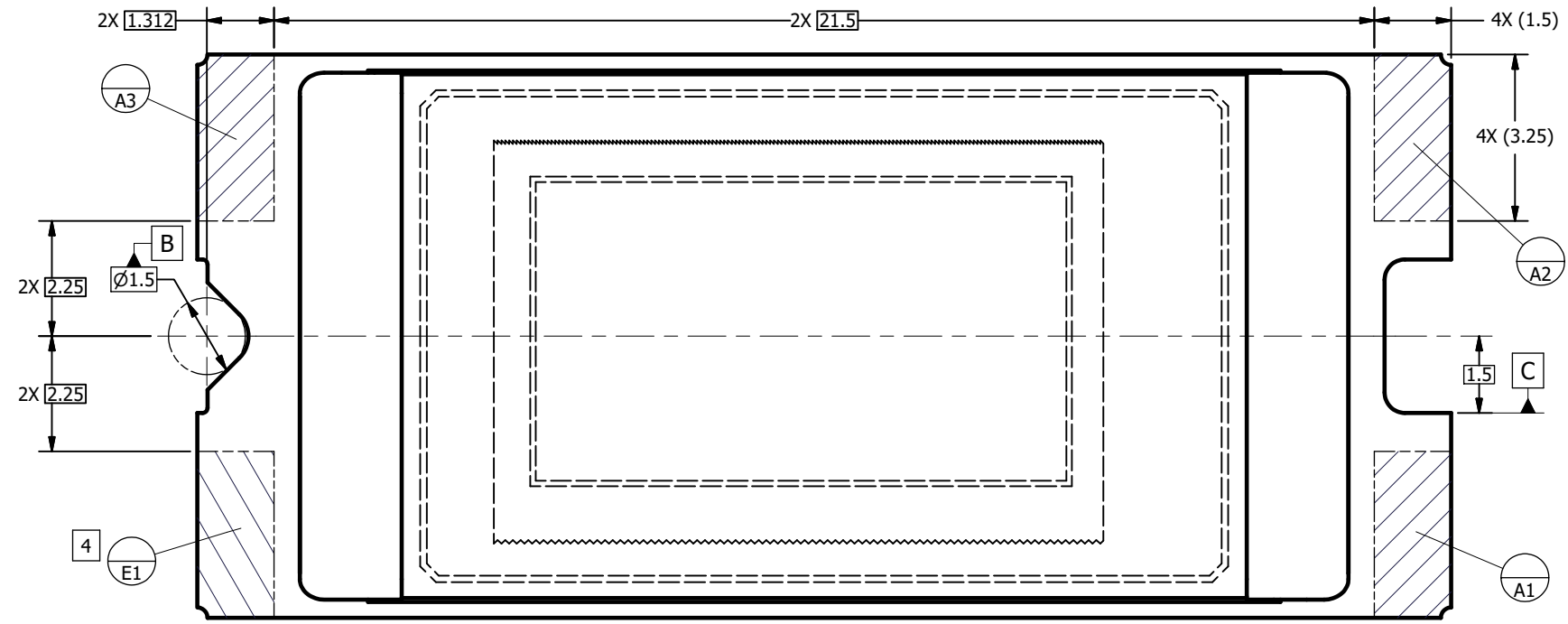
- 1 NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
- 2 SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
- 3 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
- 4 WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
- 5 ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
- 6 ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
- 7 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
- 8 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.



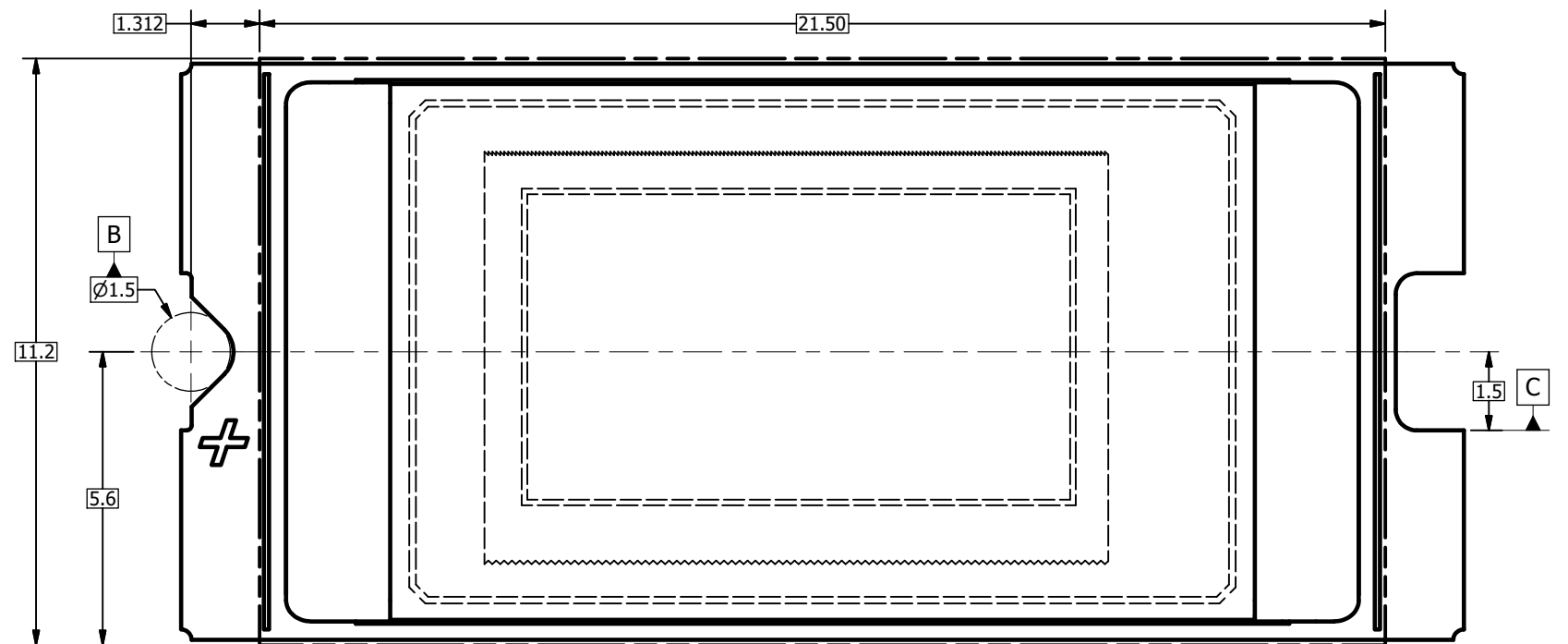
UNLESS OTHERWISE SPECIFIED
 ● DIMENSIONS ARE IN MILLIMETERS
 ● TOLERANCES:
 ANGLES ± 1'
 2 PLACE DECIMALS ± 0.25
 1 PLACE DECIMALS ± 0.50
~~● DIMENSIONAL LIMITS APPLY BEFORE PROCEEDING~~
 ● INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
~~● REMOVE ALL BURRS AND SHARP EDGES~~
 ● PARENTHETICAL INFORMATION FOR REFERENCE ONLY

DRAWN	H. GAGLIARDI	DATE	12/22/2023
ENGINEER	H. GAGLIARDI	DATE	12/22/2022
QA/CE	P. KONRAD	DATE	12/27/2022
CM	B. HASKETT	DATE	12/22/2022
APPROVED	J. MCKINLEY	DATE	12/22/2022
	M. GARCIA	DATE	1/3/2023

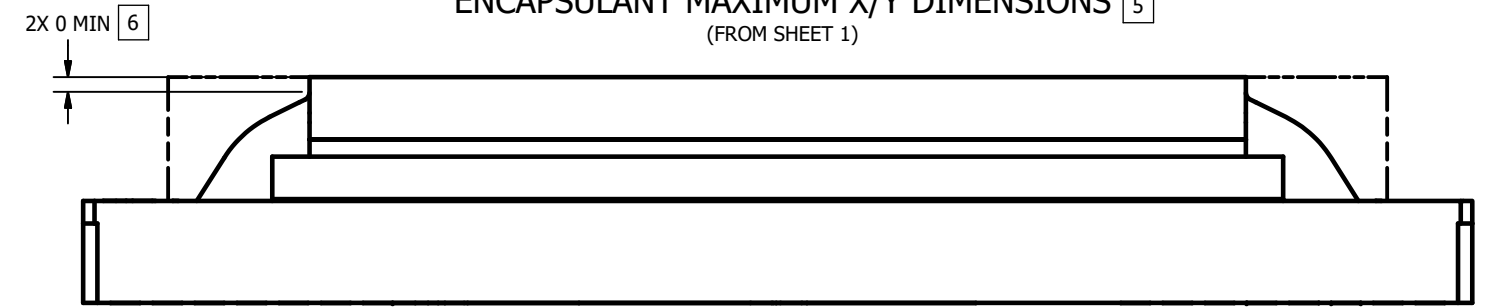
 TEXAS INSTRUMENTS <small>Dallas, Texas</small>	
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DWG NO	2518523
REV	A
SCALE	15:1
SHEET	1 OF 3



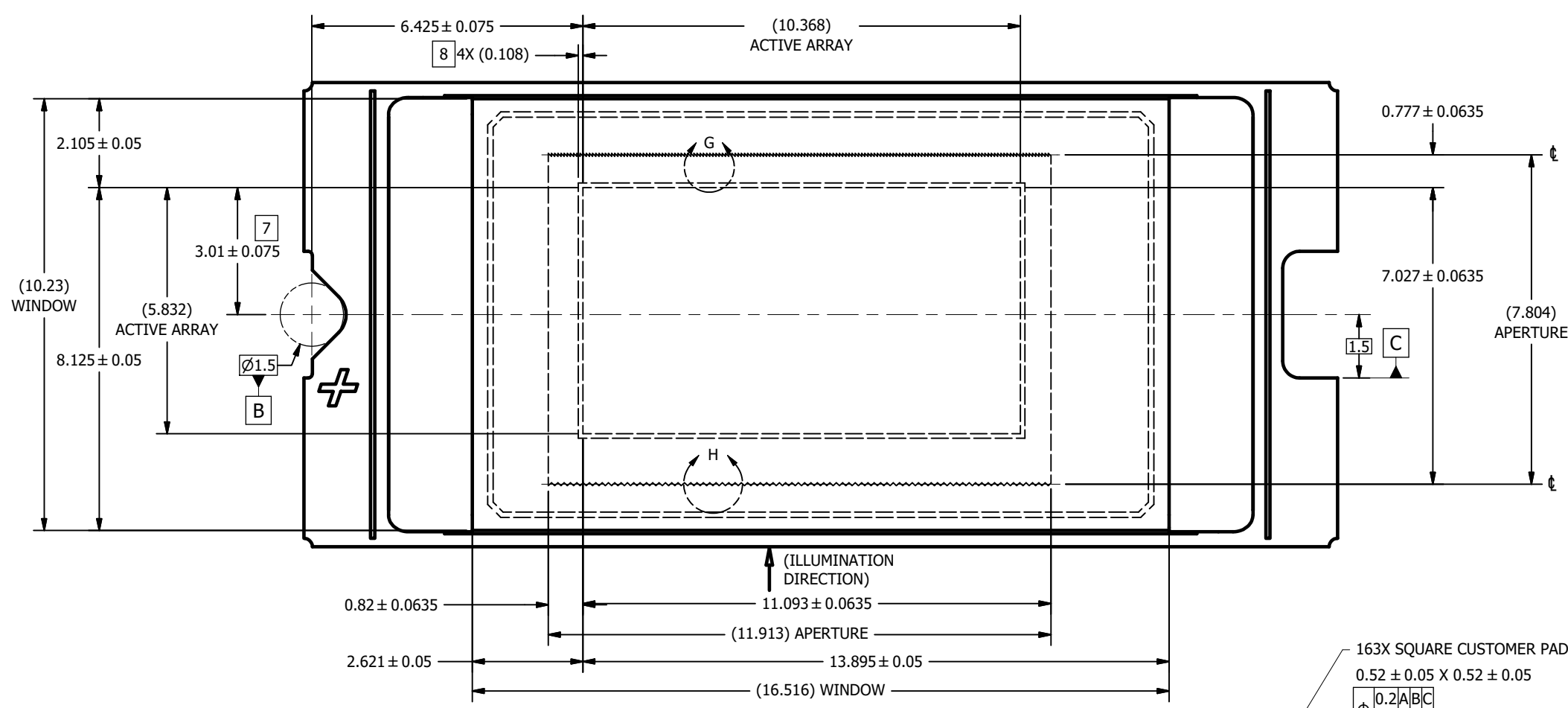
VIEW C
DATUMS A AND E
 (SUBSTRATE METALLIZATION OMITTED FOR CLARITY)
 (FROM SHEET 1)



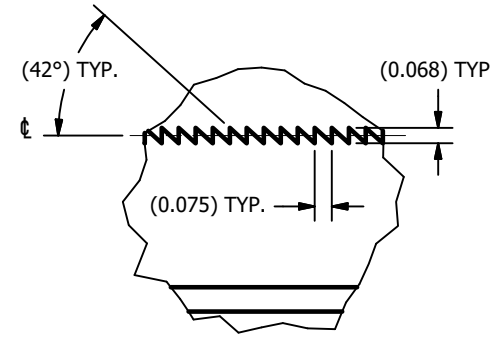
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
 (FROM SHEET 1)



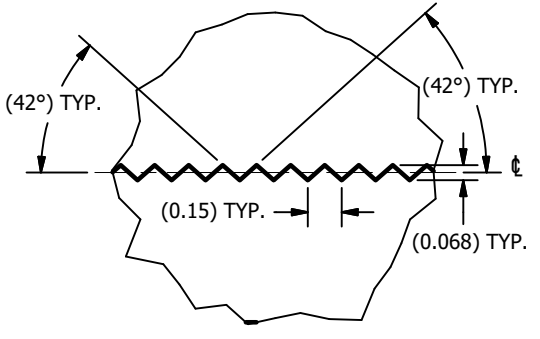
VIEW E
ENCAPSULANT MAXIMUM HEIGHT



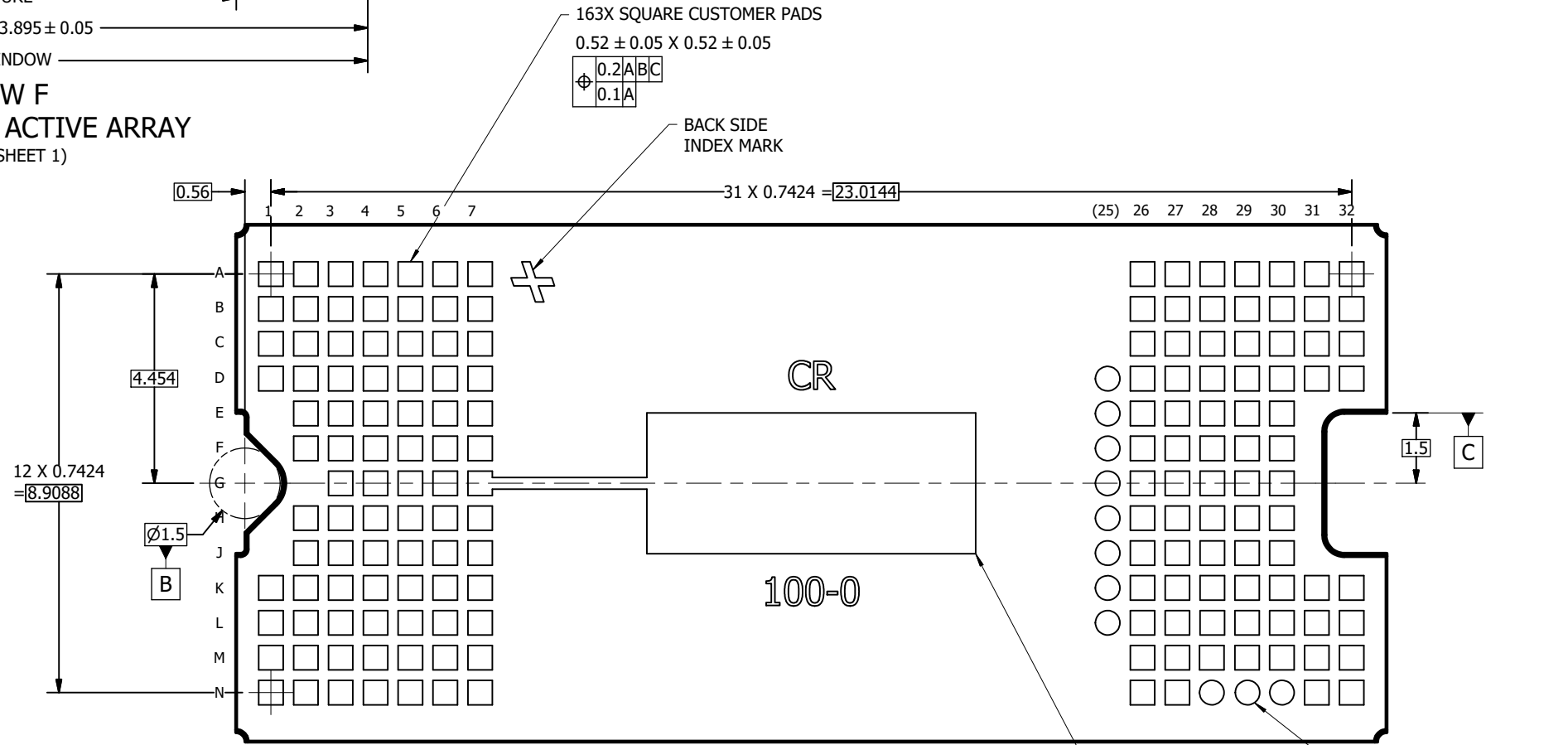
VIEW F
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL G
APERTURE TOP EDGE
SCALE 60 : 1



DETAIL H
APERTURE BOTTOM EDGE
SCALE 60 : 1



VIEW J-J
BACK SIDE METALLIZATION
(FROM SHEET 1)

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