

AFE11612-SEP 具有多通道 ADC、DAC 和温度传感器的耐辐射模拟监视器和控制器

1 特性

- 抗辐射：
 - 在 125°C 的环境温度下，单粒子锁定 (SEL) 抗扰度高达
LET = 43 MeV-cm²/mg
 - 单粒子功能中断 (SEFI) 的 LET 特征值高达 43 MeV-cm²/mg
 - 电离辐射总剂量 (TID) RLAT/RHA 特征值高达 20 krad(Si)
- 增强型航天塑料 (航天 EP)：
 - 符合 ASTM E595 释气规格要求
 - 供应商项目图 (VID) V62/22614
 - 军用级温度范围：-55°C 至 +125°C
 - 制造、组装和测试一体化基地
 - 金键合线，NiPdAu 铅涂层
 - 晶圆批次可追溯性
 - 延长了产品生命周期
 - 延长了产品变更通知周期
- 12 个单调性 12 位 DAC
 - 0V 至 5V 输出范围
 - DAC 关断至用户定义电平
- 16 输入 12 位 SAR ADC
 - 高采样率：500kSPS
 - 16 个单端输入或
2 个差分输入和 12 个单端输入
 - 可编程超限报警
- 8 个 GPIO 引脚
- 内部 2.5V 基准电压
- 两个远程温度传感器
- 内部温度传感器
- 可配置的 SPI 和 I²C 接口
 - 2.7V 至 5.5V 的工作电压

2 应用

- 命令和数据处理 (C&DH)
- 通信负载
- 雷达成像有效载荷
- 光学成像有效载荷
- 一般模拟监视和控制

3 说明

AFE11612-SEP 是一款高度集成的模拟监视和控制器件，专为高密度通用监视和控制系统而设计。该器件包含 12 个 12 位数模转换器 (DAC) 和一个 16 通道 12 位模数转换器 (ADC)。该器件还包含八个通用输入和输出 (GPIO)、两个远程温度传感器通道和一个本地温度传感器通道。

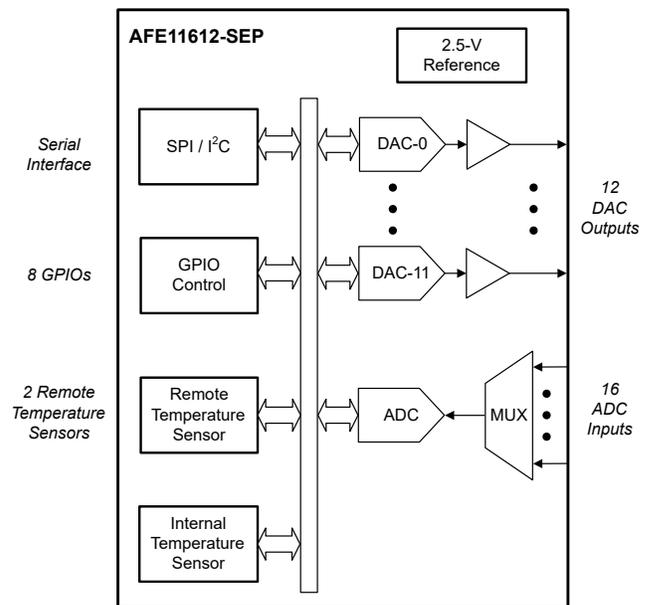
该器件具有一个 2.5V 内部基准，可将 DAC 设置为 0V 至 5V 的输出电压范围。该器件还支持通过外部基准运行。该器件支持通过 SPI 兼容接口和 I²C 兼容接口进行通信。

该器件的高集成度可显著减少组件数量并简化闭环系统设计，从而使该器件成为辐射耐受性和布板空间至关重要的高密度应用的理想选择。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
AFE11612-SEP	HTQFP (64)	10.0mm × 10.0mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



简化版原理图



4 Device and Documentation Support

4.1 Trademarks

所有商标均为其各自所有者的财产。

4.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.3 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE11612PAPSEP	Active	Production	HTQFP (PAP) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP
AFE11612PAPSEP.A	Active	Production	HTQFP (PAP) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP
V62/22614-01XE	Active	Production	HTQFP (PAP) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

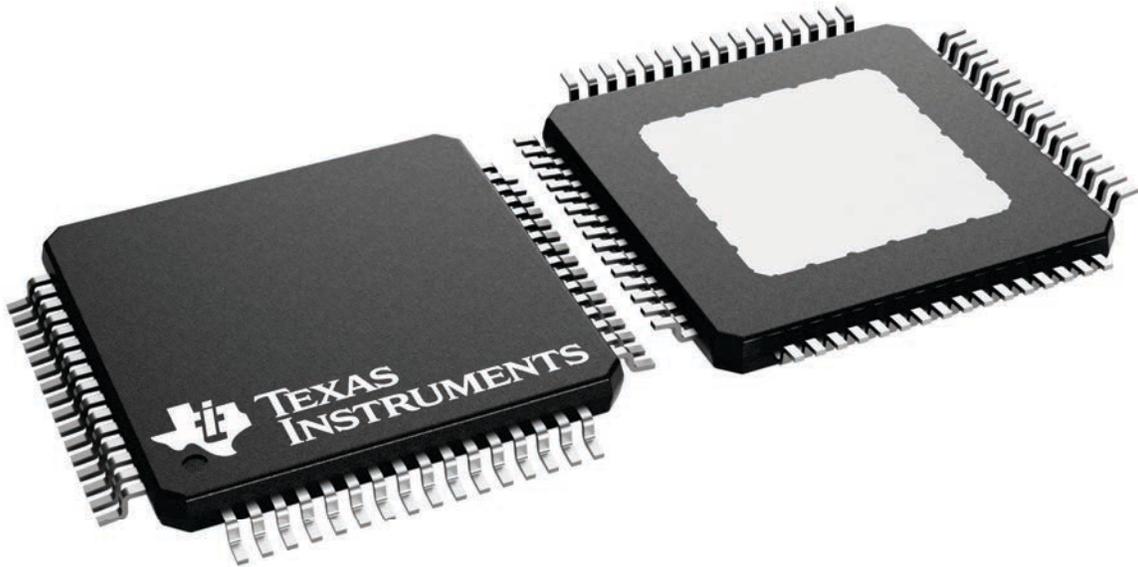
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

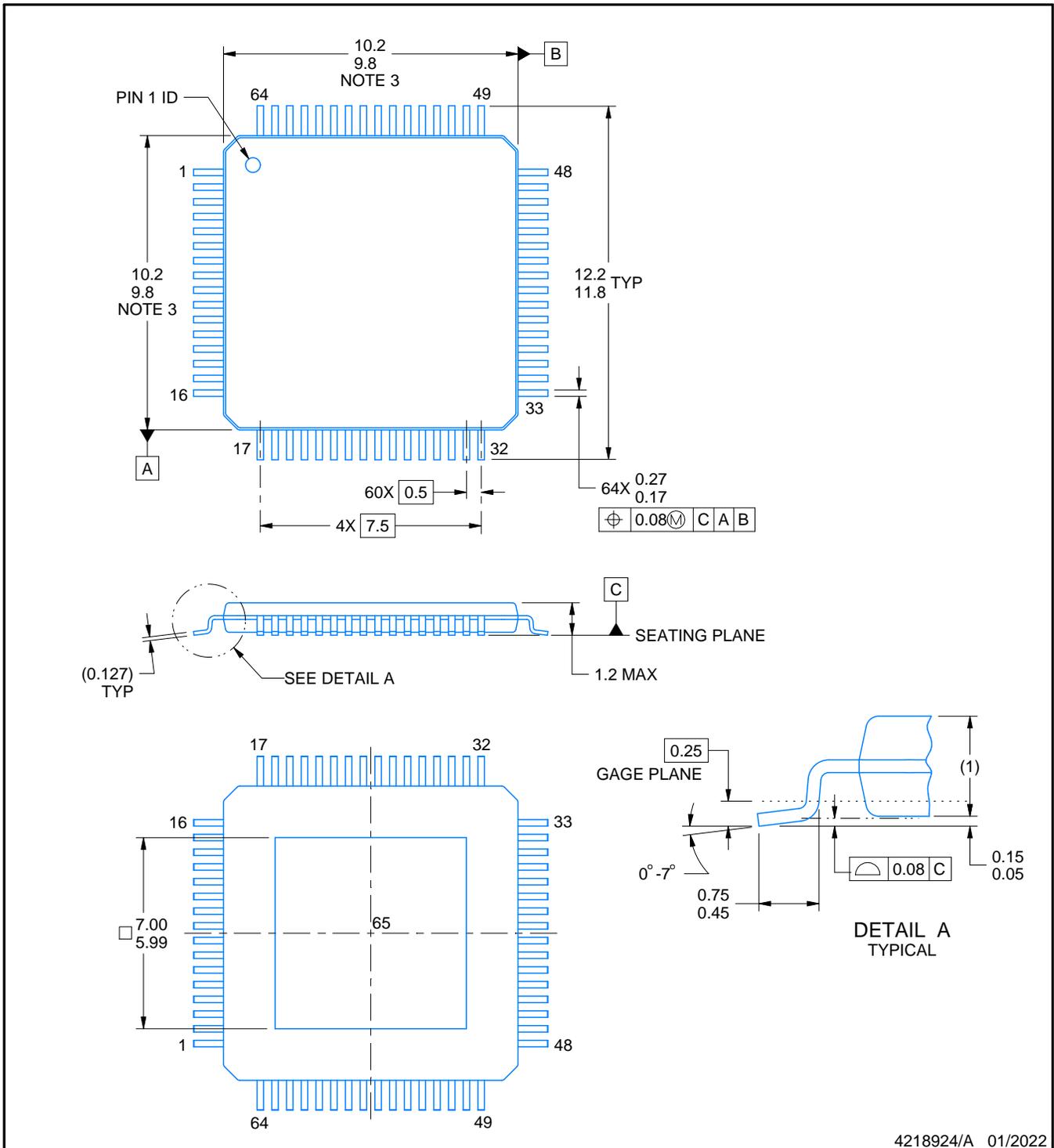
PAP0064G



PACKAGE OUTLINE

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

PowerPAD is a trademark of Texas Instruments.

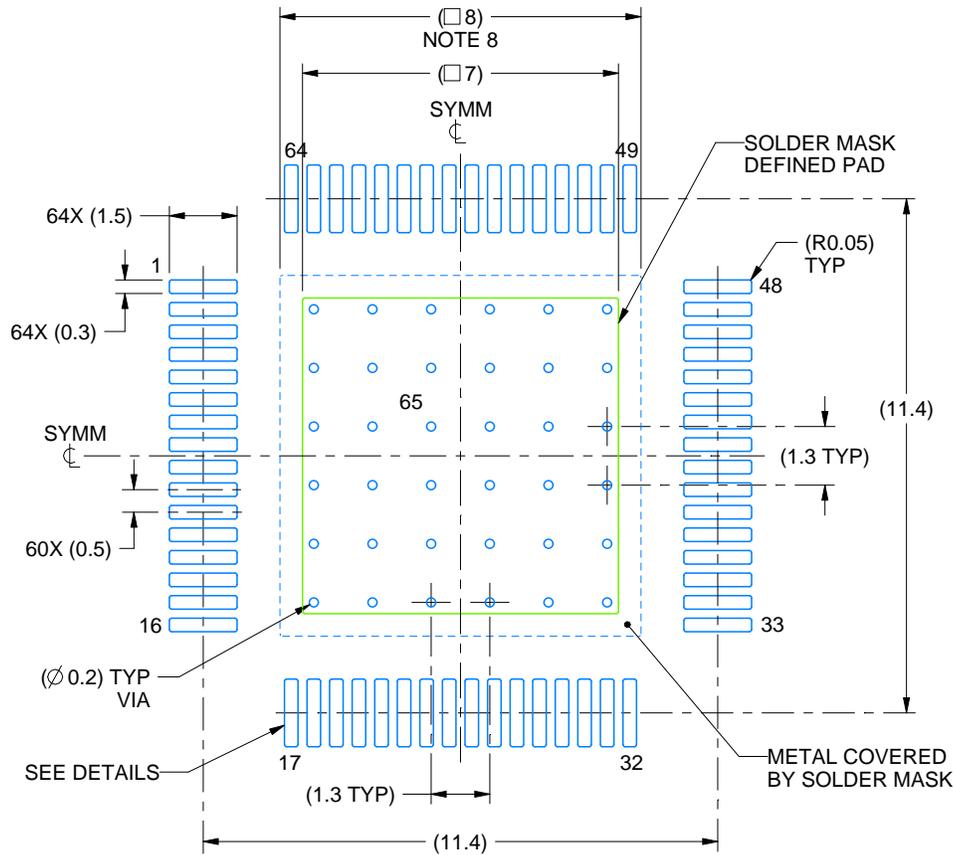
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

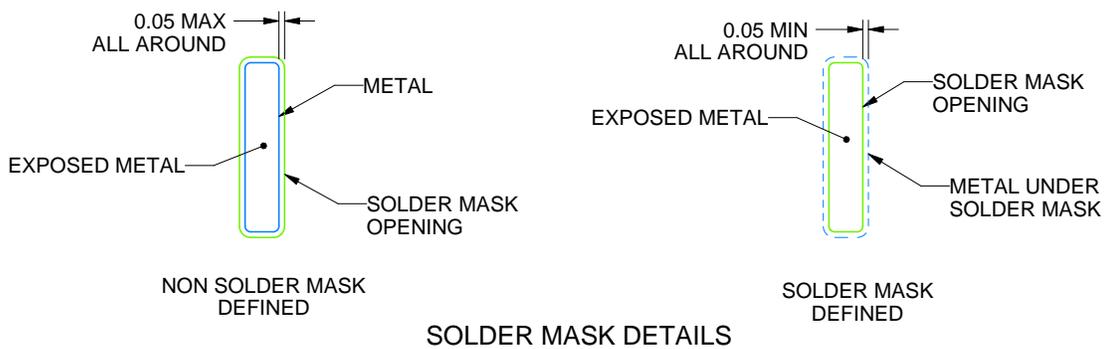
PAP0064G

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



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NOTES: (continued)

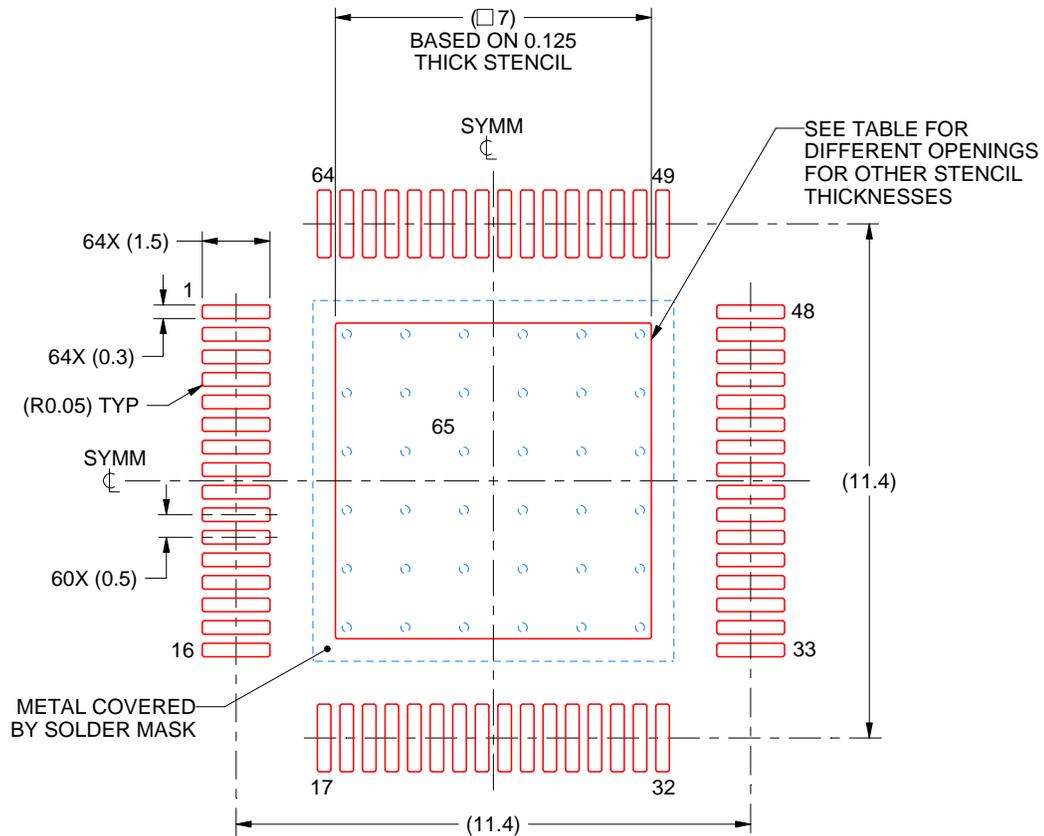
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PAP0064G

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
 EXPOSED PAD
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.83 X 7.83
0.125	7.0 X 7.0 (SHOWN)
0.15	6.39 X 6.39
0.175	5.92 X 5.92

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NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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