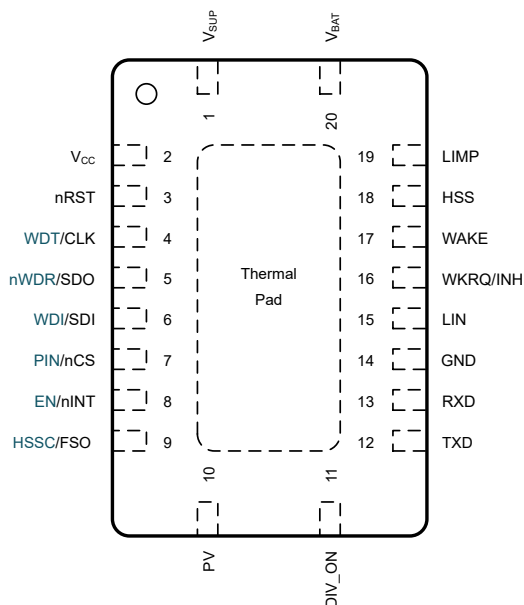


4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
April 2022	*	Initial release

5 Pin Configuration and Functions



**图 5-1. RGY Package, 20-Pin QFN
(Top View)**

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
V _{SUP}	1	I	Device supply voltage (connected to battery in series with external reverse blocking diode)
V _{CC}	2	O	Output voltage from integrated voltage regulator
nRST	3	I/O	Reset input/output (active low)
WDT/CLK	4	I	Pin control: WDT - Programmable watchdog window set input (3 levels) SPI control: CLK - SPI clock input
nWDR/SDO	5	O	Pin control: nWDR - watchdog failure output trigger SPI control: SDO - SPI serial data output
WDI/SDI	6	I	Pin control: WDI - Watchdog timer trigger input active on both rising and falling edges (Must be driven at all times) SPI control: SDI - SPI serial data input
PIN/nCS	7	I	Pin or SPI control selection pin at power up. Pin control: does not change SPI control: nCS - is SPI chip select (active low)
EN/nINT	8	I/O	Pin control: EN - Device mode change input pin SPI control: nINT - Device interrupt output pin
HSSC/FSO	9	I/O	Pin control: HSSC - High side switch control input pin SPI control: FSO - Function output pin
PV	10	O	Internal V _{BAT} voltage divider output
DIV_ON	11	I	Input to turn on the internal V _{BAT} voltage divider, active high
TXD	12	I	TXD input interface to control state of LIN output
RXD	13	O	RXD output interface reporting state of LIN bus voltage
GND, Pad	14	—	Ground
LIN	15	I/O	LIN bus single-wire transmitter and receiver
WKRQ/INH	16	O	Digital output for wake or high voltage inhibit output depending upon state of pin at power up
WAKE	17	I	High Voltage Local wake up pin
HSS	18	O	High side switch
LIMP	19	O	Used for LIMP home, watchdog event causes this pin to switch V _{SUP}
V _{BAT}	20	I	Supply voltage divider sense input (connected to battery)

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation see the following:

- LIN Standards:
 - ISO 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
 - ISO 17987-4:2016: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
 - SAEJ2602-1:2021: LIN Network for Vehicle Applications
 - LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification
- EMC requirements:
 - SAE J2962-2:
 - HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for LIN
 - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
 - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
 - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
 - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
 - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
 - IEC 61000-4-2
 - IEC 61967-4
 - CISPR25
- Conformance Test requirements:
 - ISO 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
 - SAE J2602-2:2021: LIN Network for Vehicle Applications Conformance Test

Application Notes:

[TLINx441 LDO Performance, SLLA427](#)

6.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.3 支持资源

TI E2E™ 支持论坛 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.4 Trademarks

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 术语表

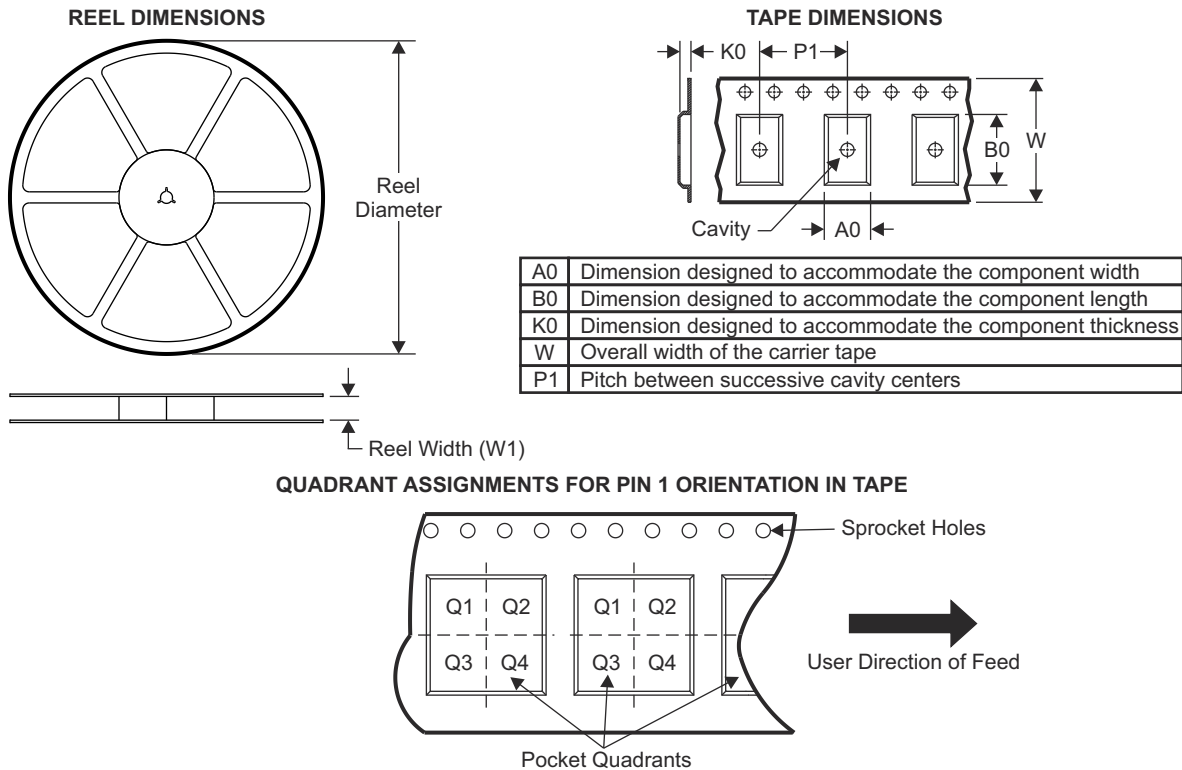
TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

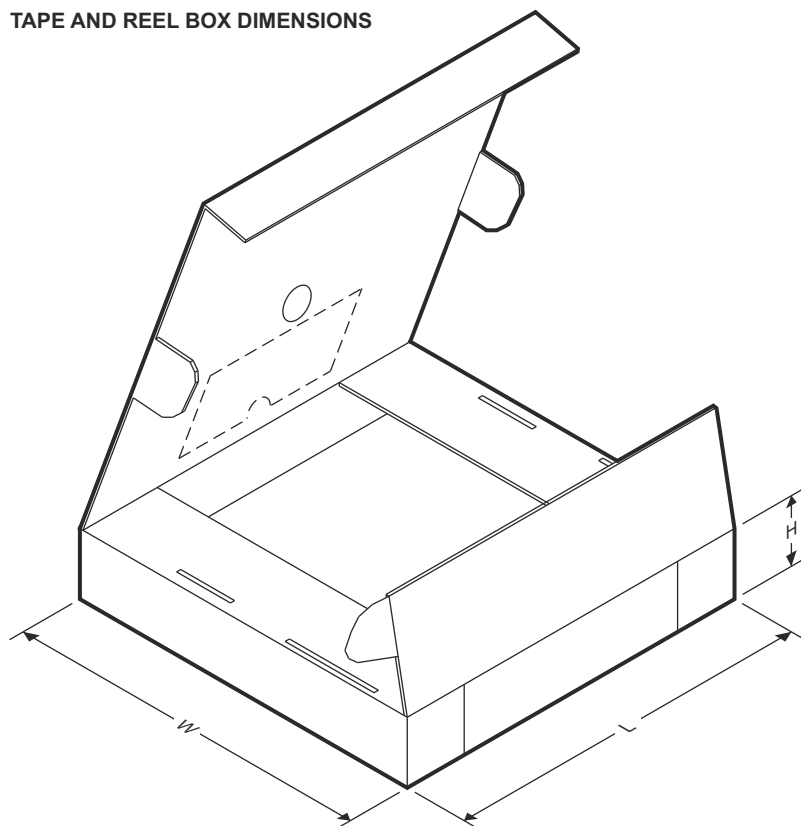


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN14313RGYRQ1	VQFN	RGY	20	3000	3330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
TLIN14315RGYRQ1	VQFN	RGY	20	3000	3330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1

TLIN1431-Q1

ZHCSQG9 - APRIL 2022

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN14313RGYRQ1	VQFN	RGY	20	3000	370.0	355.0	55.0
TLIN14315RGYRQ1	VQFN	RGY	20	3000	370.0	355.0	55.0

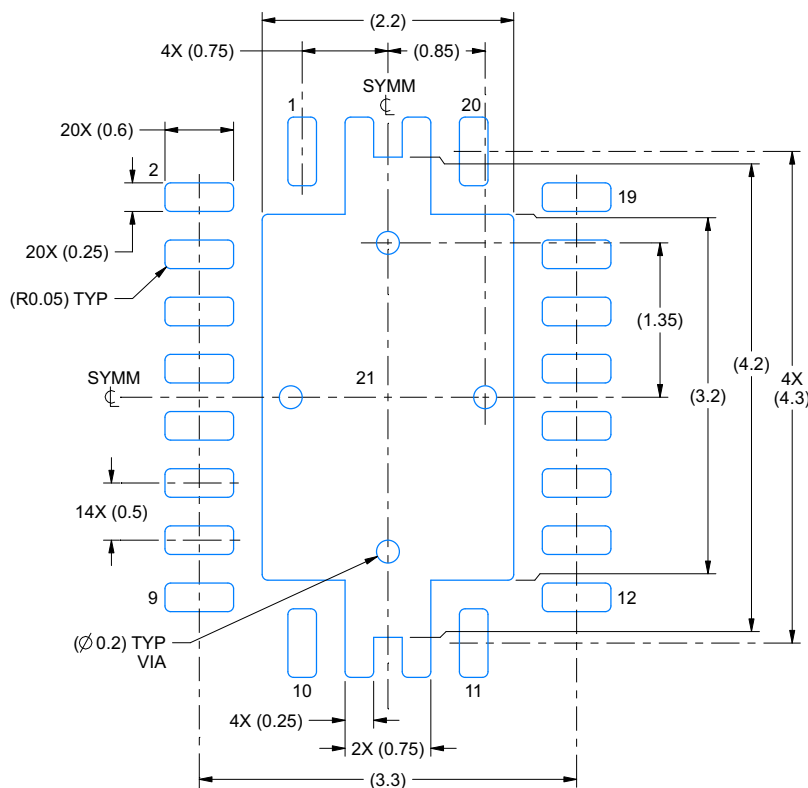
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

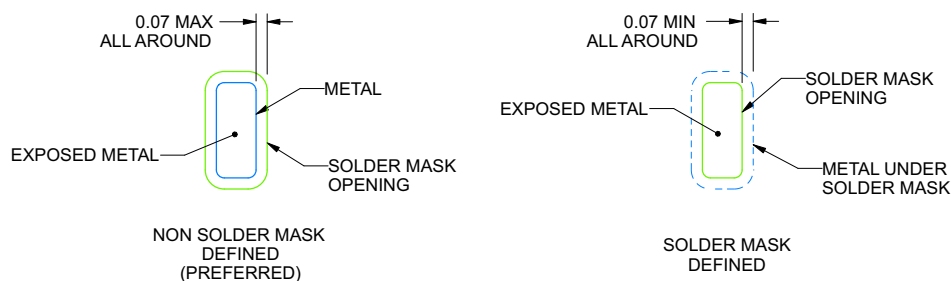
RGY0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4223814/A 06/2017

NOTES: (continued)

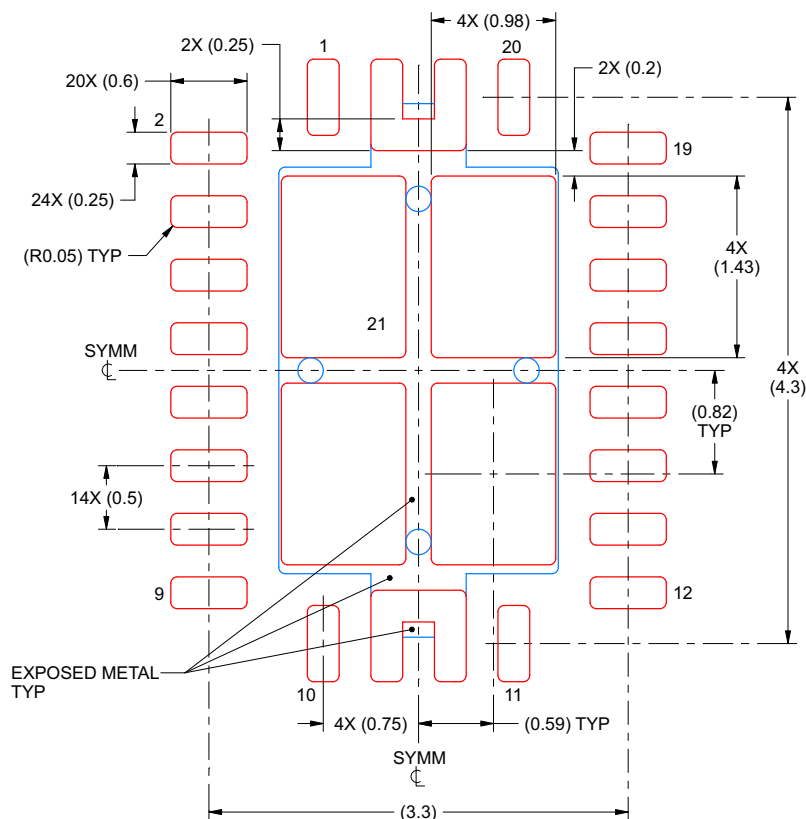
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD 21
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223814/A 06/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN14313RGYRQ1	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL313
TLIN14313RGYRQ1.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL313
TLIN14315RGYRQ1	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL315
TLIN14315RGYRQ1.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL315

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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