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**TEXAS INSTRUMENTS**

AMC3336-Q1
ZHCSM49 – APRIL 2021

# AMC3336-Q1 具有集成直流/直流转换器的高精度、±1V 输入增强型隔离式 Δ-Σ 调制器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：‒40°C 至 +125°C，$T_A$
- 3.3V 或 5V 单电源，具有集成直流/直流转换器
- ±1V 输入电压范围，针对电压测量进行了优化
- 输入电阻：1GΩ（典型值）
- 低直流误差：
  - 失调电压误差：±0.3mV（最大值）
  - 温漂±4μV/°C（最大值）
  - 增益误差：±0.2%（最大值）
  - 增益漂移：±40ppm/°C（最大值）
- 高 CMTI：90kV/μs（最小值）
- 系统级诊断功能
- 低 EMI：符合 CISPR-11 和 CISPR-25 标准
- 安全相关认证：
  - 符合 DIN VDE V 0884-11 标准的 $6000V_{PEAK}$ 增强型隔离
  - 符合 UL1577 标准且长达 1 分钟的 $4250V_{RMS}$ 隔离

## 2 应用

- 可用于以下应用的隔离式电压感应：
  - HEV/EV 车载充电器 (OBC)
  - HEV/EV 直流/直流转换器
  - HEV/EV 牵引逆变器

## 3 说明

AMC3336-Q1 是一款精密的隔离式 Δ-Σ 调制器，针对高阻抗交流电压测量进行了优化。这款完全集成的隔离式直流/直流转换器可实现器件低侧的单电源运行，使该器件成为空间受限应用的独特解决方案。增强型电容式隔离栅已通过 VDE V 0884-11 和 UL1577 认证，并支持高达 $1.2kV_{RMS}$ 的工作电压。
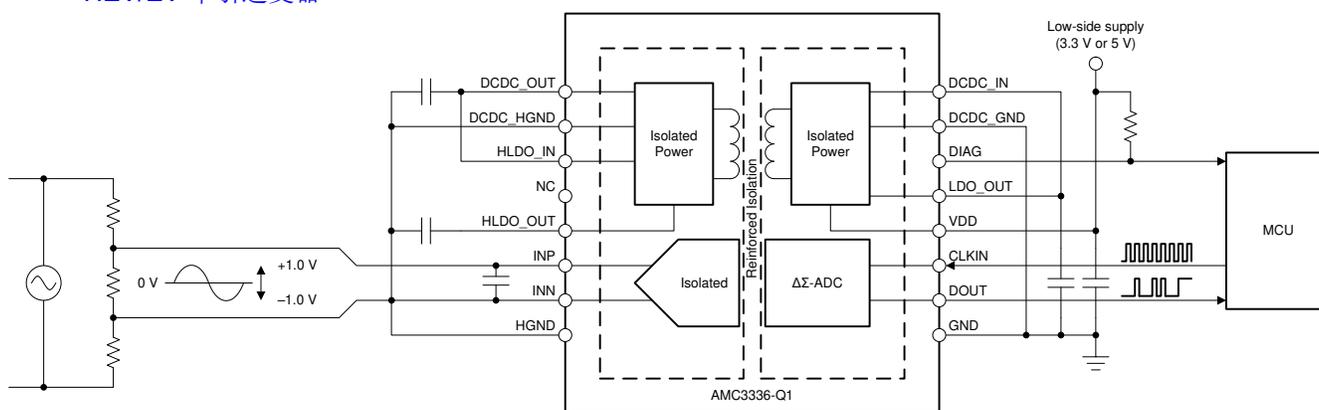
该隔离栅可将系统中以不同共模电压电平运行的各器件隔开，并保护电压较低的器件免受高电压冲击。

AMC3336-Q1 的输入针对直接连接电阻器网络或其他高阻抗电压信号源进行了优化。出色的直流精度和低温漂支持在 ‒40°C 至 +125°C 的工业级工作温度范围内进行精确的电压测量。

通过使用数字滤波器（例如 $sinc^3$ 滤波器）来抽取位流，该器件可在 78kSPS 数据速率下实现 16 位分辨率和 85dB 的动态范围。

### 器件信息[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
| --- | --- | --- |
| AMC3336-Q1 | SOIC (16) | 10.30mm x 7.50mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

English Data Sheet: SBASA83

## Table of Contents

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE | REVISION | NOTES |
|---|---|---|
| April 2021 | * | Initial Release |

## 5 Pin Configuration and Functions



Not to scale
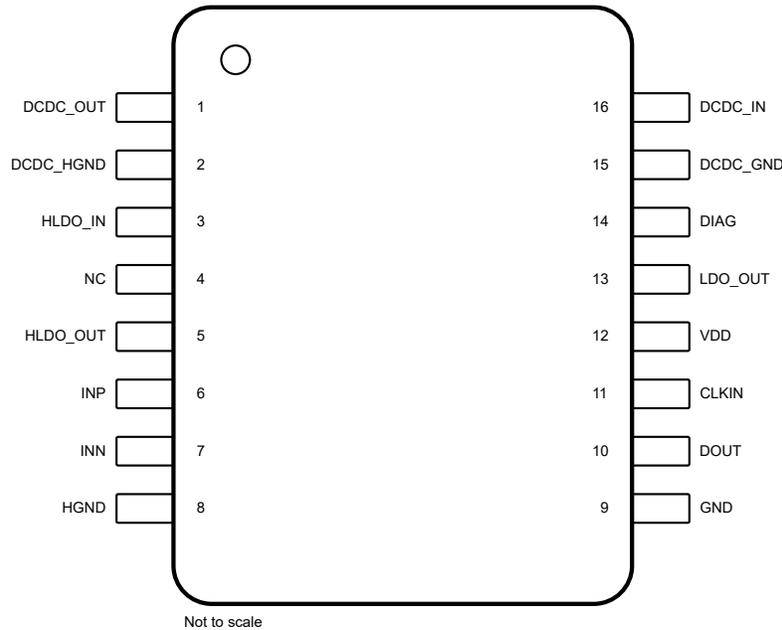
**图 5-1. DWE Package, 16-Pin SOIC, Top View**

**表 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DCDC_OUT | Power | High-side output of the DC/DC converter; connect this pin to the HLDO_IN pin.[1] |
| 2 | DCDC_HGND | High-side power ground | High-side ground reference for the DC/DC converter; connect this pin to the HGND pin. |
| 3 | HLDO_IN | Power | Input of the high-side LDO; connect this pin to the DCDC_OUT pin.[1] |
| 4 | NC | — | No internal connection. Connect this pin to the high-side ground or leave unconnected (floating). |
| 5 | HLDO_OUT | Power | Output of the high-side LDO.[1] |
| 6 | INP | Analog input | Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.[2] |
| 7 | INN | Analog input | Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.[2] |
| 8 | HGND | High-side signal ground | High-side analog signal ground; connect this pin to the DCDC_HGND pin. |
| 9 | GND | Low-side signal ground | Low-side analog signal ground; connect this pin to the DCDC_GND pin. |
| 10 | DOUT | Digital output | Modulator data output. |
| 11 | CLKIN | Digital input | Modulator clock input with internal pull-down resistor (typical value: 1.5 MΩ). |
| 12 | VDD | Low-side power | Low-side power supply.[1] |
| 13 | LDO_OUT | Power | Output of the low-side LDO; connect this pin to the DCDC_IN pin. The output of the LDO must not be loaded by external circuitry.[1] |
| 14 | DIAG | Digital output | Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used. |
| 15 | DCDC_GND | Low-side power ground | Low-side ground reference for the DC/DC converter; connect this pin to the GND pin. |
| 16 | DCDC_IN | Power | Low-side input of the DC/DC converter; connect this pin to the LDO_OUT pin.[1] |

(1)    See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2)    See the *Layout* section for details.

Product Folder Links: *AMC3336-Q1*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

see [1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power-supply voltage | VDD to GND | $-0.3$ | 6.5 | V |
| Analog input voltage | INP, INN | HGND $-6$ | HLDO_OUT + 0.5 | V |
| Digital input voltage | CLKIN | GND $-0.5$ | VDD + 0.5 | V |
| Digital output voltage | DOUT | GND $-0.5$ | VDD + 0.5 | V |
| | DIAG | GND $-0.5$ | 6.5 | |
| Input current | Continuous, any pin except power-supply pins | $-10$ | 10 | mA |
| Temperature | Junction, $T_J$ | | 150 | °C |
| | Storage, $T_{stg}$ | $-65$ | 150 | |

(1)    Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1], HBM ESD classification Level 2 | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6 | ±1000 | |

(1)    AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| VDD | Low-side power supply | VDD to GND | 3 | 3.3 | 5.5 | V |
| **ANALOG INPUT** | | | | | | |
| $V_{Clipping}$ | Differential input voltage before clipping output | $V_{IN} = V_{INP} - V_{INN}$ | | ±1.25 | | V |
| $V_{FSR}$ | Specified linear differential full-scale voltage | $V_{IN} = V_{INP} - V_{INN}$ | $-1$ | | 1 | V |
| | Absolute common-mode input voltage [1] | $(V_{INP} + V_{INN}) / 2$ to HGND | $-2$ | | $V_{HLDO\_OUT}$ | V |
| $V_{CM}$ | Operating common-mode input voltage | $(V_{INP} + V_{INN}) / 2$ to HGND | $-0.8$ | | 0.6 | V |
| **DIGITAL I/O** | | | | | | |
| $V_{IO}$ | Digital input / output voltage | | 0 | | VDD | V |
| $f_{CLKIN}$ | Input clock frequency | | 9 | 20 | 21 | MHz |
| | Input clock duty cycle | 9 MHz $\leqslant f_{CLKIN} \leqslant$ 21 MHz | 40% | 50% | 60% | |
| **TEMPERATURE RANGE** | | | | | | |
| $T_A$ | Specified ambient temperature | | $-40$ | | 125 | °C |

(1)    Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage $V_{CM}$ for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | AMC3336-Q1 | UNIT |
|---|---|---|---|
| | | DWE (SOIC) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 31 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 16.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $P_D$ | Maximum power dissipation | VDD = 5.5 V | 231 | mW |
| | | VDD = 3.6 V | 151 | |

Product Folder Links: AMC3336-Q1

## 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance[1] | Shortest pin-to-pin distance through air | $\geqslant 8$ | mm |
| CPG | External creepage[1] | Shortest pin-to-pin distance across the package surface | $\geqslant 8$ | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance - capacitive signal isolation) | $\geqslant 21$ | μm |
| | | Minimum internal gap (internal clearance - transformer power isolation) | $\geqslant 120$ | |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | $\geqslant 600$ | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage $\leqslant 600$ $V_{RMS}$ | I-III | |
| | | Rated mains voltage $\leqslant 1000$ $V_{RMS}$ | I-II | |
| **DIN VDE V 0884-11 (VDE V 0884-11): 2017-01[2]** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | At AC voltage (bipolar) | 1700 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum-rated isolation working voltage | At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test | 1200 | $V_{RMS}$ |
| | | At DC voltage | 1700 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification test) | 6000 | $V_{PK}$ |
| | | $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test) | 7200 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage[3] | Test method per IEC 60065, 1.2/50-μs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000$ $V_{PK}$ (qualification) | 6250 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge[4] | Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s | $\leqslant 5$ | pC |
| | | Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m = 10$ s | $\leqslant 5$ | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1$ s | $\leqslant 5$ | |
| $C_{IO}$ | Barrier capacitance, input to output[5] | $V_{IO} = 0.5$ $V_{PP}$ at 1 MHz | ~4.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output[5] | $V_{IO} = 500$ V at $T_A = 25°C$ | $> 10^{12}$ | Ω |
| | | $V_{IO} = 500$ V at $100°C \leqslant T_A \leqslant 125°C$ | $> 10^{11}$ | |
| | | $V_{IO} = 500$ V at $T_S = 150°C$ | $> 10^{9}$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO} = 4250$ $V_{RMS}$ or 6000 $V_{DC}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test) | 4250 | $V_{RMS}$ |

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

## 6.7 Safety-Related Certifications

| VDE | UL |
|---|---|
| Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11 | Recognized under 1577 component recognition and CSA component acceptance NO 5 programs |
| Reinforced insulation | Single protection |
| Certificate pending | Certificate pending |

## 6.8 Safety Limiting Values

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 309 | mA |
| | | $R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 472 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 73.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C | | | 1700 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of $I_S$ and $P_S$. These limits vary with the ambient temperature, $T_A$.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where $VDD_{max}$ is the maximum low-side voltage.

## 6.9 Electrical Characteristics

all minimum and maximum specifications are at $T_A$ = – 40°C to 125°C, VDD = 3.0 V to 5.5 V, INP = – 1 V to +1 V, INN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted); typical values are at $T_A$ = 25°C, CLKIN = 20 MHz, VDD = 3.3 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| $R_{IN}$ | Single-ended input resistance | INN = HGND | 0.06 | 1 | | GΩ |
| $R_{IND}$ | Differential input resistance | | 0.06 | 1 | | GΩ |
| $I_{IB}$ | Input bias current | INP = INN = HGND; $I_{IB}$ = ($I_{IBP}$ + $I_{IBN}$) / 2 | – 10 | | 10 | nA |
| $I_{IO}$ | Input offset current[1] | $I_{IO}$ = $I_{IBP}$ – $I_{IBN}$ | – 5 | ±0.5 | 5 | nA |
| $C_{IN}$ | Single-ended input capacitance | INN = HGND; $f_{IN}$ = 310 kHz, $f_{CLKIN}$ = 20 MHz | | 2 | | pF |
| $C_{IND}$ | Differential input capacitance | $f_{IN}$ = 310 kHz, $f_{CLKIN}$ = 20 MHz | | 2 | | pF |
| **ACCURACY** | | | | | | |
| $E_O$ | Offset error[1] | INP = INN = HGND, $T_A$ = 25°C | – 0.3 | ±0.04 | 0.3 | mV |
| $TCE_O$ | Offset error thermal drift[4] | | – 4 | | 4 | µV/°C |
| $E_G$ | Gain error | $T_A$ = 25°C | – 0.2% | | 0.2% | |
| $TCE_G$ | Gain error thermal drift[5] | | – 40 | | 40 | ppm/°C |
| DNL | Differential nonlinearity | Resolution: 16 bits | – 0.99 | | 0.99 | LSB |
| INL | Integral nonlinearity | Differential measurement; Resolution: 16 bits | – 4 | | 4 | LSB |
| | | Single-ended measurement; Resolution: 16 bits | – 6 | | 6 | |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 1 kHz | 80 | 84 | | dB |
| SINAD | Signal-to-noise + distortion | $f_{IN}$ = 1 kHz | 77 | 84 | | dB |
| THD | Total harmonic distortion[3] | $V_{IN}$ = 2 $V_{PP}$, $f_{IN}$ = 1 kHz | | – 93 | – 80 | dB |
| SFDR | Spurious-free dynamic range | $V_{IN}$ = 2 $V_{PP}$, $f_{IN}$ = 1 kHz | 79 | 96 | | dB |
| CMRR | Common-mode rejection ratio | INP = INN, $f_{IN}$ = 0 Hz, $V_{CM min}$ ⩽ $V_{CM}$ ⩽ $V_{CM max}$ | | – 104 | | dB |
| | | INP = INN, $f_{IN}$ = 10 kHz, – 0.5 V ⩽ $V_{IN}$ ⩽ 0.5 V | | – 89 | | |
| PSRR | Power-supply rejection ratio | VDD from 3.0 V to 5.5 V, at dc | | – 109 | | dB |
| | | INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple | | – 104 | | |
| **DIGITAL I/O** | | | | | | |
| $I_{IN}$ | Input leakage current | GND ⩽ $V_{IN}$ ⩽ VDD | | | 7 | µA |
| $C_{IN}$ | Input capacitance | | | 4 | | pF |
| $V_{IH}$ | High-level input voltage | | 0.7 × VDD | | VDD + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | – 0.3 | | 0.3 × VDD | V |
| $C_{LOAD}$ | Output load capacitance | | | 15 | 30 | pF |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = – 20 µA | VDD – 0.1 | | | V |
| | | $I_{OH}$ = – 4 mA | VDD – 0.4 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 20 µA | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | | 0.4 | |
| CMTI | Common-mode transient immunity | | 90 | 150 | | kV/µs |

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Product Folder Links: *AMC3336-Q1*

## 6.9 Electrical Characteristics (continued)

all minimum and maximum specifications are at $T_A$ = – 40°C to 125°C, VDD = 3.0 V to 5.5 V, INP = – 1 V to +1 V, INN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted); typical values are at $T_A$ = 25°C, CLKIN = 20 MHz, VDD = 3.3 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| IDD | Low-side supply current | no external load on HLDO | | 28.5 | 42.5 | mA |
| | | 1 mA external load on HLDO | | 30.5 | 44.5 | |
| VDD$_{UV}$ | VDD analog undervoltage detection threshold | VDD rising | | | 2.9 | V |
| | | VDD falling | | | 2.8 | |
| VDD$_{POR}$ | VDD digital reset threshold | VDD rising | | | 2.5 | V |
| | | VDD falling | | | 2.4 | |
| V$_{DCDC\_OUT}$ | DC/DC output voltage | DCDC_OUT to HGND | 3.1 | 3.5 | 4.65 | V |
| V$_{DCDCUV}$ | DC/DC output undervoltage detection threshold voltage | V$_{DCDC\_OUT}$ falling | 2.1 | 2.25 | | V |
| V$_{HLDO\_OUT}$ | High-side LDO output voltage | HLDO_OUT to HGND, up to 1 mA external load [2] | 3 | 3.2 | 3.4 | V |
| V$_{HLDOUV}$ | High-side LDO output undervoltage detection threshold voltage | V$_{HLDO\_OUT}$ falling | 2.4 | 2.6 | | V |
| I$_H$ | High-side supply current for auxiliary circuitry | Load connected from HLDOout to HGND; non-switching; – 40℃ ≤ $T_A$ ≤ 85℃ [2] | | | 1 | mA |
| t$_{START}$ | Device startup time | VDD step from 0 to 3.0 V to bitstrem valid | | 0.6 | 1.1 | ms |

(1)     The typical value includes one standard deviation (*sigma*) at nominal operating condition.
(2)     High-side LDO supports full external load (IH) only up to TA = 85℃. See the *Isolated DC/DC Converter* section for more details.
(3)     THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4)     Offset error temperature drift is calculated using the box method, as described by the following equation:
        $TCE_O = (Value_{MAX} - Value_{MIN}) / TempRange$
(5)     Gain error temperature drift is calculated using the box method, as described by the following equation:
        $TCE_G (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25℃)} \times TempRange) \times 10^6$

Product Folder Links: *AMC3336-Q1*

## 6.10 Switching Characteristics

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_H$ | DOUT hold time after rising edge of CLKIN | $C_{LOAD}$ = 15 pF; CLKIN 50% to DOUT 10% / 90% | 3.5 | | | ns |
| $t_D$ | Rising edge of CLKIN to DOUT valid delay | $C_{LOAD}$ = 15 pF; CLKIN 50% to DOUT 10% / 90% | | | 15 | ns |
| $t_r$ | DOUT rise time | 10% to 90%, 3.0 V $\leqslant$ VDD $\leqslant$ 3.6 V, $C_{LOAD}$ = 15 pF | | 2.5 | 6 | ns |
| | | 10% to 90%, 4.5 V $\leqslant$ VDD $\leqslant$ 5.5 V, $C_{LOAD}$ = 15 pF | | 3.2 | 6 | |
| $t_f$ | DOUT fall time | 10% to 90%, 3.0 V $\leqslant$ VDD $\leqslant$ 3.6 V, $C_{LOAD}$ = 15 pF | | 2.2 | 6 | ns |
| | | 10% to 90%, 4.5 V $\leqslant$ VDD $\leqslant$ 5.5 V, $C_{LOAD}$ = 15 pF | | 2.9 | 6 | |

## 6.11 Timing Diagrams
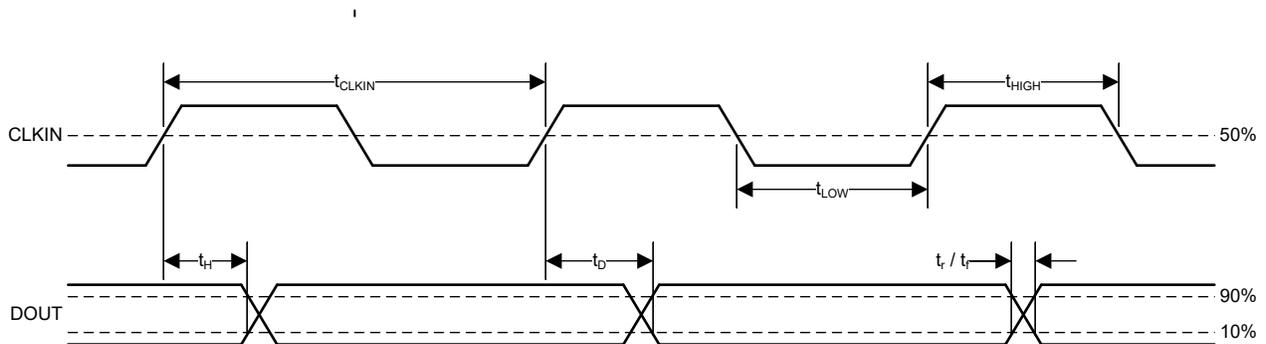


图 **6-1. Digital Interface Timing**
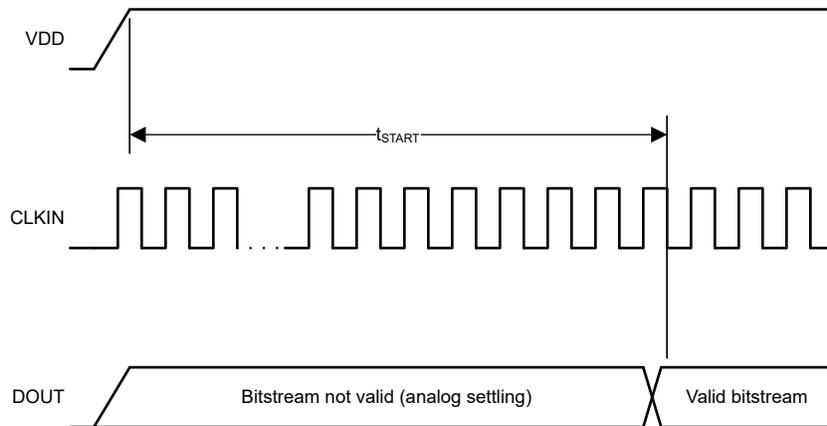


图 **6-2. Device Startup Timing**

Product Folder Links: *AMC3336-Q1*

## 6.12 Insulation Characteristics Curves
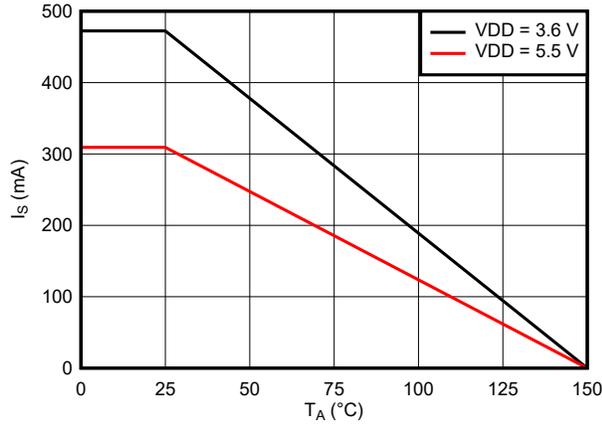


图 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE
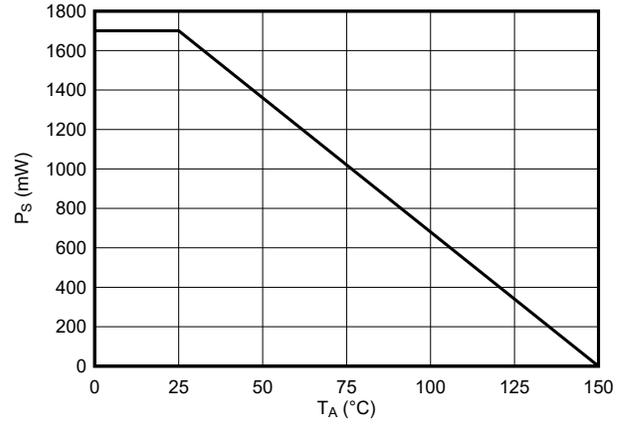


图 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE
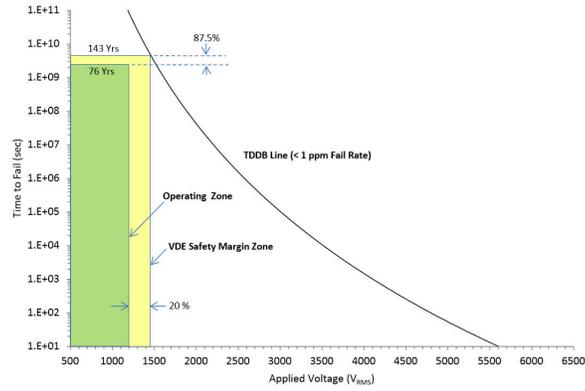


$T_A$ up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1200 $V_{RMS}$, operating lifetime = 76 years

图 6-5. Reinforced Isolation Capacitor Lifetime Projection

## 6.13 Typical Characteristics

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
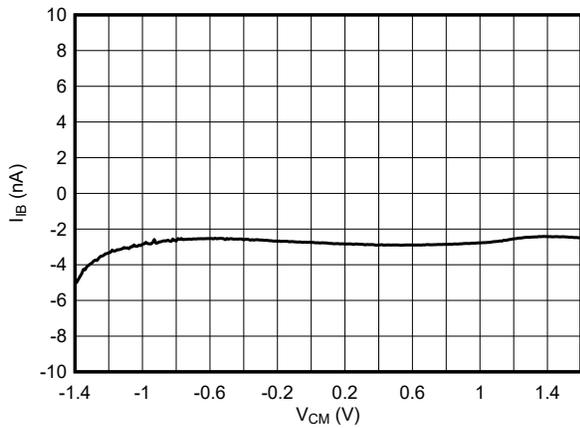
图 **6-6. Input Bias Current vs Common-Mode Input Voltage**
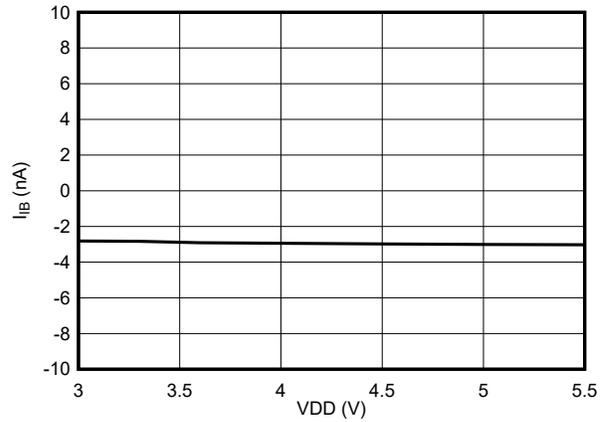
图 **6-7. Input Bias Current vs Supply Voltage**
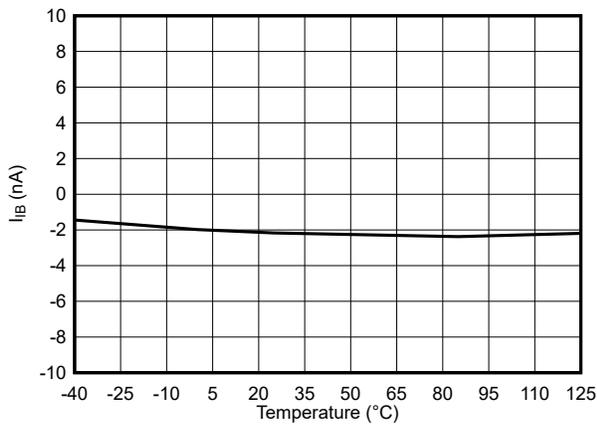
图 **6-8. Input Bias Current vs Temperature**
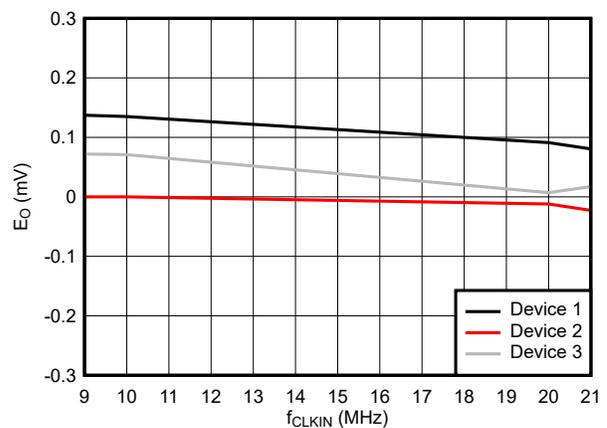
图 **6-9. Offset Error vs Clock Frequency**
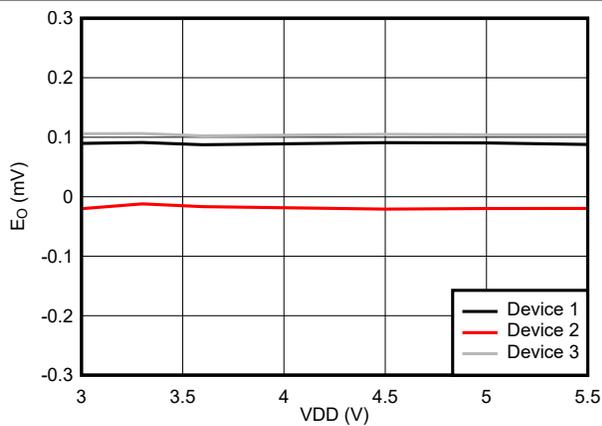
图 **6-10. Offset Error vs Supply Voltage**
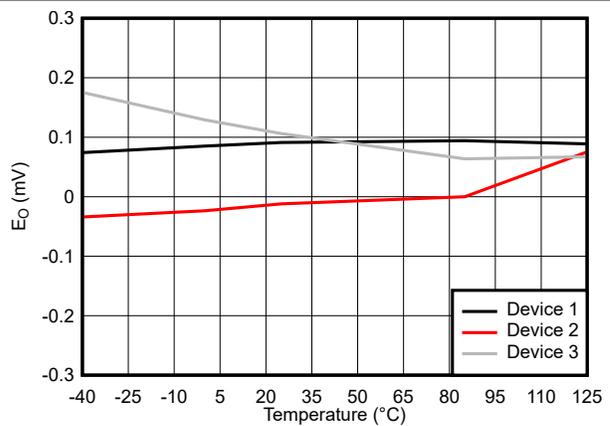
图 **6-11. Offset Error vs Temperature**

Product Folder Links: *AMC3336-Q1*

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
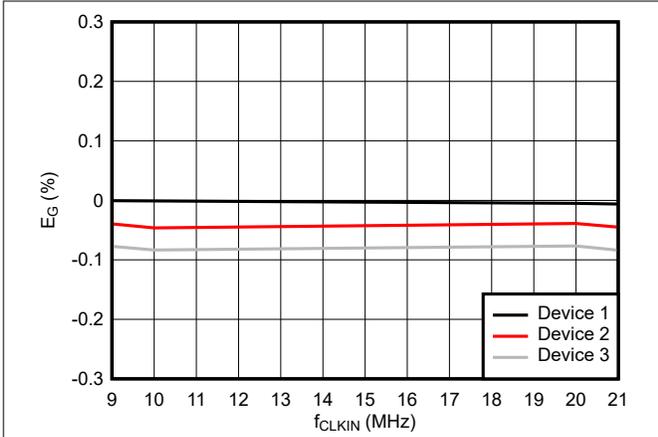


图 6-12. Gain Error vs Clock Frequency
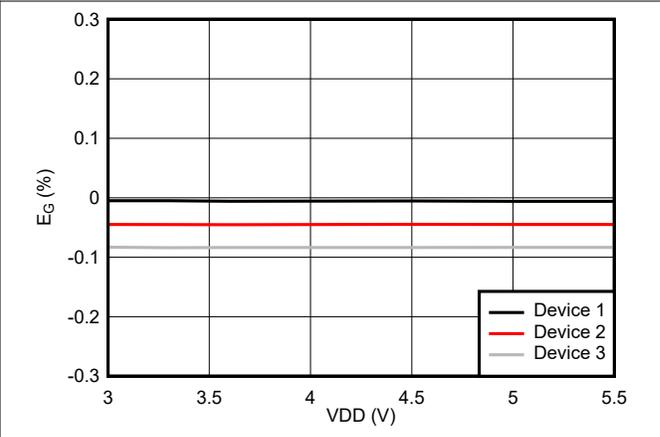


图 6-13. Gain Error vs Supply Voltage
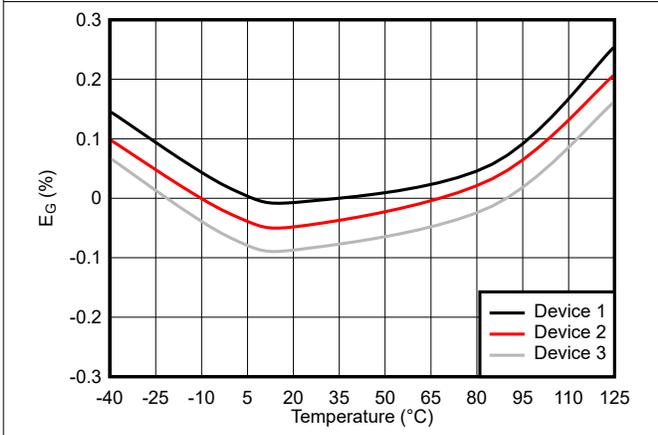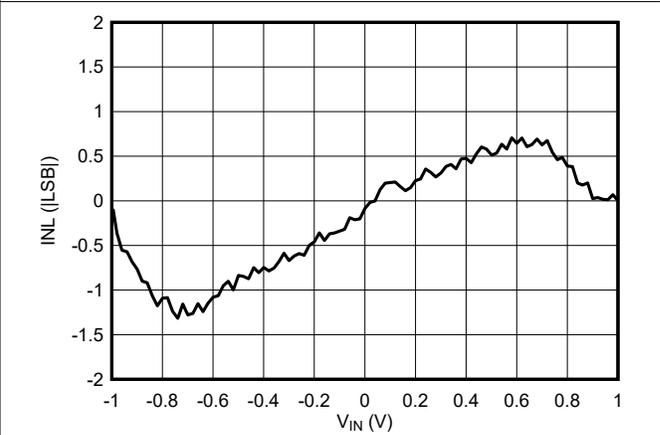


图 6-14. Gain Error vs Temperature



图 6-15. Integral Nonlinearity vs Input Voltage



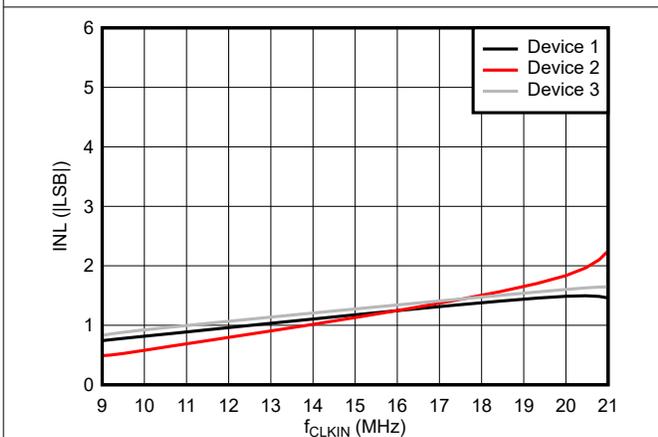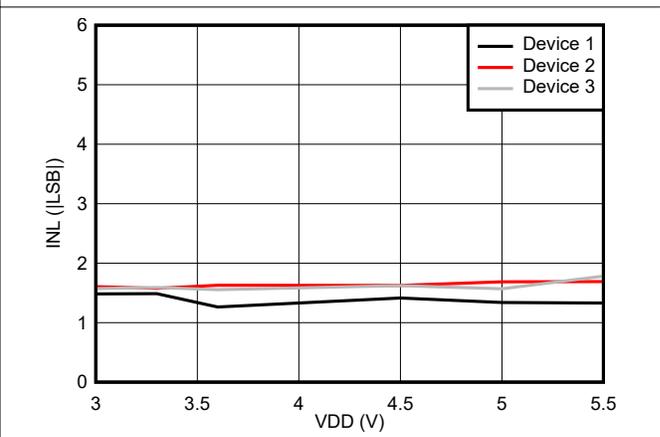图 6-16. Integral Nonlinearity vs Clock Frequency



图 6-17. Integral Nonlinearity vs Supply Voltage

Product Folder Links: *AMC3336-Q1*

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
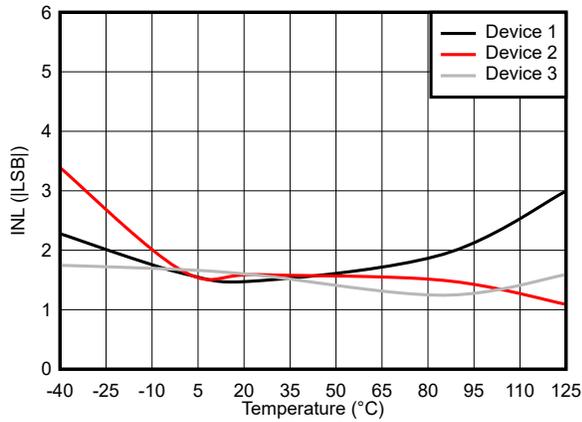


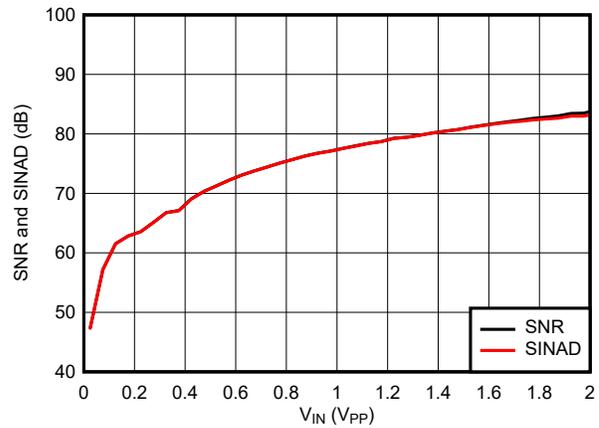图 6-18. Integral Nonlinearity vs Temperature



图 6-19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude
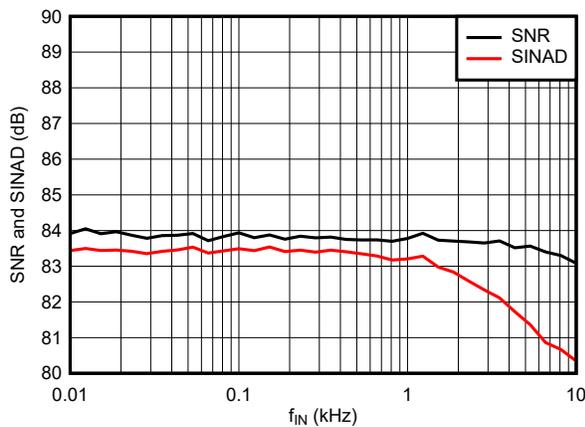


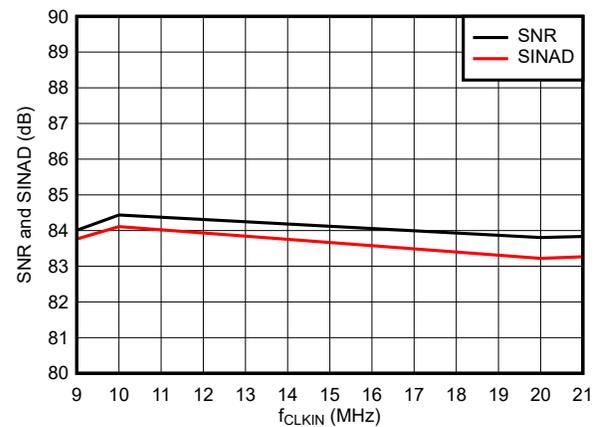图 6-20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency



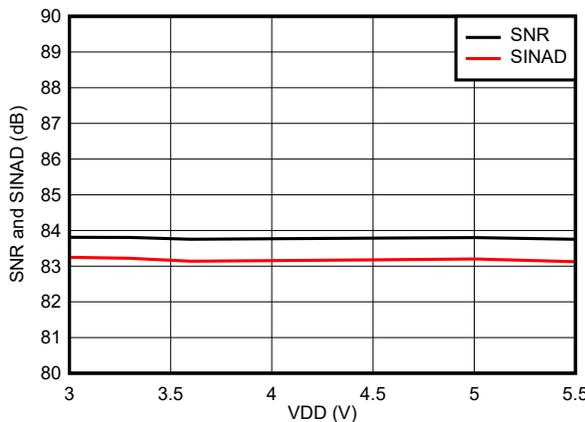图 6-21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency



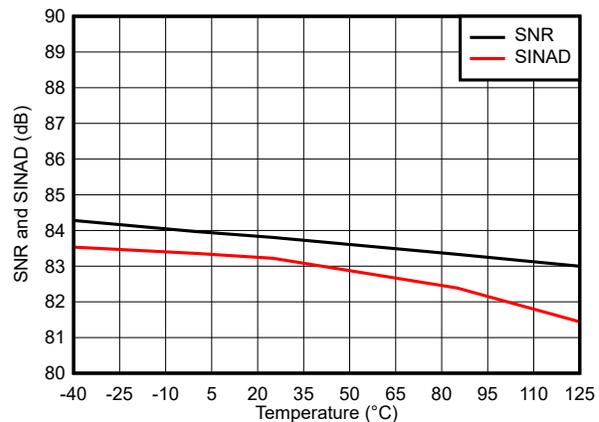图 6-22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage



图 6-23. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

Product Folder Links: *AMC3336-Q1*

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)

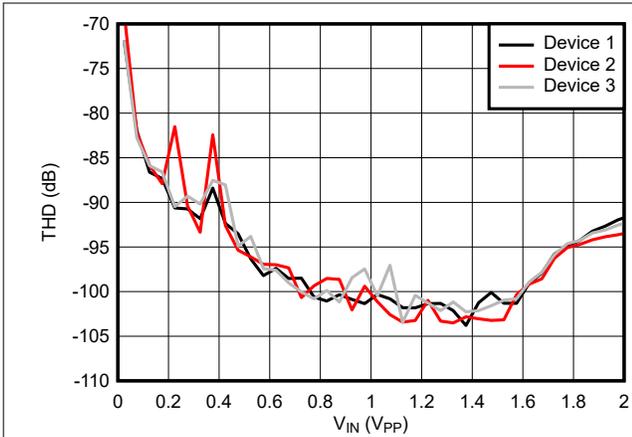图 6-24. **Total Harmonic Distortion vs Input Signal Amplitude**
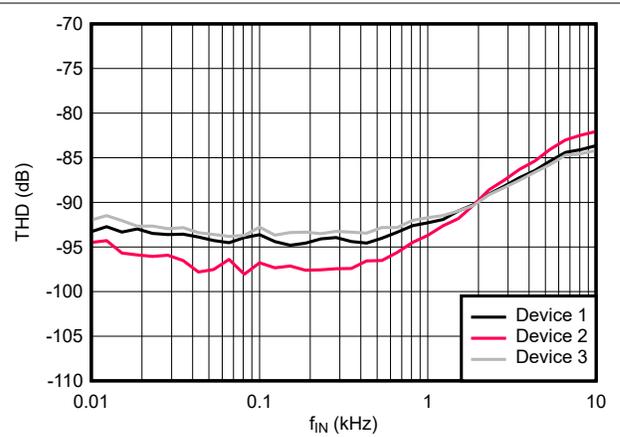
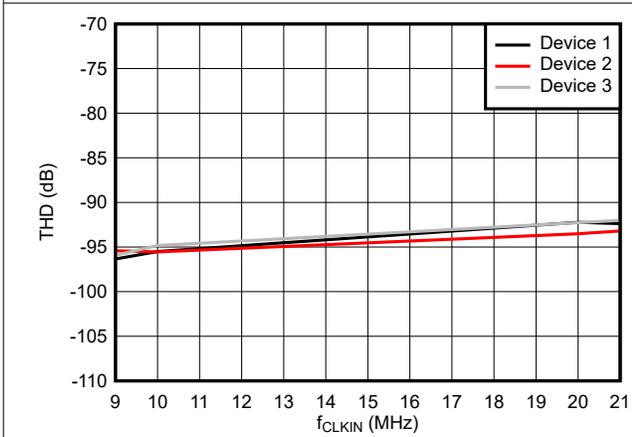图 6-25. **Total Harmonic Distortion vs Input Signal Frequency**

图 6-26. **Total Harmonic Distortion vs Clock Frequency**
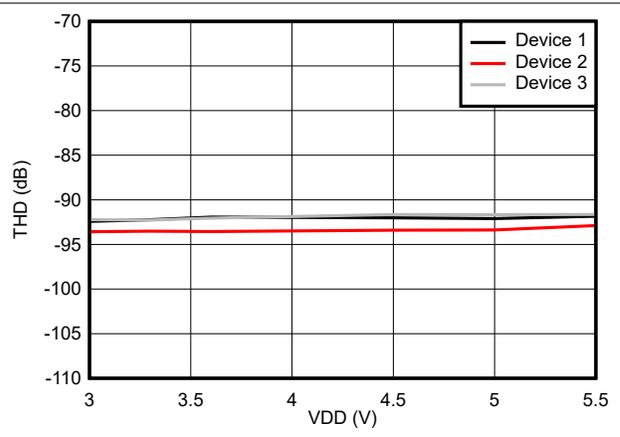
图 6-27. **Total Harmonic Distortion vs Supply Voltage**
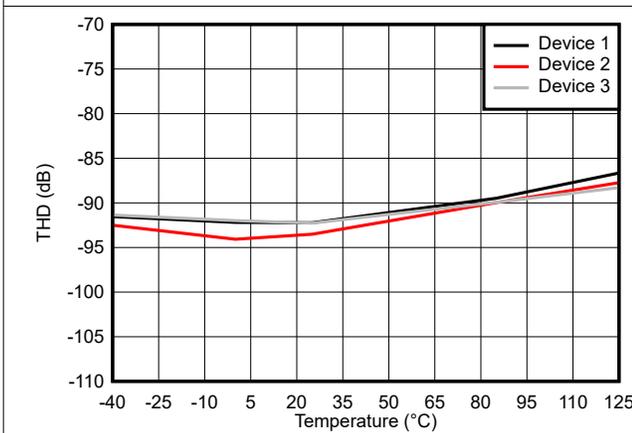
图 6-28. **Total Harmonic Distortion vs Temperature**
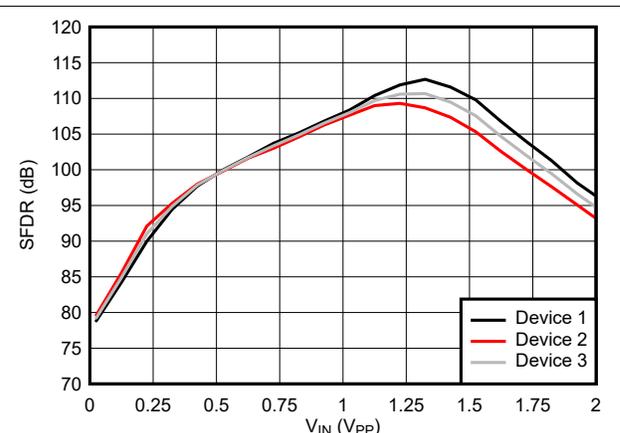
图 6-29. **Spurious-Free Dynamic Range vs Input Signal Amplitude**

Product Folder Links: *AMC3336-Q1*

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
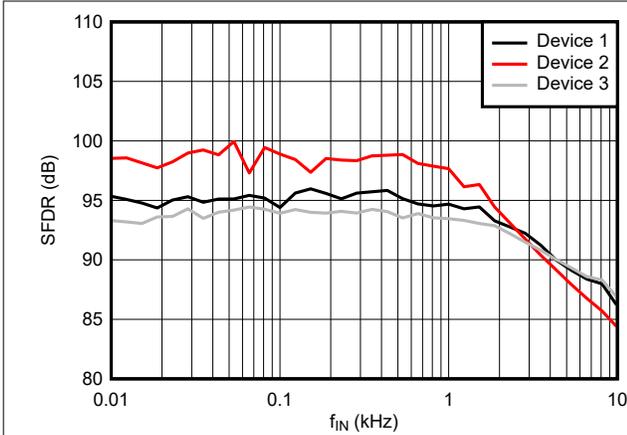
图 6-30. Spurious-Free Dynamic Range vs Input Signal Frequency
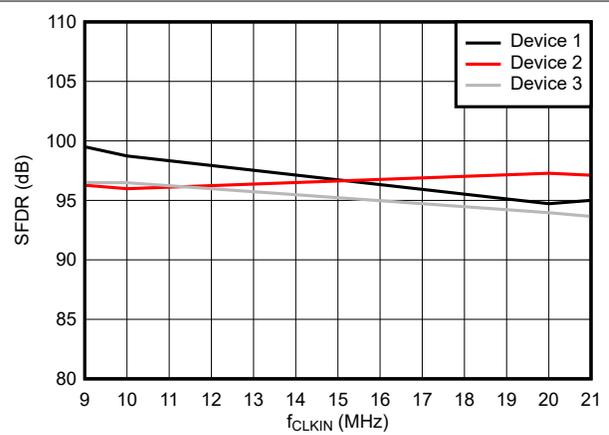
图 6-31. Spurious-Free Dynamic Range vs Clock Frequency
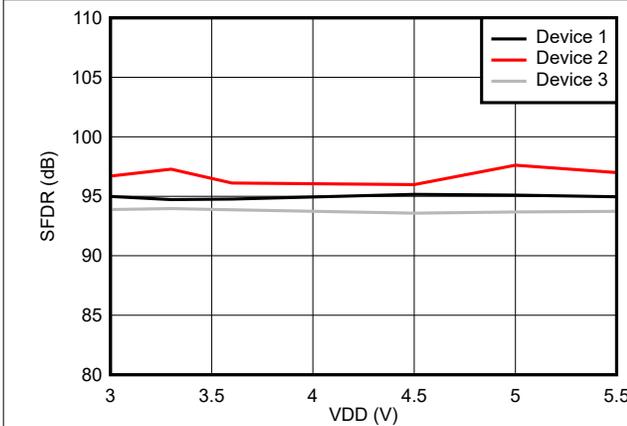
图 6-32. Spurious-Free Dynamic Range vs Supply Voltage
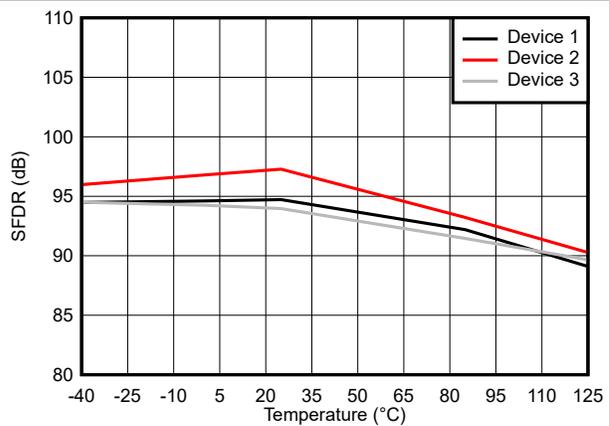
图 6-33. Spurious-Free Dynamic Range vs Temperature
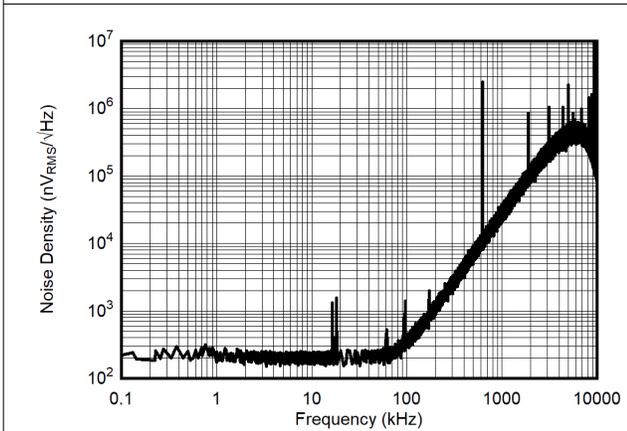
sinc$^3$, OSR = 1; Frequency bin-width equals 1 Hz

图 6-34. Noise Density With Both Inputs Shorted to HGND
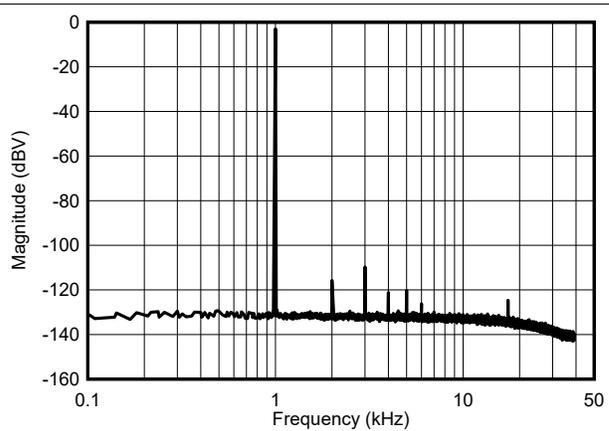
sinc$^3$, OSR = 256, $V_{IN}$ = 2 $V_{PP}$

图 6-35. Frequency Spectrum With 1-kHz Input Signal

Product Folder Links: *AMC3336-Q1*

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
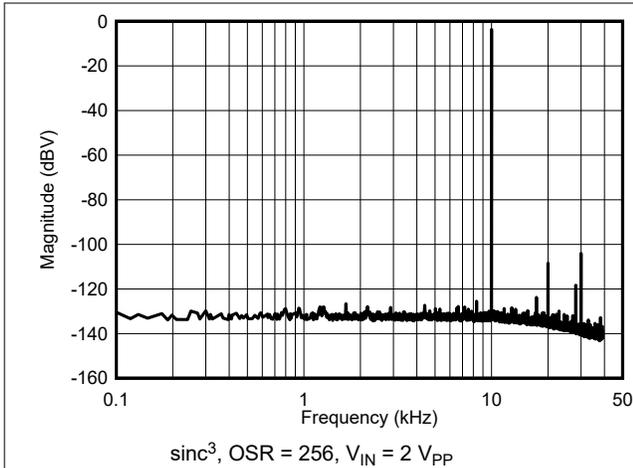
图 6-36. **Frequency Spectrum With 10-kHz Input Signal**

sinc$^3$, OSR = 256, $V_{IN}$ = 2 $V_{PP}$
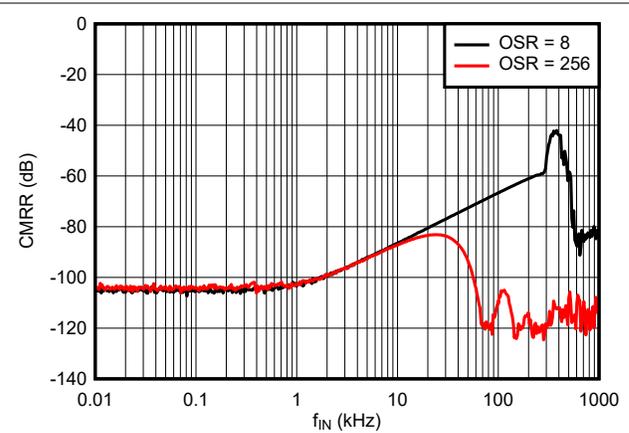
图 6-37. **Common-Mode Rejection Ratio vs Input Signal Frequency**
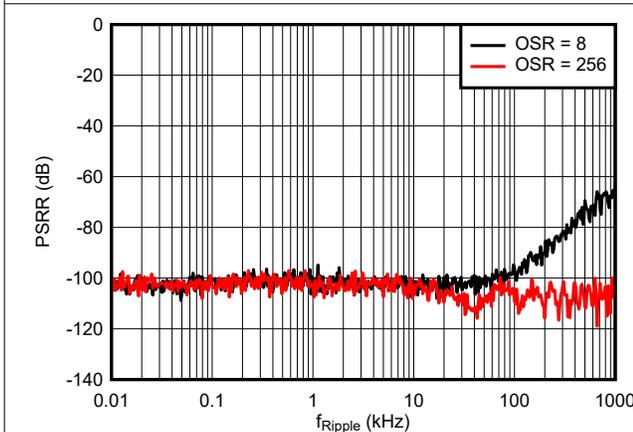
图 6-38. **Power-Supply Rejection Ratio vs Ripple Frequency**
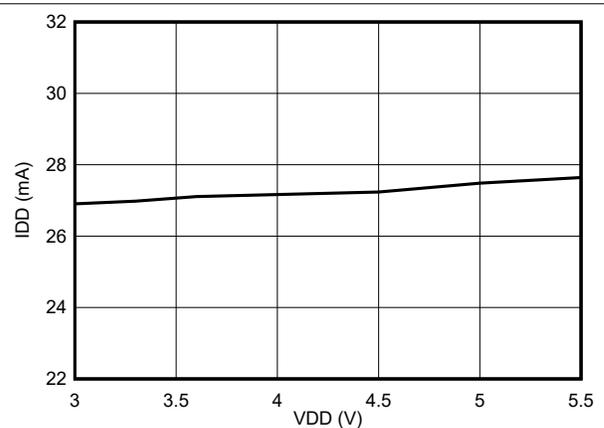
图 6-39. **Supply Current vs Supply Voltage**
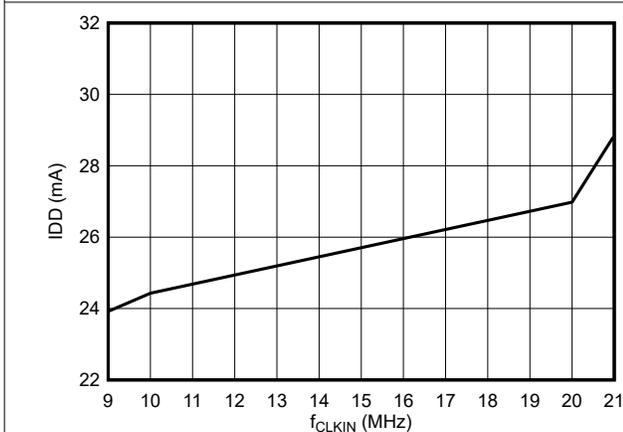
图 6-40. **Supply Current vs Clock Frequency**
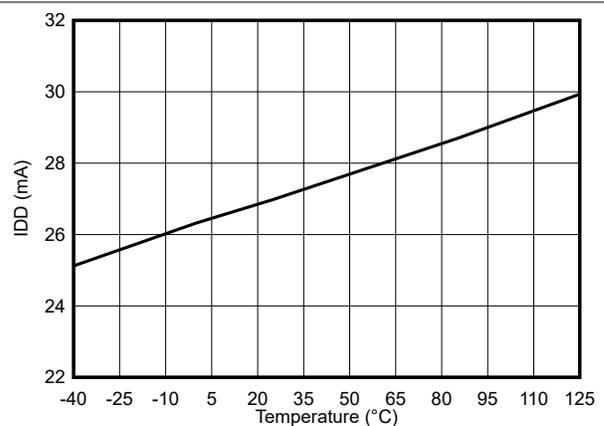
图 6-41. **Supply Current vs Temperature**

## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V , INN = AGND, $f_{CLKIN}$ = 20 MHz, sinc$^3$ filter with OSR = 256, and 16-bit resolution (unless otherwise noted)
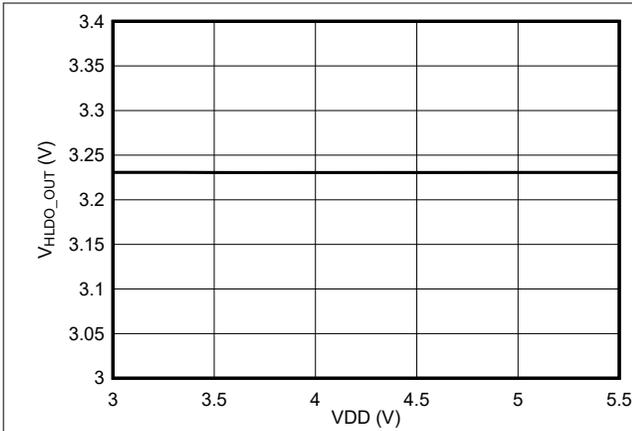
图 6-42. **High-Side LDO Output Voltage vs Supply Voltage**
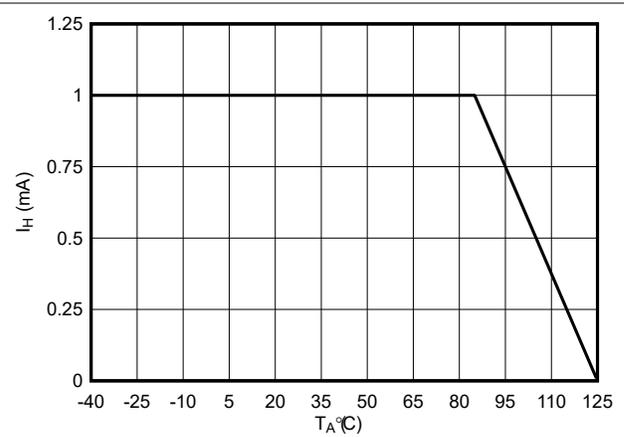
图 6-43. **$I_H$ Derating vs Ambient Temperature**

Product Folder Links: *AMC3336-Q1*

# 7 Detailed Description

## 7.1 Overview

The AMC3336-Q1 is a fully differential, precision, isolated modulator with an integrated DC/DC converter that can supply the high-side of the device from a single 3.3-V or 5-V voltage supply on the low side. The input stage of the device drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. The isolated data output DOUT of the modulator provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin. The time average of this serial bitstream output is proportional to the analog input voltage. The external clock input simplifies the synchronization of multiple measurement channels on the system level.

The signal path is isolated by a double capacitive silicon dioxide ($SiO_2$) insuation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

## 7.2 Functional Block Diagram

Product Folder Links: *AMC3336-Q1*
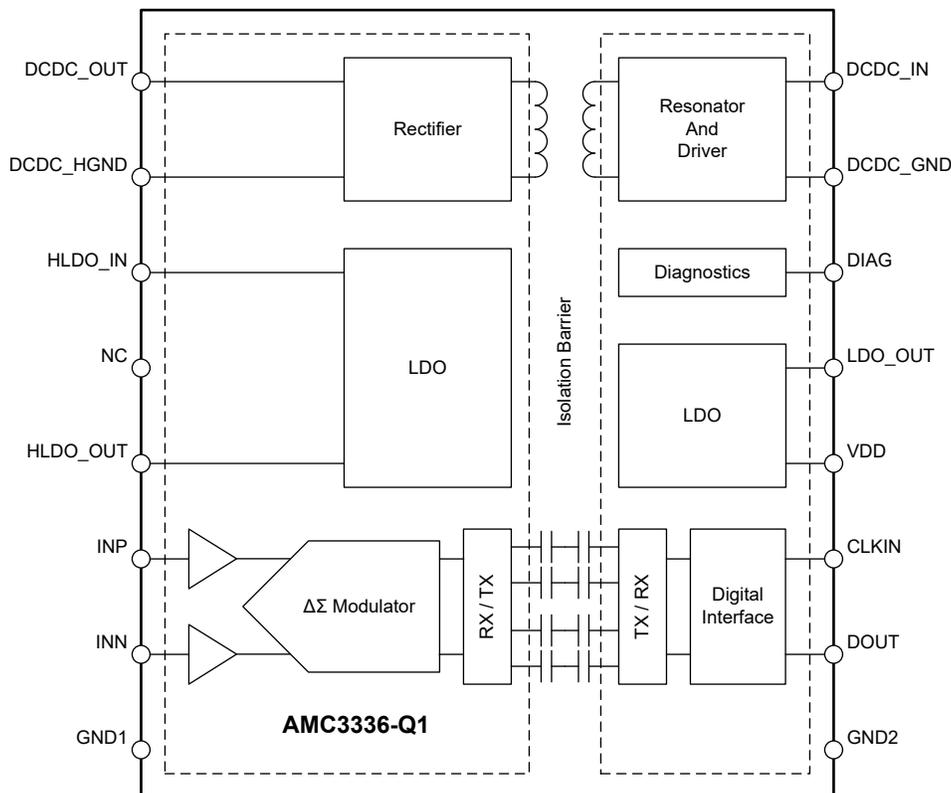
## 7.3 Feature Description

### 7.3.1 Analog Input

The high-impedance input stage of the AMC3336-Q1 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance, and low bias-current input makes the AMC3336-Q1 suitable for isolated, high-voltage-sensing applications that typically employ high impedance resistor dividers.

For reduced offset and offset drift, the input buffer is chopper-stabilized with the chopping frequency set at $f_{CLKIN}$ / 32. Quantization Noise Shaping shows the spur at 625 kHz that is generated by the chopping frequency for a modulator clock of 20 MHz.
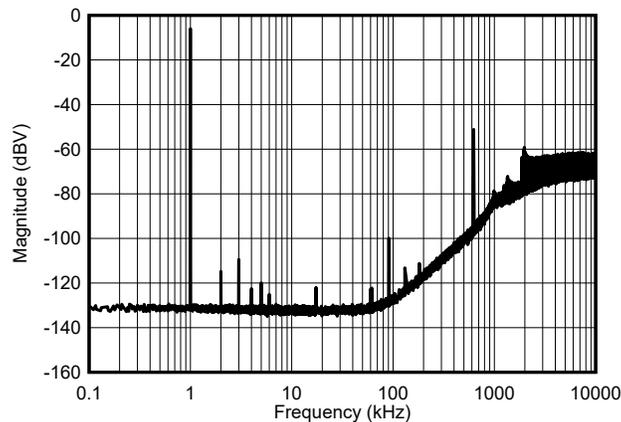


sinc[3] filter, OSR = 1, $f_{CLKIN}$ = 20 MHz, $f_{IN}$ = 1 kHz

**图 7-1. Quantization Noise Shaping**

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. Second, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range $V_{FSR}$ and within the specified input common-mode voltage range $V_{CM}$ as specified in the *Recommended Operating Conditions* table.

Product Folder Links: *AMC3336-Q1*

### 7.3.2 Modulator

图 7-2 conceptualizes the second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator implemented in the AMC3336-Q1. The analog input voltage $V_{IN}$ and the output $V_5$ of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage $V_1$ at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in an output voltage $V_3$ that is differentiated with the input signal $V_{IN}$ and the output of the first integrator $V_2$. Depending on the polarity of the resulting voltage $V_4$, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage $V_5$, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.
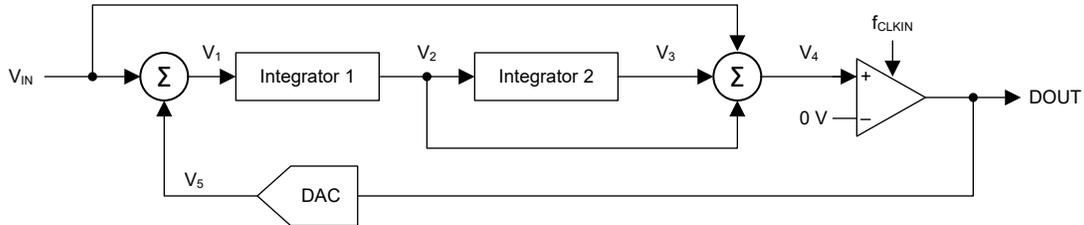


图 **7-2. Block Diagram of a Second-Order Modulator**

The modulator shifts the quantization noise to high frequencies, as depicted in Quantization Noise Shaping. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's C2000™ and Sitara™ microcontroller families offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC3336-Q1. Alternatively, a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) can be used to implement the filter.

### 7.3.3 Isolation Channel Signal Transmission

The AMC3336-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 图 7-3, to transmit the modulator output bitstream across the $SiO_2$-based isolation barrier. The transmit driver (TX) illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3336-Q1 is 480 MHz.

图 7-3 shows the concept of the on-off keying scheme.
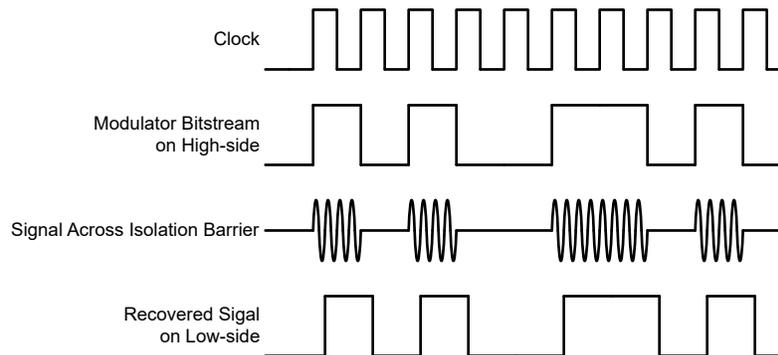


图 **7-3. OOK-Based Modulation Scheme**

### 7.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982. A differential input of – 1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC3336-Q1. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to – 1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC3336-Q1 generates a single 1 (if the input is at negative full-scale) or 0 (if the input is at positive full-scale) every 128 clock cycles to indicate proper device function (see the *Output Behavior in Case of a Full-Scale Input* section for more details). 图 7-4 shows the input voltage versus the output modulator signal.
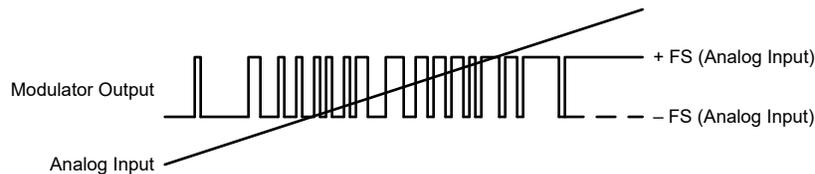


图 **7-4. Analog Input vs Modulator Output**

The density of ones in the output bitstream for any input voltage value can be calculated using 方程式 1 (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}}$$

(1)

#### 7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC3336-Q1 (that is, $|V_{IN}| \geqslant V_{Clipping}$), as shown in 图 7-5, the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed. In this way, detecting a valid full-scale input signal and differentiating it from a missing high-side supply is possible on the system level.
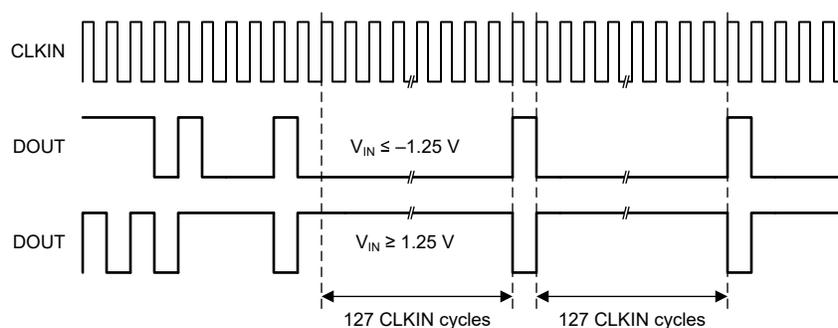


图 **7-5. Full-Scale Output of the AMC3336-Q1**

#### 7.3.4.2 Output Behavior in Case of a High-Side Supply Failure

The AMC3336-Q1 provides a fail-safe output that ensures that the output DOUT of the device offers a constant bitstream of logic 0's in case the integrated DC/DC converter output voltage is below the undervoltage detection threshold. See the *Diagnostic Output* section for more information.

### 7.3.5 Isolated DC/DC Converter

The AMC3336-Q1 offers a fully integrated isolated DC/DC converter stage that includes the following components illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the DC/DC converter. This circuit does not output a constant voltage and is not intended for driving any external load.
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path. The high-side LDO outputs a constant voltage and can provide a limited amount of current to power external circuitry.

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the $\Delta\Sigma$ modulator to minimize interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3336-Q1 and can source up to $I_H$ of additional DC current for an optional auxiliary circuit such as an active filter, preamplifier, or comparator. As shown in 图 7-6, $I_H$ is specified up to an ambient temperature of 85°C and derates linearly at higher temperatures.
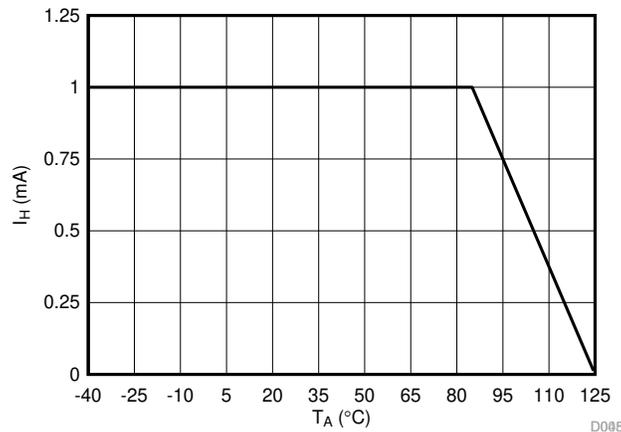
图 7-6. Derating of $I_H$ at Ambient Temperatures >85°C

### 7.3.6 Diagnostic Output

As shown in 图 7-7, the open-drain DIAG pin can be monitored to confirm the device is operational, and the output data are valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the modulator starts outputting data. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high-side). The modulator itself outputs a constant bitstream of logic 0's in this case, that is, the DOUT pin is permanently low.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. However, the modulator itself outputs a constant bitstream of logic 0's in this case, meaning that the DOUT pin is permanently low.
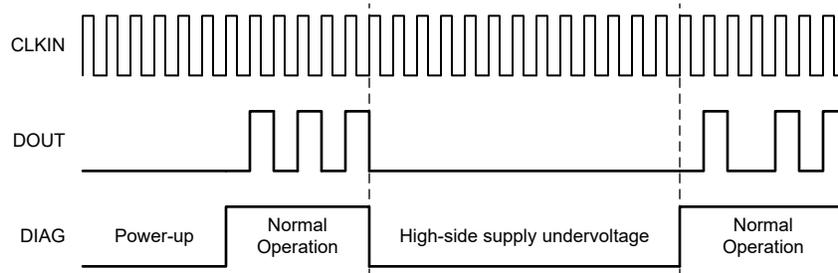


**图 7-7. DIAG and Output under Different Operating Conditions**

## 7.4 Device Functional Modes

The digital interface, including the open-drain DIAG pin are functional as soon as VDD rises above the $VDD_{POR}$ threshold. Analog functions, including the circuitry on the high-side, are enabled as soon as VDD rises above the analog under voltage lockout threshold $VDD_{UV}$ .

At power-down, analog functions are disabled as VDD falls below the $VDD_{UV}$ (falling) voltage level. The digital interface, including the open-drain DIAG pin remain functional until VDD drops below the $VDD_{POR}$ (falling) voltage level. 图 7-8 shows the different enable thresholds for the AMC3336-Q1.
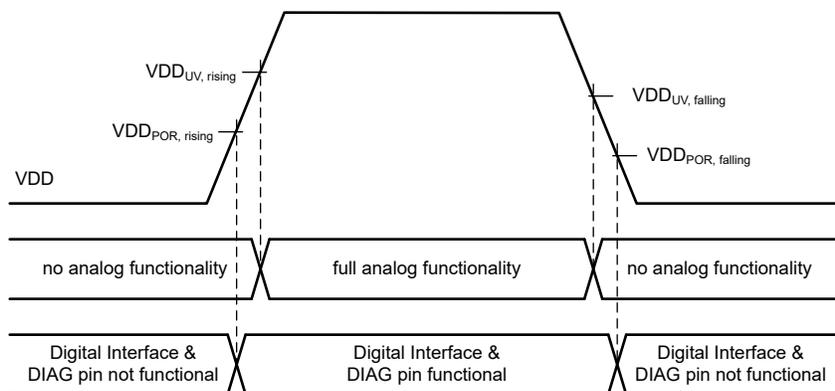


**图 7-8. AMC3336-Q1 Enable Thresholds**

Below the $VDD_{POR}$ voltage level the digital output pins are not actively driven, that is they are in a high-impedance state but clamped to one diode-voltage above the VDD supply.

# 8 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 8.1 Application Information

The very high input impedance, low AC and DC errors, and low temperature drift make the AMC3336-Q1 a high-performance solution for voltage-sensing applications. The integrated DC/DC converter simplifies the system design and allows for measuring signals independent from any high-side supply that is required with conventional isolated modulators.

### 8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, as calculated by 方程式 2, built with minimal effort and hardware, is a sinc$^3$-type filter:

$$H(z) = \left( \frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3$$

(2)

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is done with a sinc$^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits, unless specified otherwise. The measured effective number of bits (ENOB) as a function of the OSR is illustrated in 图 8-3 or the *Typical Application* section.

An example code for implementing a sinc$^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

## 8.2 Typical Application

### 8.2.1 On-Board Charger Application

Isolated modulators are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. Typical applications are AC line voltage measurements at the input of a power factor correction (PFC) stage of an onboard charger (OBC), DC measurements at the output of a PFC stage or DC/DC converter, or phase voltage measurements in traction inverters. The AMC3336-Q1 integrates an isolated power supply for the high-voltage side and therefore is particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

图 8-1 shows a simplified schematic of the AMC3336-Q1 in an OBC where the AC phase voltage on the grid-side must to be measured. At that location in the system, there is no supply readily available for powering the isolated modulator. The integrated isolated power supply, together with its bipolar input voltage range, makes the AMC3336-Q1 ideally suited for AC line-voltage sensing.

At the output of the PFC stage a second AMC3336-Q1 is used for sensing the DC-link voltage. This example also shows the proper connection for implementing a differential measurement that typically results in best measurement accuracy and linearity.
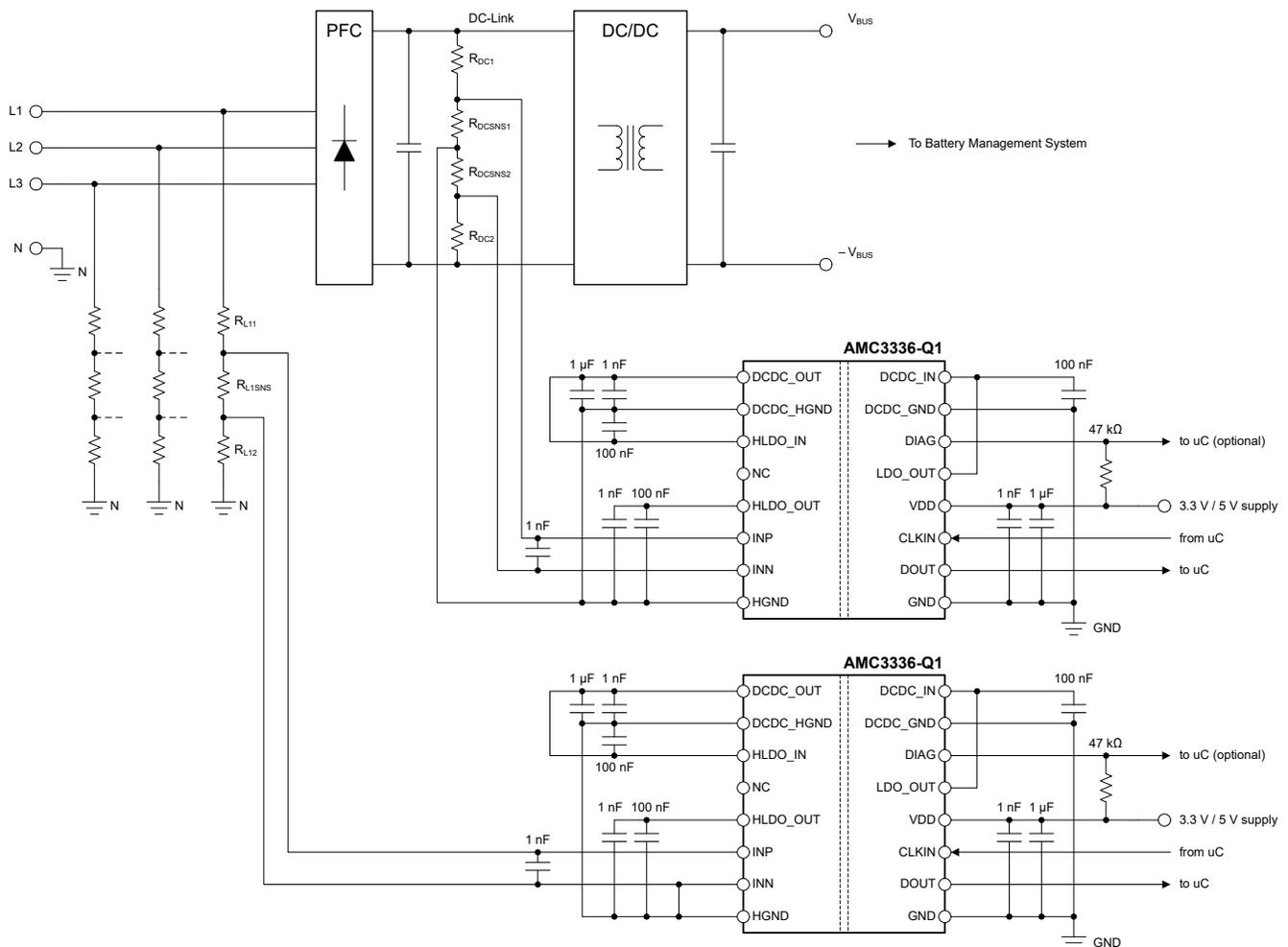


图 8-1. The AMC3336-Q1 in a Typical Application

Product Folder Links: *AMC3336-Q1*

### 8.2.1.1 Design Requirements

表 8-1 lists the parameters for this typical application.

**表 8-1. Design Requirements**

| PARAMETER | 120-$V_{RMS}$ LINE VOLTAGE | 230-$V_{RMS}$ LINE VOLTAGE |
|---|---|---|
| System input voltage | 120 V ±10%, 60 Hz | 230 V ±10%, 50 Hz |
| Low-side supply voltage | 3.3 V or 5 V | 3.3 V or 5 V |
| Maximum resistor operating voltage | 75 V | 75 V |
| Voltage drop across the sense resistor (RSNS) for a linear response | ±1 V (maximum) | ±1 V (maximum) |
| Current through the resistive divider, $I_{CROSS}$ | 100 $\mu$A | 100 $\mu$A |

### 8.2.1.2 Detailed Design Procedure

This discussion covers the 230-$V_{RMS}$ example. The procedure for calculating the resistive divider for the 120-$V_{RMS}$ use case is identical.

The 100-$\mu$A crosscurrent requirement at peak input voltage (360 V) determines that the total impedance of the resistive divider is 3.6 M$\Omega$. The impedance of the resistive divider is dominated by the top and bottom resistors (shown exemplary as RL11 and RL12 in 图 8-1) and the voltage drop across RL1SNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V, therefore the total, minimum number of unit resistors in the top and bottom portion of the resistive divider is 360 V / 75 V = 5. The calculated unit value is 3.6 M$\Omega$ / 5 = 720 k$\Omega$ and the next closest value from the E96-series is 715 k$\Omega$.

RL1SNS is sized such that the voltage drop across the resistor at maximum input voltage (360 V) equals the linear full-scale range input voltage ($V_{FSR}$) of the AMC3336-Q1 that is +1 V. This voltage is calculated as RL1SNS = $V_{FSR}$ / ($V_{Peak}$ – $V_{FSR}$) x ($R_{TOP}$ + $R_{BOT}$), where ($R_{TOP}$ + $R_{BOT}$) is the total value of the RL11 and RL12 resistor strings (5 x 715 k$\Omega$ = 3575 k$\Omega$). RL1SNS is calculated as 9.96 k$\Omega$ and the next closest value from the E96-series is 10 k$\Omega$.

表 8-2 summarizes the design of the resistive divider.

**表 8-2. Resistor Value Examples**

| PARAMETER | 120-$V_{RMS}$ LINE VOLTAGE | 230-$V_{RMS}$ LINE VOLTAGE |
|---|---|---|
| Peak voltage | 190 V | 360 V |
| Unit resistor value, RL11Xand RL12X | 634 k$\Omega$ | 715 k$\Omega$ |
| Number of unit resistors in RL11 | 1 | 2 |
| Number of unit resistors in RL12 | 2 | 3 |
| Sense resistor value, RL1SNS | 10 k$\Omega$ | 10 k$\Omega$ |
| Total resistance value | 1912 k$\Omega$ | 3585 k$\Omega$ |
| Resulting current through resistive divider, $I_{CROSS}$ | 99.4 $\mu$A | 100.4 $\mu$A |
| Resulting full-scale voltage drop across sense resistor RL1SNS | 0.994 V | 1.004 V |
| Peak power dissipated in unit resistor RL11X and RL12X | 6.3mW | 7.2 mW |
| Peak power dissipated in resistive divider | 18.9 mW | 36.2 mW |

The AMC3336-Q1 requires a single 3.3-V or 5-V supply on its low-side. The high-side supply is internally generated by an integrated DC/DC converter, as explained in the *Isolated DC/DC Converter* section.

#### 8.2.1.2.1 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency ($f_{CLKIN}$) of the internal $\Delta \Sigma$ modulator
- The DC impedance of the filter does not generate significant voltage drop in the analog input lines
- The source impedance of the analog inputs are equal

Most voltage-sensing applications use high-impedance resistive dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in 图 8-2) is sufficient to filter the input signal.



**AMC3336-Q1**
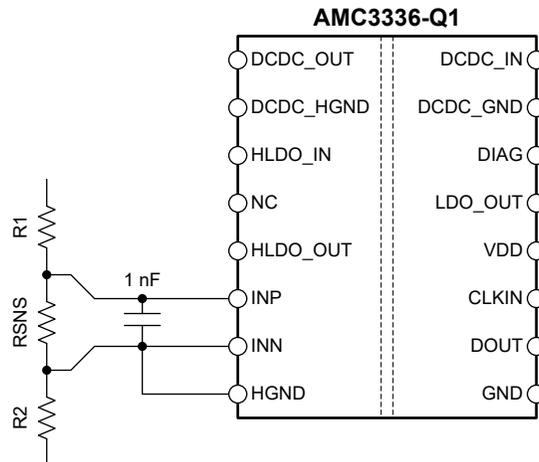
图 8-2. Input Filter

#### 8.2.1.2.2 Bitstream Filtering

For modulator output bitstream filtering, a device from TI's C2000™ or Sitara™ microcontroller families is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high-accuracy results for the control loop and one fast-response path for overcurrent detection.

A *delta-sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter-order to achieve the desired output resolution and filter response time.

### 8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and $\Delta\Sigma$ modulators. 图 8-3 shows the ENOB of the AMC3336-Q1 with different oversampling ratios. By using 方程式 3, this number can also be calculated from the SINAD:

SINAD = 1.76 dB + 6.02 dB x ENOB (3)
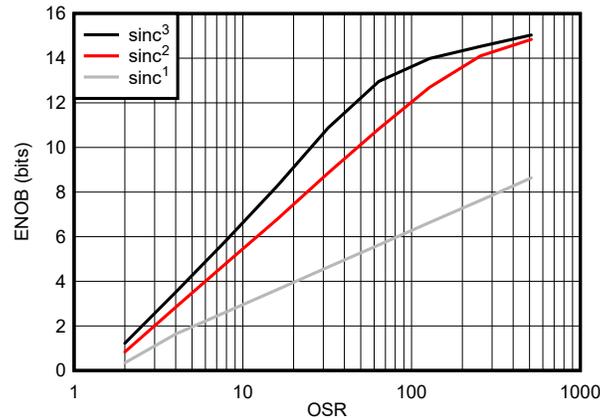


**图 8-3. Measured Effective Number of Bits vs Oversampling Ratio**

### 8.2.2 What To Do and What Not To Do

Do not leave the inputs of the AMC3336-Q1 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the modulator outputs a bitstream that is undefined.

Connect the high-side ground (HGND) to INN, either directly or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range, as specified in the *Recommended Operating Conditions* table.

The high-side LDO can source a limited amount of current ($I_H$) to power external circuitry. Take care not to over-load the high-side LDO and be aware of the drating of $I_H$ at high temperatures as explined in the *Isolated DC/DC Converter* section.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the HLDO_OUT pin.

# 9 Power Supply Recommendations

The AMC3336-Q1 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V (or 5 V). TI recommends a low ESR decoupling capacitor of 1 nF (C8 in 图 9-1) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR, 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3336-Q1, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the sense resistor that is connected to the negative input (INN) of the device. IIN and HGND can be shorted together directly at the device pins. The high-side DC/DC ground terminal (DCDC_HGND) is also shorted to HGND directly at the device pins.
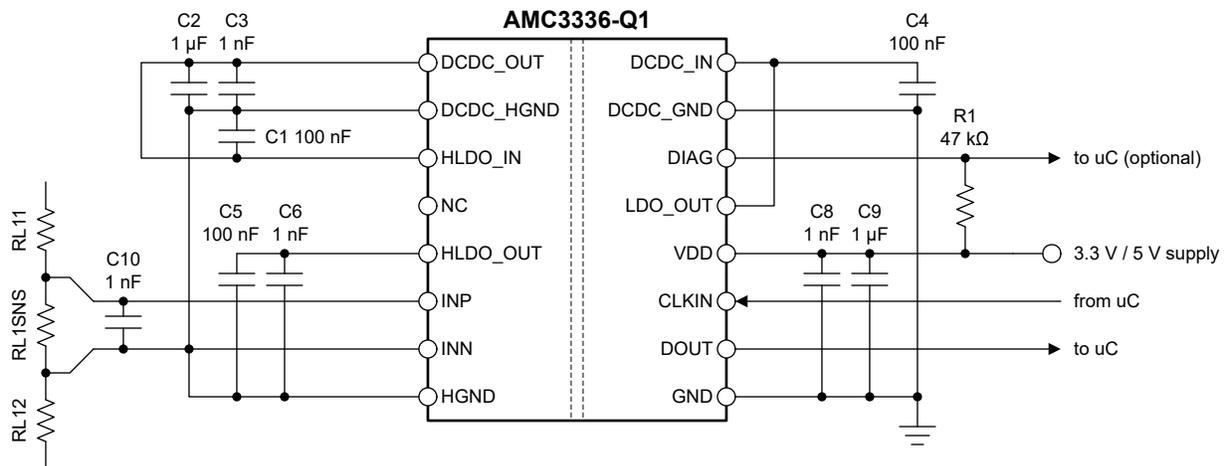


图 9-1. Decoupling the AMC3336-Q1

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

表 9-1 lists components suitable for use with the AMC3336-Q1. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3336-Q1.

表 9-1. Recommended External Components

| DESCRIPTION | PART NUMBER | MANUFACTURER | SIZE (EIA, L x W) |
|---|---|---|---|
| **VDD** | | | |
| C8 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |
| C9 | 1 µF ± 10%, X7R, 25 V | 12063C105KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |
| **DC/DC CONVERTER** | | | |
| C4 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C3 | 1 nF ± 10%, X7R, 50 V | C0603C102K5RACTU | Kemet | 0603, 1.6 mm x 0.8 mm |
| C2 | 1 µF ± 10%, X7R, 25 V | CGA3E1X7R1E105K080AC | TDK | 0603, 1.6 mm x 0.8 mm |
| **HLDO** | | | |
| C1 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C5 | 100 nF ± 5%, NP0, 50 V | C3216NP01H104J160AA | TDK | 1206, 3.2 mm x 1.6 mm |
| C6 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |

Product Folder Links: AMC3336-Q1

## 10 Layout

### 10.1 Layout Guidelines

图 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors. The same reference designators are used as in the *Power Supply Recommendations* section. Decoupling capacitors are placed as close as possible to the AMC3336-Q1 supply pins. For best performance, place the sense resistor close to the INP and INN inputs of the AMC3336-Q1 and keep the layout of both connections symmetrical.

This layout is used on the AMC3336-Q1 EVM and supports CISPR-11 compliant electromagnetic radiation levels.
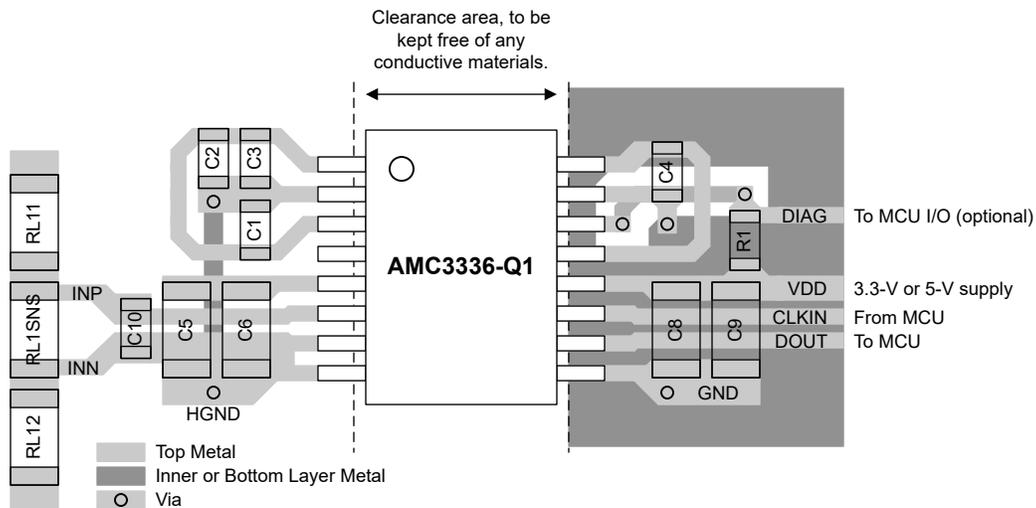
### 10.2 Layout Example



图 **10-1. Recommended Layout of the AMC3336-Q1**

Product Folder Links: *AMC3336-Q1*

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

#### 11.1.1.1 Isolation Glossary

See the *Isolation Glossary*

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

## 11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

TI Glossary        This glossary lists and explains terms, acronyms, and definitions.

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要声明和免责声明

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AMC3336QDWERQ1 | Active | Production | SOIC (DWE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3336Q |
| AMC3336QDWERQ1.A | Active | Production | SOIC (DWE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3336Q |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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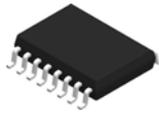
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AMC3336-Q1 :**

• Catalog : AMC3336

NOTE: Qualified Version Definitions:
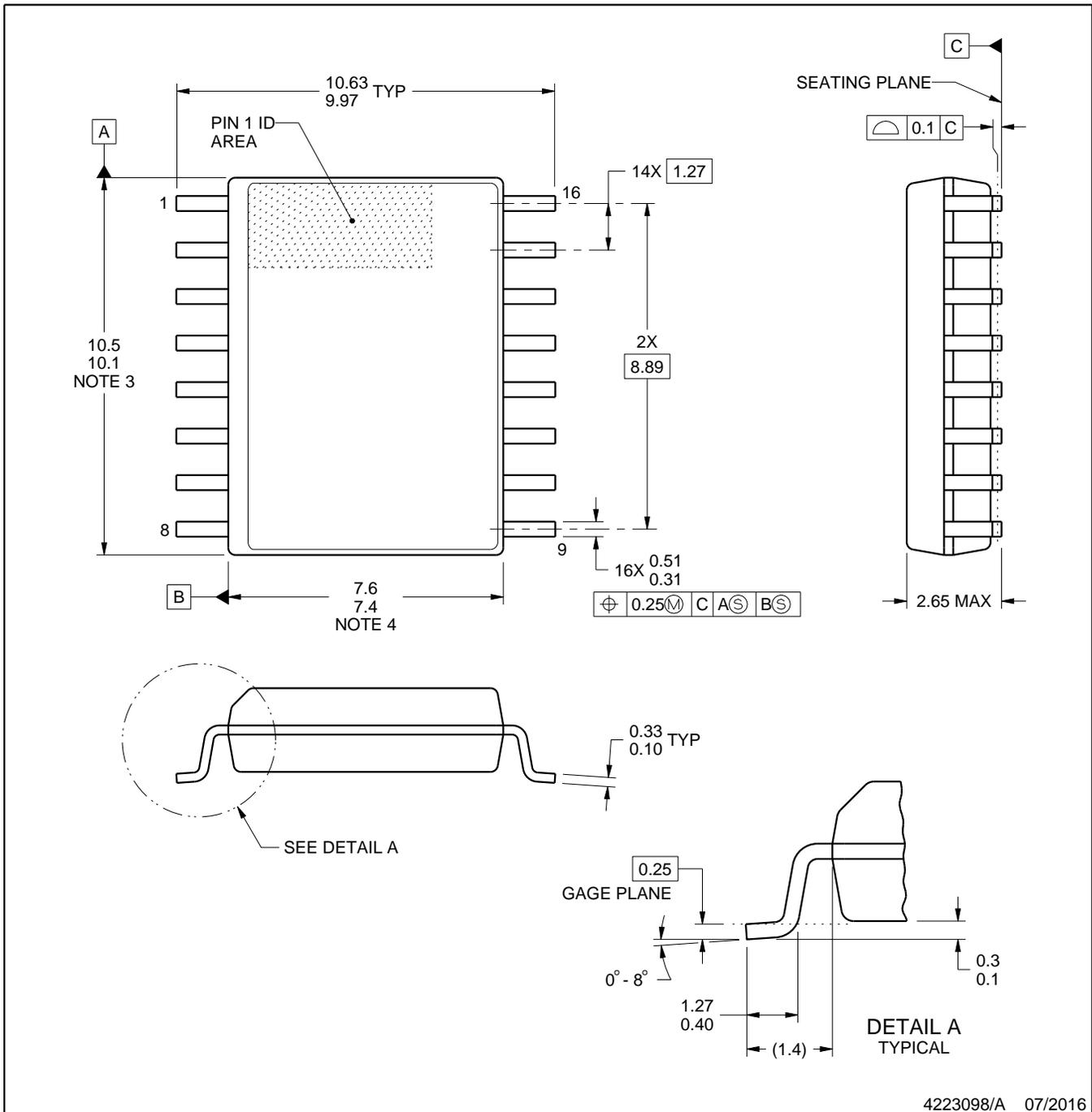
- Catalog - TI's standard catalog product

C

SEATING PLANE

0.1 C

10.63
9.97 TYP

A

PIN 1 ID
AREA

14X 1.27

1

16

10.5
10.1
NOTE 3

2X
8.89

8

9

16X 0.51
0.31

B

7.6
7.4
NOTE 4

0.25 M  C  A S  B S

2.65 MAX

0.33
0.10 TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

1.27
0.40

(1.4)

0.3
0.1

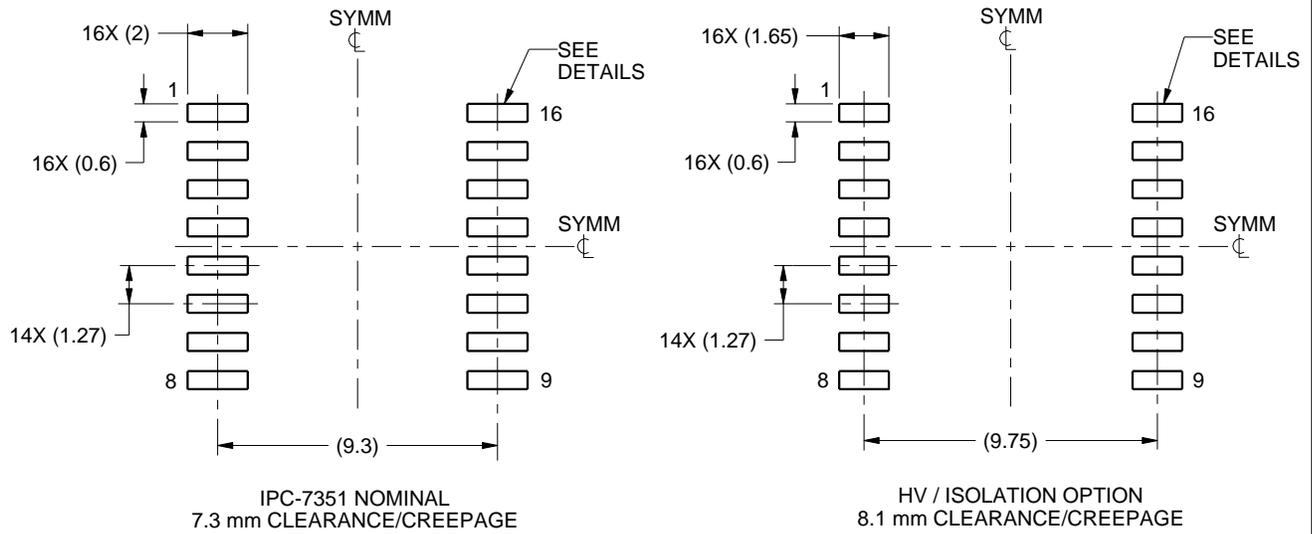DETAIL A
TYPICAL

4223098/A    07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

16X (2)

SYMM

SEE
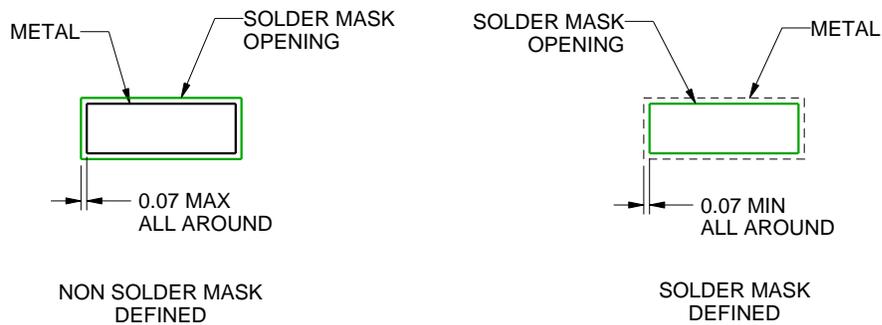DETAILS

1

16X (0.6)

16

SYMM

14X (1.27)

8

9

(9.3)

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

16X (1.65)

SYMM

SEE
DETAILS

1

16X (0.6)

16

SYMM

14X (1.27)

8

9

(9.75)

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X

METAL

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
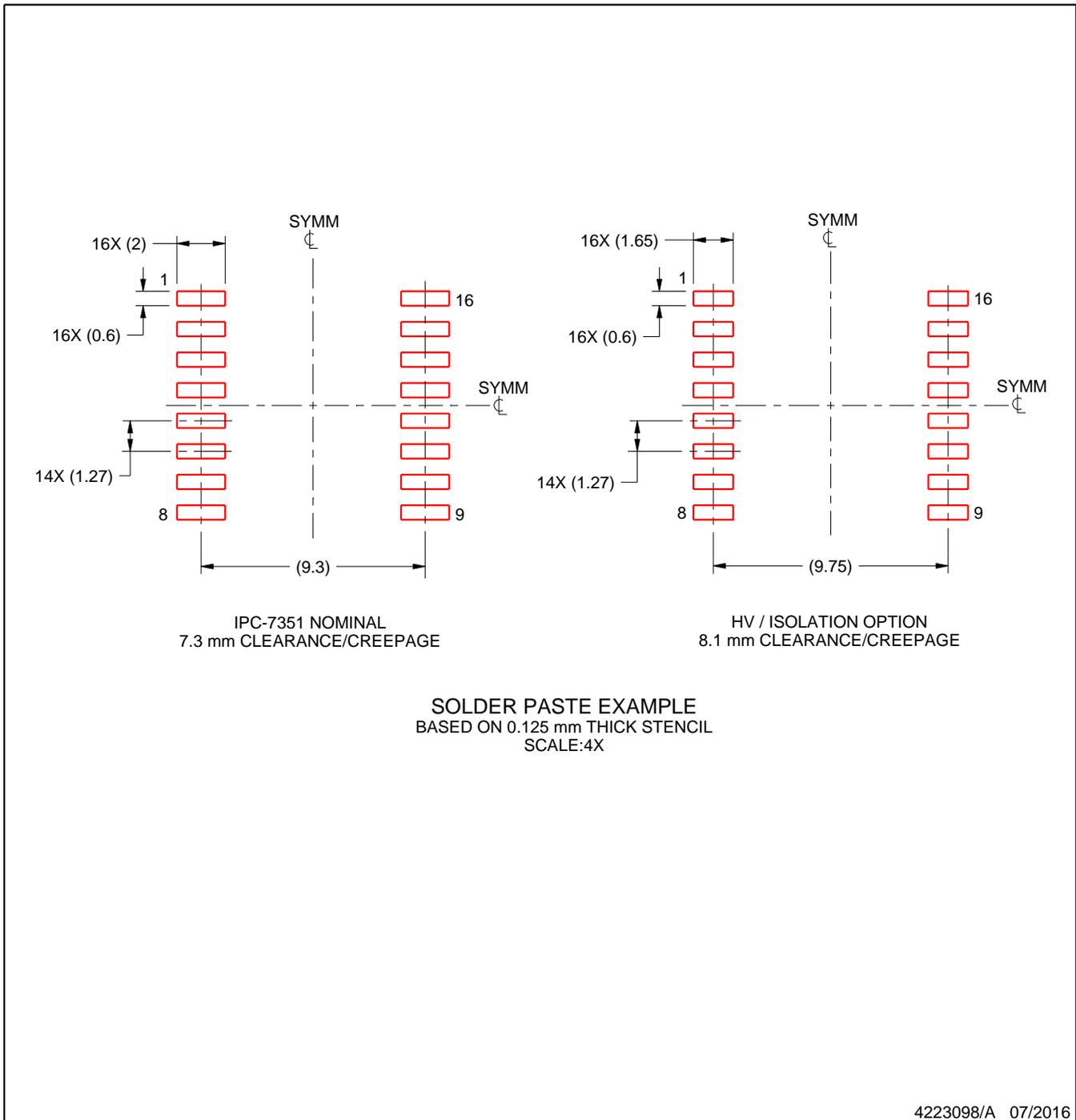
4223098/A   07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A   07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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