

LMK1D120x 低附加抖动 LVDS 缓冲器

1 特性

- 具有 2 路输入和 4 路输出 (2:4) 或 8 路输出 (2:8) 的高性能 LVDS 时钟缓冲器系列。
- 输出频率最高可达 2GHz。
- 电源电压：1.71 V 至 3.465 V
- 低附加抖动：156.25MHz 下最大抖动小于 60fs RMS (12kHz 至 20MHz)
 - 超低相位本底噪声：-164dBc/Hz (典型值)
- 超低传播延迟：< 575ps (最大值)
- 输出偏斜：20ps (最大值)
- 通用输入接受 LVDS、LVPECL、LVCMOS、LP-HCSL、HCSL 和 CML 输入
- LVDS 基准电压 (V_{AC_REF}) 适用于容性耦合输入
- 工业温度范围：-40°C 至 105°C
- 可用封装：
 - LMK1D1204：3mm × 3mm 16 引脚 VQFN (RGT) 封装
 - LMK1D1208：5mm × 5mm 28 引脚 VQFN (RHD) 封装

2 应用

- 电信及网络
- 医疗成像
- 测试和测量
- 无线基础设施
- 专业音频、视频和标牌

3 说明

LMK1D120x 时钟缓冲器能够以超低的时钟分配偏斜，将两个可选时钟输入 (IN0 和 IN1) 之一分配给 4 或 8 对差分 LVDS 时钟输出 (OUT0 至 OUT7)。LMK1D12x 系列可接受两个时钟源传入一个输入多路复用器。输入可以为 LVDS、LVPECL、LP-HCSL、HCSL、CML 或 LVCMOS。

LMK1D12x 专为驱动 50 Ω 传输线路而设计。在以单端模式驱动输入的情况下，必须将图 9-6 中所示的适当偏置电压施加到未使用的负输入引脚。

IN_SEL 引脚用于选择要发送到输出的输入。如果该引脚保持开路，该引脚将禁用输出 (逻辑低电平)。该器件支持失效防护功能。该器件还整合了输入迟滞，可防止在没有输入信号的情况下输出随机振荡。

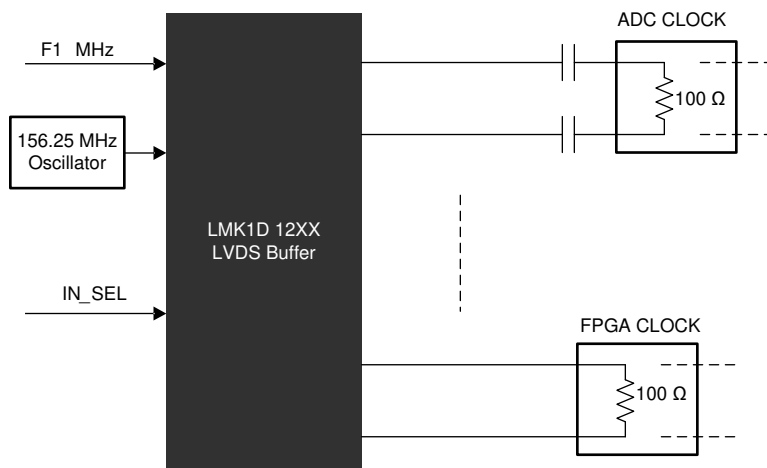
该器件可在 1.8V、2.5V 或 3.3V 电源环境下工作，温度范围是 -40°C 至 105°C (环境温度)。下表显示了 LMK1D12x 封装类型：

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值) ⁽²⁾
LMK1D1204	VQFN (16)	3.00mm × 3.00mm
LMK1D1208	VQFN (28)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



应用示例



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (August 2021) to Revision B (June 2023)	Page
• 将表标题从“器件信息”更改为“封装信息”	1
• Added the <i>Device Comparison</i> table for LMK1Dxxxx buffer family of devices.....	3
• Moved the <i>Power Supply Recommendations</i> and <i>Layout</i> sections to the <i>Application and Implementation</i> section.....	18

Changes from Revision * (December 2020) to Revision A (August 2021)	Page
• 首次公开发布.....	1

5 Device Comparison

表 5-1. Device Comparison

DEVICE	DEVICE TYPE	FEATURES	OUTPUT SWING	PACKAGE	BODY SIZE
LMK1D2108	Dual 1:8	Global output enable and swing control through pin control	350 mV	VQFN (48)	7.00 mm × 7.00 mm
			500 mV		
LMK1D2106	Dual 1:6	Global output enable and swing control through pin control	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D2104	Dual 1:4	Global output enable and swing control through pin control	350 mV	VQFN (28)	5.00 mm × 5.00 mm
			500 mV		
LMK1D2102	Dual 1:2	Global output enable and swing control through pin control	350 mV	VQFN (16)	3.00 mm × 3.00 mm
			500 mV		
LMK1D1216	2:16	Global output enable control through pin control	350 mV	VQFN (48)	7.00 mm × 7.00 mm
			500 mV		
LMK1D1212	2:12	Global output enable control through pin control	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208P	2:8	Individual output enable control through pin control	350 mV	VQGN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208I	2:8	Individual output enable control through I ² C	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208	2:8	Global output enable control through pin control	350 mV	VQFN (28)	5.00 mm × 5.00 mm
LMK1D1204P	2:4	Individual output enable control through pin control	350 mV	VQGN (28)	5.00 mm × 5.00 mm
LMK1D1204	2:4	Global output enable control through pin control	350 mV	VQFN (16)	3.00 mm × 3.00 mm

6 Pin Configuration and Functions

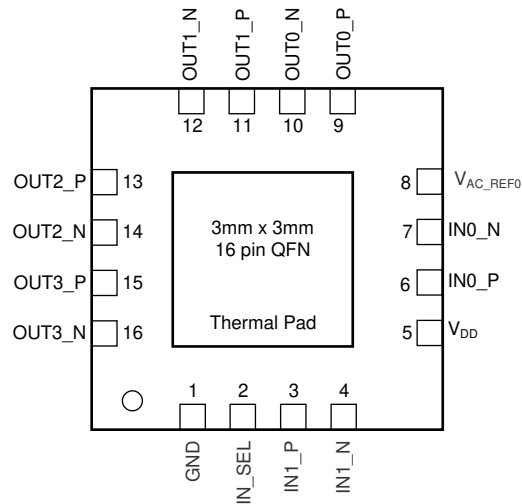


图 6-1. LMK1D1204: RGT Package 16-Pin VQFN Top View

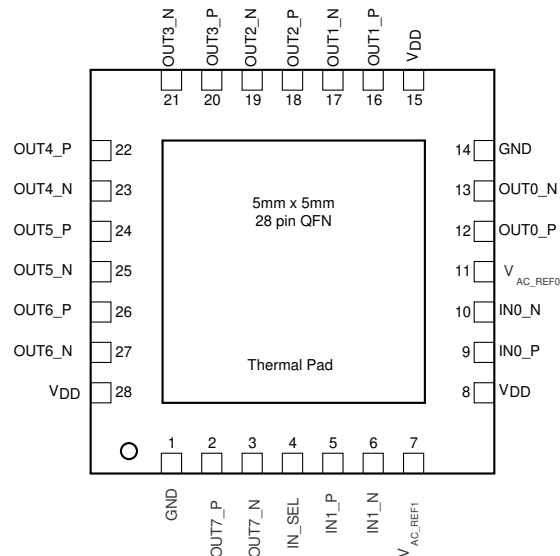


图 6-2. LMK1D1208: RHD Package 28-Pin VQFN Top View

表 6-1. Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	LMK1D1204	LMK1D1208		
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT				
IN0_P	6	9	I	Primary: Differential input pair or single-ended input
IN0_N	7	10		
IN1_P	3	5	I	Secondary: Differential input pair or single-ended input.
IN1_N	4	6		Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N.
INPUT SELECT				
IN_SEL	2	4	I	Input Selection with an internal 500-k Ω pullup and 320-k Ω pulldown resistor, selects input port; (See 表 9-1)

表 6-1. Pin Functions (continued)

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	LMK1D1204	LMK1D1208		
BIAS VOLTAGE OUTPUT				
V _{AC_REF0}	8	11	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-μF capacitor to GND on this pin.
V _{AC_REF1}	—	7		
DIFFERENTIAL CLOCK OUTPUT				
OUT0_P	9	12	O	Differential LVDS output pair number 0
OUT0_N	10	13		
OUT1_P	11	16	O	Differential LVDS output pair number 1
OUT1_N	12	17		
OUT2_P	13	18	O	Differential LVDS output pair number 2
OUT2_N	14	19		
OUT3_P	15	20	O	Differential LVDS output pair number 3
OUT3_N	16	21		
OUT4_P	—	22	O	Differential LVDS output pair number 4
OUT4_N		23		
OUT5_P	—	24	O	Differential LVDS output pair number 5
OUT5_N		25		
OUT6_P	—	26	O	Differential LVDS output pair number 6
OUT6_N		27		
OUT7_P	—	2	O	Differential LVDS output pair number 7
OUT7_N		3		
SUPPLY VOLTAGE				
V _{DD}	5	8	P	Device Power Supply (1.8V or 2.5V or 3.3V)
		15		
		28		
GROUND				
GND	1	1	G	Ground
	—	14		
MISC				
DAP	DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
NC	—	—	NC	No Connection

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	– 0.3	3.6	V
V _{IN}	Input voltage	– 0.3	3.6	V
V _O	Output voltage	– 0.3	V _{DD} + 0.3	V
I _{IN}	Input current	– 20	20	mA
I _O	Continuous output current	– 50	50	mA
T _J	Junction temperature		135	°C
T _{stg}	Storage temperature ⁽²⁾	– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Device unpowered

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90% of V _{DD})	0.1		20	ms
T _A	Operating free-air temperature		– 40		105	°C
T _J	Operating junction temperature		– 40		135	°C

7.4 Electrical Characteristics

V_{DD} = 1.8 V ± 5 %, – 40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS					
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)					
f _{IN}	Input frequency	Clock input	DC	250	MHz
V _{IN,S-E}	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4	3.465	V
dV _{IN} /dt	Input Slew Rate (20% to 80% of the amplitude)		0.05		V/ns
I _{IH}	Input high current	V _{DD} = 3.465 V, V _{IH} = 3.465 V		50	μA

$V_{DD} = 1.8 \text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are at $V_{DD} = 1.8 \text{ V}$, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IL}	Input low current	V _{DD} = 3.465 V, V _{IL} = 0 V	- 30			μA
C _{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT (Applies to V _{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f _{IN}	Input frequency	Clock input			2	GHz
V _{IN,DIFF(P-P)}	Differential input voltage peak-to-peak {2*(V _{INP} -V _{INN})}	V _{ICM} = 1 V (V _{DD} = 1.8 V)	0.3		2.4	V _{PP}
		V _{ICM} = 1.25 V (V _{DD} = 2.5 V/3.3 V)	0.3		2.4	
V _{ICM}	Input common mode voltage	V _{IN,DIFF(P-P)} > 0.4 V (V _{DD} = 1.8 V/2.5/3.3 V)	0.25		2.3	V
I _{IH}	Input high current	V _{DD} = 3.465 V, V _{INP} = 2.4 V, V _{INN} = 1.2 V			30	μA
I _{IL}	Input low current	V _{DD} = 3.465 V, V _{INP} = 0 V, V _{INN} = 1.2 V	- 30			μA
C _{IN_S-E}	Input capacitance (Single-ended)	at 25°C		3.5		pF
LVDS DC OUTPUT CHARACTERISTICS						
V _{OC(SS)}	Steady-state common mode output voltage	V _{IN,DIFF(P-P)} = 0.3 V, R _{LOAD} = 100 Ω (V _{DD} = 1.8 V)	1		1.2	V
		V _{IN,DIFF(P-P)} = 0.3 V, R _{LOAD} = 100 Ω (V _{DD} = 2.5 V/3.3 V)	1.1		1.375	
LVDS AC OUTPUT CHARACTERISTICS						
V _{ring}	Output overshoot and undershoot	V _{IN,DIFF(P-P)} = 0.3 V, R _{LOAD} = 100 Ω , f _{OUT} = 491.52 MHz	- 0.1		0.1	V _{OD}
I _{OS}	Short-circuit output current (differential)	V _{OUTP} = V _{OUTN}	- 12		12	mA
I _{OS(cm)}	Short-circuit output current (common-mode)	V _{OUTP} = V _{OUTN} = 0	- 24		24	mA
t _{PD}	Propagation delay	V _{IN,DIFF(P-P)} = 0.3 V, R _{LOAD} = 100 Ω (2)	0.3		0.575	ns
t _{SK_PP}	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			250	ps
t _{SK_P}	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (4)	- 20		20	ps
t _{RJIT(ADD)}	Random additive Jitter (rms)	f _{IN} = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12 kHz - 20 MHz, with output load R _{LOAD} = 100 Ω		50	60	fs, RMS
Phase noise	Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R _{LOAD} = 100 Ω	PN _{1kHz}		- 143		dBc/Hz
		PN _{10kHz}		- 152		
		PN _{100kHz}		- 157		
		PN _{1MHz}		- 160		
		PN _{floor}		- 164		
MUX _{ISO}	Mux Isolation	f _{IN} = 156.25 MHz. The difference in power level at f _{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
ODC	Output duty cycle	With 50% duty cycle input	45		55	%

$V_{DD} = 1.8\text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are at $V_{DD} = 1.8\text{ V}$, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R/t_F	Output rise and fall time	20% to 80% with $R_{LOAD} = 100\ \Omega$			300	ps
V_{AC_REF}	Reference output voltage	$V_{DD} = 2.5\text{ V}$, $I_{LOAD} = 100\ \mu\text{A}$	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) $V_{DD} = 2.5\text{ V}/3.3\text{ V}$						
PSNR	Power Supply Noise Rejection ($f_{carrier} = 156.25\text{ MHz}$)	10 kHz, 100 mVpp ripple injected on V_{DD}		- 70		dBc
		1 MHz, 100 mVpp ripple injected on V_{DD}		- 50		

- (1) Measured between single-ended/differential input crossing point to the differential output crossing point.
 (2) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

7.5 Typical Characteristics

The 图 7-1 captures the variation of the LMK1D1208 current consumption with input frequency and supply voltage. The LMK1D1204 follows a similar trend. 图 7-2 shows the variation of the differential output voltage (VOD) swept across frequency. This result is applicable to LMK1D1204 as well.

It is important to note that 图 7-1 and 图 7-2 serve as a guidance to the users on what to expect for the range of operating frequency supported by LMK1D120x. It is crucial to note that these graphs were plotted for a limited number of frequencies and load conditions which may not represent the customer system.

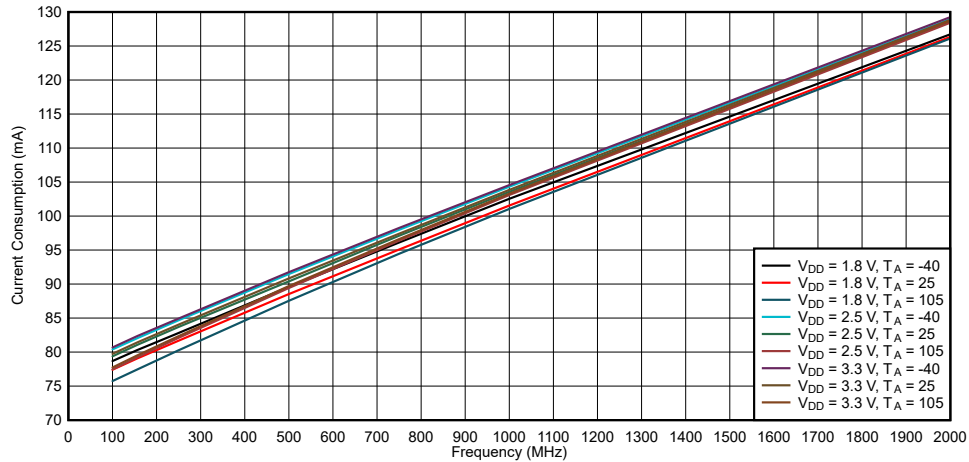


图 7-1. LMK1D1208 Current Consumption vs. Frequency

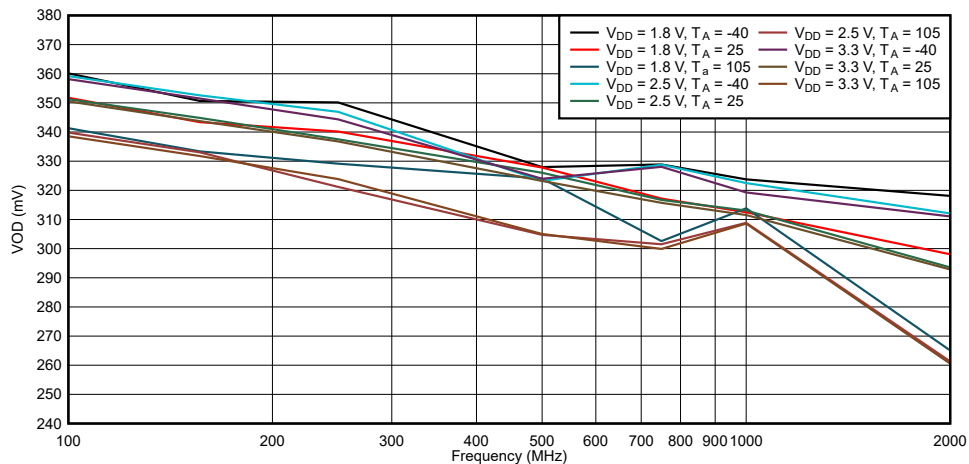


图 7-2. LMK1D1208 VOD vs. Frequency

8 Parameter Measurement Information

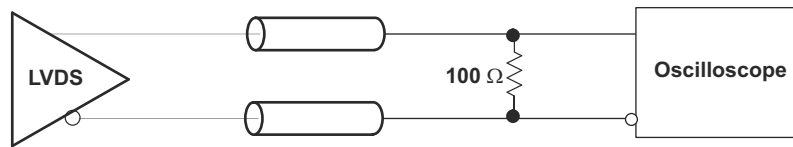


图 8-1. LVDS Output DC Configuration During Device Test

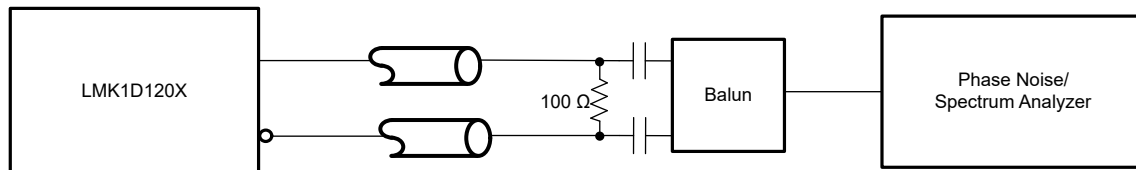


图 8-2. LVDS Output AC Configuration During Device Test

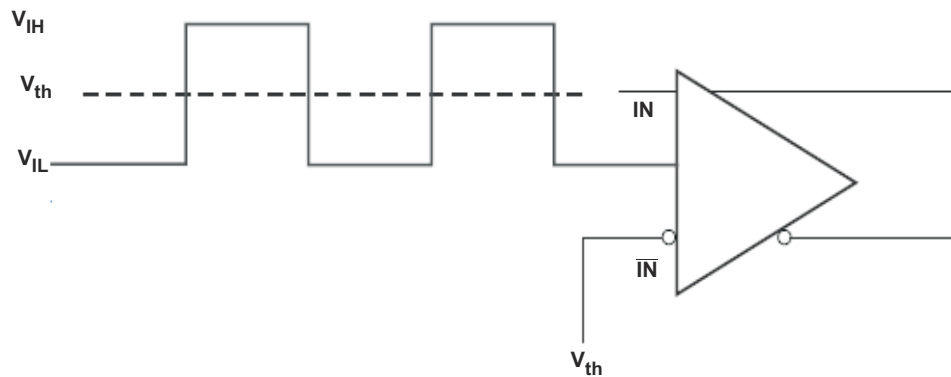


图 8-3. DC-Coupled LVCMOS Input During Device Test

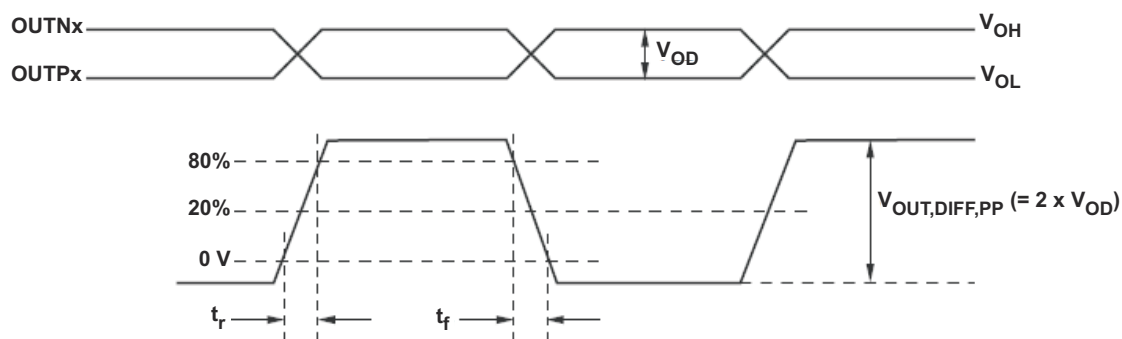
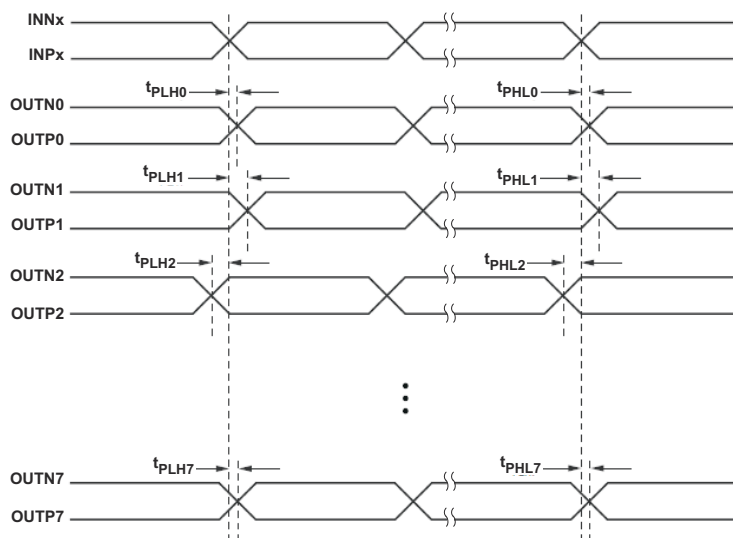


图 8-4. Output Voltage and Rise/Fall Time



- A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, 2, \dots, 7$)
- B. Part to part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices ($n = 0, 1, 2, \dots, 7$)

图 8-5. Output Skew and Part-to-Part Skew

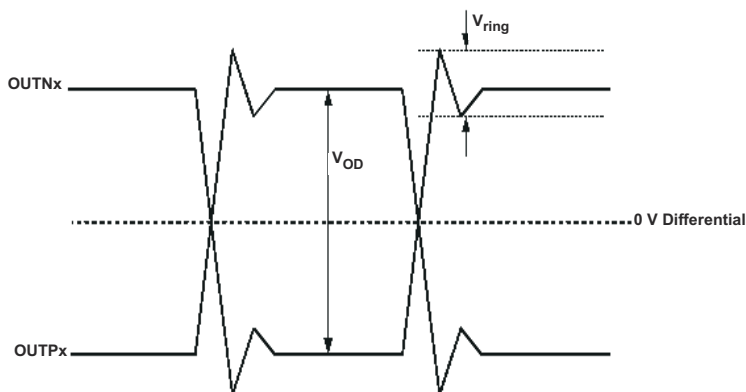


图 8-6. Output Overshoot and Undershoot

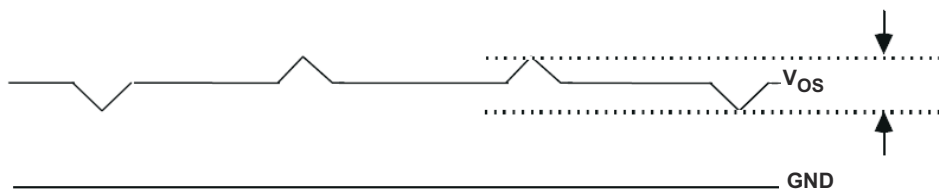


图 8-7. Output AC Common Mode

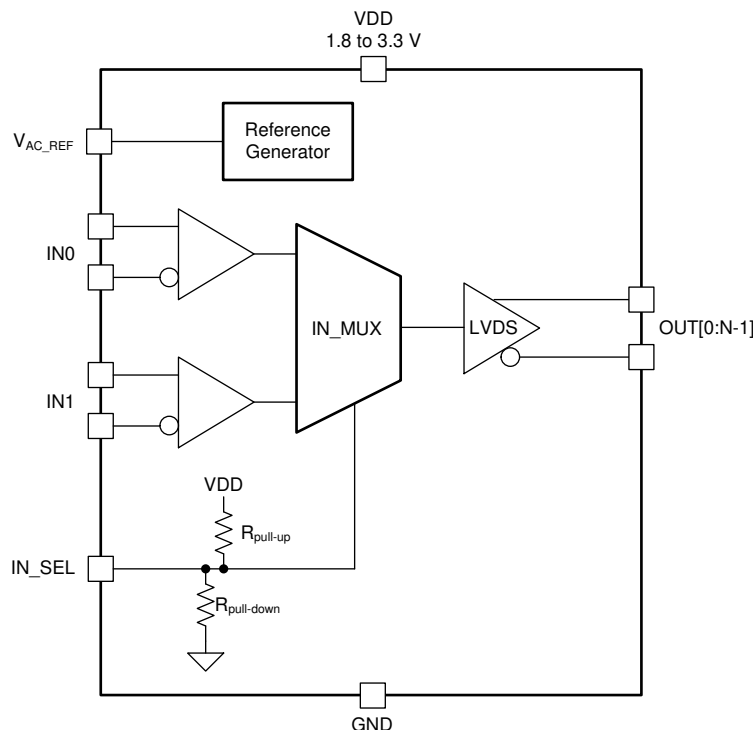
9 Detailed Description

9.1 Overview

The LMK1D120x LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50- Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D12XX, AC-coupling must be used. If the LVDS receiver has internal 100- Ω termination, external termination must be omitted.

9.2 Functional Block Diagram



9.3 Feature Description

The LMK1D120x is a low additive jitter LVDS fan-out buffer that can generate up to eight copies of two selectable LVPECL, LVDS, LP-HCSL, HCSL or LVCMOS inputs. The LMK1D120x can accept reference clock frequencies up to 2 GHz while providing low output skew.

9.3.1 Fail-Safe Input and Hysteresis

The LMK1D120x family of devices is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to [Specifications](#) for more information on the maximum input supported by the device. User should note that incorporating the fail-safe inputs also results in a slight increase in clock input pin capacitance.

The device also incorporates an input hysteresis which prevents random oscillation in absence of an input signal. Furthermore, this feature allows the input pins to be left open.

9.3.2 Input Mux

The LMK1D120x family of devices has a 2:1 input mux. This feature allows the user to select between the two clock inputs (using the IN_SEL pin) to the device and fan it out to the outputs. More information on the input selection is provided in the next section.

9.4 Device Functional Modes

The two inputs of the LMK1D120x are internally muxed together and can be selected through the control pin (see 表 9-1). Unused input can be left floating thus reducing the need for additional components. Both AC- and DC-coupling schemes can be used with the LMK1D120x to provide greater system flexibility.

表 9-1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	IN0_P, IN0_N
1	IN1_P, IN1_N
Open	None ⁽¹⁾

(1) The input buffers are disabled and the outputs are static logic low.

9.4.1 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100- Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D120x can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in 图 9-1 and 图 9-2 (respectively).

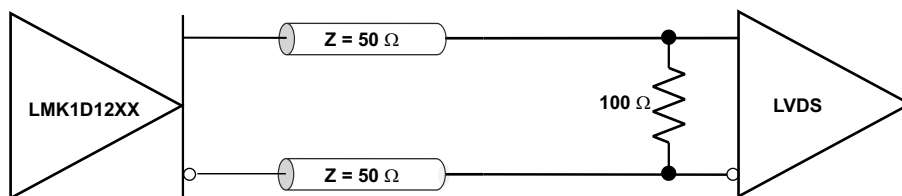


图 9-1. Output DC Termination

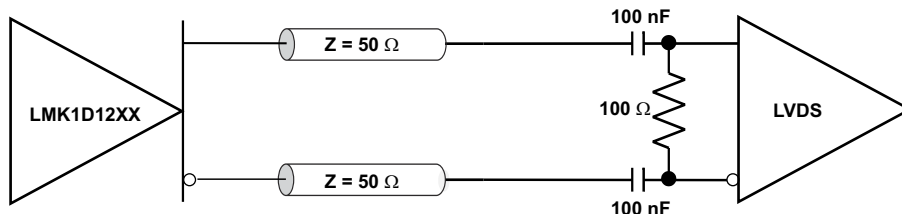


图 9-2. Output AC Termination (With the Receiver Internally Biased)

9.4.2 Input Termination

The LMK1D120x input stage is designed with flexibility in mind to allow the user to drive the device with a wide variety of signal types. This device can be interfaced with LVDS, LVPECL, LP-HCSL, HCSL, CML or LVCMOS drivers. Please refer to [Electrical Characteristics](#) for more details.

LVDS drivers can be connected to LMK1D120x inputs with DC- and AC-coupling as shown 图 9-3 and 图 9-4 (respectively).

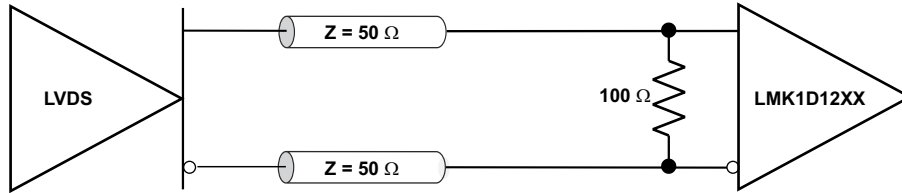


图 9-3. LVDS Clock Driver Connected to LMK1D120x Input (DC-Coupled)

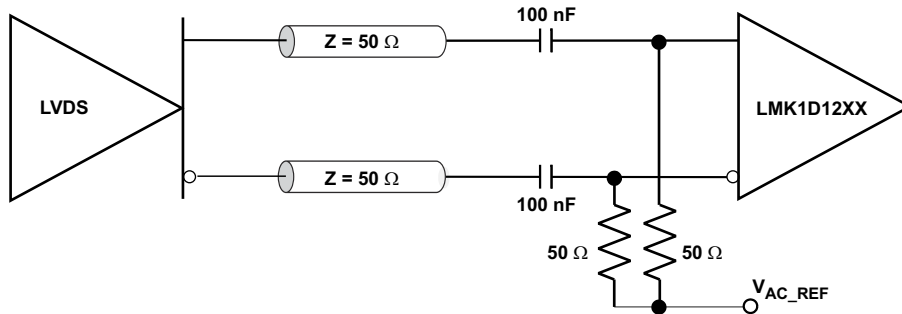


图 9-4. LVDS Clock Driver Connected to LMK1D120x Input (AC-Coupled)

图 9-5 shows how to connect LVPECL inputs to the LMK1D120x. The series resistors are required to reduce the LVPECL signal swing if the signal swing is $>1.6 V_{pp}$.

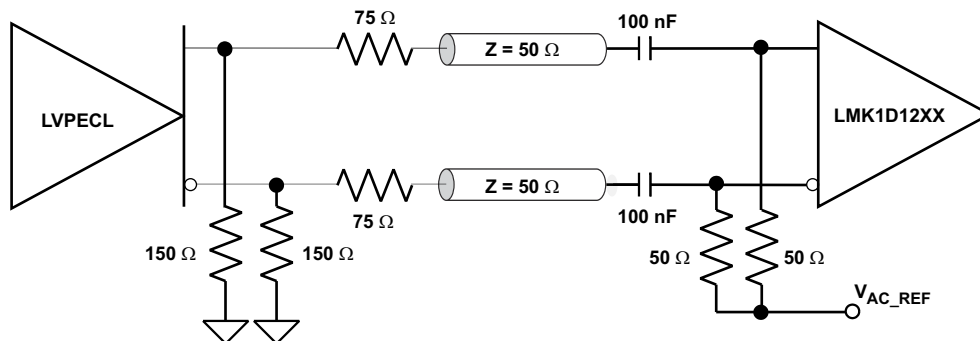


图 9-5. LVPECL Clock Driver Connected to LMK1D120x Input

图 9-6 illustrates how to couple a LVCMOS clock input to the LMK1D120x directly.

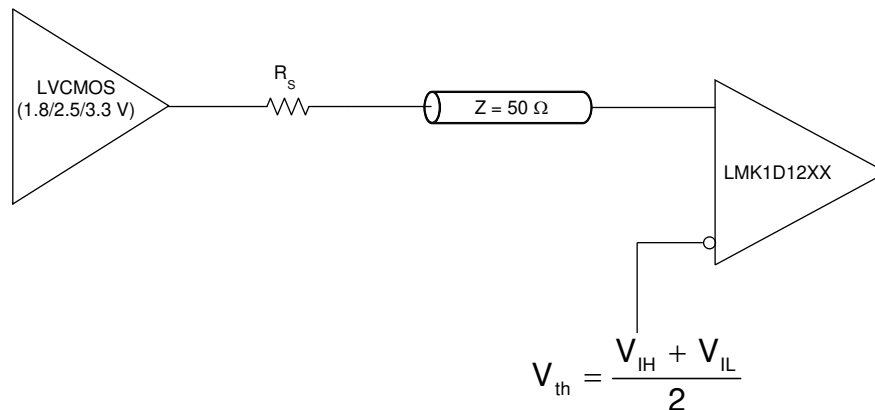


图 9-6. 1.8-V/2.5-V/3.3-V LVCMOS Clock Driver Connected to LMK1D120x Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-k Ω resistors.

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The LMK1D120x is a low additive jitter universal to LVDS fan-out buffer with 2 selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

10.2 Typical Application

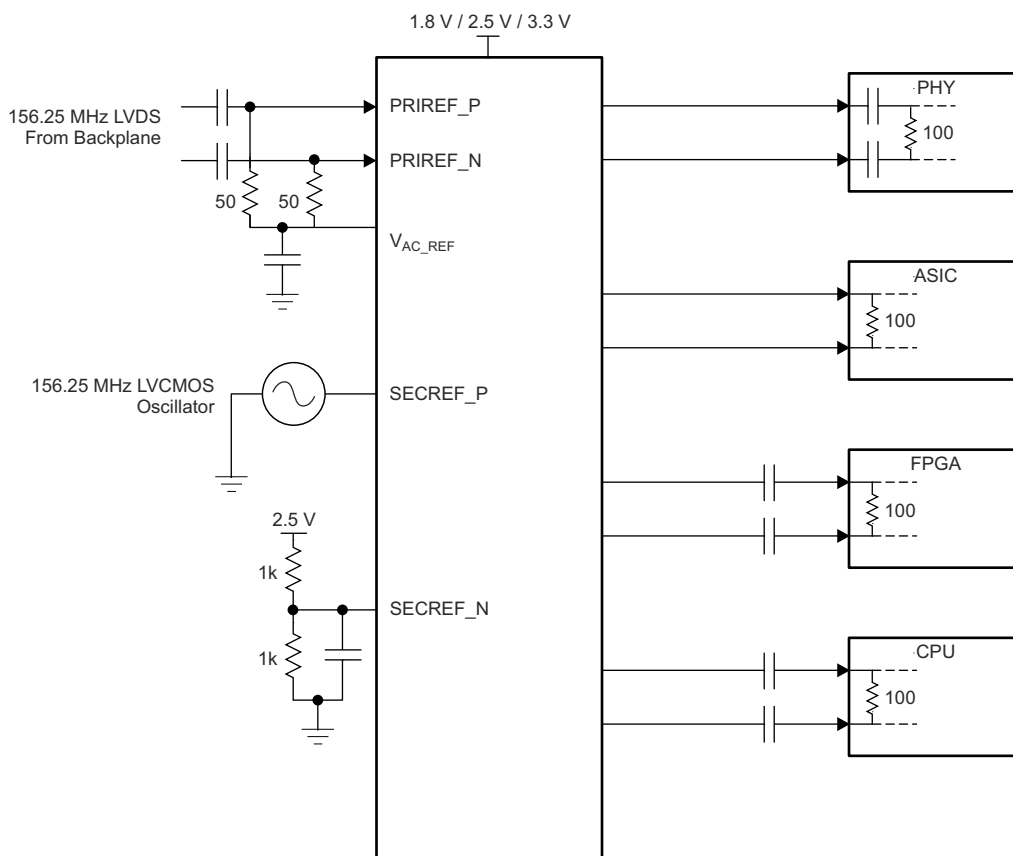


图 10-1. Fan-Out Buffer for Line Card Application

10.2.1 Design Requirements

The LMK1D120x shown in [Figure 10-1](#) is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1- μ F capacitors are used to reduce noise on both V_{AC_REF} and $SECREP_N$. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC-coupling with an LVDS driver such as the LMK1D120x. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D120x. Again, no additional components are required.
- The FPGA requires external AC-coupling, but has internal termination. 0.1- μ F capacitors are placed to provide AC-coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- Unused outputs of the LMK1D device are terminated differentially with a 100- Ω resistor for optimum performance.

10.2.2 Detailed Design Procedure

See [Input Termination](#) for proper input terminations, dependent on single-ended or differential inputs.

See [LVDS Output Termination](#) for output termination schemes depending on the receiver application.

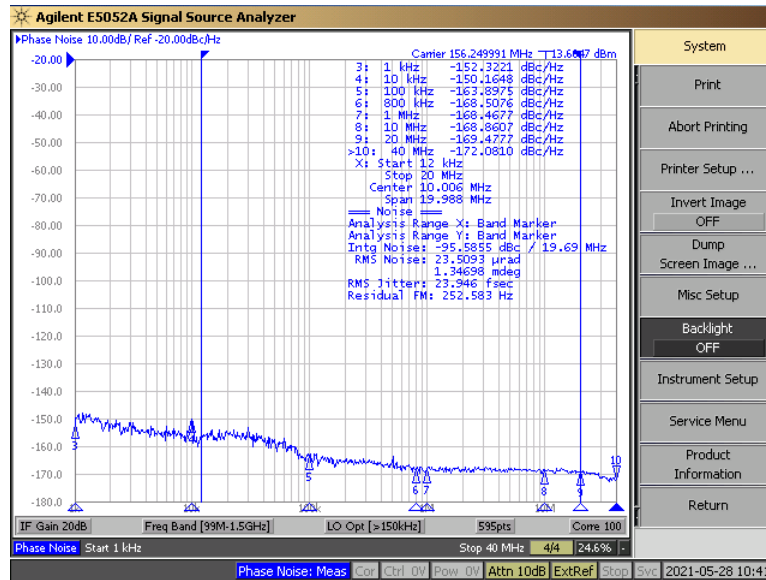
TI recommends unused outputs to be terminated differentially with a 100- Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

See [Power Supply Recommendations](#) for recommended filtering techniques. A reference layout is provided in [Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board](#) (SCAU043).

10.2.3 Application Curves

The LMK1D1208's low additive noise is shown below. The low noise 156.25-MHz source with 24-fs RMS jitter shown in 图 10-2 drives the LMK1D1208, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (图 10-3). The resultant additive jitter is a low 39.7-fs RMS for this configuration. Note that this result applies to the LMK1D1204 device as well.



A. Reference signal is low-noise Rohde and Schwarz SMA100B

图 10-2. LMK1D208 Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)

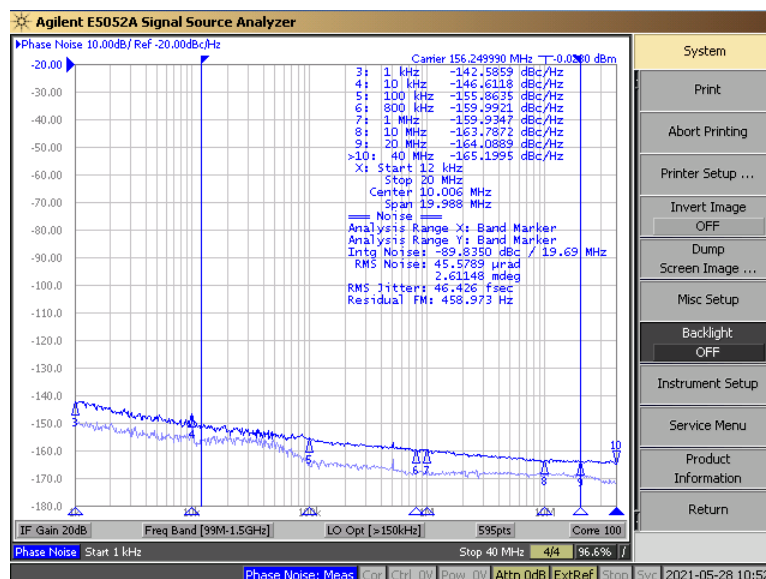


图 10-3. LMK1D1208 Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

The 图 10-4 captures the low close-in phase noise of the LMK1D1208 device. The LMK1D1204 and LMK1D1208 have excellent flicker noise as a result of superior process technology and design. This enables their use for clock distribution in radar systems, medical imaging systems etc which require ultra-low close-in phase noise clocks.

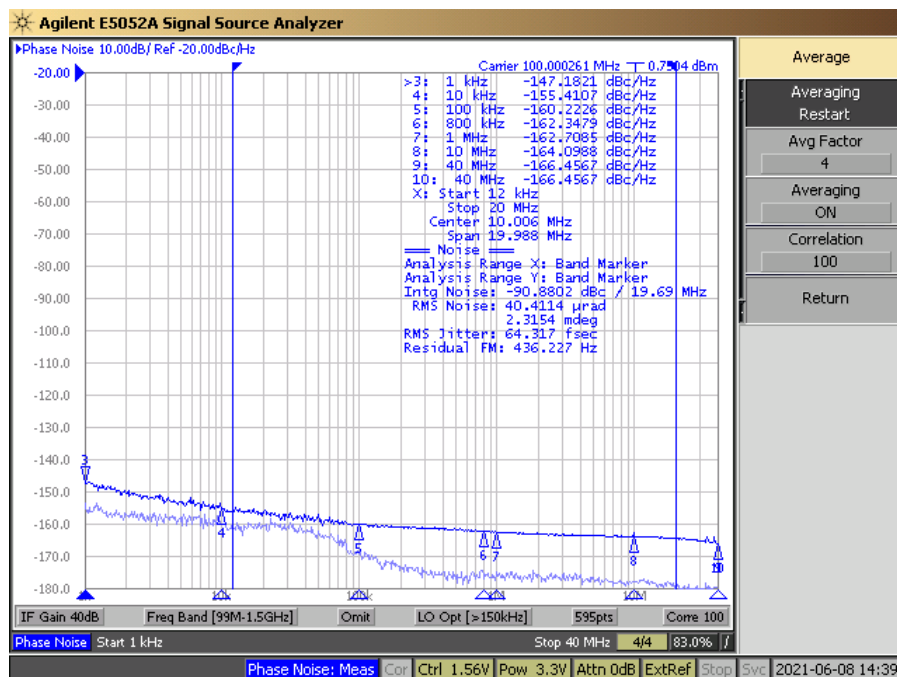


图 10-4. LMK1D1208 Output Phase Noise, 100 MHz, 1 kHz offset: -147 dBc/Hz

10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC-resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

图 10-5 shows this recommended power-supply decoupling method.

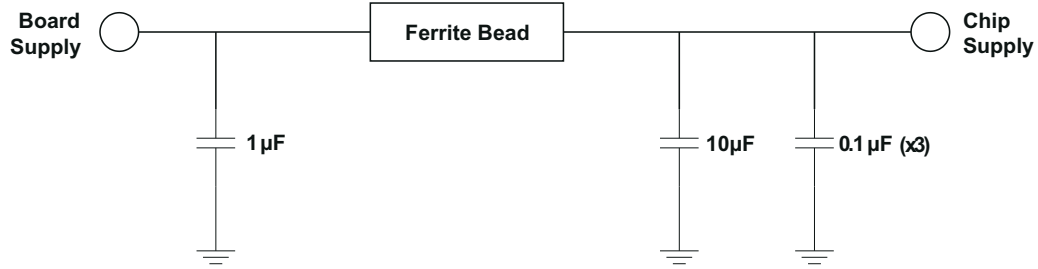


图 10-5. Power Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. 图 10-6 shows a recommended land and via pattern for LMK1D1208.

10.4.2 Layout Example

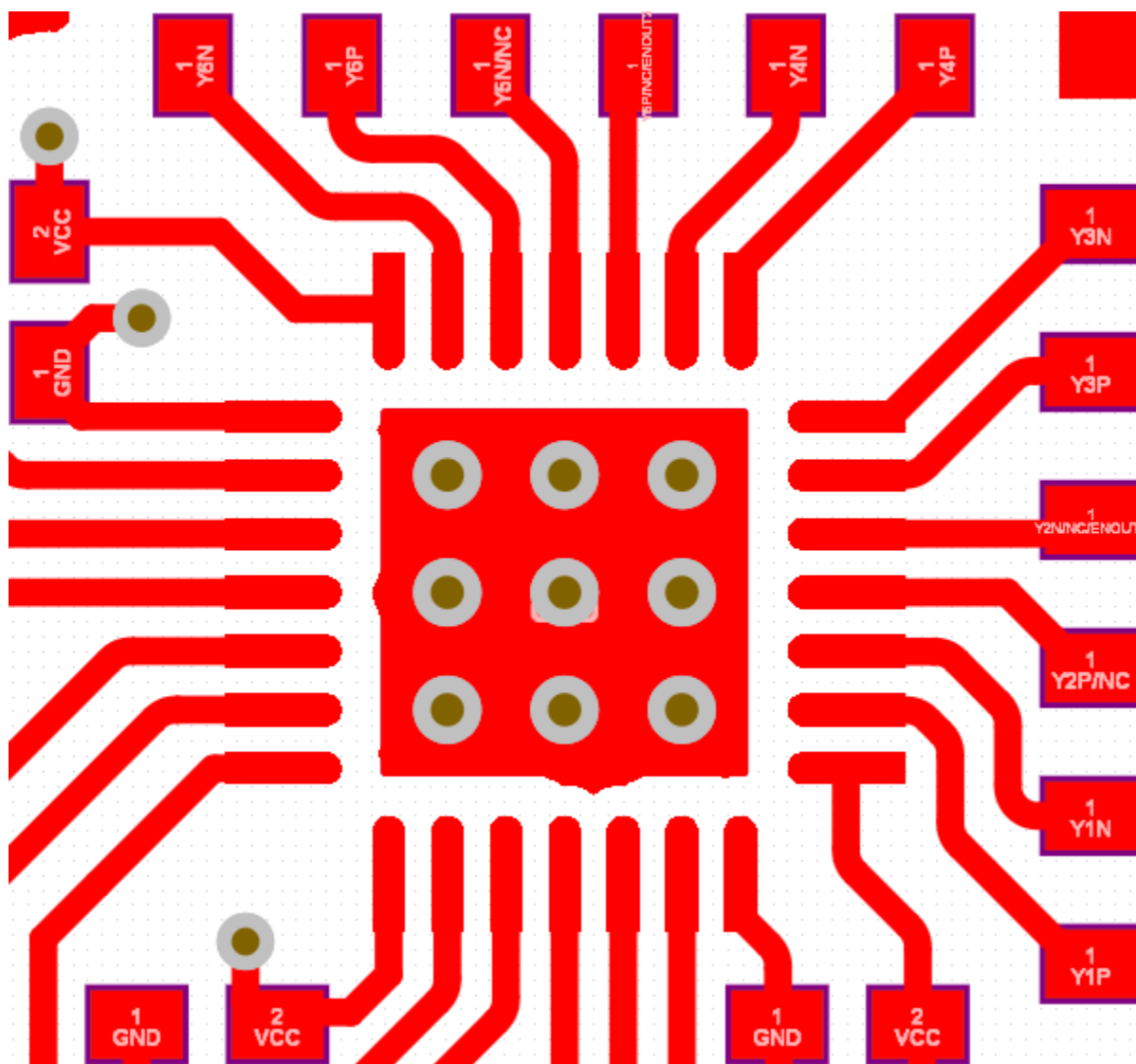


图 10-6. Recommended PCB Layout, Top Layer

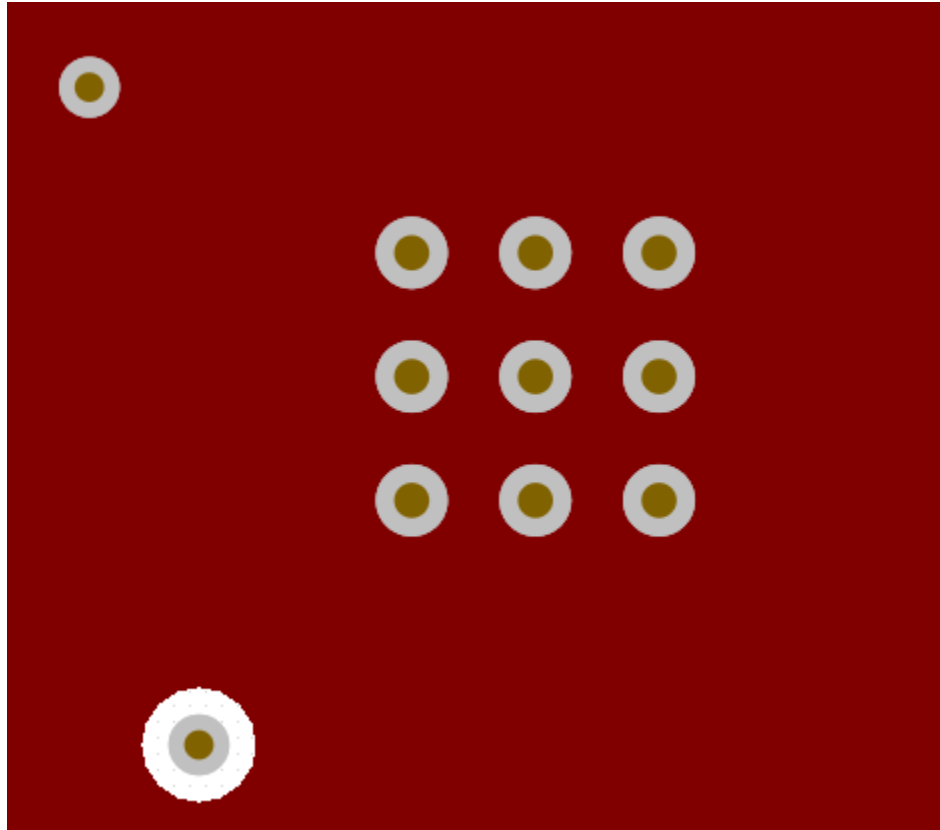


图 10-7. PCB Layout, GND Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board](#) (SCAU043)
- [Power Consumption of LVPECL and LVDS](#) (SLYT127)
- [Semiconductor and IC Package Thermal Metrics](#) (SPRA953)
- [Using Thermal Calculation Tools for Analog Components](#) (SLUA556)

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1D1204RGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1204RGTR.B	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1204RGTRG4	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1204RGTRG4.B	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1204RGTT	Active	Production	VQFN (RGT) 16	250 SMALL T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1204RGTT.B	Active	Production	VQFN (RGT) 16	250 SMALL T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 105	LD1204
LMK1D1208RHDR	Active	Production	VQFN (RHD) 28	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208
LMK1D1208RHDR.B	Active	Production	VQFN (RHD) 28	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208
LMK1D1208RHDT	Active	Production	VQFN (RHD) 28	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208
LMK1D1208RHDT.B	Active	Production	VQFN (RHD) 28	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208
LMK1D1208RHDTG4	Active	Production	VQFN (RHD) 28	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208
LMK1D1208RHDTG4.B	Active	Production	VQFN (RHD) 28	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1204RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK1D1204RGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK1D1204RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK1D1208RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMK1D1208RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMK1D1208RHDTG4	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1204RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
LMK1D1204RGTRG4	VQFN	RGT	16	3000	367.0	367.0	35.0
LMK1D1204RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
LMK1D1208RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
LMK1D1208RHDT	VQFN	RHD	28	250	210.0	185.0	35.0
LMK1D1208RHDTG4	VQFN	RHD	28	250	210.0	185.0	35.0

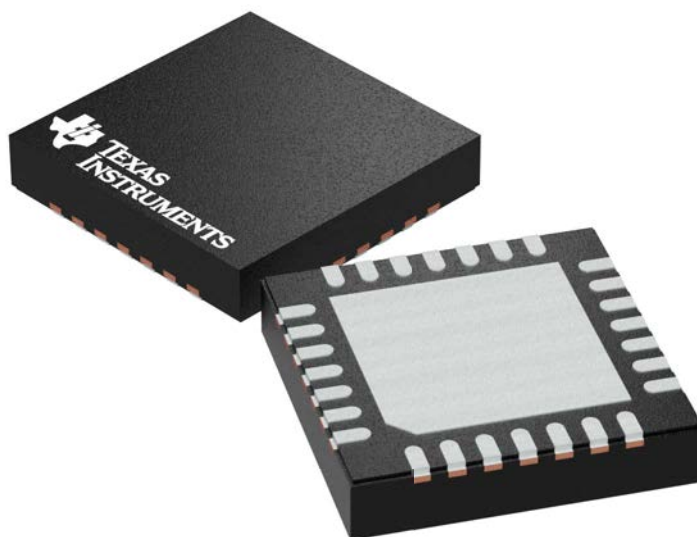
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

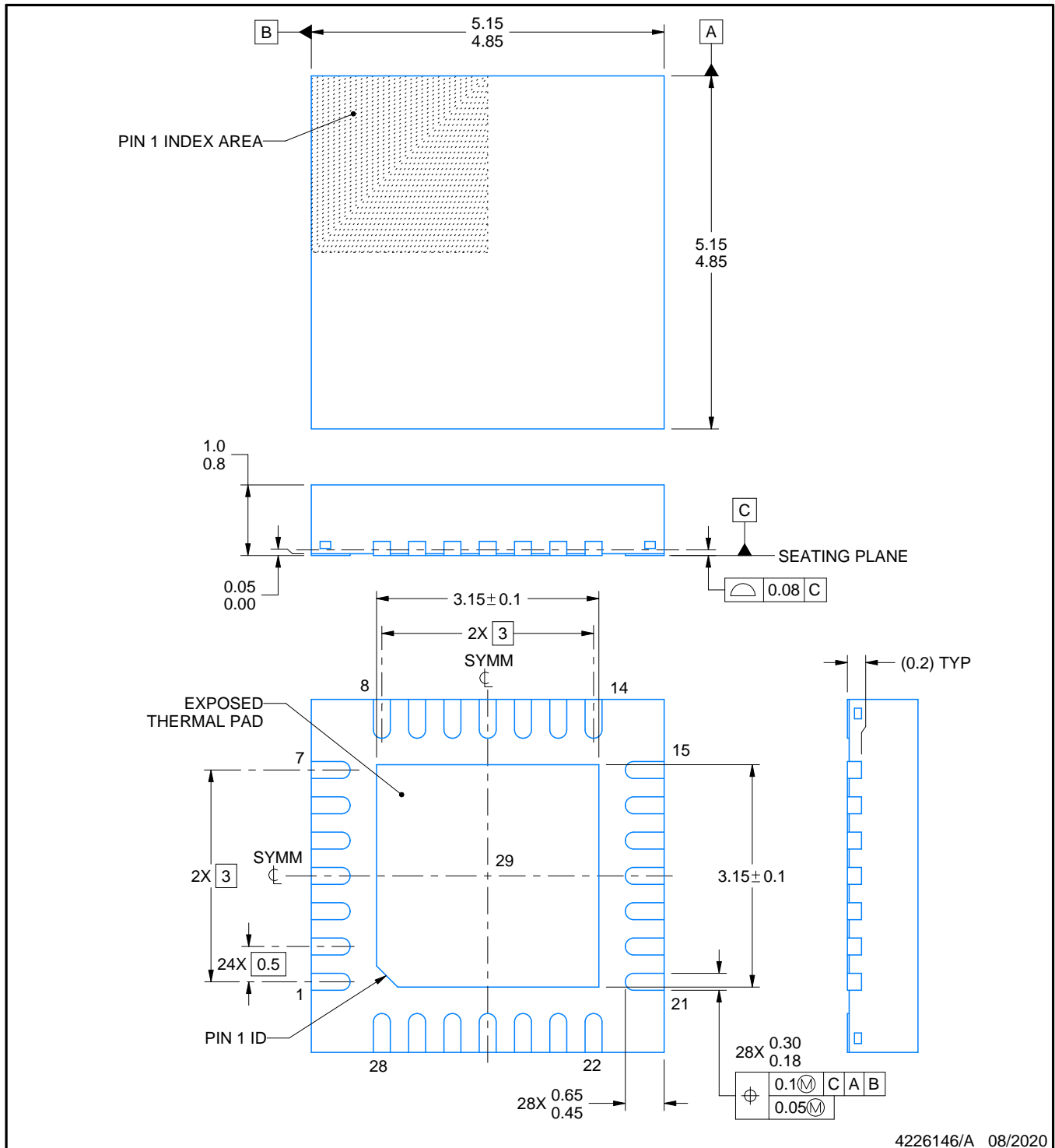
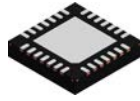
5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204400/G



4226146/A 08/2020

NOTES:

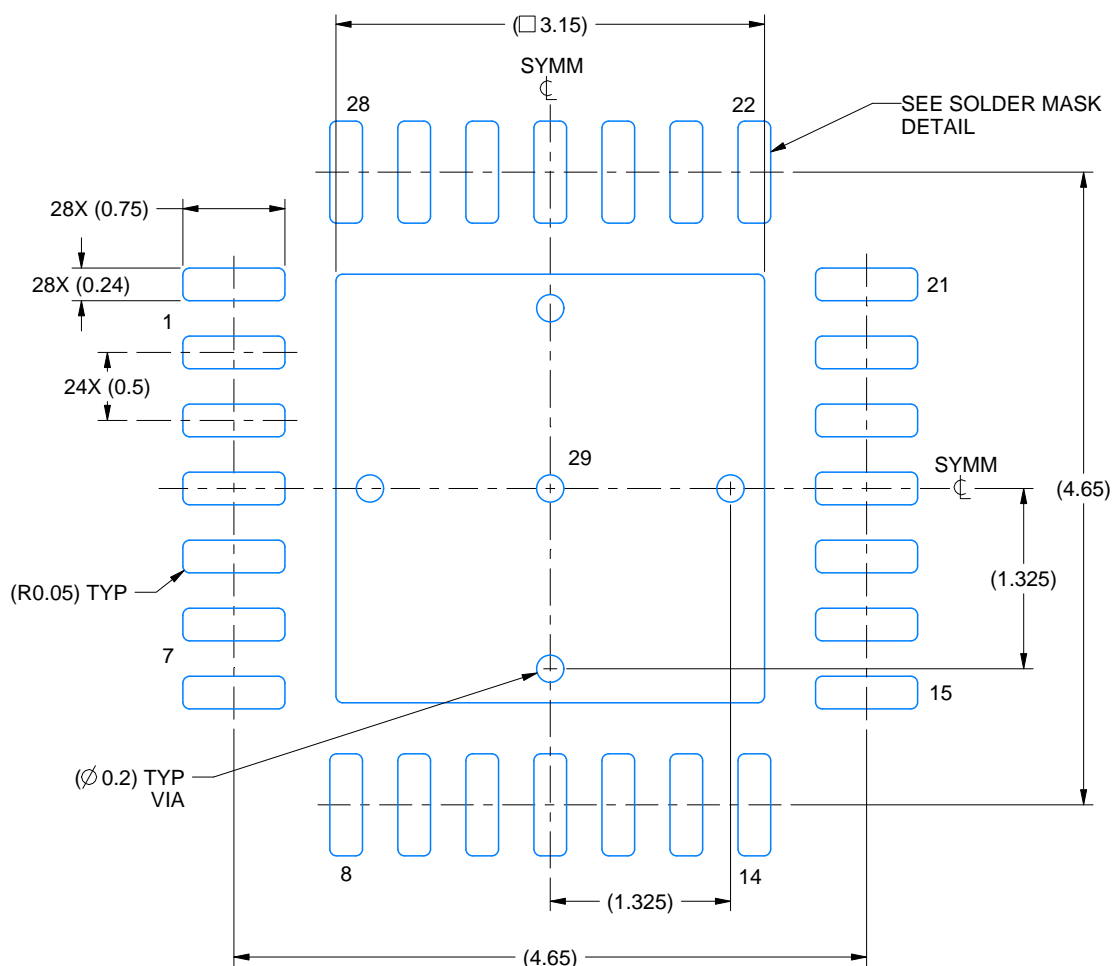
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

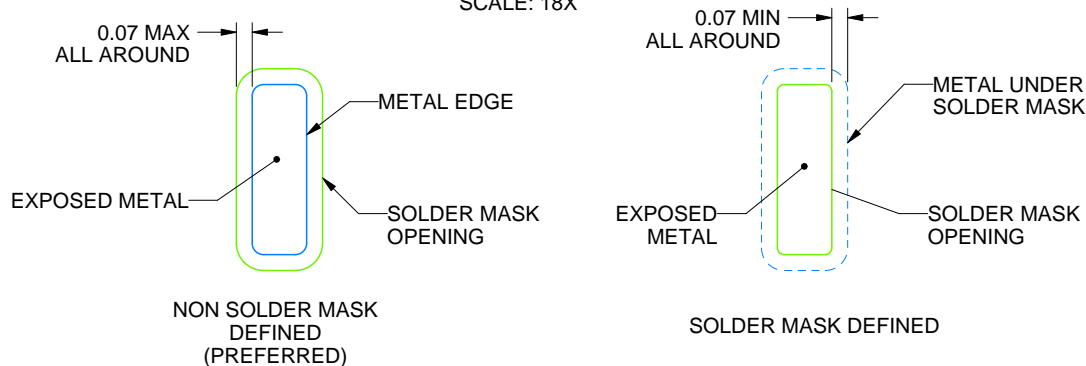
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

4226146/A 08/2020

NOTES: (continued)

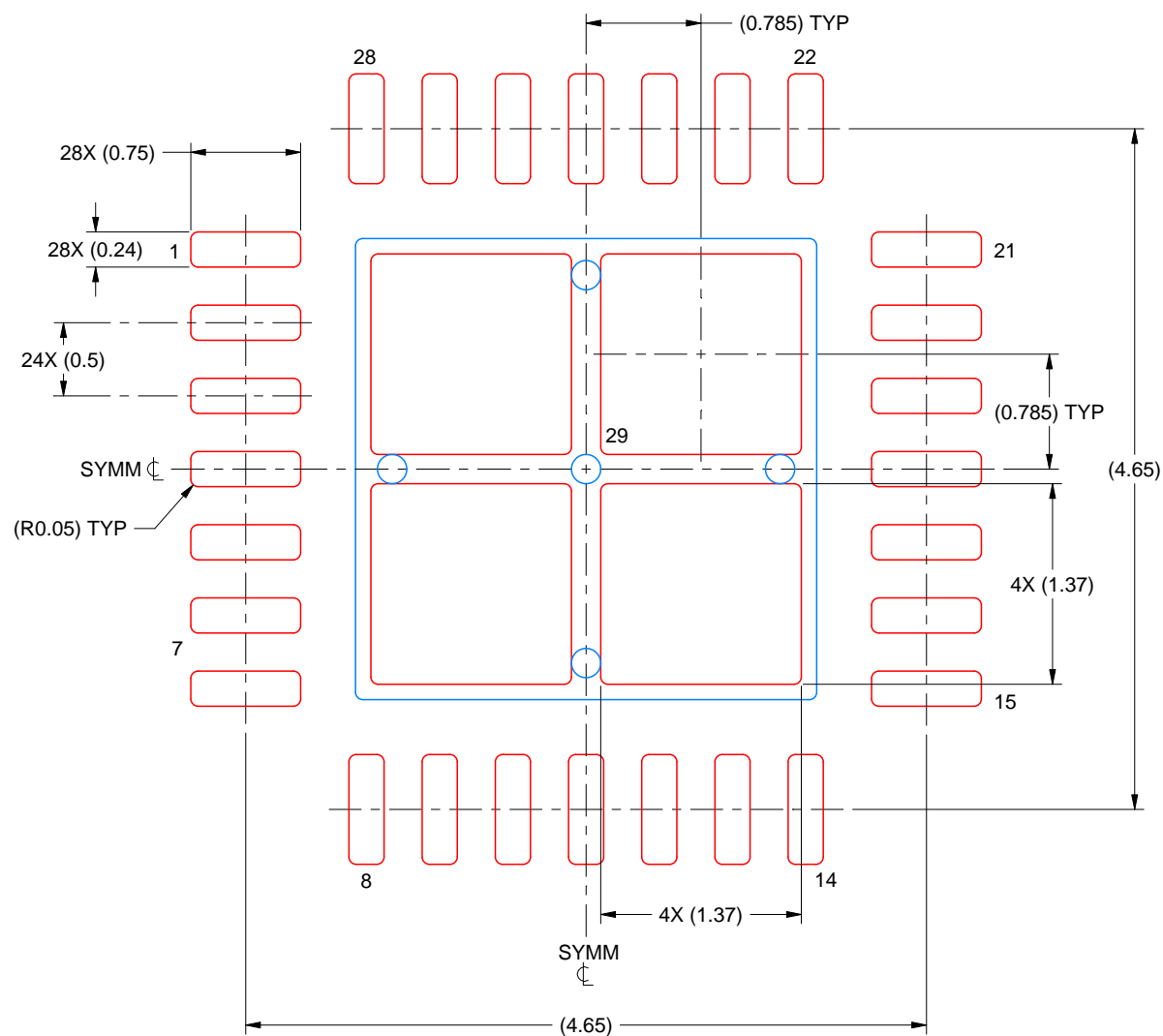
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 20X

EXPOSED PAD 29
 76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226146/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGT 16

GENERIC PACKAGE VIEW

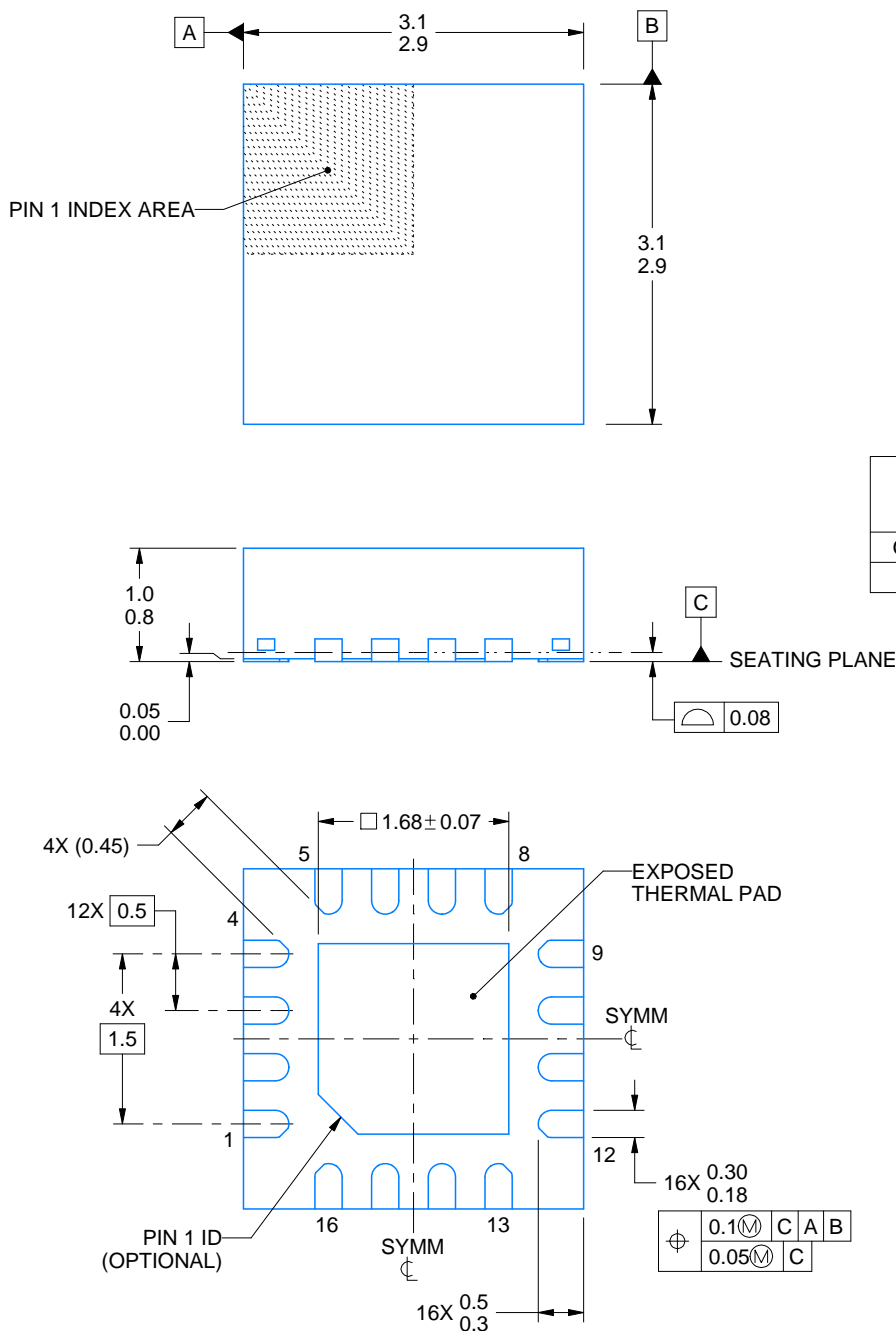
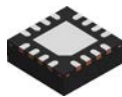
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



4222419/E 07/2025

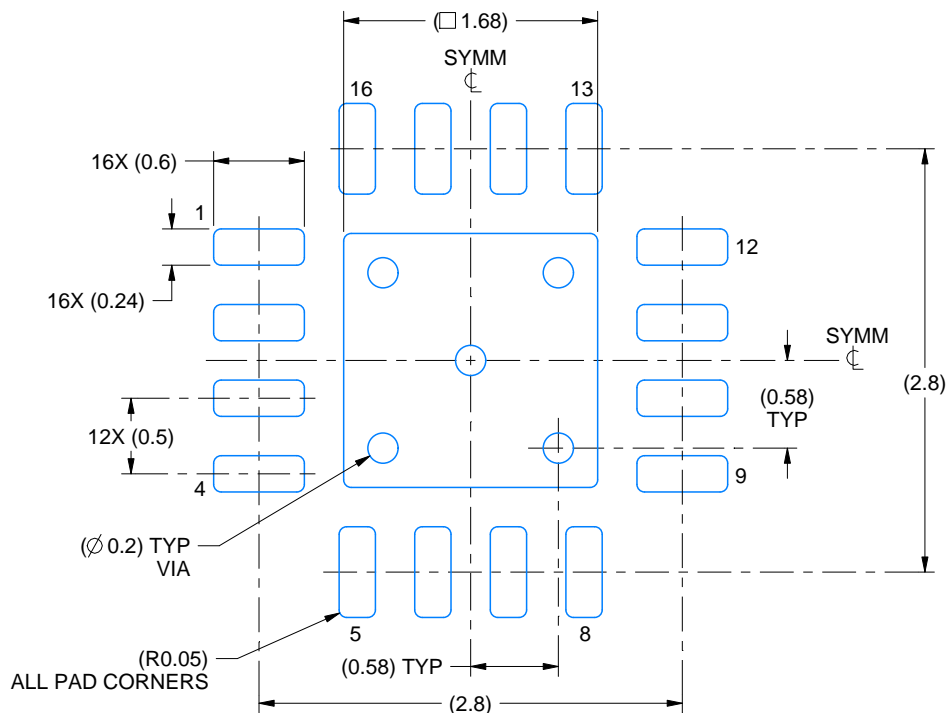
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

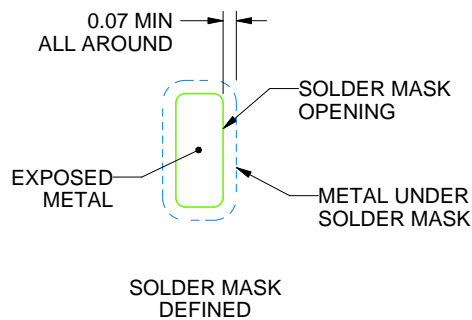
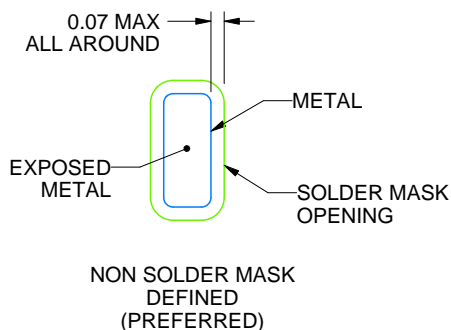
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/E 07/2025

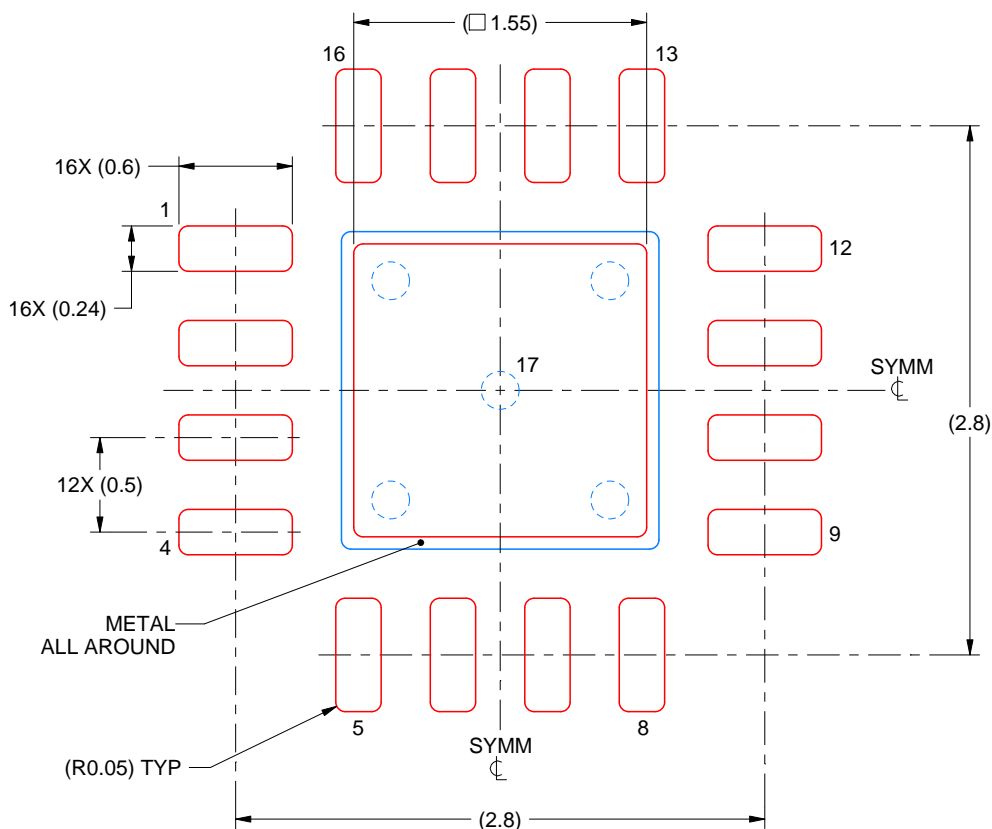
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月