具有 ±1V 双极输入和 2.5V 基准电压输出的 AMC1035 Δ-Σ 调制器

1 特性

- 针对电压和温度感应进行了优化的 Δ-Σ 调制器：
  - ±1V 输入电压范围
  - 高差分输入电阻：1.6GΩ（典型值）
  - 集成 2.5V、±5mA 基准，可实现比例测量
- 出色的直流性能：
  - 失调电压误差：±0.5mV（最大值）
  - 温漂：±6µV/°C（最大值）
  - 增益误差：±0.25%（最大值）
  - 增益漂移：±45ppm/°C（最大值）
  - 比例增益漂移：±15ppm/°C（最大值）
- 可选曼彻斯特编码式或未编码式位流输出
- 完整的额定工作温度范围：–40°C 至 +125°C

2 应用

- 工业应用中的交流电压和温度 感应：
  - 电机驱动器
  - 光电逆变器
  - 不间断电源
  - 工业运输系统

3 说明

AMC1035 是一款精密 Δ-Σ 调制器，可在 3.0V 至 5.5V 的单电源下运行，且具有 9MHz 至 21MHz 的时钟信号。在曼彻斯特模式下，额定时钟范围为 9MHz 至 11MHz。该器件的差分 ±1V 输入结构经过优化，可适应工业应用中的典型高噪声 环境。

AMC1035 可选择曼彻斯特编码式输出位流，这样便无需考虑接收器件的设置和保留时间要求并减少总体电路布局工作。当用于与数字滤波器（例如集成到 TMS320F28004x、TMS320F2807x 或 TMS320F2837x 微控制器系列中）一起抽取输出位流时，该器件可在 82kSPS 的数据速率下实现具有 87dB 动态范围的 16 位分辨率。

AMC1035 的内部基准源支持比例电路架构，可最大限度降低电源电压变化和温漂对测量精度的负面影响。

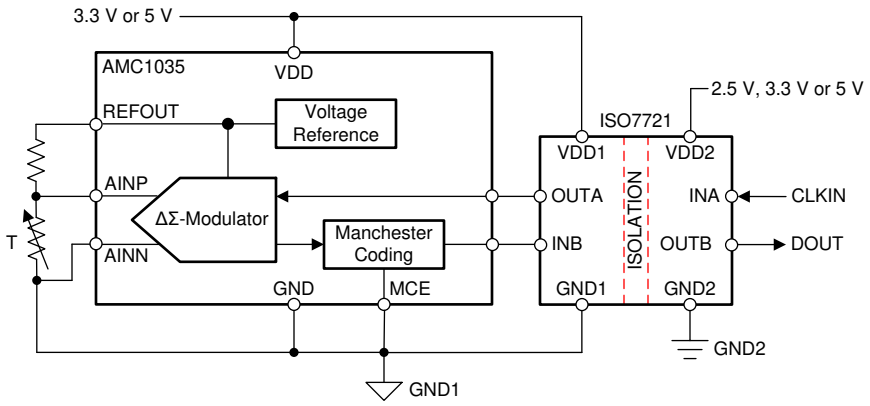
AMC1035 还可用于与数字隔离器和隔离电源一起实现交流电力线电压检测。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1035	SOIC (8)	4.9mm x 3.9mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用示例



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (November 2018) to Revision B **Page**

- Deleted PSRR specification for T_A > 85°C from *Reference Output* section of *Electrical Characteristics* table ... 6
- 已更改 SINAD equation ... 22

Changes from Original (August 2018) to Revision A **Page**

- 已更改 将文档状态从“预告信息”更改为“生产数据” ... 1

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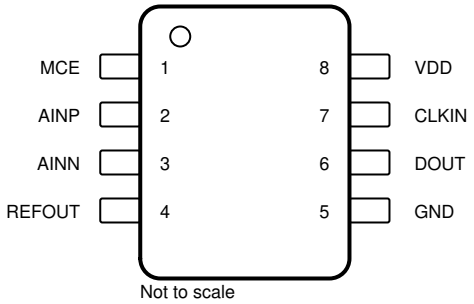
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MCE	I	Manchester coding enabled, active high, with internal pulldown resistor (typical value: 200 kΩ). The polarity of this signal must not be changed when the clock signal is applied.
2	AINP	I	Noninverting analog input.
3	AINN	I	Inverting analog input.
4	REFOUT	O	Reference output: 2.5 V nominal, maximum ±5-mA sink and source capability.
5	GND	—	Ground reference.
6	DOUT	O	Modulator bitstream data output, updated with the rising edge of the clock signal present on CLKIN. This pin is a Manchester coded output if MCE is pulled high. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.
7	CLKIN	I	Modulator clock input: 9 MHz to 21 MHz with an internal pulldown resistor (typical value: 200 kΩ). The clock signal must be applied continuously for proper device operation; see the *Clock Input* section for additional details.
8	VDD	—	Power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)

	MIN	MAX	UNIT
Supply voltage, VDD to GND	–0.3	7	V
Analog input voltage at AINP, AINN	GND – 5	VDD + 0.5	V
Analog output voltage at REFOUT	GND – 0.5	VDD + 0.5	V
Digital input voltage at CLKIN or MCE	GND – 0.5	VDD + 0.5	V
Digital output voltage at DOUT	GND – 0.5	VDD + 0.5	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{AINP} – V_{AINN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{AINP} – V_{AINN}$	–1		1	V
	Absolute common-mode input voltage (1)	$(V_{AINP} + V_{AINN}) / 2$ to GND	–2		VDD	V
V_{CM}	Operating common-mode input voltage (2)	$(V_{AINP} + V_{AINN}) / 2$ to GND, 3.0 V ≤ VDD < 4 V, $V_{AINP} = V_{AINN}$	–1.4		VDD – 1.4	V
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 3.0 V ≤ VDD < 4.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V	–0.8		VDD – 2.4	
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 4 V ≤ VDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	–1.4		2.7	
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 4.5 V ≤ VDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V	–0.8		2.1	
DIGITAL INPUT						
	Input voltage	V_{MCE} or V_{CLKIN} to GND	GND		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) See the *Analog Input* section for more details.

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6.4 Thermal Information

THERMAL METRIC(1)		AMC1035 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = GND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMuv}(1)	Negative common-mode undervoltage detection level(2)	$(V_{AINP} + V_{AINN}) / 2$, $V_{AINP} = V_{AINN}$			–1.45	V
		$(V_{AINP} + V_{AINN}) / 2$, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V			–0.85	
V_{CMov}(1)	Positive common-mode overvoltage detection level(2)	3.0 V ≤ VDD < 4 V, $V_{AINP} = V_{AINN}$			VDD – 1.35	V
		3.0 V ≤ VDD < 4.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V			VDD – 2.35	
		4 V ≤ VDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	2.75			
		4.5 V ≤ VDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V	2.15			
R_{IN}	Single-ended input resistance	AINN = GND	0.1	0.4		GΩ
R_{IND}	Differential input resistance		0.16	1.6		GΩ
C_{IN}	Single-ended input capacitance	AINN = GND		2		pF
C_{IND}	Differential input capacitance			2		pF
I_{IB}	Input bias current	AINP = AINN = GND, $(I_{AINP} + I_{AINN}) / 2$	–10	±3	10	nA
TCI_{IB}	Input bias current thermal drift	AINP = AINN = GND, $(I_{AINP} + I_{AINN}) / 2$		±5		pA/°C
I_{IO}	Input offset current	$I_{IO} = I_{AINP} – I_{AINN}$	–5	±1	5	nA
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–104		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, –0.5 V ≤ V_{IN} ≤ 0.5 V		–88		
DC ACCURACY						
	Resolution(3)		16			Bits
INL	Integral nonlinearity(4)	Resolution: 16 bits	–12	±2	12	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = GND	–0.5	±0.03	0.5	mV
TCE_O	Offset error thermal drift(5)		–6	±0.1	6	µV/°C
E_G	Gain error	Initial, at T_A = 25°C	–0.25%	±0.02%	0.25%	
		Initial, at T_A = 25°C, ratiometric mode	–0.3%	±0.02%	0.3%	
TCE_G	Gain error thermal drift(6)		–45	±20	45	ppm/°C
		Ratiometric mode	–15	±4	15	
PSRR	Power-supply rejection ratio	AINP = AINN = GND, at dc		–90		dB
		AINP = AINN = GND, 10 kHz, 100-mV ripple		–84		

(1) See the *Analog Input* section for more details.
(2) The common-mode overvoltage detection level has a typical hysteresis of 35 mV.
(3) The filter output is truncated to 16 bits. 16 bits of no missing codes is specified by design.
(4) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(5) Offset error drift is calculated using the box method, as described by the following equation: $TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$.
(6) Gain error drift is calculated using the box method, as described by the following equation: $TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = GND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	81	87		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77	83		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–87	–78	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	78	87		dB
REFERENCE OUTPUT						
V_{REFOUT}	Reference output voltage	Initial, at T_A = 25°C, no load	2.495	2.5	2.505	V
TCV_{REFOUT}	Reference output voltage drift		–50	±20	50	ppm/°C
I_{REFOUT}	Reference output current	C_{LOAD} < 1 nF(7)	–5		5	mA
	Load regulation	Load to GND or VDD		0.15	0.35	mV/mA
I_{SC}	Short-circuit current	REFOUT to GND		23		mA
		REFOUT to VDD		–21		
PSRR	Power-supply rejection ratio		–200	±30	200	µV/V
DIGITAL INPUTS (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	GND ≤ V_{IN} ≤ VDD			35	µA
C_{IN}	Input capacitance			3		pF
V_{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
DIGITAL OUTPUT: CMOS						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 21 MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	VDD – 0.1			V
		I_{OH} = –4 mA	VDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
I_{VDD}	High-side supply current	3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		5.2	6.8	mA
		3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF(8)		4.6	6.1	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		6.4	8.3	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF(8)		5.4	7.2	

(7) Capacitive load with a value ≥ 1nF requires series resistor to be connected to the REFOUT pin. See the *Reference Output* section for more details.
(8) Typical value is specified at f_{CLKIN} = 10 MHz, maximum value is specified at f_{CLKIN} = 11 MHz.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	MCE = 0	9	20	21	MHz
		MCE = 1	9	10	11	
$Duty_{Cycle}$	CLKIN clock duty cycle(1)		40%	50%	60%	
t_{H1}	DOUT hold time after rising edge of CLKIN	MCE = 0, C_{LOAD} = 15 pF	6			ns
t_{H2}	DOUT hold time after rising edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	6		23	ns
t_{H3}	DOUT hold time after falling edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	10		26	ns
t_{D1}	Rising edge of CLKIN to DOUT valid delay	MCE = 0, C_{LOAD} = 15 pF			25	ns
t_{D2}	Rising edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	11		27	ns
t_{D3}	Falling edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	15		30	ns
t_r	DOUT rise time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.5	3.5	
t_f	DOUT fall time	90% to 10%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5.8	ns
		90% to 10%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	4.4	
t_{ASTART}	Analog startup time	VDD step to 3.0 V, 0.1% settling, CLKIN applied		0.25		ms

(1) The duty cycle of DOUT equals the clock duty cycle of the applied CLKIN signal.

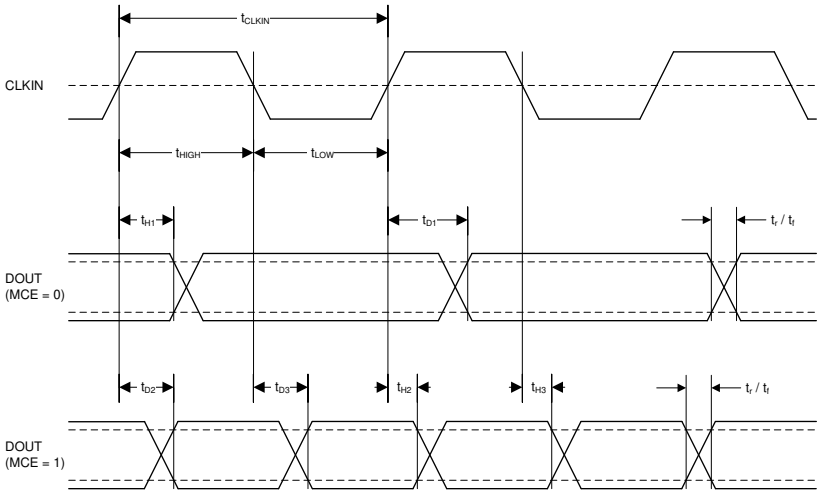

图 1. Digital Interface Timing

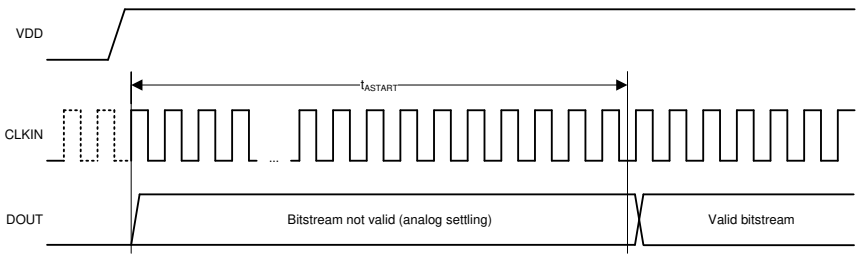

图 2. Device Startup Timing

6.7 Typical Characteristics

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

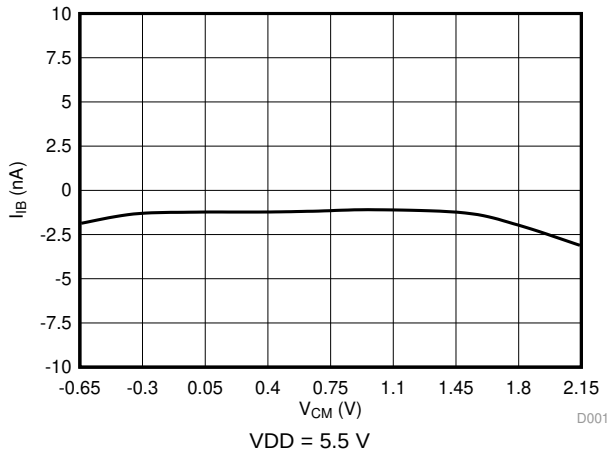

图 3. Input Bias Current vs Common-Mode Input Voltage

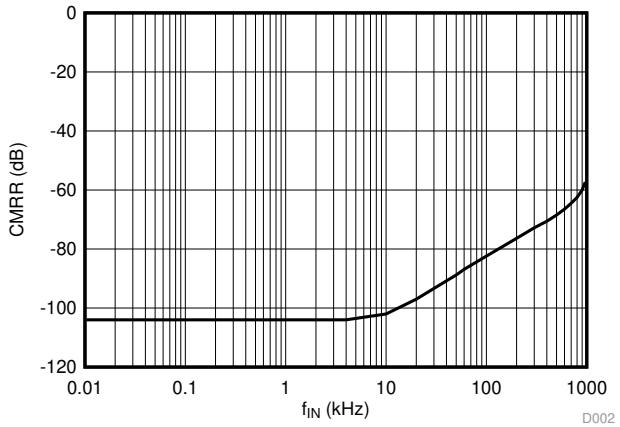

图 4. Common-Mode Rejection Ratio vs Input Signal Frequency

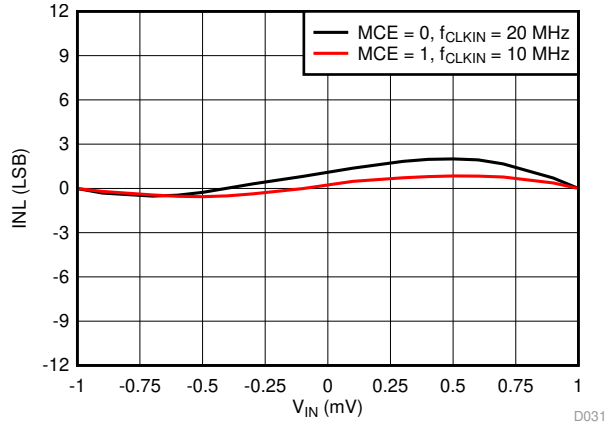

图 5. Integral Nonlinearity vs Input Voltage

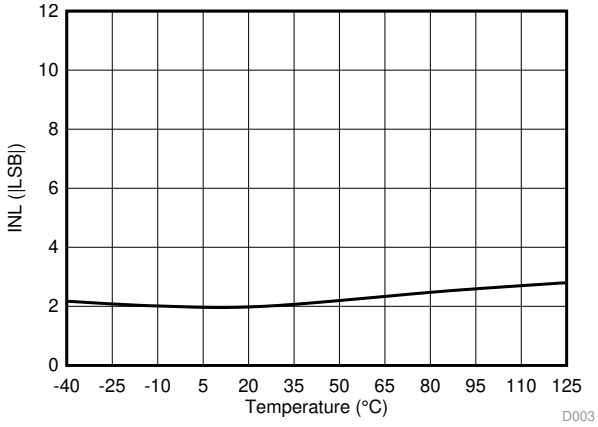

图 6. Integral Nonlinearity vs Temperature

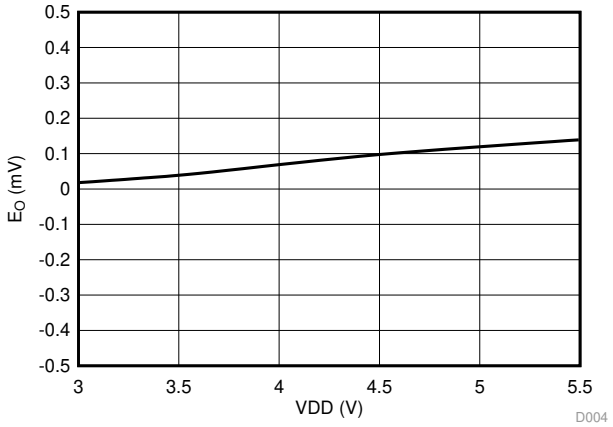

图 7. Offset Error vs Supply Voltage

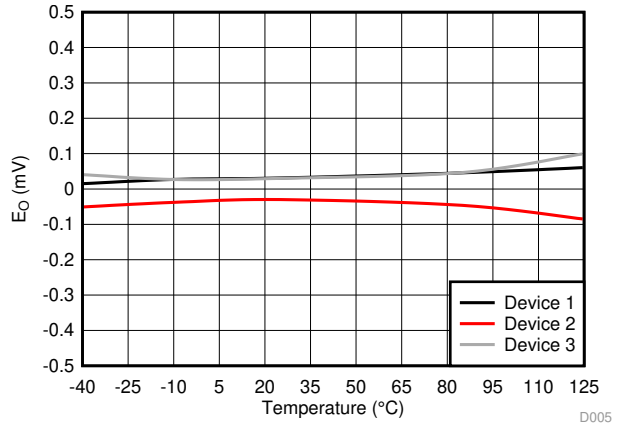

图 8. Offset Error vs Temperature

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Typical Characteristics (接下页)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

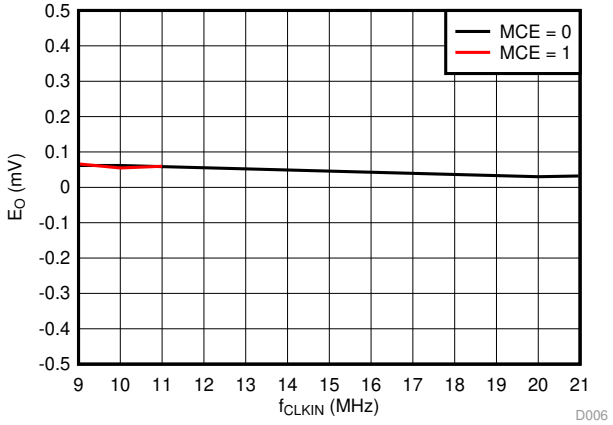

图 9. Offset Error vs Clock Frequency

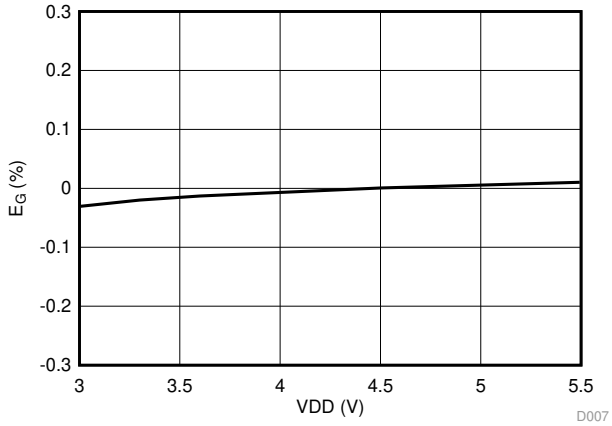

图 10. Gain Error vs Supply Voltage

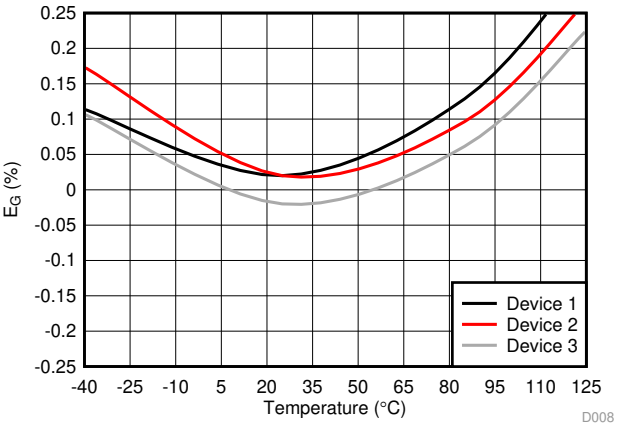

图 11. Gain Error vs Temperature

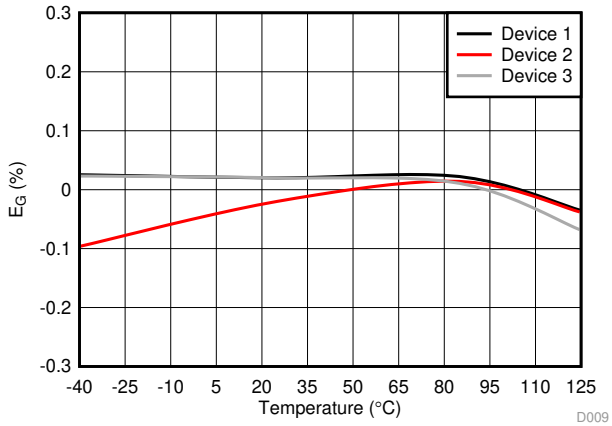

图 12. Ratiometric Gain Error vs Temperature

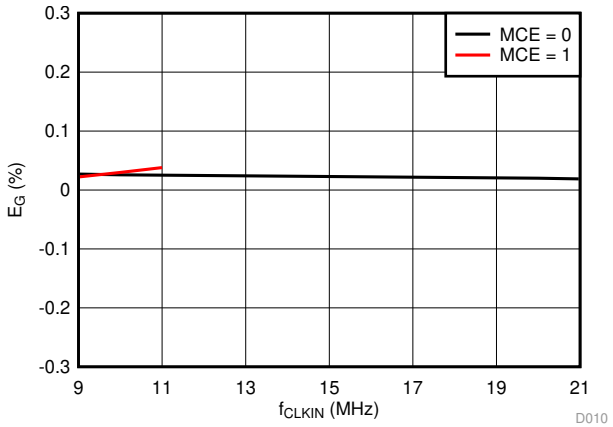

图 13. Gain Error vs Clock Frequency

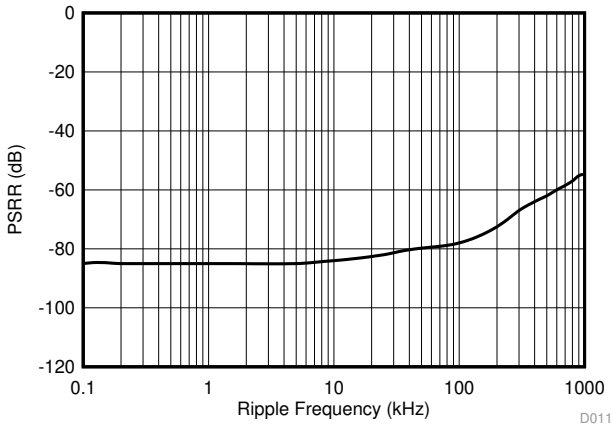

图 14. Power-Supply Rejection Ratio vs Ripple Frequency

Typical Characteristics (接下页)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

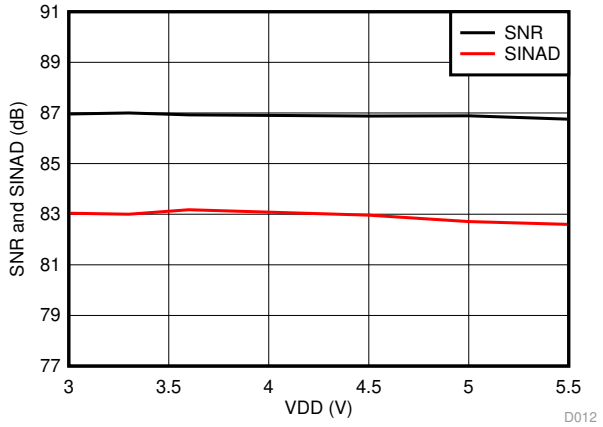

图 15. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage

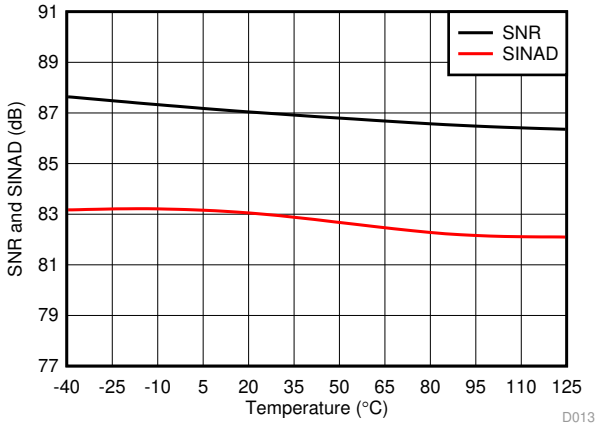

图 16. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

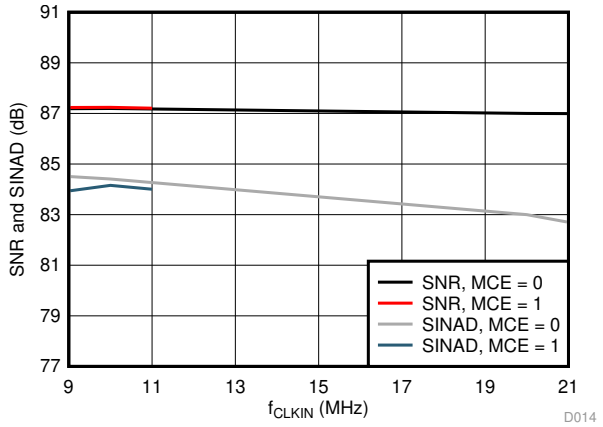

图 17. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

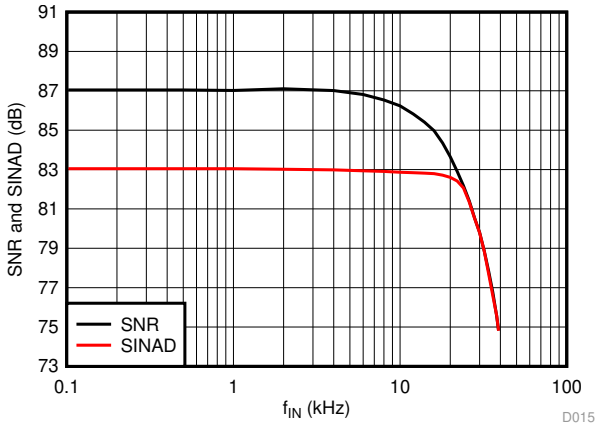

图 18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

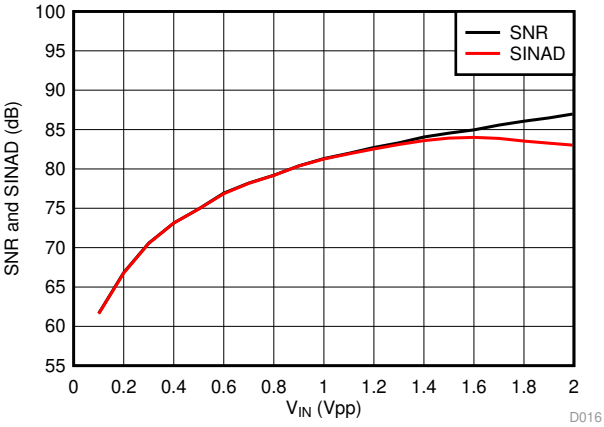

图 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

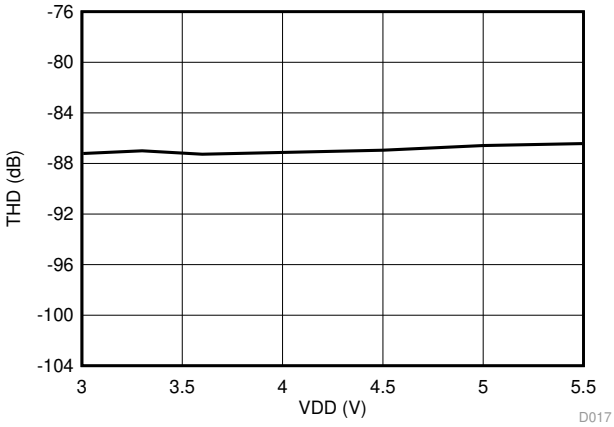

图 20. Total Harmonic Distortion vs Supply Voltage

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Typical Characteristics (接下页)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

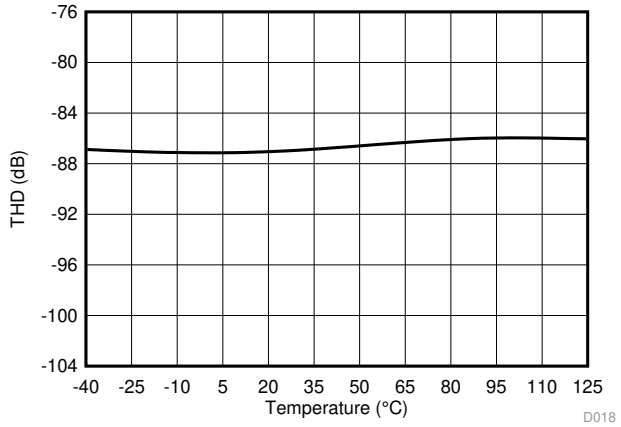


图 21. Total Harmonic Distortion vs Temperature

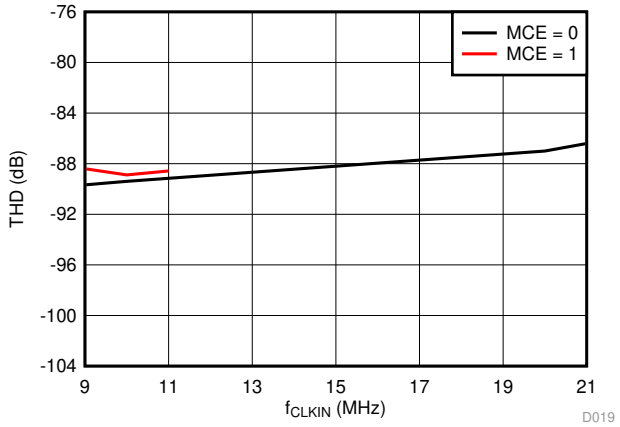


图 22. Total Harmonic Distortion vs Clock Frequency

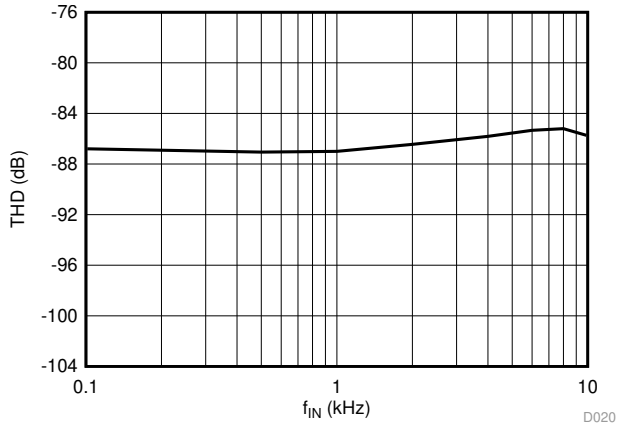


图 23. Total Harmonic Distortion vs Input Signal Frequency

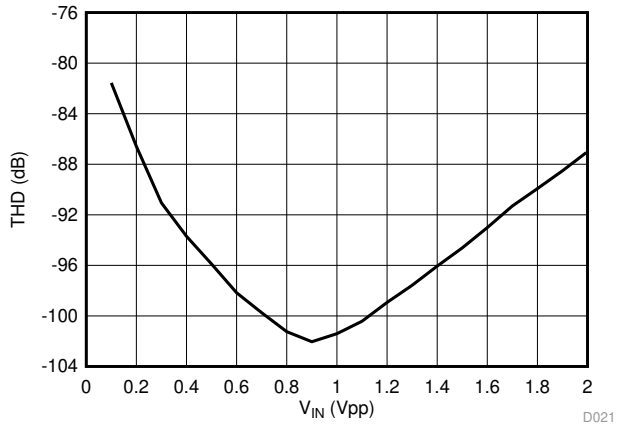


图 24. Total Harmonic Distortion vs Input Signal Amplitude

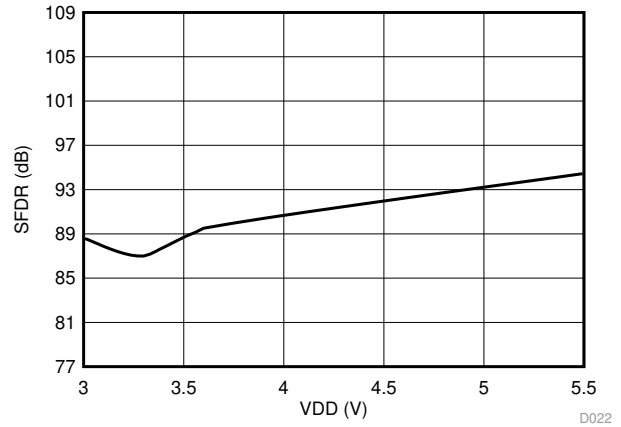


图 25. Spurious-Free Dynamic Range vs Supply Voltage

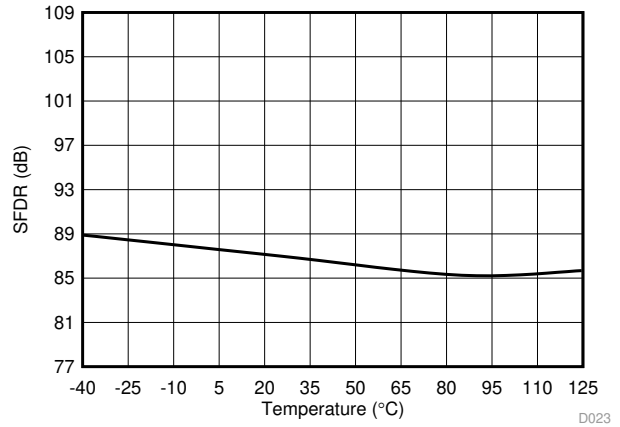


图 26. Spurious-Free Dynamic Range vs Temperature

Typical Characteristics (接下页)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

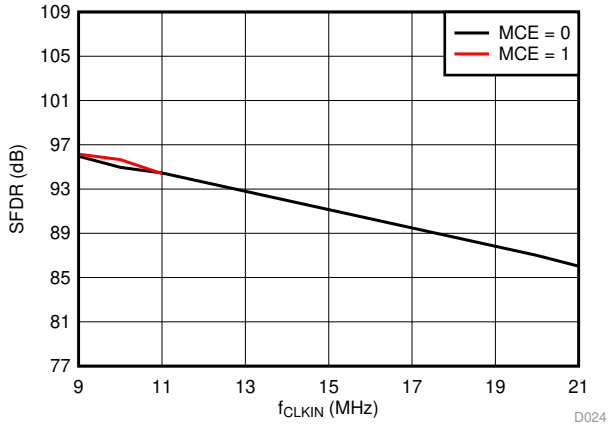


图 27. Spurious-Free Dynamic Range vs Clock Frequency

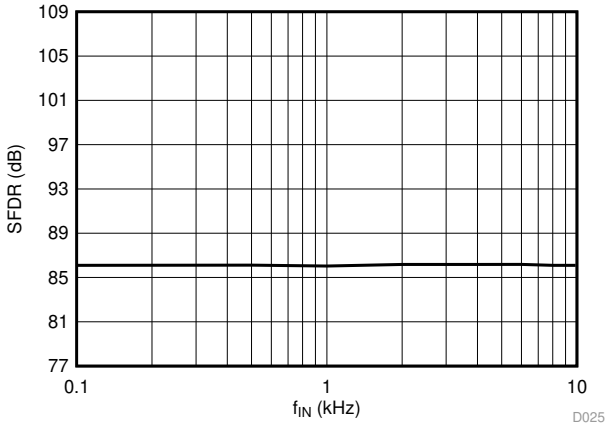


图 28. Spurious-Free Dynamic Range vs Input Signal Frequency

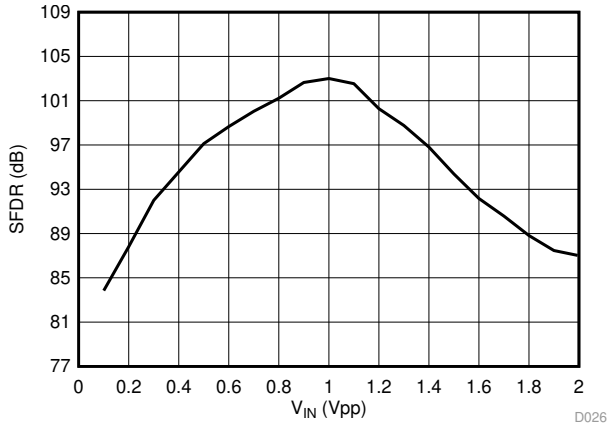
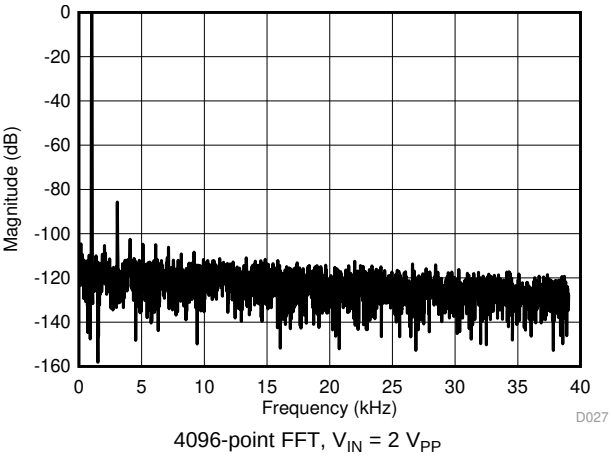
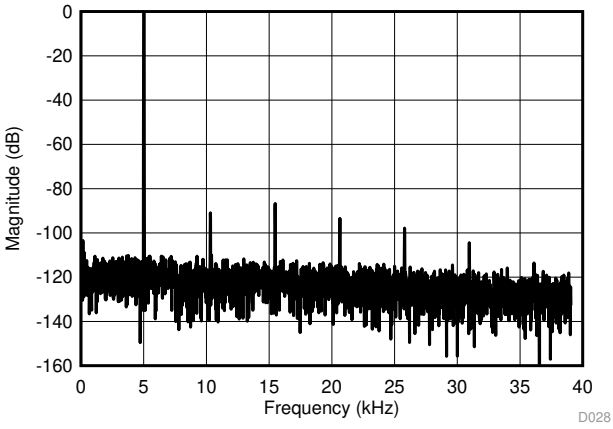


图 29. Spurious-Free Dynamic Range vs Input Signal Amplitude



4096-point FFT, V_{IN} = 2 V_{PP}

图 30. Frequency Spectrum With 1-kHz Input Signal



4096-point FFT, V_{IN} = 2 V_{PP}

图 31. Frequency Spectrum With 5-kHz Input Signal

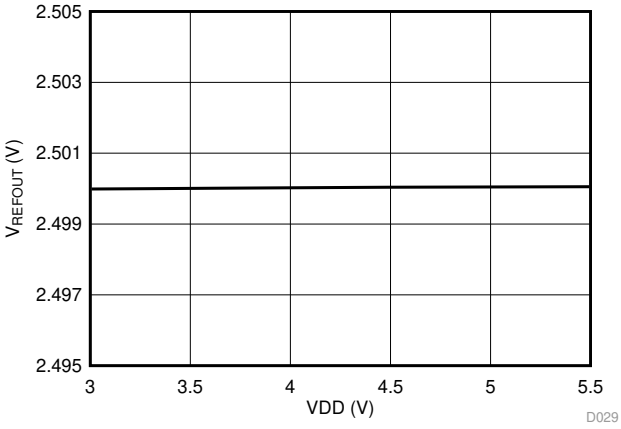


图 32. Reference Output Voltage vs Supply Voltage

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Typical Characteristics (接下页)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

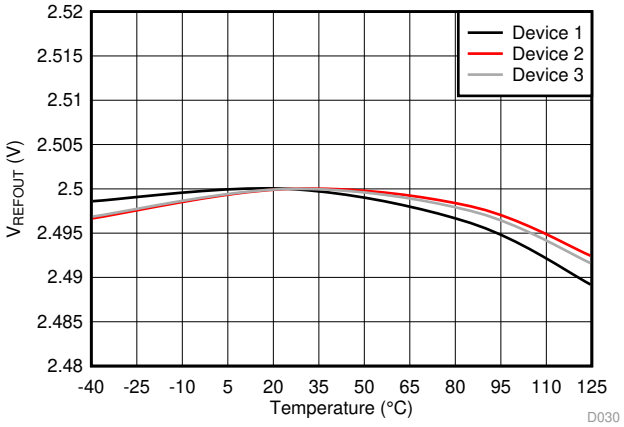


图 33. Reference Output Voltage vs Temperature

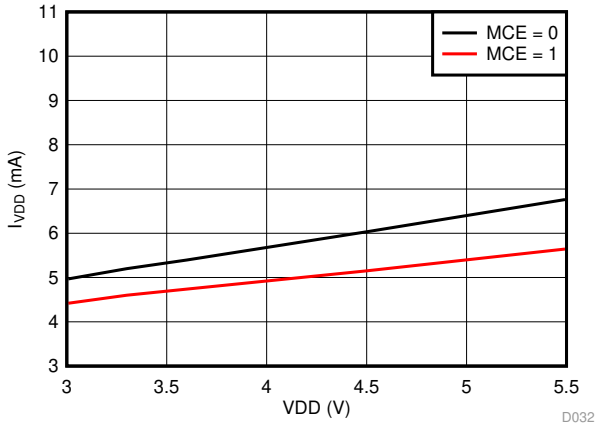


图 34. Supply Current vs Supply Voltage

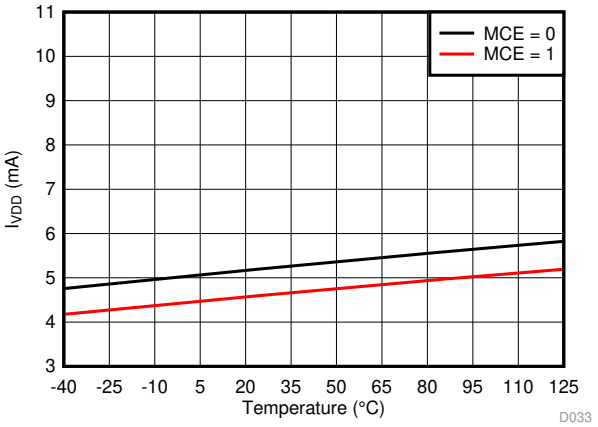


图 35. Supply Current vs Temperature

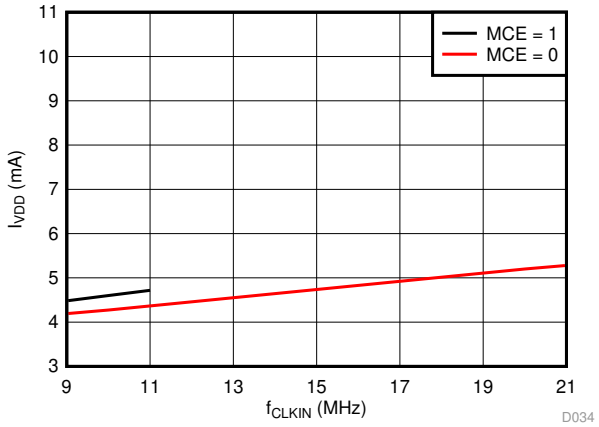


图 36. Supply Current vs Clock Frequency

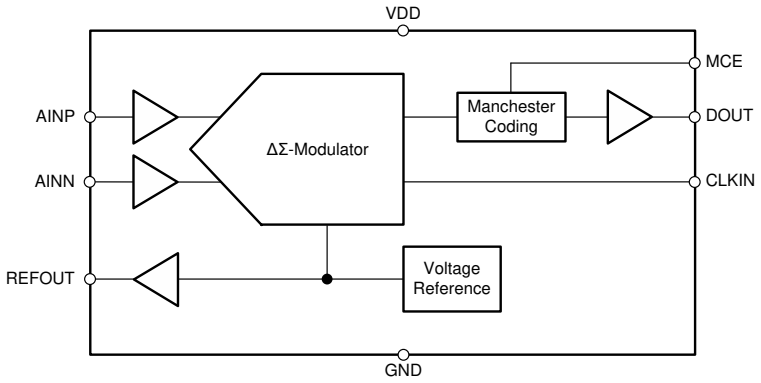
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1035 is a chopper-stabilized buffer, followed by the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 9 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1035. The 1.6-GΩ differential input resistance of the analog input stage supports low gain-error signal sensing in high-voltage applications using resistive dividers. The external clock input simplifies the synchronization of multiple measurement channels on the system level. The extended frequency range of up to 21 MHz supports higher performance levels compared to the other solutions available on the market.

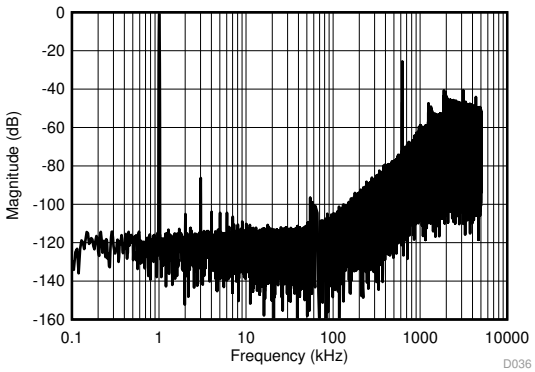
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1035 incorporates front-end circuitry that contains a buffered sampling stage, followed by a ΔΣ modulator. To support a bipolar input range, the device uses a charge pump that allows single-supply operation to simplify the overall system design and minimize the circuit cost. For reduced offset and offset drift, the input buffer is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. 图 37 shows the spur created by the switching frequency.



$sinc^3$ filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

图 37. Quantization Noise Shaping

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Feature Description (接下页)

The linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±1 V, and within the specified input common-mode range.

图 38 shows the specified common-mode input voltage that applies for the full-scale input voltage range as specified in this document along with the corresponding common-mode undervoltage and overvoltage threshold levels.

If smaller input signals are used, the operational common-mode input voltage range widens. 图 39 shows the common-mode input voltage that applies with no differential input signal; that is, when the voltage applied on AINP is equal to the voltage applied on AINN. The common-mode input voltage range scales with the actual differential input voltage between this range and the range in 图 38.

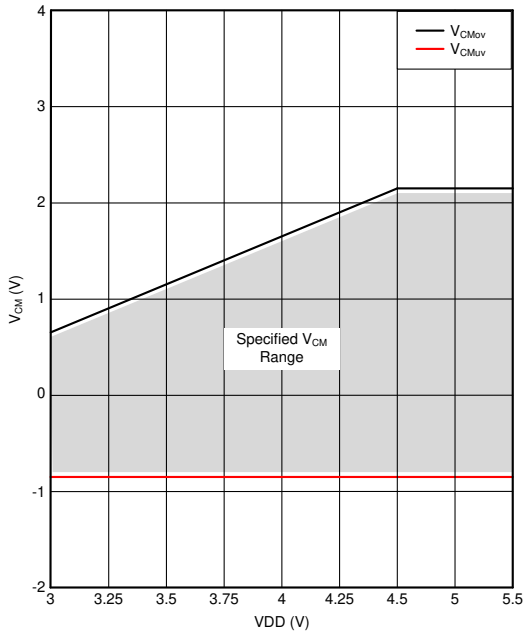

图 38. Common-Mode Input Voltage Range With a Full-Scale Differential Input Signal of ±1.25 V

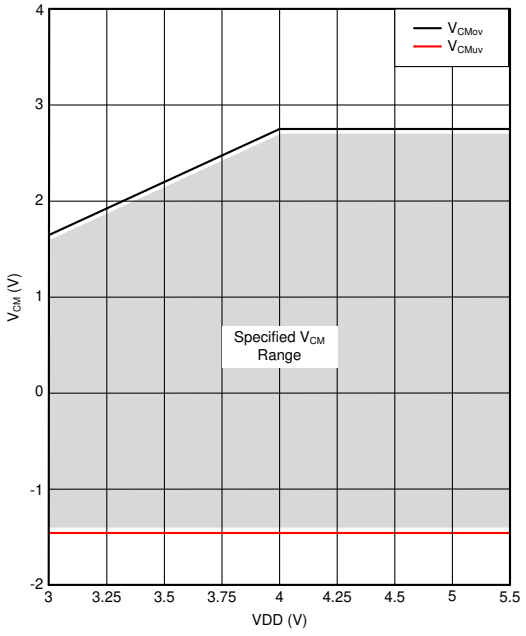

图 39. Common-Mode Input Voltage Range With a Zero Differential Input Signal

Feature Description (接下页)

7.3.2 Modulator

The modulator implemented in the AMC1035 (such as the one conceptualized in 图 40) is a second-order, switched-capacitor, feed-forward ΔΣ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

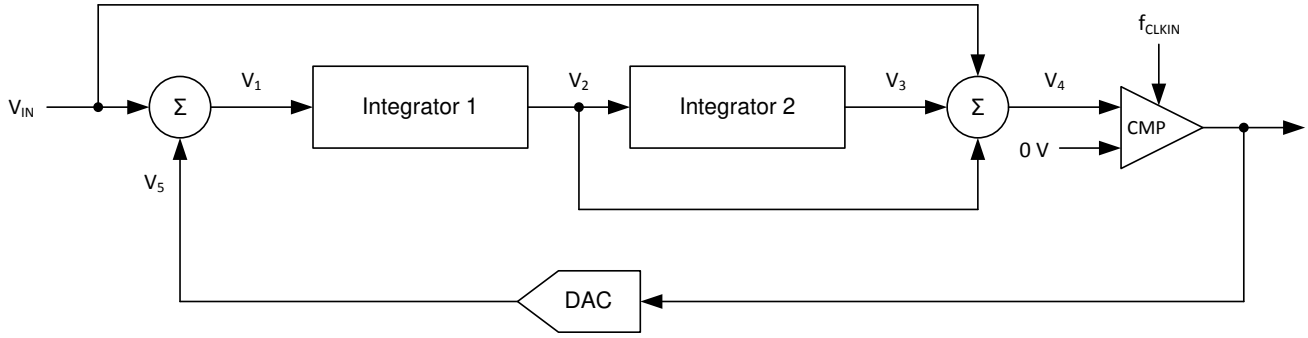

图 40. Block Diagram of a Second-Order Modulator

As depicted in 图 37, the modulator shifts the quantization noise to high frequencies. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F28004x, TMS320F2807x, and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1035. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters for a simple system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the AMC1210 (a four-channel digital sinc filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

7.3.3 Reference Output

The AMC1035 offers a voltage reference output that can source or sink current to significantly reduce the gain error thermal drift in ratiometric applications as specified in the *Electrical Characteristics* table. The *IGBT Temperature Sensing* section provides an example of a ratiometric use case for the AMC1035.

The reference output can drive capacitive loads less than 1 nF. Use a series resistor to avoid oscillations and degradation of performance for capacitive loads ≥ 1 nF. 表 1 lists the recommended series resistor values for given capacitor value examples. Interpolate for capacitive loads with a value between the given examples.

表 1. Series Resistor Value for Capacitive Loads ≥ 1 nF on REFOUT Pin

CAPACITIVE LOAD ON REFOUT PIN	1 nF	3.3 nF	10 nF	33 nF	100 nF	330 nF	1 µF	3.3 µF	10 µF
Recommended series resistor	33 Ω	56 Ω	47 Ω	33 Ω	15 Ω	10 Ω	5.6 Ω	3.3 Ω	1.8 Ω

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7.3.4 Clock Input

The AMC1035 system clock is provided externally at the CLKIN pin. The clock signal must be applied continuously for proper device operation.

To support the bipolar input voltage range with a single supply, the AMC1035 includes a charge pump. This charge pump stops operating if the clock signal is below the specified frequency range or if the signal is paused or missing. Additionally, the input bias current increases beyond the specified range and significantly reduces the input resistance of the device. When the clock signal is paused or missing, the modulator stops the analog signal conversion and the digital output signal remains frozen in the last logic state. When the clock signal is applied again after a pause, the internal analog circuitry biasing must settle for proper device performance. In this case, consider the t_{ASTART} specification in the *Switching Characteristics* table.

7.3.5 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982 (an unsigned code). A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1035 with performance as specified in this document. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1035 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). 图 41 shows the input voltage versus the output modulator signal.

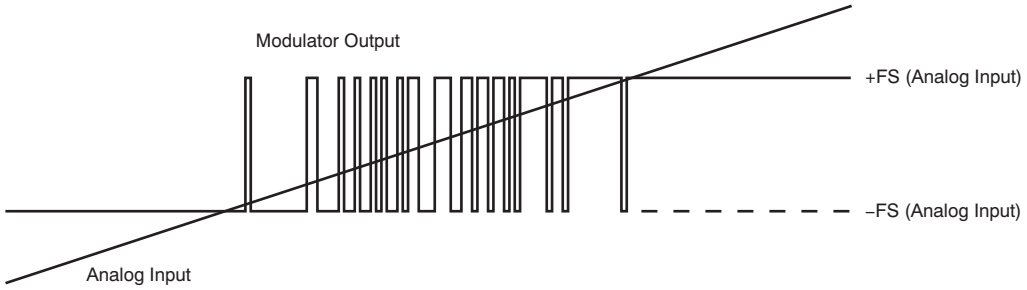

图 41. Analog Input versus the AMC1035 Modulator Output

公式 1 calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The modulator bitstream on the DOUT pin changes with the rising edge of the clock signal applied on the CLKIN pin. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.

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7.3.6 Manchester Coding Feature

The AMC1035 offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. The Manchester coding combines the clock and data information using exclusive-OR (XOR) logical operation that results in a bitstream free of DC components. 图 42 shows the resulting bitstream from this coding. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN. To enable Manchester coding on the AMC1035, pull the input pin MCE high. The DOUT signal is inverted if the MCE status changes when CLKIN is high.

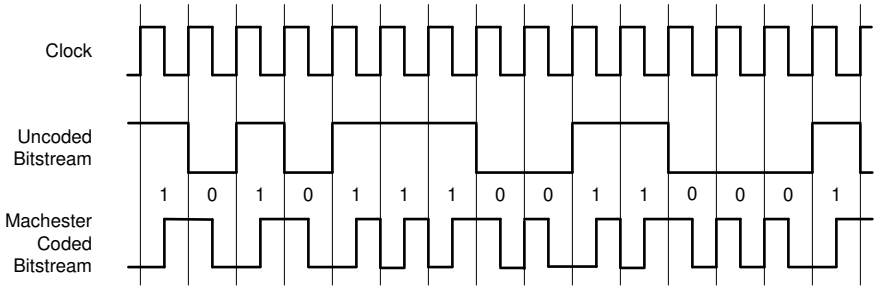

图 42. Manchester Coded Output of the AMC1035

7.4 Device Functional Modes

The AMC1035 is operational when the power supply VDD and clock signal CLKIN are applied, as specified in 图 39 and the *Switching Characteristics* table.

7.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1035 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in 图 43, depending on the actual polarity of the signal being sensed. This feature is also supported with Manchester-coded output and allows full-scale and invalid input signals to be identified as described in the *Fail-Safe Output* section and can be used for advanced system-level diagnostics.

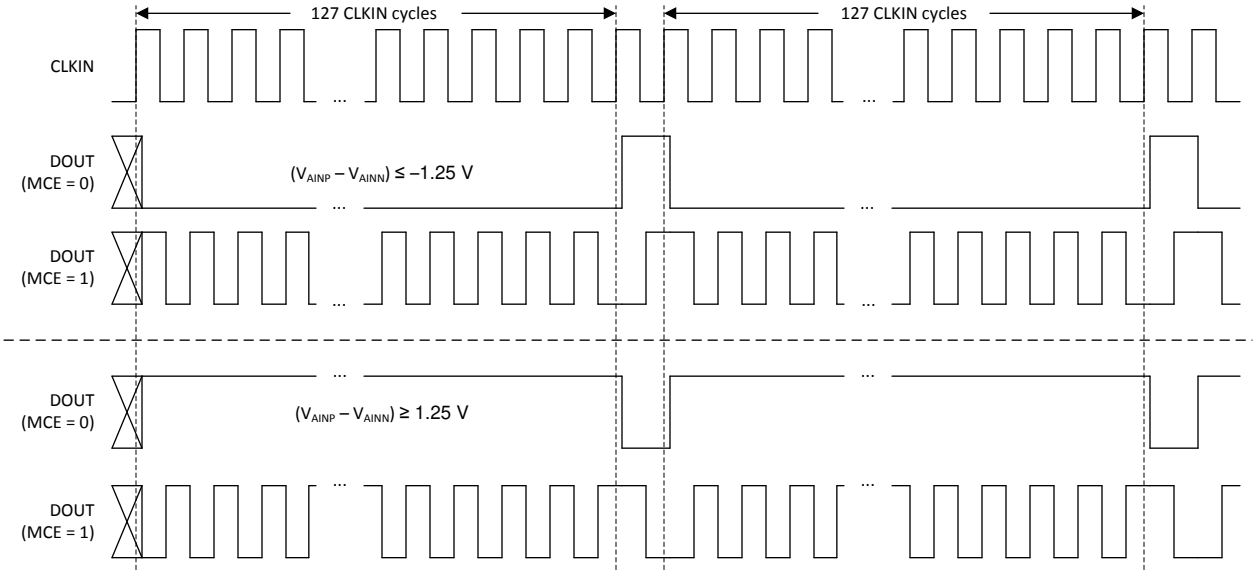

图 43. Overrange Output of the AMC1035

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Device Functional Modes (接下页)

7.4.2 Fail-Safe Output

图 44 shows that if the common-mode voltage of the input reaches or exceeds the specified common-mode undervoltage, V_{CMuv}, or overvoltage detection level, V_{CMov} as defined in the *Electrical Characteristics* table, the DOUT of the AMC1035 is held at steady-state high.

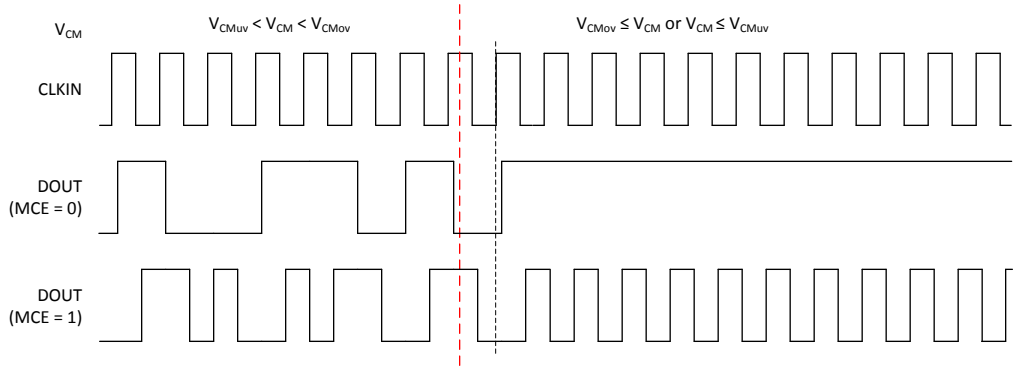

图 44. Fail-Safe Output of the AMC1035

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). 公式 2 shows a $sinc^3$-type filter, which is a very simple filter, built with minimal effort and hardware:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

8.2 Typical Applications

8.2.1 Voltage Sensing

ΔΣ modulators are widely used in frequency inverter designs because of their high AC and DC performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), and other industrial applications.

图 45 shows a simplified schematic of a motor drive application with the AMC1035 used for the DC-link and output phase voltage sensing. In this example, all resistive dividers reference to the negative DC-link voltage that is also used as a ground reference point for the microcontroller. An additional fifth AMC1035 can be used for temperature sensing of the insulated-gate bipolar transistor (IGBT) module; see the *IGBT Temperature Sensing* section for more details.

Current feedback is performed with shunt resistors (R_{SHUNT}) and TI's AMC1306M25 isolated modulators. Depending on the system design, either all three or only two motor phase currents are sensed.

Depending on the overall digital processing power requirements and with a total of eight ΔΣ modulator bitstreams to be processed by the MCU, a derivate from either the low-cost single-core TMS320F2807x or the dual-core TMS320F2837x families can be used in this application.

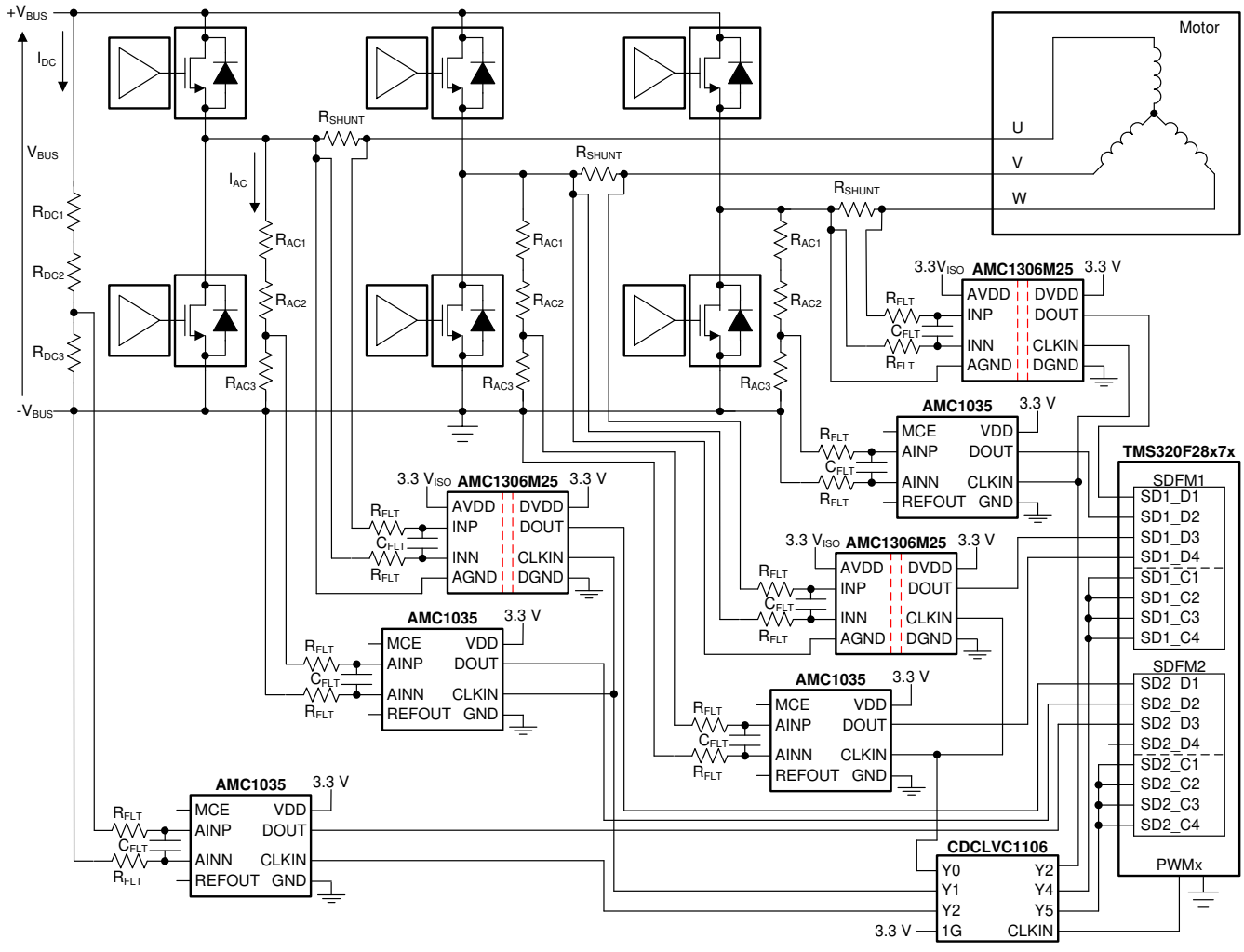

图 45. The AMC1035 in a Frequency Inverter Application

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Typical Applications (接下页)

8.2.1.1 Design Requirements

表 2 lists the parameters for this typical application.

表 2. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Voltage drop across the sensing resistor R_{DC1} for a linear response	1 V (maximum)
Voltage drop across the sensing resistors R_{ACx} for a linear response	±1 V (maximum)
Current through the sensing resistors R_{ACx}	±100 µV (maximum)

8.2.1.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive dividers to limit the cross current to the desired values:

- For the voltage sensing on the DC bus: $R_{DC1} + R_{DC2} + R_{DC3} = V_{BUS} / I_{DC}$
- For the voltage sensing on the output phases U, V, and W: $R_{AC1} + R_{AC2} + R_{AC3} = V_{PHASE\ (max)} / I_{AC}$

Consider the following two restrictions to choose the proper value of the resistors R_{DC3} and R_{AC3}:

- The voltage drop caused by the nominal voltage range of the system must not exceed the recommended input voltage range of the AMC1035: $V_{xC3} \leq V_{FSR}$
- The voltage drop caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{xC3} \leq V_{Clipping}$

Use similar approach for calculation of the shunt resistor values R_{SHUNT} and see the AMC1306M25 data sheet for further details.

表 3 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the DC bus.

表 3. Resistor Value Examples for DC Bus Sensing

PARAMETER	600-V DC BUS	800-V DC Bus
Resistive divider resistor R_{DC1}	3.01 MΩ	4.22 MΩ
Resistive divider resistor R_{DC2}	3.01 MΩ	4.22 MΩ
Sense resistor R_{DC3}	10 kΩ	10.5 kΩ
Resulting current through resistive divider I_{DC}	99.5 µA	94.7 µA
Resulting voltage drop on sense resistor V_{RDC3}	0.995 V	0.994 V

表 4 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 230 V and 690 V on the output phases.

表 4. Resistor Value Examples for Output Phase Voltage Sensing

PARAMETER	±400-V_{AC} PHASE	±690-V_{AC} PHASE
Resistive divider resistor R_{AC1}	2.0 MΩ	3.48 MΩ
Resistive divider resistor R_{AC2}	2.0 MΩ	3.48 MΩ
Sense resistor R_{AC3}	10.0 kΩ	10.0 kΩ
Resulting current through resistive divider I_{AC}	99.8 µA	99.0 µA
Resulting voltage drop on sense resistor V_{RAC3}	±0.998 V	±0.990 V

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Use a power supply with a nominal voltage of 3.3 V to directly connect all modulators to the microcontroller.

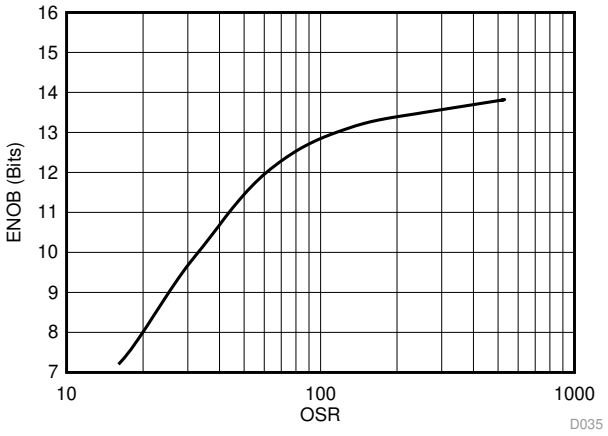
For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These MCU families support up to eight channels of dedicated hardwired filter structures called sigma-delta filter modules (SDFMs) that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one that offers a fast response path for overcurrent detection. Use one of the pulse-width modulation (PWM) sources inside the MCU to generate the clock for the modulators and for easy synchronization of all feedback signals and the switching control of the gate drivers.

图 45 uses a clock buffer to distribute the clock reference signal generated on one of the PWM outputs of the MCU (called PWMx in 图 45) to all modulators used in the circuit and as a reference for the digital filters in the MCU. In this example, TI's CDCLVC1106 is used for this purpose. Each CDCLVC1106 output can drive a load of 8 pF that is sufficient to drive up to two modulator and up to four SDFM clock inputs.

8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. 图 46 shows the ENOB of the AMC1035 with different oversampling ratios on a sinc3 filter. This number is calculated from the SINAD by using 公式 3 in this document.

$$SINAD = 1.76\ dB + 6.02\ dB \times ENOB \quad (3)$$



Sinc3 filter

图 46. Measured Effective Number of Bits vs Oversampling Ratio

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8.2.2 IGBT Temperature Sensing

The high input impedance of the AMC1035 is optimized for usage in voltage-sensing applications. Additionally, the internal voltage reference supports temperature sensing using a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) sensor often integrated in the IGBT module.

The same reference is internally used by the modulator, resulting in a ratiometric system solution that minimizes the overall temperature drift of the sensing path. 图 47 shows a simplified schematic of the AMC1035 used for temperature sensing of the IGBT module.

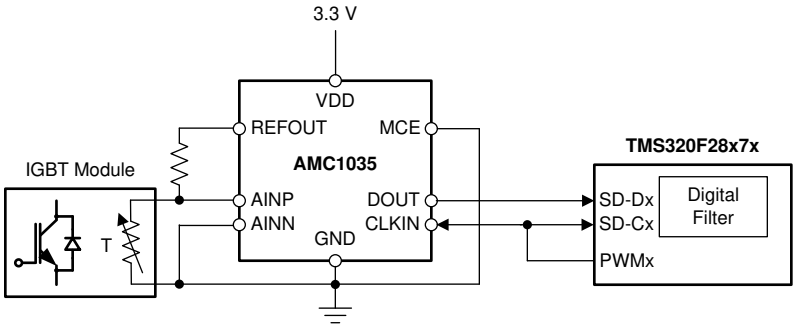

图 47. Using the AMC1035 for Temperature Sensing

8.2.3 What to Do and What Not to Do

Do not leave the analog inputs of the AMC1035 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current may drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes. In both cases, the modulator outputs a fail-safe bitstream as described in the *Fail-Safe Output* section.

9 Power Supply Recommendations

For decoupling of the power supply, a 0.1-µF capacitor is recommended to be placed as close to the VDD pin of the AMC1035 as possible, as shown in 图 48, followed by an additional capacitor in the range of 1 µF to 10 µF.

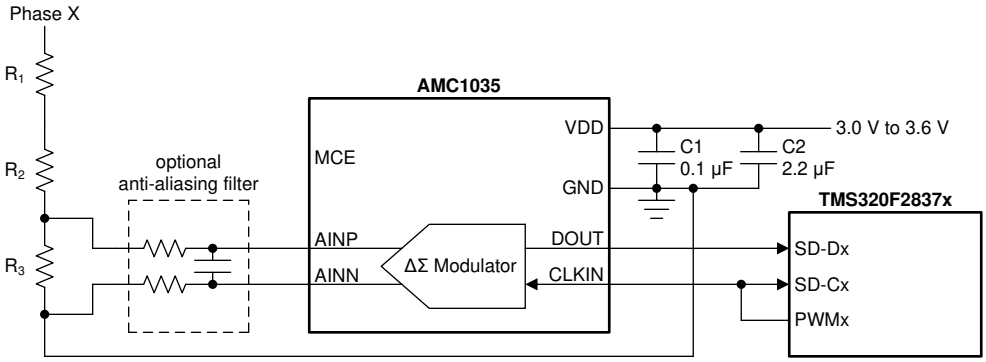

图 48. Decoupling the AMC1035

Safety considerations or high common-mode voltage levels may require the AMC1035 to be galvanically isolated from other parts of the system. 图 49 shows an example of a circuit that uses the ISO7721 to isolate the signal path and the SN6501 and a transformer to generate the required isolated power.

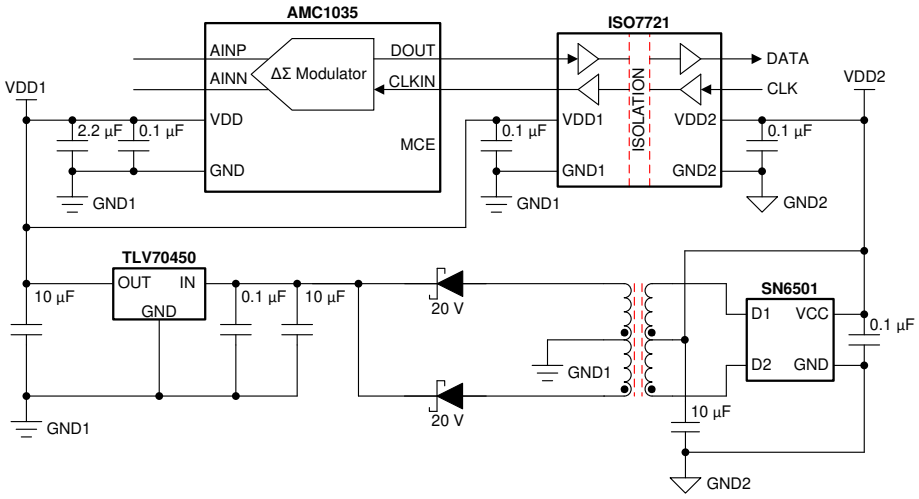

图 49. Galvanic Isolation of the AMC1035

图 50 shows an alternative solution that uses the ISOW7821 to isolate the signal path and provide the isolated power supply for the AMC1035.

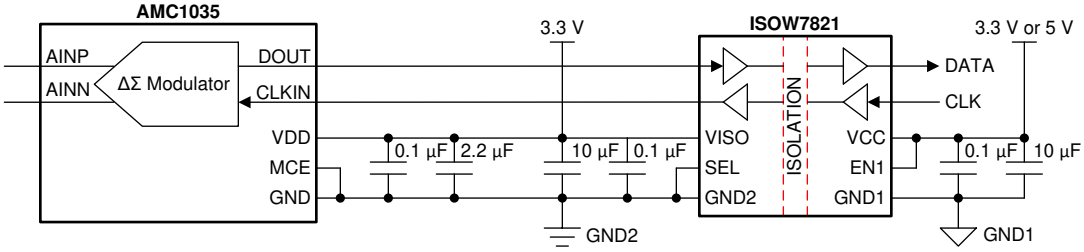

图 50. Galvanic Isolation of the AMC1035 for PCB Space-Constrained Applications

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10 Layout

10.1 Layout Guidelines

图 51 shows two layout recommendations for designs based on 1206-SMD or 0603-SMD size decoupling capacitors placed as close as possible to the AMC1035. For best performance, place the AMC1035 as close as possible to the source of the analog signal to be converted and keep the layout of the AINP and AINN traces symmetrical.

10.2 Layout Example

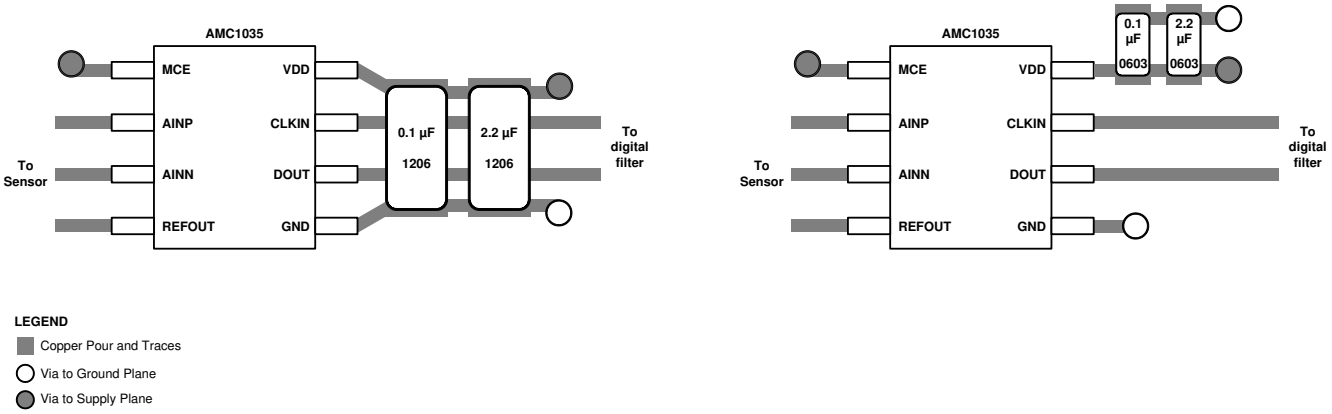

图 51. Recommended Layout of the AMC1035

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TMS320F28004x Piccolo™ 微控制器》数据表*
- 德州仪器 (TI)，*《TMS320F2807x Piccolo™ 微控制器》数据表*
- 德州仪器 (TI)，*《TMS320F2837xD 双核 Delfino™ 微控制器》数据表*
- 德州仪器 (TI)，*《具有优异 EMC 性能的 ISO772x 高速双通道数字隔离器》数据表*
- 德州仪器 (TI)，*《MSP430F677x 多相位仪表计量片上系统》数据表*
- 德州仪器 (TI)，*《适用于二阶 Δ-Σ 调制器的 AMC1210 四路数字滤波器》数据表*
- 德州仪器 (TI)，*《将 ADS1202 与 FPGA 数字滤波器结合，以便在电机控制应用中进行 电流测量》中的电流》应用报告*
- 德州仪器 (TI)，*《具有高 CMTI 的 AMC1306x 小型、高精度、增强型隔离式 Δ-Σ 调制器》数据表*
- 德州仪器 (TI)，*《CDCLVC11xx 3.3V 和 2.5V LVCMOS 高性能时钟缓冲器系列》数据表*
- 德州仪器 (TI)，*《LM117、LM317-N 宽温度范围三引脚可调稳压器》数据表*
- 德州仪器 (TI)，*《用于隔离式电源的 SN6502 低噪声 350mA 410kHz 变压器驱动器》数据表*
- 德州仪器 (TI)，*《具有集成式高效低辐射直流/直流转换器的 ISOW7821 高性能 5000V_{RMS} 增强型双通道数字隔离器》数据表*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1035D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035
AMC1035D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035
AMC1035DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035
AMC1035DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC1035 :

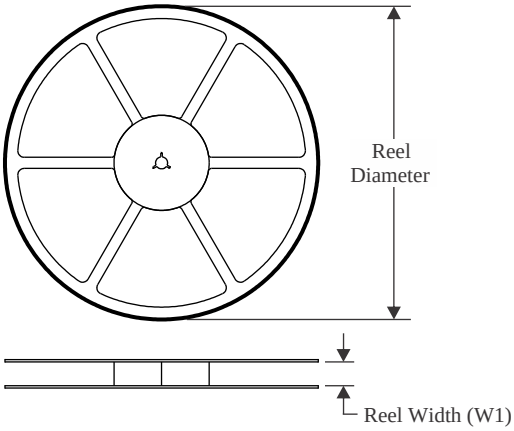
- Automotive : AMC1035-Q1

NOTE: Qualified Version Definitions:

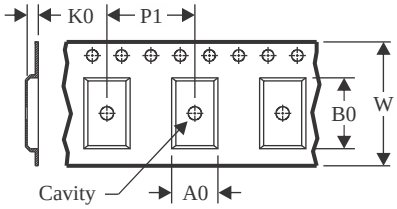
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

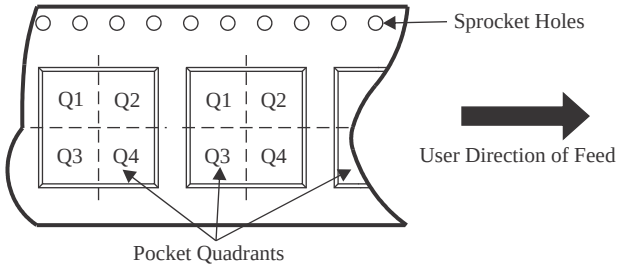


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

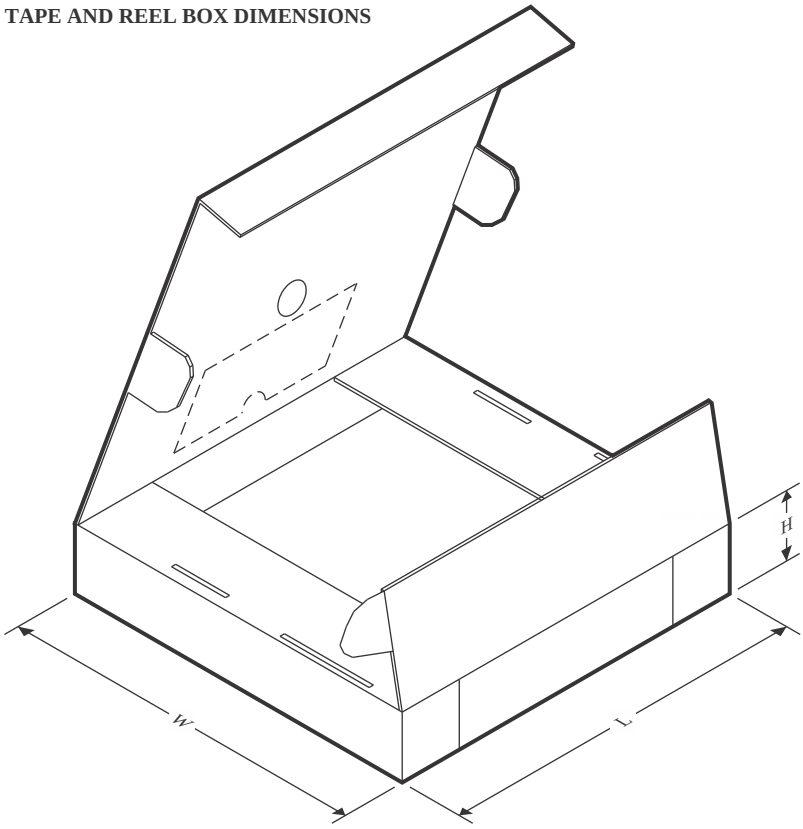
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1035DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

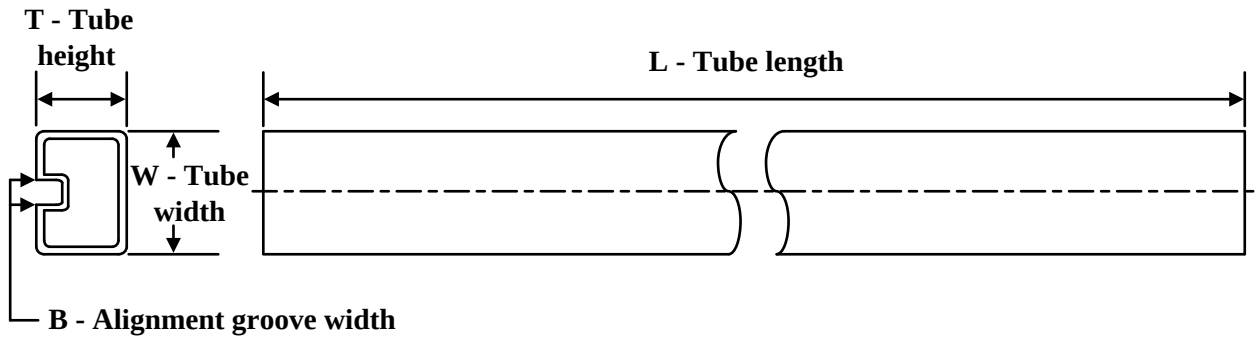
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

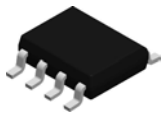
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1035DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1035D	D	SOIC	8	75	507	8	3940	4.32
AMC1035D.B	D	SOIC	8	75	507	8	3940	4.32

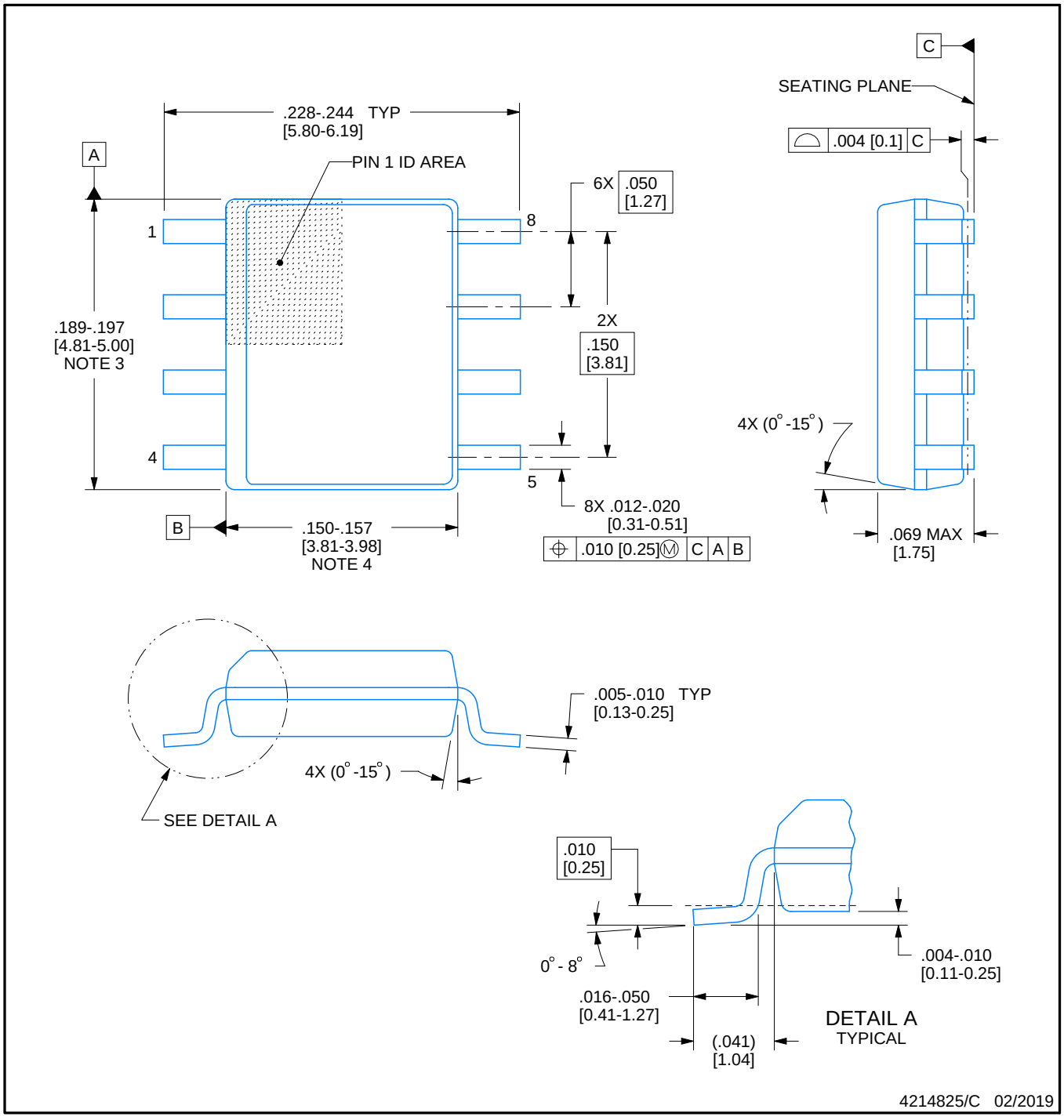


PACKAGE OUTLINE

D0008A

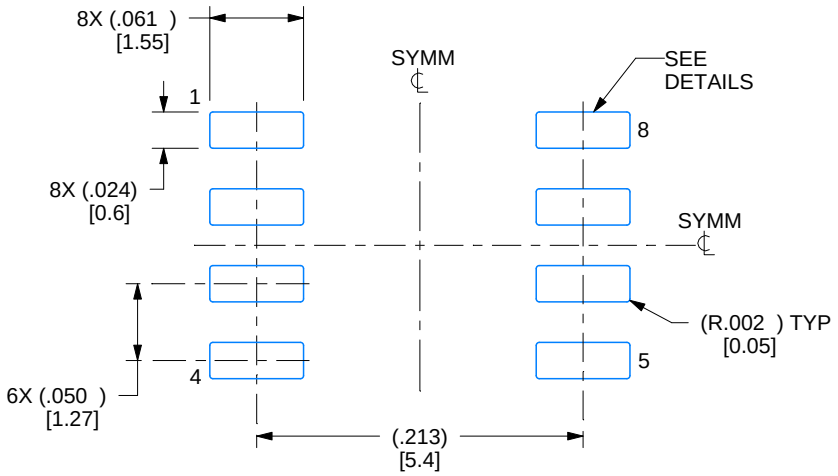
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

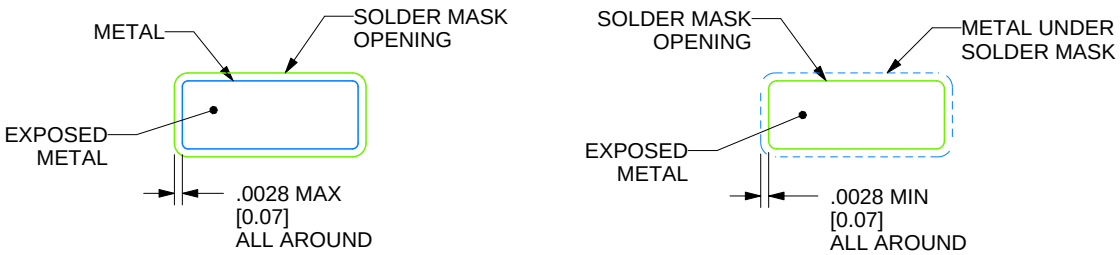


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

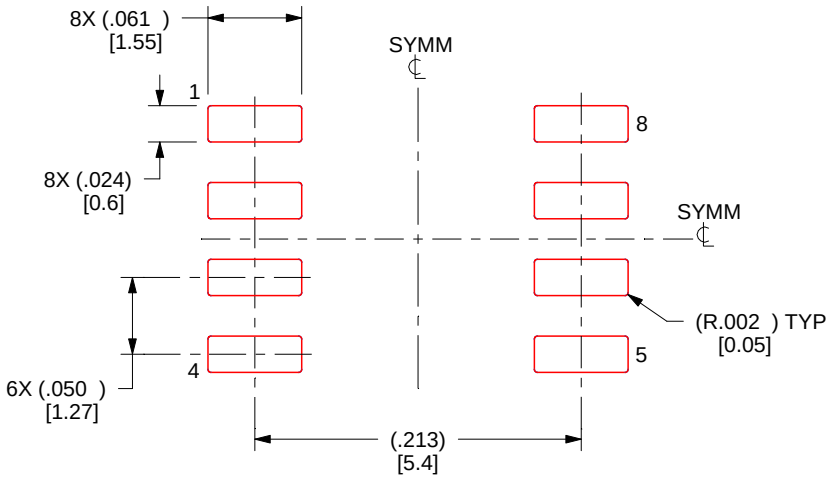
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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