

# 适用于汽车系统，具有集成式 ADC 和可调湿性电流的 TIC12400-Q1 24 路输入多开关检测接口 (MSDI)

## 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 的工作环境温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C4B
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- 旨在支持 12V 汽车系统，并提供过压和欠压警告
- 监控多达 24 路直接开关输入，并可配置其中 10 路输入以监控接地或连接到电池的开关
- 开关输入可承受高达 40V 的电压（负载突降条件）和低至 -24V 的电压（反极性条件）
- 6 种可配置的湿性电流设置：
  - （0mA、1mA、2mA、5mA、10mA 和 15mA）
- 适用于多位模拟开关监控的 10 位集成 ADC
- 适用于数字开关监控并具有 4 个可编程阈值的集成比较器
- 轮询模式下的超低工作电流：
  - 68  $\mu$ A 典型值（ $t_{\text{POLL}} = 64\text{ms}$ ， $t_{\text{POLL\_ACT}} = 128 \mu\text{s}$ ，全部 24 路输入均有效，比较器模式，所有开关均打开）
- 使用 3.3V/5V 串行外设接口 (SPI) 协议直接与 MCU 对接
- 可产生中断来支持所有输入的唤醒操作
- 集成电池和温度传感
- 采用适当的外部组件根据 ISO-10605 在输入引脚上实现  $\pm 8\text{kV}$  接触放电 ESD 保护
- 38 引脚 TSSOP 封装

## 2 应用

- 车身控制模块和网关
- 汽车照明
- 制热和制冷
- 电动座椅
- 后视镜

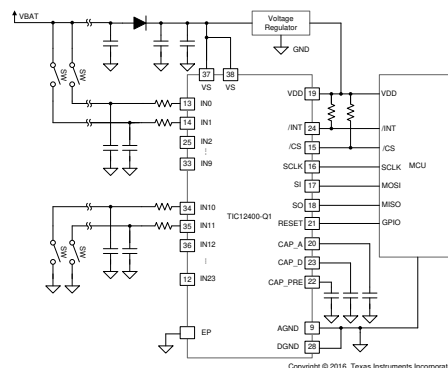
## 3 说明

TIC12400-Q1 是一款先进的多开关检测接口 (MSDI)，用于检测 12V 汽车系统中的外部开关状态。TIC12400-Q1 配有集成的 10 位 ADC，用于对多位模拟开关进行监控，并采用比较器以独立于 MCU 的方式对数字开关进行监控。可为 ADC 和比较器设定检测阈值，从而支持各种开关拓扑和系统非理想特性。该器件监控多达 24 路直接开关输入，并可配置其中 10 路输入以监控接地或连接到电池的开关。可为每路输入设定 6 种独特的湿性电流设置，从而支持不同的应用场景。该器件支持所有开关输入的唤醒操作，因此无需持续使 MCU 保持活动状态，进而可降低系统功耗。TIC12400-Q1 还提供集成故障检测、ESD 保护和诊断功能，从而提高系统稳健性。TIC12400-Q1 支持 2 种工作模式：连续模式和轮询模式。连续模式下将连续提供湿性电流。轮询模式下将根据可编程计时器来定期接通湿性电流以对输入状态进行采样，从而显著降低系统功耗。

### 器件信息

| 器件型号        | 封装 <sup>(1)</sup> | 封装尺寸（标称值）       |
|-------------|-------------------|-----------------|
| TIC12400-Q1 | TSSOP (38)        | 9.70mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision B (February 2020) to Revision C (February 2022)</b> | <b>Page</b> |
|--|-------------|
| • 添加了 特性 “提供功能安全” .....  | <b>1</b>    |
| • 将提到的旧术语实例全部更改为控制器和响应器.....   | <b>1</b>    |

| <b>Changes from Revision A (September 2017) to Revision B (February 2020)</b> | <b>Page</b> |
|---|-------------|
| • Added ADC error for 0 mA current setting in 节 6.5 table.....                | <b>6</b>    |
| • Added RIN_SC spec for $V_S$ above 7 V in 节 6.5 table.....                   | <b>6</b>    |
| • Added RIN_COMP spec for $V_S$ above 7 V in 节 6.5 table.....                 | <b>6</b>    |
| • Changed WC_CFG0 for CSO and CSI in matrix mode in 表 8-59 .....              | <b>115</b>  |

| <b>Changes from Revision * (August 2017) to Revision A (September 2017)</b>   | <b>Page</b> |
|---|-------------|
| • Changed the $I_{WETT}$ value in the <i>Electrical Characteristics</i> table.....  | <b>6</b>    |
| • Changed From: $4.5\text{ V} \leq V_S \leq 5\text{ V}$ To: $4.5\text{ V} \leq V_S < 5.5\text{ V}$ in 图 6-6 .....   | <b>11</b>   |
| • Changed From: $4.5\text{ V} \leq V_S \leq 35\text{ V}$ To: $5.5\text{ V} \leq V_S \leq 35\text{ V}$ in 图 6-7 .....  | <b>11</b>   |
| • Changed the <i>Microcontroller Wake-Up</i> section, and 图 8-9 .....   | <b>24</b>   |
| • Changed 表 9-5 .....   | <b>123</b>  |
| • Changed text in list item 2 From: <i>current ranging between 4.3 mA and 5.6 mA</i> . To: <i>current ranging between 4.5 mA and 5.5 mA (for <math>V_S - IN_X \geq 3\text{ V}</math> condition)</i> . ..... | <b>123</b>  |

## 5 Pin Configuration and Functions

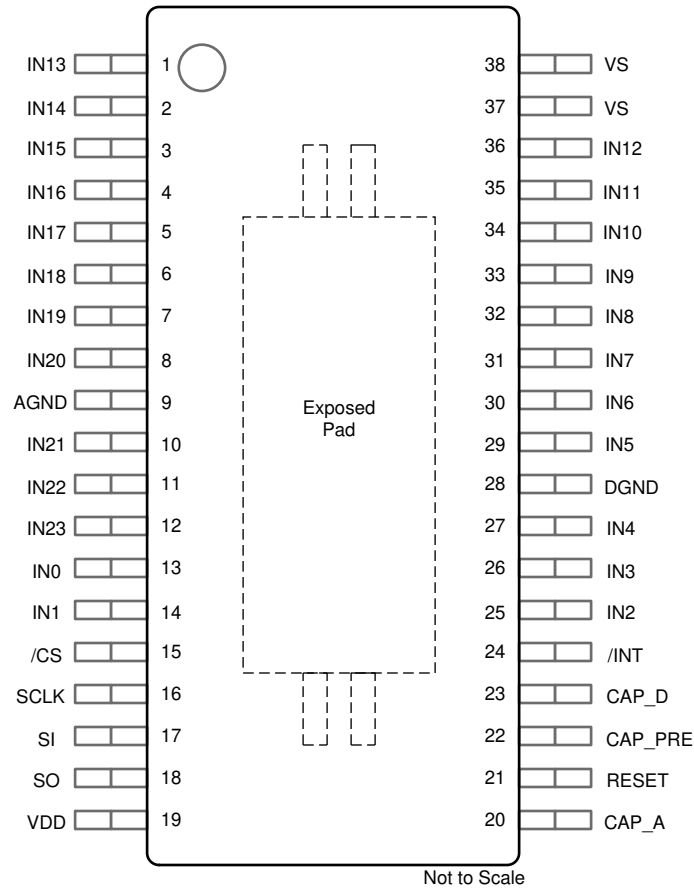


图 5-1. DCP (TSSOP) Package, 38-Pin, Top View

### Pin Functions

| PIN |                 | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----|-----------------|---------------------|---|
| NO. | NAME            |                     |   |
| 1   | IN13            | I/O                 | Ground switch monitoring input with current source.                                       |
| 2   | IN14            | I/O                 | Ground switch monitoring input with current source.                                       |
| 3   | IN15            | I/O                 | Ground switch monitoring input with current source.                                       |
| 4   | IN16            | I/O                 | Ground switch monitoring input with current source.                                       |
| 5   | IN17            | I/O                 | Ground switch monitoring input with current source.                                       |
| 6   | IN18            | I/O                 | Ground switch monitoring input with current source.                                       |
| 7   | IN19            | I/O                 | Ground switch monitoring input with current source.                                       |
| 8   | IN20            | I/O                 | Ground switch monitoring input with current source.                                       |
| 9   | AGND            | P                   | Ground for analog circuitry.  |
| 10  | IN21            | I/O                 | Ground switch monitoring input with current source.                                       |
| 11  | IN22            | I/O                 | Ground switch monitoring input with current source.                                       |
| 12  | IN23            | I/O                 | Ground switch monitoring input with current source.                                       |
| 13  | IN0             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source. |
| 14  | IN1             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source. |
| 15  | $\overline{CS}$ | I                   | Active-low input. Chip select from the controller for the SPI Interface.                  |
| 16  | SCLK            | I                   | Serial clock output from the controller for the SPI Interface.                            |
| 17  | SI              | I                   | Serial data input for the SPI Interface.  |

**Pin Functions (continued)**

| PIN |                 | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----|-----------------|---------------------|---|
| NO. | NAME            |                     |   |
| 18  | SO              | O                   | Serial data output for the SPI Interface.   |
| 19  | V <sub>DD</sub> | P                   | 3.3 V to 5.0 V logic supply for the SPI communication. The SPI I/Os are not fail-safe protected: VDD needs to be present during any SPI traffic to avoid excessive leakage currents and corrupted SPI I/O logic levels.   |
| 20  | CAP_A           | I/O                 | External capacitor connection for the analog LDO. Use capacitance value of 100 nF.  |
| 21  | RESET           | I                   | Keep RESET low for normal operation and drive RESET high and release it to perform a hardware reset of the device. The RESET pin is connected to ground via a 1M $\Omega$ pull-down resistor. If not used, the RESET pin shall be grounded to avoid any accidental device reset due to coupled noise onto this pin. |
| 22  | CAP_Pre         | I/O                 | External capacitor connection for the pre-regulator. Use capacitance value of 1 $\mu$ F.  |
| 23  | CAP_D           | I/O                 | External capacitor connection for the digital LDO. Use capacitance value of 100 nF.   |
| 24  | INT             | O                   | Open drain output. Pulled low (internally) upon change of state on the input or occurrence of a special event.  |
| 25  | IN2             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 26  | IN3             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 27  | IN4             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 28  | DGND            | P                   | Ground for digital circuitry.   |
| 29  | IN5             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 30  | IN6             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 31  | IN7             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 32  | IN8             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 33  | IN9             | I/O                 | Ground/V <sub>BAT</sub> switch monitoring input with configurable current sink or source.   |
| 34  | IN10            | I/O                 | Ground switch monitoring input with current source.   |
| 35  | IN11            | I/O                 | Ground switch monitoring input with current source.   |
| 36  | IN12            | I/O                 | Ground switch monitoring input with current source.   |
| 37  | V <sub>S</sub>  | P                   | Power supply input pin.   |
| 38  | V <sub>S</sub>  | P                   | Power supply input pin.   |
| --- | EP              | P                   | Exposed Pad. The exposed pad is not electrically connected to AGND or DGND. Connect EP to the board ground to achieve rated thermal and ESD performance.  |

(1) I = input, O = output, I/O = input and output, P = power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

|  |   | MIN  | MAX               | UNIT |
|--|---|------|-------------------|------|
| Input voltage                                  | V <sub>S</sub> , INT                      | -0.3 | 40 <sup>(2)</sup> | V    |
|  | V <sub>DD</sub> , SCLK, SI, SO, CS, RESET | -0.3 | 6                 | V    |
|  | IN0- IN23                                 | -24  | 40 <sup>(2)</sup> | V    |
|  | CAP_Pre                                   | -0.3 | 5.5               | V    |
|  | CAP_A                                     | -0.3 | 5.5               | V    |
|  | CAP_D                                     | -0.3 | 2                 | V    |
| Operating junction temperature, T <sub>J</sub> |   | -40  | 150               | °C   |
| Storage temperature, T <sub>stg</sub>          |   | -55  | 155               | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Tested for load dump and jump start conditions with nominal operating voltage no greater than 16 V for the life of a 12-V automotive system. Refer to [§ 9.2](#) for more details.

### 6.2 ESD Ratings

|                    |                         |  | VALUE                              | UNIT  |
|--------------------|-------------------------|--|------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>  | All pins                           | ±2000 |
|                    |                         |  | Pins IN0-IN23 <sup>(2)</sup>       | ±4000 |
|                    |                         | Charged-device model (CDM), per AEC Q100-011   | All pins                           | ±500  |
|                    |                         |  | Corner pins (pin 1, 19, 20 and 38) | ±750  |
|                    |                         | Contact discharge, un-powered, per ISO- 10605:<br>• External components: capacitor = 15 nF; resistor = 10 Ω<br>• ESD generator parameters: storage capacitance = 150 pF; discharge resistance = 330 Ω or 2000 Ω          | Pins IN0-IN23                      | ±8000 |
|                    |                         | Contact discharge, powered-up, per ISO- 10605:<br>• External components: capacitor = 15 nF; resistor = 33 Ω<br>• ESD generator parameters: storage capacitance = 150 pF or 330pF; discharge resistance = 330 Ω or 2000 Ω | Pins IN0-IN23                      | ±8000 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) ±4-kV rating on pins IN0-IN23 are stressed with respect to GND (with AGND, DGND, and EP tied together).

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range and V<sub>S</sub> = 12 V (unless otherwise noted).

|                     |                                | MIN               | NOM | MAX               | UNIT |
|---------------------|--------------------------------|-------------------|-----|-------------------|------|
| V <sub>S</sub>      | Power supply voltage           | 4.5               |     | 35 <sup>(2)</sup> | V    |
| V <sub>DD</sub>     | Logic supply voltage           | 3.0               |     | 5.5               | V    |
| V <sub>INT</sub>    | INT pin voltage                | 0                 |     | 35 <sup>(2)</sup> | V    |
| V <sub>INX</sub>    | IN0 to IN23 input voltage      | 0                 |     | 35 <sup>(2)</sup> | V    |
| V <sub>RESET</sub>  | RESET pin voltage              | 0                 |     | 5.5               | V    |
| V <sub>SPI_IO</sub> | SPI input/output logic level   | 0                 |     | V <sub>DD</sub>   | V    |
| f <sub>SPI</sub>    | SPI communication frequency    | 20 <sup>(1)</sup> |     | 4M                | Hz   |
| T <sub>A</sub>      | Operating free-air temperature | -40               |     | 125               | °C   |

- (1) Lowest frequency characterized.
- (2) Tested for load dump and jump start conditions with nominal operating voltage no greater than 16-V for the life of a 12-V automotive system. Refer to [§ 9.2](#) for more details.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TIC12400-Q1 | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | DCP (TSSOP) |      |
|                               |  | 38 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 33.6        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 18.4        | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 15.2        | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.5         | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 15.0        | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 1.2         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Over operating free-air temperature range,  $V_S = 4.5\text{ V}$  to  $35\text{ V}$ , and  $V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted).

| PARAMETER                   |   | TEST CONDITIONS  |  | MIN  | TYP | MAX | UNIT |
|-----------------------------|---|--|--|------|-----|-----|------|
| POWER SUPPLY                |   |  |  |      |     |     |      |
| I <sub>S_CONT</sub>         | Continuous mode V <sub>S</sub> power supply current                         | Continuous mode, I <sub>WETT</sub> = 10 mA, all switches open, no active ADC conversion or comparator comparison, no unserviced interrupt      |  |      | 5.6 | 7   | mA   |
| I <sub>S_POLL_COMP_25</sub> | Polling mode V <sub>S</sub> power supply average current in comparator mode | T <sub>A</sub> = 25°   | Polling mode, t <sub>POLL</sub> = 64 ms, t <sub>POLL_ACT</sub> = 128 μs, all 24 channels active and configured to comparator mode, all switches open, I <sub>WETT</sub> = 10 mA, no unserviced interrupt |      | 68  | 100 | μA   |
| I <sub>S_POLL_COMP_85</sub> |   | T <sub>A</sub> = -40° to 85°C  |  |      | 68  | 110 | μA   |
| I <sub>S_POLL_COMP</sub>    |   | T <sub>A</sub> = -40° to 125°C   |  |      | 68  | 170 | μA   |
| I <sub>S_POLL_ADC_25</sub>  | Polling mode V <sub>S</sub> power supply average current in ADC mode        | T <sub>A</sub> = 25°   | Polling mode, t <sub>POLL</sub> = 64 ms, t <sub>POLL_ACT</sub> = 128 μs, all 24 channels active and configured to ADC mode, all switches open, I <sub>WETT</sub> = 10 mA, no unserviced interrupt        |      | 75  | 105 | μA   |
| I <sub>S_POLL_ADC_85</sub>  |   | T <sub>A</sub> = -40° to 85°C  |  |      | 75  | 120 | μA   |
| I <sub>S_POLL_ADC</sub>     |   | T <sub>A</sub> = -40° to 125°C   |  |      | 75  | 180 | μA   |
| I <sub>S_RESET</sub>        | Reset mode V <sub>S</sub> power supply current                              | Reset mode, V <sub>RESET</sub> = V <sub>DD</sub> . V <sub>S</sub> = 12 V, all switches open, T <sub>A</sub> =25°C                              |  |      | 12  | 17  | μA   |
| I <sub>S_IDLE_25</sub>      | V <sub>S</sub> power supply average current in idle state                   | TRIGGER bit in CONFIG register = logic 0, T <sub>A</sub> = 25°C, no unserviced interrupt   |  |      | 50  | 75  | μA   |
| I <sub>S_IDLE_85</sub>      |   | TRIGGER bit in CONFIG register = logic 0, T <sub>A</sub> = -40°C to 85°C, no unserviced interrupt  |  |      | 50  | 95  | μA   |
| I <sub>S_IDLE</sub>         |   | TRIGGER bit in CONFIG register = logic 0, T <sub>A</sub> = -40°C to 125°C, no unserviced interrupt   |  |      | 50  | 145 | μA   |
| I <sub>DD</sub>             | Logic supply current from V <sub>DD</sub>                                   | SCLK = SI = 0 V, $\overline{CS}$ = $\overline{INT}$ = V <sub>DD</sub> , no SPI communication   |  |      | 1.5 | 10  | μA   |
| V <sub>POR_R</sub>          | Power on reset (POR) voltage for V <sub>S</sub>                             | Threshold for rising V <sub>S</sub> from device OFF condition resulting in INT pin assertion and a flagged POR bit in the INT_STAT register    |  | 3.85 |     | 4.5 | V    |
| V <sub>POR_F</sub>          |   | Threshold for falling V <sub>S</sub> from device normal operation to reset mode and loss of SPI communication                                  |  | 1.95 |     | 2.8 | V    |
| V <sub>OV_R</sub>           | Over-voltage (OV) condition for V <sub>S</sub>                              | Threshold for rising V <sub>S</sub> from device normal operation resulting in INT pin assertion and a flagged OV bit in the INT_STAT register  |  | 35   |     | 40  | V    |
| V <sub>OV_HYST</sub>        | Over-voltage (OV) condition hysteresis for V <sub>S</sub>                   |  |  | 1    |     | 3.5 | V    |
| V <sub>UV_R</sub>           | Under-voltage (UV) condition for V <sub>S</sub>                             | Threshold for rising V <sub>S</sub> from under-voltage condition resulting in INT pin assertion and a flagged UV bit in the INT_STAT register  |  | 3.85 |     | 4.5 | V    |
| V <sub>UV_F</sub>           |   | Threshold for falling V <sub>S</sub> from under-voltage condition resulting in INT pin assertion and a flagged UV bit in the INT_STAT register |  | 3.7  |     | 4.4 | V    |
| V <sub>UV_HYST</sub>        | Under-voltage (UV) condition hysteresis for V <sub>S</sub> <sup>(1)</sup>   |  |  | 75   |     | 275 | mV   |
| V <sub>DD_F</sub>           |   | Threshold for falling V <sub>DD</sub> resulting in loss of SPI communication   |  | 2.5  |     | 2.9 | V    |
| V <sub>DD_HYST</sub>        | Valid V <sub>DD</sub> voltage hysteresis                                    |  |  | 50   |     | 150 | mV   |

## 6.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_S = 4.5\text{ V}$  to  $35\text{ V}$ , and  $V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted).

| PARAMETER  |   | TEST CONDITIONS  |  | MIN  | TYP  | MAX  | UNIT |
|--|---|--|--|------|------|------|------|
| WETTING CURRENT ACCURACY (DIGITAL SWITCHES, MAXIMUM RESISTANCE VALUE WITH SWITCH CLOSED ≤ 100Ω , MINIMUM RESISTANCE VALUE WITH SWITCH OPEN ≥ 5000 Ω) |   |  |  |      |      |      |      |
| I <sub>WETT</sub> (CSO)  | Wetting current accuracy for CSO (switch closed)                                | 1 mA setting   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V  | 0.84 | 1    | 1.14 | mA   |
|  |   | 2 mA setting   |  | 1.71 | 2    | 2.32 |      |
|  |   | 5 mA setting   | 4.5 V ≤ V <sub>S</sub> < 5 V   | 2.39 |      | 5.5  |      |
|  |   |  | 5 V ≤ V <sub>S</sub> ≤ 35 V  | 4.3  | 5    | 5.6  |      |
|  |   | 10 mA setting  | 4.5 V ≤ V <sub>S</sub> < 6 V   | 2.4  |      | 11   |      |
|  |   |  | 6 V ≤ V <sub>S</sub> ≤ 35 V  | 8.4  | 10   | 11.4 |      |
|  |   | 15 mA setting  | 4.5 V ≤ V <sub>S</sub> < 6.5 V   | 2.4  |      | 16.5 |      |
|  |   |  | 6.5 V ≤ V <sub>S</sub> ≤ 35 V  | 12.5 | 15   | 17   |      |
| I <sub>WETT</sub> (CSI)  | Wetting current accuracy for CSI (switch closed)                                | 1 mA setting   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V  | 0.75 | 1.1  | 2.05 | mA   |
|  |   | 2 mA setting   |  | 1.6  | 2.2  | 3.3  |      |
|  |   | 5 mA setting   |  | 4.3  | 5.6  | 7.1  |      |
|  |   | 10 mA setting  |  | 9.2  | 11.5 | 13.4 |      |
|  |   | 15 mA setting  | 4.5 V ≤ V <sub>S</sub> < 6 V   | 11   | 16.5 | 19.2 |      |
|  |   |  | 6 V ≤ V <sub>S</sub> ≤ 35 V  | 13.7 | 16.5 | 19.2 |      |
| V <sub>CSI_DROP_OPEN</sub>   | Voltage drop from IN <sub>x</sub> pin to AGND across CSI (switch open)          | 10 mA setting, R <sub>SW</sub> = 5 kΩ  | 4.5 V ≤ V <sub>S</sub> ≤ 35 V  |      |      | 1.7  | V    |
|  |   | 15 mA setting, R <sub>SW</sub> = 5 kΩ  |  |      |      | 1.7  |      |
| V <sub>CSI_DROP_CLOSED</sub>   | Voltage drop from IN <sub>x</sub> pin to ground across CSI (switch closed)      | 2 mA setting, I <sub>IN</sub> = 1 mA (4.5V ≤ VS ≤ 35V)   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V  |      |      | 1.2  | V    |
|  |   | 5 mA setting, I <sub>IN</sub> = 1mA or 2 mA  |  |      |      | 1.3  | V    |
|  |   | 10 mA setting, I <sub>IN</sub> = 1 mA, 2 mA, or 5 mA   |  |      |      | 1.5  | V    |
|  |   | 15 mA setting, I <sub>IN</sub> = 1 mA, 2 mA, 5 mA, or 10 mA  |  |      |      | 2.1  | V    |
| WETTING CURRENT ACCURACY (ANALOG SWITCHES)   |   |  |  |      |      |      |      |
| I <sub>WETT</sub>  | Wetting current accuracy  | 1 mA setting   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, V <sub>S</sub> - V <sub>INX</sub> ≥ 2.5 V | 0.88 | 1    | 1.13 | mA   |
|  |   | 2 mA setting   |  | 1.8  | 2    | 2.25 |      |
|  |   | 5 mA setting   | 5.5 V ≤ V <sub>S</sub> ≤ 35 V, V <sub>S</sub> - V <sub>INX</sub> ≥ 2.5 V | 4.3  | 5    | 5.5  |      |
|  |   |  | 5.5 V ≤ V <sub>S</sub> ≤ 35 V, V <sub>S</sub> - V <sub>INX</sub> ≥ 3 V   | 4.5  | 5    | 5.5  |      |
|  |   | 10 mA setting  | 6 V ≤ V <sub>S</sub> ≤ 35 V, V <sub>S</sub> - V <sub>INX</sub> ≥ 4 V     | 9    | 10   | 11   |      |
|  |   | 15 mA setting  | 6.5 V ≤ V <sub>S</sub> ≤ 35 V, V <sub>S</sub> - V <sub>INX</sub> ≥ 5 V   | 12.5 | 15   | 16.5 |      |
| LEAKAGE CURRENTS   |   |  |  |      |      |      |      |
| I <sub>IN_LEAK_OFF</sub>   | Leakage current at input IN <sub>x</sub> when channel is disabled               | 0 V ≤ V <sub>INx</sub> ≤ V <sub>S</sub> , channel disabled (EN_IN <sub>x</sub> register bit= logic 0)  |  | -4   |      | 5.3  | μA   |
| I <sub>IN_LEAK_OFF_25</sub>  |   | 0 V ≤ V <sub>INx</sub> ≤ V <sub>S</sub> , channel disabled (EN_IN <sub>x</sub> register bit= logic 0), T <sub>A</sub> = 25°C                         |  | -0.5 |      | 0.5  |      |
| I <sub>IN_LEAK_0mA</sub>   | Leakage current at input IN <sub>x</sub> when wetting current setting is 0mA    | 0 V ≤ V <sub>INx</sub> ≤ 6 V, 6 V ≤ V <sub>S</sub> ≤ 35 V , I <sub>WETT</sub> setting = 0 mA   |  | -110 |      | 110  | μA   |
|  |   |  |  |      |      |      | μA   |
| I <sub>IN_LEAK_LOSS_OF_GND</sub>   | Leakage current at input IN <sub>x</sub> under loss of GND condition            | V <sub>S</sub> = 24 V, 0 V ≤ V <sub>INx</sub> ≤ 24 V, all grounds (AGND, DGND, and EP) = 24 V, V <sub>DD</sub> shorted to the grounds <sup>(1)</sup> |  | -5   |      |      | μA   |
| I <sub>IN_LEAK_LOSS_OF_VS</sub>  | Leakage current at input IN <sub>x</sub> under loss of V <sub>S</sub> condition | 0 V ≤ V <sub>INx</sub> ≤ 24 V, V <sub>S</sub> shorted to the grounds = 0 V, V <sub>DD</sub> = 0 V  |  |      |      | 5    | μA   |
| LOGIC LEVELS   |   |  |  |      |      |      |      |



## 6.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_S = 4.5\text{ V}$  to  $35\text{ V}$ , and  $V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted).

| PARAMETER   |   | TEST CONDITIONS  |  | MIN                | TYP                | MAX                | UNIT |
|---|---|--|--|--------------------|--------------------|--------------------|------|
| V <sub>INT_L</sub>  | INT output low voltage  | I <sub>INT</sub> = 2 mA  |  |                    |                    | 0.35               | V    |
|   |   | I <sub>INT</sub> = 4 mA  |  |                    |                    | 0.6                |      |
| V <sub>SO_L</sub>   | SO output low voltage   | I <sub>SO</sub> = 2 mA   |  |                    |                    | 0.2V <sub>DD</sub> | V    |
| V <sub>SO_H</sub>   | SO output high voltage  | I <sub>SO</sub> = -2 mA  |  | 0.8V <sub>DD</sub> |                    |                    | V    |
| V <sub>IN_L</sub>   | SI, SCLK, and $\overline{CS}$ input low voltage                 |  |  |                    | 0.3V <sub>DD</sub> |                    | V    |
| V <sub>IN_H</sub>   | SI, SCLK, and $\overline{CS}$ input high voltage                |  |  | 0.7V <sub>DD</sub> |                    |                    | V    |
| V <sub>RESET_L</sub>  | RESET input low voltage   |  |  |                    |                    | 0.8                | V    |
| V <sub>RESET_H</sub>  | RESET input high voltage  |  |  | 1.6                |                    |                    | V    |
| R <sub>RESET_25</sub>   | RESET pin internal pull-down resistor                           | V <sub>RESET</sub> = 0 to 5.5 V, T <sub>A</sub> =25°C                                |  | 0.85               | 1.25               | 1.7                | MΩ   |
| R <sub>RESET</sub>  |   | V <sub>RESET</sub> = 0 to 5.5 V, T <sub>A</sub> = -40° to 125°C                      |  | 0.2                |                    | 2.1                |      |
| SWITCH INPUT AND V <sub>S</sub> MEASUREMENT CONVERSION PARAMETERS |   |  |  |                    |                    |                    |      |
| RES   | Resolution  |  |  | 10                 |                    |                    | Bits |
| V <sub>OFFSET</sub>   | ADC Offset error  | 0 mA setting   |  | - 1                | 0                  | 1                  | LSB  |
| V <sub>FSE</sub>  | ADC Full-scale error  | 0 mA setting   |  | - 10               | 0                  | 10                 | LSB  |
| OUT <sub>SW</sub>   | Switch input conversion output                                  | 1 mA setting   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 100 Ω resistance to ground at INx | 12                 | 17                 | 26                 | LSB  |
|   |   |  | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 300 Ω resistance to ground at INx | 42                 | 51                 | 64                 |      |
|   |   |  | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 600 Ω resistance to ground at INx | 87                 | 102                | 122                |      |
|   |   | 2 mA setting   | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 100 Ω resistance to ground at INx | 28                 | 34                 | 45                 | LSB  |
|   |   |  | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 300 Ω resistance to ground at INx | 89                 | 102                | 122                |      |
|   |   |  | 4.5 V ≤ V <sub>S</sub> ≤ 35 V, 600 Ω resistance to ground at INx | 181                | 205                | 236                |      |
|   |   | 5 mA setting   | 5 V ≤ V <sub>S</sub> ≤ 35 V, 100 Ω resistance to ground at INx   | 72                 | 85                 | 105                | LSB  |
|   |   |  | 5 V ≤ V <sub>S</sub> ≤ 35 V, 300 Ω resistance to ground at INx   | 223                | 256                | 296                |      |
|   |   |  | 5 V ≤ V <sub>S</sub> ≤ 35 V, 600 Ω resistance to ground at INx   | 393                | 512                | 620                |      |
|   |   | 10 mA setting  | 6 V ≤ V <sub>S</sub> ≤ 35 V, 100 Ω resistance to ground at INx   | 142                | 171                | 202                | LSB  |
|   |   |  | 6 V ≤ V <sub>S</sub> ≤ 35 V, 250 Ω resistance to ground at INx   | 333                | 427                | 486                |      |
|   |   |  | 6 V ≤ V <sub>S</sub> ≤ 35 V, 400 Ω resistance to ground at INx   | 430                | 683                | 823                |      |
|   |   | 15 mA setting  | 6.5 V ≤ V <sub>S</sub> ≤ 35 V, 100 Ω resistance to ground at INx | 166                | 256                | 301                | LSB  |
|   |   |  | 6.5 V ≤ V <sub>S</sub> ≤ 35 V, 200 Ω resistance to ground at INx | 325                | 512                | 582                |      |
|   |   |  | 6.5 V ≤ V <sub>S</sub> ≤ 35 V, 300 Ω resistance to ground at INx | 450                | 768                | 879                |      |
| OUT <sub>VS</sub>   | V <sub>S</sub> measurement output tolerance to full-scale range | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO= 0 in register CONFIG |  |                    |                    | ±2%                |      |
|   |   | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO= 1 in register CONFIG |  |                    |                    | ±2%                |      |
| V <sub>FSR</sub>  | Input full-scale range  | INx measurements   |  |                    | 6                  |                    | V    |
|   |   | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO= 0 in register CONFIG |  |                    | 9                  |                    |      |
|   |   | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO= 1 in register CONFIG |  |                    | 30                 |                    |      |



## 6.5 Electrical Characteristics (continued)

Over operating free-air temperature range,  $V_S = 4.5\text{ V}$  to  $35\text{ V}$ , and  $V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted).

| PARAMETER                 |   | TEST CONDITIONS   | MIN  | TYP | MAX  | UNIT |
|---------------------------|---|---|------|-----|------|------|
| R <sub>IN, SC</sub>       | Input resistance  | INx measurements  |      | 240 |      | kΩ   |
|                           | ADC Equivalent input resistance, V <sub>S</sub> above 7 V | Input switch measurement, I <sub>LOAD</sub> = 30 μA                                   | 135  | 234 | 356  | kΩ   |
| R <sub>IN, COMP</sub>     | ADC Equivalent input resistance, V <sub>S</sub> above 7 V | THRES_COMP Setting = 2 V  | 88   | 130 | 172  | kΩ   |
|                           |   | THRES_COMP Setting = 2.7 V  | 85   | 126 | 170  |      |
|                           |   | THRES_COMP Setting = 3 V  | 73   | 105 | 137  |      |
|                           |   | THRES_COMP Setting = 4 V  | 68   | 95  | 124  |      |
| R <sub>RATIO</sub>        | Input voltage divider factor <sup>(1)</sup>               | INx measurements  |      | 2   |      | -    |
|                           |   | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO = 0 in register CONFIG |      | 3   |      | -    |
|                           |   | V <sub>S</sub> measurements (V <sub>S</sub> ≥ 4.5 V), VS_RATIO = 1 in register CONFIG |      | 10  |      | -    |
| COMPARATOR PARAMETERS     |   |   |      |     |      |      |
| V <sub>TH_COMP_2V</sub>   | Comparator threshold for 2 V                              | THRES_COMP = 2 V  | 1.85 |     | 2.25 | V    |
| V <sub>TH_COMP_2p7V</sub> | Comparator threshold for 2.7 V                            | THRES_COMP = 2.7 V  | 2.4  |     | 2.9  | V    |
| V <sub>TH_COMP_3V</sub>   | Comparator threshold for 3 V                              | THRES_COMP = 3 V  | 2.85 |     | 3.3  | V    |
| V <sub>TH_COMP_4V</sub>   | Comparator threshold for 4 V                              | THRES_COMP = 4 V  | 3.7  |     | 4.35 | V    |
| V <sub>S_COMP</sub>       | Minimum V <sub>S</sub> requirement for proper detection   | THRES_COMP = 2 V  | 4.5  |     |      | V    |
|                           |   | THRES_COMP = 2.7 V  | 5    |     |      |      |
|                           |   | THRES_COMP = 3 V  | 5.5  |     |      |      |
|                           |   | THRES_COMP = 4 V  | 6.5  |     |      |      |
| R <sub>IN, COMP</sub>     | Comparator equivalent input resistance                    | THRES_COMP = 2 V  | 30   | 130 |      | kΩ   |
|                           |   | THRES_COMP = 2.7 V  | 35   | 130 |      |      |
|                           |   | THRES_COMP = 3 V  | 35   | 105 |      |      |
|                           |   | THRES_COMP = 4 V  | 43   | 95  |      |      |

(1) Verified by design.

## 6.6 Timing Requirements

$V_S = 4.5\text{ V}$  to  $35\text{ V}$ ,  $V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$ , and  $10\text{ pF}$  capacitive load on SO unless otherwise noted; verified by design and characterization.

| PARAMETER  |   | TEST CONDITION  | MIN  | NOM | MAX | UNIT          |
|--|---|---|------|-----|-----|---------------|
| <b>SWITCH MONITORING, INTERRUPT, STARTUP AND RESET</b> |   |   |      |     |     |               |
| $t_{\text{POLL\_ACT}}$                                 | Polling active time accuracy  | Polling mode  | -12% |     | 12% |               |
| $t_{\text{POLL\_ACT\_M}}$                              | Polling active time accuracy for matrix inputs  | Polling mode with matrix enabled                      | -12% |     | 12% |               |
| $t_{\text{POLL}}$                                      | Polling time accuracy   | Polling mode  | -12% |     | 12% |               |
| $t_{\text{COMP}}$                                      | Comparator detection time   |   |      | 18  |     | $\mu\text{s}$ |
| $t_{\text{ADC}}$                                       | ADC Conversion time   | Sample and hold time included                         |      | 24  |     | $\mu\text{s}$ |
| $t_{\text{CCP\_TRANS}}$                                | Transition time between last input sampling and start of clean current  |   |      | 20  |     | $\mu\text{s}$ |
| $t_{\text{CCP\_ACT}}$                                  | Clean current active time   |   | -12% |     | 12% |               |
| $t_{\text{STARTUP}}$                                   | Polling startup time  |   | 200  | 300 | 400 | $\mu\text{s}$ |
| $t_{\text{INT\_ACTIVE}}$                               | Active INT assertion duration   |   | 1.5  | 2   | 2.5 | ms            |
| $t_{\text{INT\_INACTIVE}}$                             | INT de-assertion duration during a pending interrupt  |   | 3    | 4   | 5   | ms            |
| $t_{\text{INT\_IDLE}}$                                 | Interrupt idle time   |   | 80   | 100 | 120 | $\mu\text{s}$ |
| $t_{\text{RESET}}$                                     | Time required to keep the RESET pin high to successfully reset the device (no pending interrupt) <sup>(1)</sup> |   | 2    |     |     | $\mu\text{s}$ |
| $t_{\text{REACT}}$                                     | Delay between a fault event (OV, UV, TW, or TSD) to a high to low transition on the INT pin                     | See Figure 7-2 for OV example.                        |      |     | 20  | $\mu\text{s}$ |
| <b>SPI INTERFACE</b>                                   |   |   |      |     |     |               |
| $t_{\text{LEAD}}$                                      | Falling edge of $\overline{\text{CS}}$ to rising edge of SCLK setup time  |   | 100  |     |     | ns            |
| $t_{\text{LAG}}$                                       | Falling edge of SCLK to rising edge of $\overline{\text{CS}}$ setup time  |   | 100  |     |     | ns            |
| $t_{\text{SU}}$  | SI to SCLK falling edge setup time  |   | 30   |     |     | ns            |
| $t_{\text{HOLD}}$                                      | SI hold time after falling edge of SCLK   |   | 20   |     |     | ns            |
| $t_{\text{VALID}}$                                     | Time from rising edge of SCLK to valid SO data  |   |      |     | 70  | ns            |
| $t_{\text{SO(EN)}}$                                    | Time from falling edge of $\overline{\text{CS}}$ to SO low-impedance  |   |      |     | 60  | ns            |
| $t_{\text{SO(DIS)}}$                                   | Time from rising edge of $\overline{\text{CS}}$ to SO high-impedance  | Loading of $1\text{ k}\Omega$ to GND. See Figure 7-3. |      |     | 60  | ns            |
| $t_{\text{R}}$   | SI, $\overline{\text{CS}}$ , and SCLK signals rise time   |   |      | 5   | 30  | ns            |
| $t_{\text{F}}$   | SI, $\overline{\text{CS}}$ , and SCLK signals fall time   |   |      | 5   | 30  | ns            |
| $t_{\text{INTER\_FRAME}}$                              | Delay between two SPI communication ( $\overline{\text{CS}}$ low) sequences                                     |   | 1.5  |     |     | $\mu\text{s}$ |
| $t_{\text{CKH}}$                                       | SCLK High time  |   | 120  |     |     | ns            |
| $t_{\text{CKL}}$                                       | SCLK Low time   |   | 120  |     |     | ns            |
| $t_{\text{INITIATION}}$                                | Delay between valid $V_{DD}$ voltage and initial SPI communication  |   | 45   |     |     | $\mu\text{s}$ |

(1) If there is a pending interrupt (/INT pin asserted low), it can take up to 1ms for the device to complete the reset.

## 6.7 Typical Characteristics

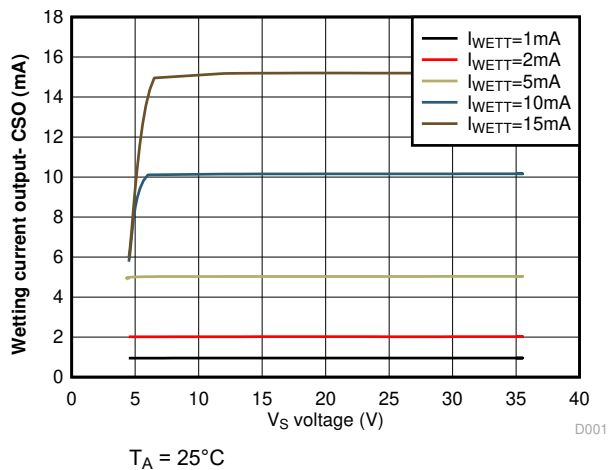


图 6-1. Wetting Current Output - CSO vs.  $V_S$  Voltage

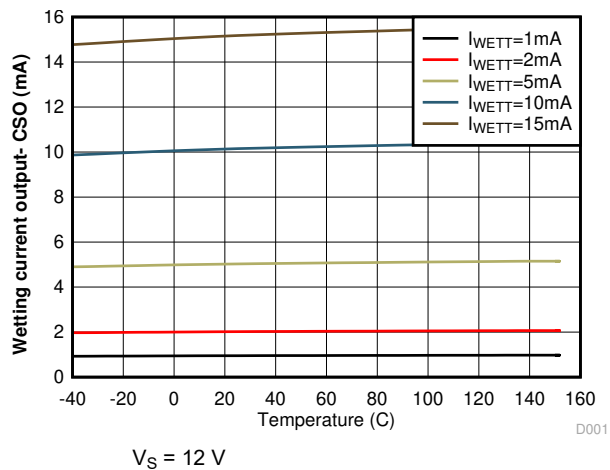


图 6-2. Wetting Current Output - CSO vs. Temperature

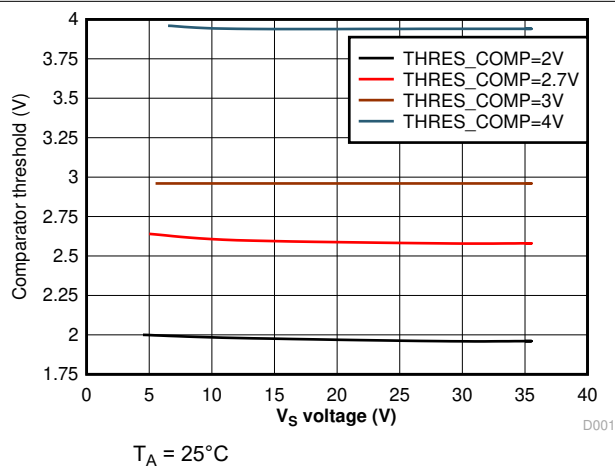


图 6-3. Comparator Threshold vs.  $V_S$  Voltage

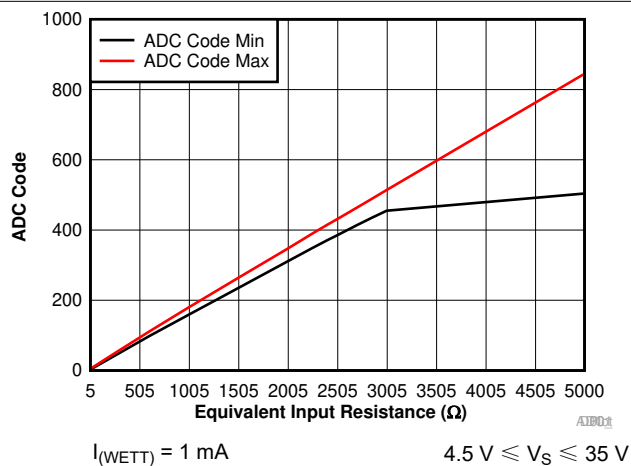


图 6-4. ADC Code vs. Equivalent Input Resistance

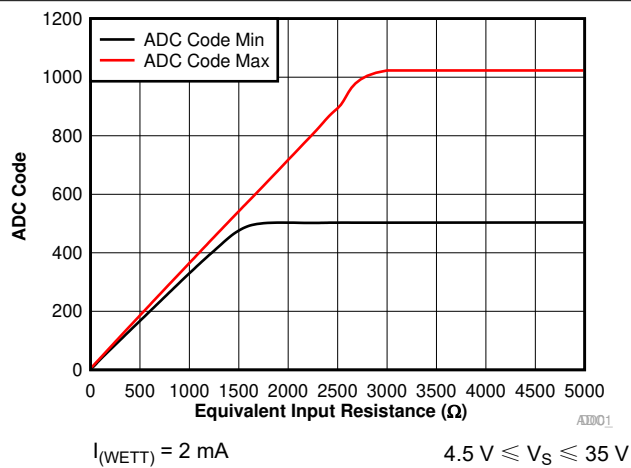


图 6-5. ADC Code vs. Equivalent Input Resistance

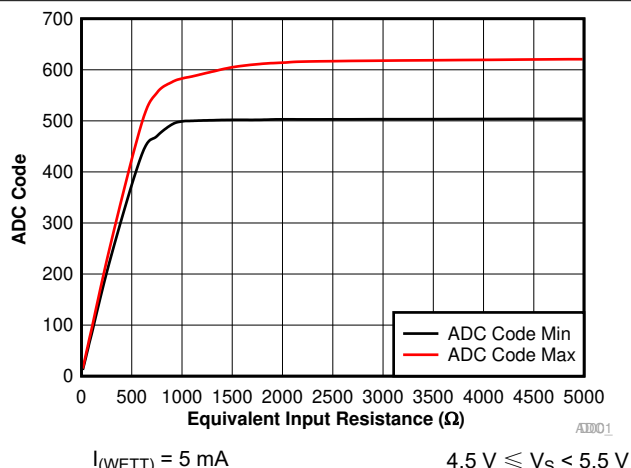


图 6-6. ADC Code vs. Equivalent Input Resistance

## 6.7 Typical Characteristics (continued)

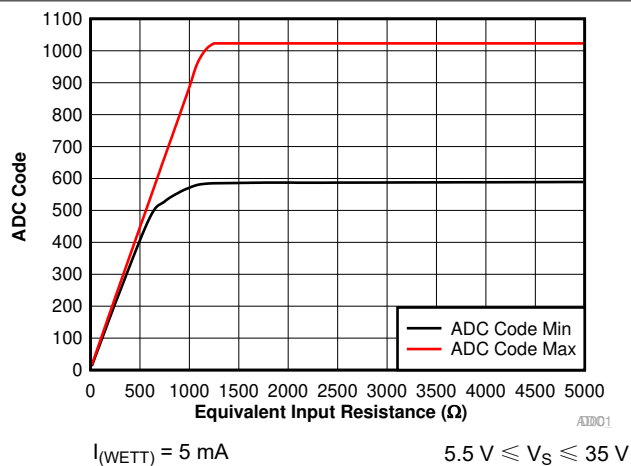


图 6-7. ADC Code vs. Equivalent Input Resistance

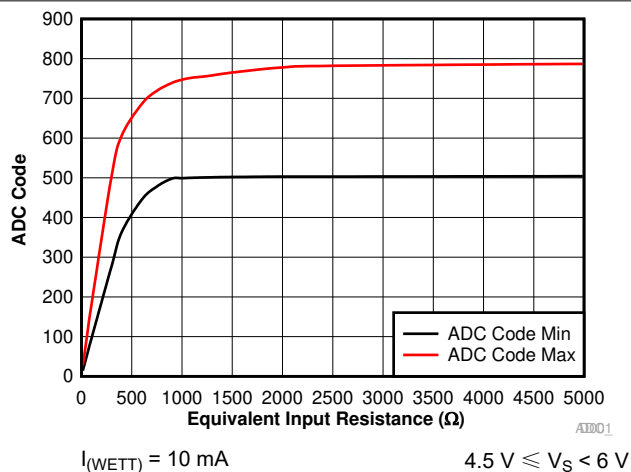


图 6-8. ADC Code vs. Equivalent Input Resistance

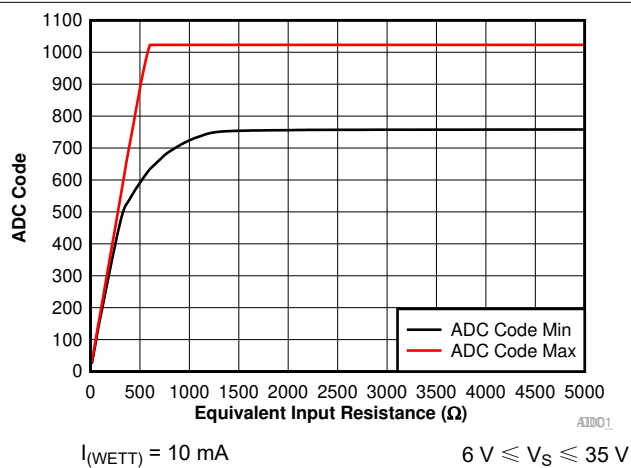


图 6-9. ADC Code vs. Equivalent Input Resistance

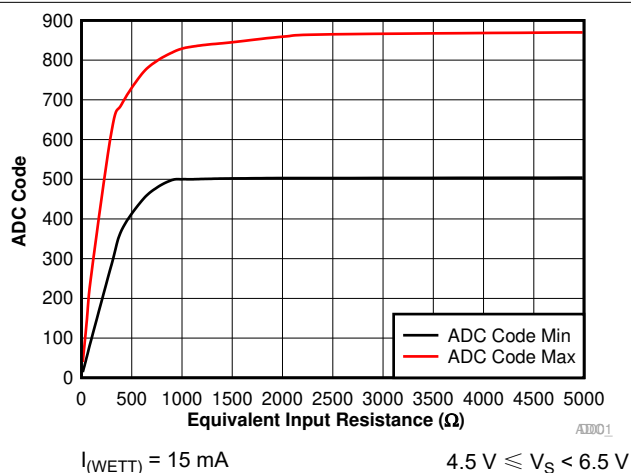


图 6-10. ADC Code vs. Equivalent Input Resistance

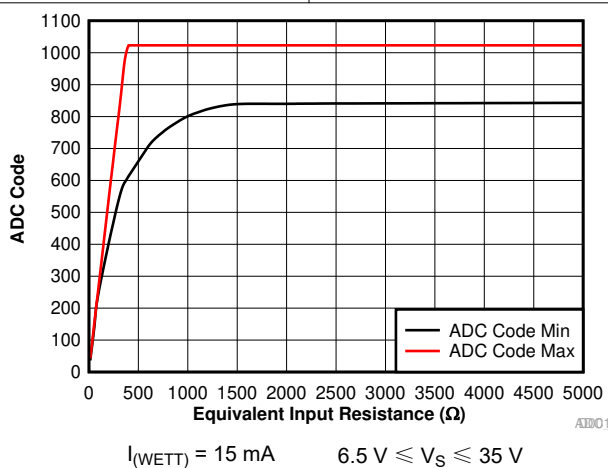


图 6-11. ADC Code vs. Equivalent Input Resistance

## 7 Parameter Measurement Information

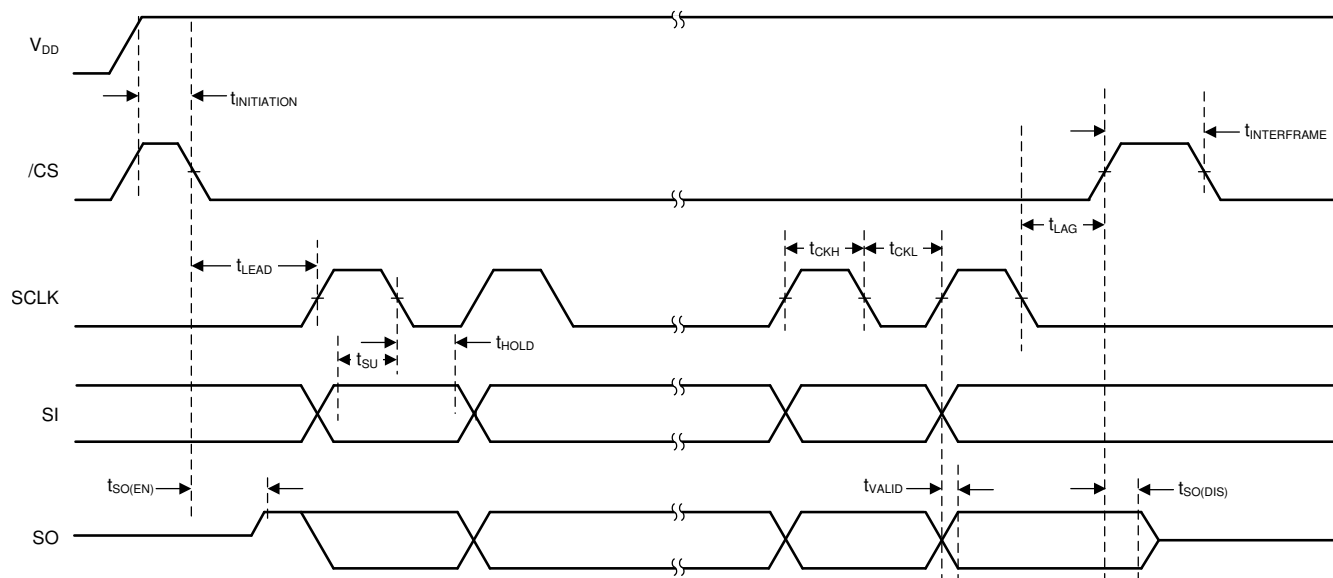


图 7-1. SPI Timing Parameters

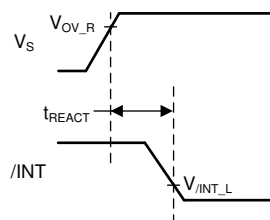


图 7-2.  $t_{REACT}$  Timing Parameters

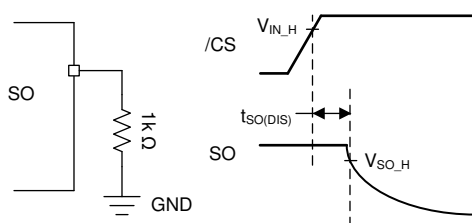


图 7-3.  $t_{SO(DIS)}$  Timing Parameters

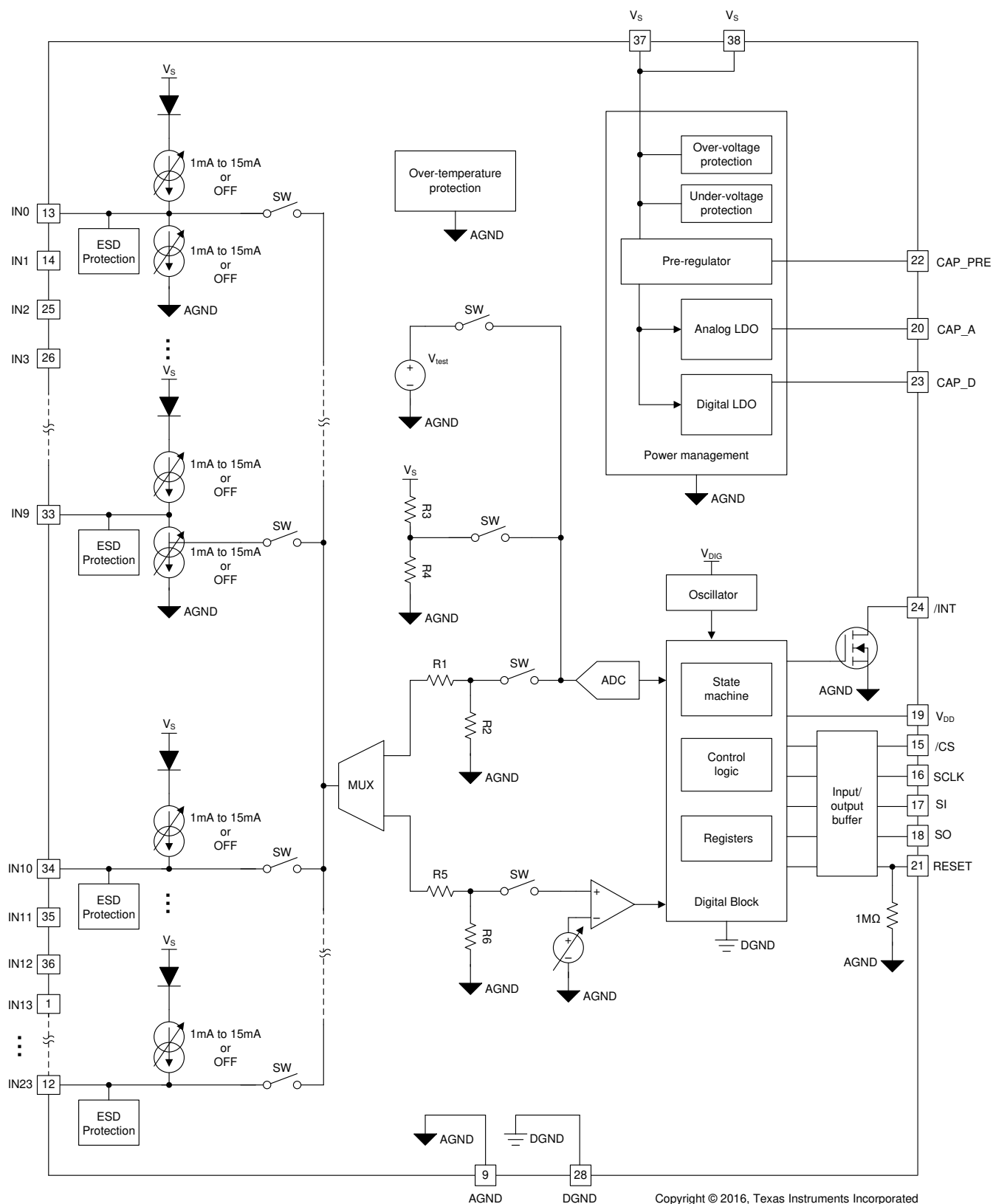
## 8 Detailed Description

### 8.1 Overview

The TIC12400-Q1 is an advanced 24-input Multiple Switch Detection Interface (MSDI) device designed to detect external mechanical switch status in a 12 V automotive system by acting as an interface between the switches and the low-voltage microcontroller. The TIC12400-Q1 is an integrated solution that replaces many discrete components and provides integrated protection, input serialization, and system wake-up capability.

The device monitors 14 switches to GND and 10 additional switches that can be programmed to be connected to either GND or  $V_{BAT}$ . It features SPI interface to report individual switch status and provides programmability to control the device operation. The TIC12400-Q1 features a 10-bit ADC which is useful to monitor analog inputs such as resistor coded switches that have multiple switching positions. To monitor only digital switches, an integrated comparator can be used instead to monitor the input status. The device has 2 modes of operation: continuous mode and polling mode. The polling mode is a low-power mode that can be activated to reduce current drawn in the system by only turning on the wetting current for a small duty cycle to detect switch status changes. An interrupt is generated upon detection of switch status change and it can be used to wake up the microcontroller to bring the entire system back to operation.

## 8.2 Functional Block Diagram





## 8.3 Feature Description

### 8.3.1 $V_S$ Pin

The  $V_S$  supply provides power to the entire chip and it is designed to be connected directly to a 12 V automotive battery via a reverse-polarity blocking diode.

### 8.3.2 $V_{DD}$ Pin

The  $V_{DD}$  supply is used to determine the logic level on the SPI communication interface, source the current for the SO driver, and sets the pull-up voltage for the  $\overline{CS}$  pin. It can also be used as a possible external pull-up supply for the  $\overline{INT}$  pin in addition to the  $V_S$  and it shall be connected to a 3 V to 5.5 V logic supply. Removing  $V_{DD}$  from the device disables SPI communications but does not reset the register configurations.

### 8.3.3 Device Initialization

When the device is powered up for the first time, the condition is called Power-On Reset (POR), which sets the registers to their default values and initializes the device state machine. The internal POR controller holds the device in a reset condition until  $V_S$  has reached  $V_{POR\_R}$ , at which the reset condition is released with the device registers and state machine initialized to their default values. After the initialization process is completed, the  $\overline{INT}$  pin is asserted low to notify the microcontroller, and the register bit POR in the INT\_STAT register is asserted to logic 1. The SPI flag bit POR is also asserted at the SPI output (SO).

During device initialization, factory settings are programmed into the device to allow accurate device operation. The device performs a self-check after the device is programmed to ensure correct settings are loaded. If the self-check returns an error, the CHK\_FAIL bit in the INT\_STAT register will be flagged to logic 1 along with the POR bit. If this event occurs the microcontroller is recommended to initiate software reset (see section [Software Reset](#)) to re-initialize the device to allow the correct settings to be re-programmed.

### 8.3.4 Device Trigger

After device initialization, the TIC12400-Q1 is ready to be configured. The microcontroller can use SPI commands to program desired settings to the configuration registers. Once the device configuration is completed, the microcontroller is required to set the bit TRIGGER in the CONFIG register to logic 1 in order to activate wetting current and start external switch monitoring.

After switch monitoring initiates, the configuration registers turn into read-only registers (with the exception of the TRIGGER, CRC\_T, and RESET bits in the CONFIG register and all bits in the CCP\_CFG1 register). If at any time the device setting needs to be re-configured, the microcontroller is required to first set the bit TRIGGER in the CONFIG register to logic 0 to stop wetting current and switch monitoring. The microcontroller can then program configuration registers to the desired settings. Once the re-configuration is completed the microcontroller can set the TRIGGER bit back to logic 1 to re-start switch monitoring.

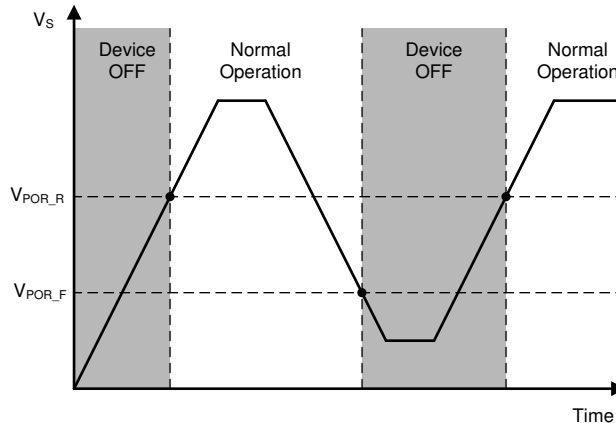
Note the cyclic redundancy check (CRC) feature stays accessible when TRIGGER bit is in logic 1, allowing the microcontroller to verify device settings at all time. Refer to section [Cyclic Redundancy Check \(CRC\)](#) for more details of the CRC feature.

### 8.3.5 Device Reset

There are 3 ways to reset the TIC12400-Q1 and re-initialize all registers to their default values:

#### 8.3.5.1 $V_S$ Supply POR

The device is turned off and all register contents are lost if the  $V_S$  voltage drops below  $V_{POR\_F}$ . To turn the device back on, the  $V_S$  voltage must be raised back above  $V_{POR\_R}$ , as illustrated in [Figure 8-1](#). The device then starts the initialization process as described in section [Device Initialization](#).



**图 8-1.  $V_S$  is Lowered Below the POR Threshold, Then Ramped Back Up to Complete a POR Cycle**

### 8.3.5.2 Hardware Reset

Microcontroller can toggle the RESET pin to perform a hardware reset to the device. The RESET pin is internally pulled-down via a resistor (1.25 M $\Omega$  typical) and must be kept low for normal operation. When the RESET pin is toggled high, the device enters the reset state with most of the internal blocks turned off and consumes very little current of  $I_{S\_RESET}$ . Switch monitoring and SPI communications are stopped in the reset state, and all register contents are cleared. When RESET pin is toggled back low, all the registers are set to their default values and the device state machine is re-initialized, similar to a POR event. When the re-initialization process is completed the  $\overline{INT}$  pin is asserted low, and the interrupt register bit POR and the SPI status flag POR are both asserted to notify the microcontroller that the device has completed the reset process.

Note in order to successfully reset the device, the RESET pin needs to be kept high for a minimum duration of  $t_{RESET}$ . The pin is required to be driven with a stable input (below  $V_{RESET\_L}$  for logic low or above  $V_{RESET\_H}$  for logic H) to prevent the device from accidental reset.

### 8.3.5.3 Software Reset

In addition to hardware reset the microcontroller can also issue a SPI command to initiate software reset. Software reset is triggered by setting the RESET bit in the register CONFIG to logic 1, which re-initializes the device with all registers set to their default values. Once the re-initialization process is completed, the  $\overline{INT}$  pin is asserted low, and the interrupt register bit POR and the SPI status flag POR are both asserted to notify the microcontroller that the device has completed the reset process.

### 8.3.6 $V_S$ Under-Voltage (UV) Condition

During normal operation of a typical 12 V automotive system, the  $V_S$  voltage is usually quite stable and stays well above 11 V. However, the  $V_S$  voltage may drop temporarily during certain vehicle operations, such as cold cranking. If the  $V_S$  voltage drops below  $V_{UV\_F}$ , the TIC12400-Q1 enters the under-voltage (UV) condition since there is not enough voltage headroom for the device to accurately generate wetting currents. The following describes the behavior of the TIC12400-Q1 under UV condition:

1. All current sources and sinks de-activate and switch monitoring stops.
2. Interrupt is generated by asserting the  $\overline{INT}$  pin low and the bit UV in the interrupt register (INT\_STAT) is flagged to logic 1. The bit UV\_STAT is asserted to logic 1 in the register IN\_STAT\_MISC. The OI SPI flag is asserted during any SPI transactions. The  $\overline{INT}$  pin is released and the interrupt register (INT\_STAT) is cleared on the rising edge of CS provided that the interrupt register has been read during the SPI transaction.
3. SPI communication stays active, and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without interruption.
4. The device continues to monitor the  $V_S$  voltage, and the UV condition sustains if the  $V_S$  voltage continues to stay below  $V_{UV\_R}$ . No further interrupt is generated once cleared.

Note: the device resets as described in section [VS Supply POR](#) if the  $V_S$  voltage drops below  $V_{POR\_F}$ .

When the  $V_S$  voltage rises above  $V_{UV\_R}$ , the  $\overline{INT}$  pin is asserted low to notify the microcontroller that the UV condition no longer exists. The UV bit in the register INT\_STAT is flagged to logic 1 and the bit UV\_STAT bit is de-asserted to logic 0 in the register IN\_STAT\_MISC to reflect the clearance of the UV condition. The device resumes operation using current register settings (regardless of the  $\overline{INT}$  pin and SPI communication status) with polling restarted from the first enabled channel. The Switch State Change (SSC) interrupt is generated at the end of the first polling cycle and the detected switch status becomes the baseline switch status for subsequent polling cycles. The content of the INT\_STAT register, once read by the microcontroller, is cleared, and the  $\overline{INT}$  pin is released afterwards.

The following diagram describes the TIC12400-Q1 operation at various different  $V_S$  voltages. If the  $V_S$  voltage stays above  $V_{UV\_F}$  (Case 1), the device stays in normal operation. If the  $V_S$  voltage drops below  $V_{UV\_F}$  but stays above  $V_{POR\_F}$  (Case 2), the device enters the UV condition. If  $V_S$  voltage drops below  $V_{POR\_F}$  (Case 3), the device resets and all register settings are cleared. The microcontroller is then required to re-program all the configuration registers in order to resume normal operation after the  $V_S$  voltage recovers.

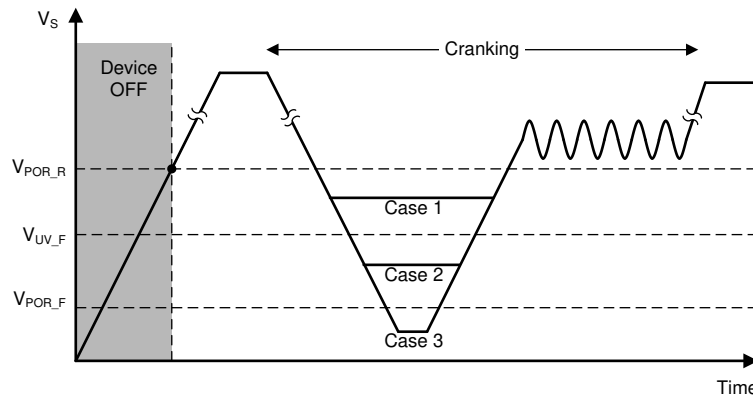


图 8-2. TIC12400-Q1 Operation at Various  $V_S$  Voltage Levels

### 8.3.7 $V_S$ Over-Voltage (OV) Condition

If  $V_S$  voltage rises above  $V_{OV\_R}$ , the TIC12400-Q1 enters the over-voltage (OV) condition to prevent damage to internal structures of the device on the  $V_S$  and INx (for battery-connected switches) pins. The following describes the behavior of the TIC12400-Q1 under OV condition:

1. All current sources and sinks de-activate and switch monitoring stops.
2. Interrupt is generated by asserting the  $\overline{INT}$  pin low and the bit OV in the interrupt register (INT\_STAT) is flagged to logic 1. The bit OV\_STAT is asserted to logic 1 in the register IN\_STAT\_MISC. The OI SPI flag is asserted during any SPI transactions. The  $\overline{INT}$  pin is released and the interrupt register (INT\_STAT) is cleared on the rising edge of CS provided that the interrupt register has been read during the SPI transaction.
3. SPI communication stays active, and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without any interruption.
4. The device continues to monitor the  $V_S$  voltage, and the OV condition sustains if the  $V_S$  voltage continues to stay above  $V_{OV\_R} - V_{OV\_HYST}$ . No further interrupt is generated once cleared.

When the  $V_S$  voltage drops below  $V_{OV\_R} - V_{OV\_HYST}$ , the  $\overline{INT}$  pin is asserted low to notify the microcontroller that the over-voltage condition no longer exists. The OV bit in the register INT\_STAT is flagged to logic 1 and the bit OV\_STAT bit is de-asserted to logic 0 in the register IN\_STAT\_MISC to reflect the clearance of the OV condition. The device resumes operation using current register settings (regardless of the  $\overline{INT}$  pin and SPI communication status) with polling restarted from the first enabled channel. The Switch State Change (SSC) interrupt is generated at the end of the first polling cycle and the detected switch status becomes the baseline status for subsequent polling cycles. The content of the INT\_STAT register, once read by the microcontroller, is cleared and the  $\overline{INT}$  pin is released afterwards.

### 8.3.8 Switch Inputs Settings

IN0 to IN23 are inputs connected to external mechanical switches. The switch status of each input, whether open or closed, is indicated by the status registers. 表 8-1 below describes various settings that can be configured for each input. Note: some settings are shared between multiple inputs. It is required to first stop device operation by setting the TRIGGER bit low in the register CONFIG before making any configuration changes, as described in [Device Trigger](#).

表 8-1. TIC12400-Q1 Wetting Current and Threshold Setting Details

| Input | Threshold                |                               | Wetting Current | Current Source (CSO) /<br>Current Sink (CSI) | Supported Switch<br>Type        |
|-------|--------------------------|-------------------------------|-----------------|--|---------------------------------|
|       | Comparator Input<br>Mode | ADC Input Mode                |                 |  |                                 |
| IN0   | THRES_COMP_IN<br>0_IN3   | THRES0 to<br>THRES7           | WC_IN0_IN1      | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN1   |                          | THRES0 to<br>THRES7           |                 | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN2   |                          | THRES0 to<br>THRES7           | WC_IN2_IN3      | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN3   |                          | THRES0 to<br>THRES7           |                 | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN4   | THRES_COMP_IN<br>4_IN7   | THRES0 to<br>THRES7           | WC_IN4          | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN5   |                          | THRES0 to<br>THRES7           | WC_IN5          | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN6   |                          | THRES0 to<br>THRES7           | WC_IN6_IN7      | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN7   |                          | THRES0 to<br>THRES7           |                 | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN8   | THRES_COMP_IN<br>8_IN11  | THRES0 to<br>THRES7           | WC_IN8_IN9      | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN9   |                          | THRES0 to<br>THRES7           |                 | CSO<br>CSI                                   | Switch to GND<br>Switch to VBAT |
| IN10  |                          | THRES0 to<br>THRES7           | WC_IN10         | CSO  | Switch to GND                   |
| IN11  |                          | THRES0 to<br>THRES7           | WC_IN11         | CSO  | Switch to GND                   |
| IN12  | THRES_COMP_IN<br>12_IN15 | THRES2A<br>THRES2B            | WC_IN12_13      | CSO  | Switch to GND                   |
| IN13  |                          | THRES2A<br>THRES2B            |                 | CSO  | Switch to GND                   |
| IN14  |                          | THRES2A<br>THRES2B            | WC_IN14_15      | CSO  | Switch to GND                   |
| IN15  |                          | THRES2A<br>THRES2B            |                 | CSO  | Switch to GND                   |
| IN16  | THRES_COMP_IN<br>16_IN19 | THRES2A<br>THRES2B            | WC_IN16_17      | CSO  | Switch to GND                   |
| IN17  |                          | THRES2A<br>THRES2B            |                 | CSO  | Switch to GND                   |
| IN18  |                          | THRES3A<br>THRES3B<br>THRES3C | WC_IN18_19      | CSO  | Switch to GND                   |
| IN19  |                          | THRES3A<br>THRES3B<br>THRES3C |                 | CSO  | Switch to GND                   |

表 8-1. TIC12400-Q1 Wetting Current and Threshold Setting Details (continued)

| Input | Threshold                |   | Wetting Current | Current Source (CSO) /<br>Current Sink (CSI) | Supported Switch<br>Type |
|-------|--------------------------|---|-----------------|--|--------------------------|
|       | Comparator Input<br>Mode | ADC Input Mode                                    |                 |  |                          |
| IN20  | THRES_COMP_IN<br>20_IN23 | THRES3A<br>THRES3B<br>THRES3C                     | WC_IN20_21      | CSO  | Switch to GND            |
| IN21  |                          | THRES3A<br>THRES3B<br>THRES3C                     |                 | CSO  | Switch to GND            |
| IN22  |                          | THRES3A<br>THRES3B<br>THRES3C                     | WC_IN22         | CSO  | Switch to GND            |
| IN23  |                          | THRES3A<br>THRES3B<br>THRES3C<br>THRES8<br>THRES9 | WC_IN23         | CSO  | Switch to GND            |

### 8.3.8.1 Input Current Source and Sink Selection

Among the 24 inputs, IN10 to IN23 are intended for monitoring only ground-connected switches and are connected to current sources. IN0 to IN9 can be programmed to monitor either ground-connected switches or battery-connected switches by configuring the [CS\\_SELECT](#) register. The default configuration of the IN0-IN9 inputs after POR is to monitor ground-connected switches (current sources are selected). To set an input to monitor battery-connected switches, set the corresponding bit to logic 1.

### 8.3.8.2 Input Mode Selection

The TIC12400-Q1 has a built-in ADC and a comparator that can be used to monitor resistor coded switches or digital switches. Digital switch inputs have only two states, either open or closed, and can be adequately detected by a comparator. Resistor coded switches may have multiple positions that need to be detected and an ADC is appropriate to monitor the different states. Each input of the TIC12400-Q1 can be individually programmed to use either a comparator or an ADC by configuring the appropriate bits in the [MODE](#) register depending on the knowledge of the external switch connections. The benefit of using a comparator instead of an ADC to monitor digital switches is its reduced polling time which translates to overall power saving when the device operates in the low-power polling mode.

Comparator input mode is selected by default for all enabled inputs upon device reset.

### 8.3.8.3 Input Enable Selection

The TIC12400-Q1 provides switch status monitoring for up to 24 inputs, but there might be circumstances in which not all inputs need to be constantly monitored. The microcontroller may choose to enable or disable monitoring of certain inputs by configuring the [IN\\_EN](#) register. Setting the corresponding bit to logic 0 deactivates the wetting current source and sink, and stops switch status monitoring for the input. Disabling monitoring of unused inputs reduces overall power consumption of the device.

All inputs are disabled by default upon device reset.

### 8.3.8.4 Thresholds Adjustment

When an input is configured as comparator input mode, the threshold level for interrupt generation can be programmed by setting the [THRES\\_COMP](#) register. The threshold level settings can be set for each individual input groups and each group consists of 4 inputs. Four threshold levels are available: 2 V, 2.7 V, 3 V, and 4 V.

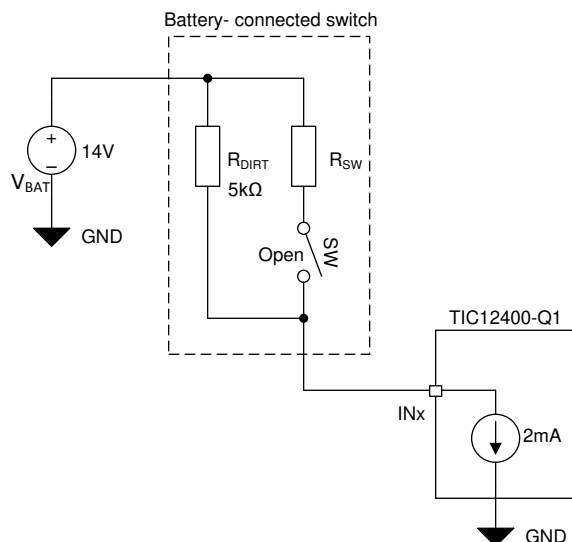
When an input is configured as ADC input mode the threshold level for interrupt generation can be configured from 0 to 1023 different levels by setting the [THRES\\_CFG1](#) to [THRES\\_CFG2](#) registers. One threshold level can be programmed individually for each of the inputs from IN0 to IN11. Additionally, one common threshold, shared between inputs IN0 to IN11, can be programmed by configuring the THRES\_COM bits in register [MATRIX](#). The common threshold acts independently from the threshold THRES0 to THRES7. Inputs IN12 to IN17 use 2 preset threshold levels (THRES2A and THRES2B). Inputs 18 to 22 use 3 preset threshold levels (THRES3A, THRES3B, and THRES3C). Input 23 uses 5 preset threshold levels (THRES3A, THRES3B, THRES3C, THRES8, and THRES9).

When multiple threshold settings are used for ADC inputs, the thresholds levels need to be configured properly. Use the rules below (see [表 8-2](#)) when setting up the threshold levels:

**表 8-2. Proper Threshold Configuration for ADC Inputs**

| INPUT        | PROPER THRESHOLD CONFIGURATION                                    |
|--------------|---|
| IN12 to IN17 | THRES2B $\geq$ THRES2A  |
| IN18 to IN22 | THRES3C $\geq$ THRES3B $\geq$ THRES3A                             |
| IN23         | THRES9 $\geq$ THRES8 $\geq$ THRES3C $\geq$ THRES3B $\geq$ THRES3A |

Remember to use caution when setting up the threshold for switches that are connected externally to the battery as there is a finite voltage drop (as high as  $V_{CSI\_DROP\_OPEN}$  for 10 mA and 15 mA settings) across the current sinks. Therefore, even for an open switch, the voltage on the INx pin can be as high as  $V_{CSI\_DROP\_OPEN}$  and the detection threshold shall be configured above it. It shall also be noted that a lower wetting current sink setting may not be strong enough to pull the INx pin close to ground in the presence of a leaky open external switch, as illustrated in the diagram below (see [图 8-3](#)). In this example, the external switch, although in the open state, has large leakage current and can be modelled as an equivalent resistor ( $R_{DIRT}$ ) of 5 k $\Omega$ . The 2 mA current sink is only able to pull the INx pin voltage down to 4 V, even if the switch is in the open state.



**图 8-3. Example Showing the Calculation of the INx Pin Voltage for A Leaky Battery-Connected Switch**

It is possible to configure an input to ADC input mode, instead of comparator input mode, to monitor single-threshold digital switches. The following programming procedure is recommended under such configuration:

**表 8-3. Recommended Threshold Configuration When Using an ADC Input to Monitor Digital Switches**

| INPUT        | RECOMMENDED THRESHOLD CONFIGURATION   |
|--------------|---|
| IN0 to IN11  | Configure the desired threshold to one of the settings from THRES0 to THRES7 and map it accordingly   |
| IN12 to IN17 | <ul style="list-style-type: none"> <li>Configure the desired threshold to THRES2B</li> <li>Set THRES2A to the same code as THRES2B</li> <li>Disable interrupt generation for THRES2A by configuring the INT_EN_CFG1 or INT_EN_CFG2 register.</li> </ul>   |
| IN18 to IN22 | <ul style="list-style-type: none"> <li>Configure the desired threshold to THRES3C</li> <li>Set THRES3A and THRES3B to the same code as THRES3C.</li> <li>Disable interrupt generation for THRES3A and THRES3B by configuring the INT_EN_CFG3 or INT_EN_CFG4 register.</li> </ul>                    |
| IN23         | <ul style="list-style-type: none"> <li>Configure the desired threshold to THRES9</li> <li>Set THRES3A, THRES3B, THRES3C, and THRES8 to the same code as THRES9.</li> <li>Disable interrupt generation for THRES3A, THRES3B, THRES3C, and THRES8 by configuring the INT_EN_CFG4 register.</li> </ul> |

**8.3.8.5 Wetting Current Configuration**

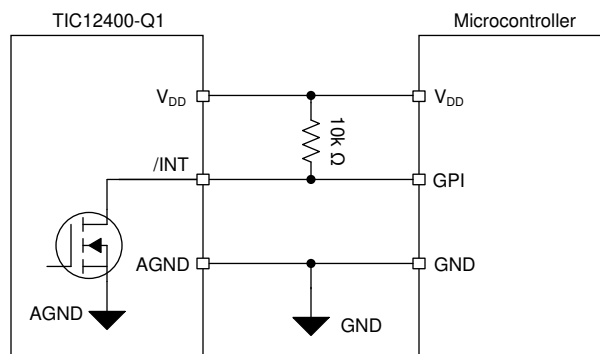
There are 6 different wetting current settings (0 mA, 1 mA, 2 mA, 5 mA, 10 mA, and 15 mA) that can be programmed by configuring the [WC\\_CFG0](#) and [WC\\_CFG1](#) registers. 0 mA is selected by default upon device reset.

To monitor resistor coded switches, a lower wetting current setting (1 mA, 2 mA, or 5 mA) is generally desirable to get the resolution needed to resolve different input voltages while keeping them within the ADC full-scale range (0 V to 6 V). Higher wetting current settings (10 mA and 15 mA) are useful to clean switch contact oxidation that may form on the surface of an open switch contact. If switch contact cleaning is required for resistor coded switches, the clean current polling (CCP) feature (Refer to [§ 8.4.3.1](#)) can be activated to generate short cleaning pulses periodically using higher wetting current settings at the end of every polling cycle.

The accuracy of the wetting current has stronger dependency on the  $V_S$  voltage when  $V_S$  voltage is low. The lower the  $V_S$  voltage falls, the more deviation on the wetting currents from their nominal values. Refer to  $I_{WETT}(CSO)$  and  $I_{WETT}(CSI)$  specifications for more details.

**8.3.9 Interrupt Generation and  $\overline{INT}$  Assertion**

The  $\overline{INT}$  pin is an active-low, open-drain output that asserts low when an event such as switch input state change, temperature warning, over-voltage shutdown, and so fourth, is detected by the TIC12400-Q1. An external pull-up resistor to  $V_{DD}$  is needed on the  $\overline{INT}$  pin (see [图 8-4](#)). The  $\overline{INT}$  pin can also be connected directly to a 12 V automotive battery to support the microcontroller wake-up feature, as describe in [§ 8.3.9.3](#).

**图 8-4.  $\overline{INT}$  Connection Example #1**



### 8.3.9.1 $\overline{\text{INT}}$ Pin Assertion Scheme

TIC12400-Q1 supports two configurable schemes for  $\overline{\text{INT}}$  assertion: static and dynamic. The scheme can be adjusted by configuring the INT\_CONFIG bit in the CONFIG register.

If the static  $\overline{\text{INT}}$  assertion scheme is used (INT\_CONFIG = 0 in the CONFIG register), the  $\overline{\text{INT}}$  pin is asserted low upon occurrence of an event. The  $\overline{\text{INT}}$  pin is released on the rising edge of  $\overline{\text{CS}}$  only if a READ command has been issued to read the INT\_STAT register while  $\overline{\text{CS}}$  is low, otherwise the  $\overline{\text{INT}}$  will be kept low indefinitely. The content of the INT\_STAT interrupt register is latched on the first rising edge of SCLK after  $\overline{\text{CS}}$  goes low for every SPI transaction, and the content is cleared upon a READ command issued to the INT\_STAT register, as illustrated in 图 8-5.

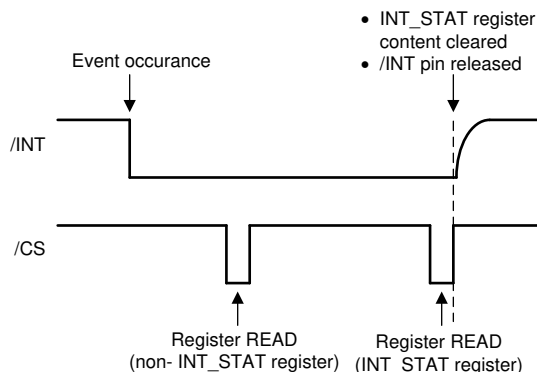


图 8-5. Static  $\overline{\text{INT}}$  Assertion Scheme

In some system implementations an edge-triggered based microcontroller might potentially miss the  $\overline{\text{INT}}$  assertion if it is configured to the static scheme, especially when the microcontroller is in the process of waking up. To prevent missed  $\overline{\text{INT}}$  assertion and improve robustness of the interrupt behavior, the TIC12400-Q1 provides the option to use the dynamic assertion scheme for the  $\overline{\text{INT}}$  pin. When the dynamic scheme is used (INT\_CONFIG= 1 in the CONFIG register), the  $\overline{\text{INT}}$  pin is asserted low for a duration of  $t_{\text{INT\_ACTIVE}}$  and is de-asserted back to high if the INT\_STAT register has not been read after  $t_{\text{INT\_ACTIVE}}$  has elapsed. The  $\overline{\text{INT}}$  is kept high for a duration of  $t_{\text{INT\_INACTIVE}}$ , and is re-asserted low after  $t_{\text{INT\_INACTIVE}}$  has elapsed. The  $\overline{\text{INT}}$  pin continues to toggle until the INT\_STAT register is read.

If the INT\_STAT register is read when  $\overline{\text{INT}}$  pin is asserted low, the  $\overline{\text{INT}}$  pin is released on the READ command's  $\overline{\text{CS}}$  rising edge and the content of the INT\_STAT register is also cleared, as shown in 图 8-6. If the INT\_STAT register is read when  $\overline{\text{INT}}$  pin is de-asserted, the content of the INT\_STAT register is cleared on the READ command's  $\overline{\text{CS}}$  rising edge, and the  $\overline{\text{INT}}$  pin is not re-asserted back low, as shown in 图 8-7.

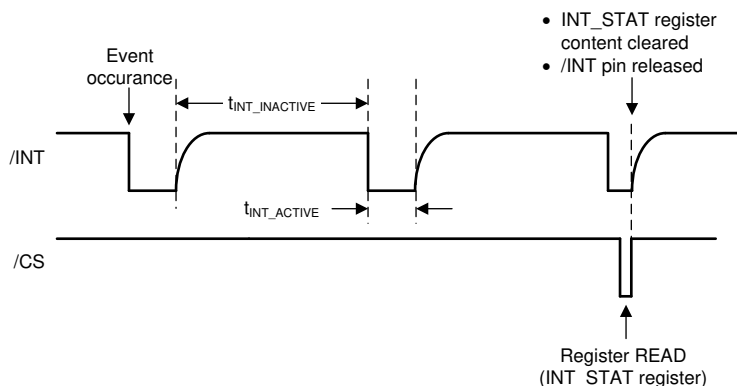


图 8-6. Dynamic  $\overline{\text{INT}}$  Assertion Scheme With INT\_STAT Register Read During  $t_{\text{INT\_ACTIVE}}$

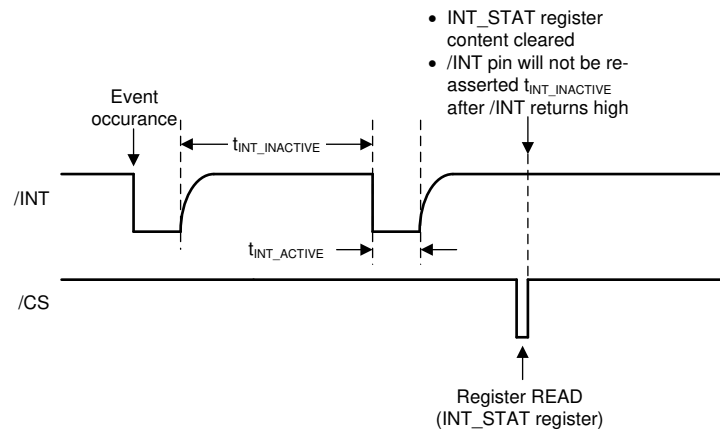


图 8-7. Dynamic  $\overline{\text{INT}}$  Assertion Scheme With INT\_STAT Register Read During  $t_{\text{INT\_INACTIVE}}$

The static  $\overline{\text{INT}}$  assertion scheme is selected by default upon device reset. The  $\overline{\text{INT}}$  pin assertion scheme can only be changed when bit TRIGGER is logic 0 in the CONFIG register.

### 8.3.9.2 Interrupt Idle Time ( $t_{\text{INT\_IDLE}}$ ) Time

Interrupt idle time ( $t_{\text{INT\_IDLE}}$ ) is implemented in TIC12400-Q1 to:

- Allow the  $\overline{\text{INT}}$  pin enough time to be pulled back high by the external pull-up resistor and allow the next assertion to be detectable by an edge-triggered microcontroller.
- Minimize the chance of glitching on the  $\overline{\text{INT}}$  pin if back-to-back events occur.

When there is a pending interrupt event and the interrupt event is not masked,  $t_{\text{INT\_IDLE}}$  is applied after the READ command is issued to the INT\_STAT register. If another event occurs during the interrupt idle time the INT\_STAT register content is updated instantly but the  $\overline{\text{INT}}$  pin is not asserted low until  $t_{\text{INT\_IDLE}}$  has elapsed. If another READ command is issued to the INT\_STAT register during  $t_{\text{INT\_IDLE}}$ , the INT\_STAT register content is cleared immediately, but the  $\overline{\text{INT}}$  pin is not re-asserted back low after  $t_{\text{INT\_IDLE}}$  has elapsed. An example of the interrupt idle time is given below to illustrate the  $\overline{\text{INT}}$  pin behavior under the static  $\overline{\text{INT}}$  assertion schemes:

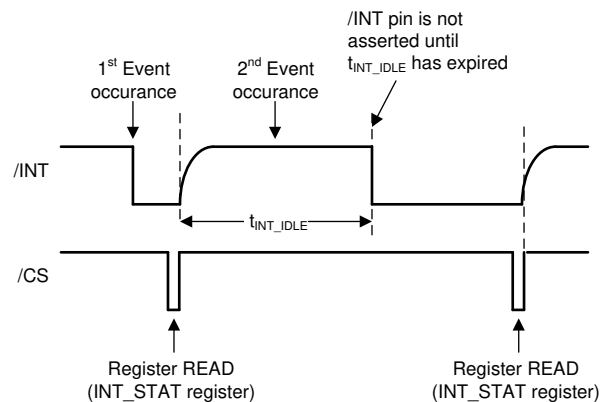


图 8-8.  $\overline{\text{INT}}$  Assertion Scheme With  $t_{\text{INT\_IDLE}}$

### 8.3.9.3 Microcontroller Wake-Up

Using a few external components, the  $\overline{\text{INT}}$  pin can be used for wake-up purpose to activate a voltage regulator via its inhibit inputs. An implementation example is shown in 图 8-9. This implementation is especially useful for waking up a microcontroller in sleep mode to allow significant system-level power savings.

Before the wake-up event, the  $\overline{\text{INT}}$  pin is in high impedance state on the TIC12400-Q1. The microcontroller can be kept in sleep state with all its GPIOs in logic low. Hence, Q2 remains off with its based in logic low state and the base of Q1 is weakly pulled-high to the  $V_S$  level. This causes Q1 to remain off, and the LDO\_EN signal is pulled-down to logic low to disable the regulator's output.  $V_{DD}$  is therefore unavailable to both the TIC12400-Q1

device and the microcontroller and SPI communication is not supported. Switch status monitoring, however, is still active in the TIC12400-Q1.

When an event such as switch status change, temperature warning, O V and so fourth occurs, the  $\overline{\text{INT}}$  pin is asserted low by TIC12400-Q1, causing Q1 to turn on to activate the voltage regulator. The microcontroller is then reactivated, and the communication between the microcontroller and the TIC12400-Q1 is reestablished. The microcontroller can then access stored event information using SPI communication. Note: since the  $\overline{\text{INT}}$  pin is de-asserted after the INT\_STAT register is read, the microcontroller is required to keep the regulator on by driving the  $\mu\text{C\_LDO\_EN}$  signal high. This allows  $V_{\text{DD}}$  to stay high to provide power to the microcontroller and support SPI communications.

The wake-up implementation is applicable only when the device is configured to use the static  $\overline{\text{INT}}$  assertion scheme.

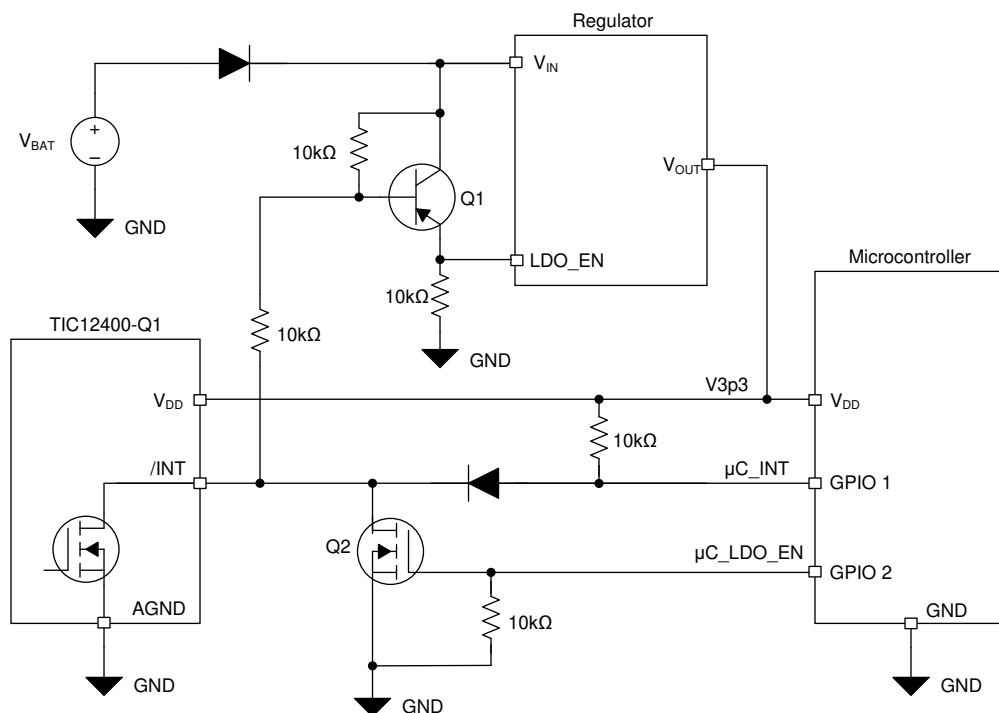


图 8-9.  $\overline{\text{INT}}$  Connection to Support Microcontroller Wake-Up

#### 8.3.9.4 Interrupt Enable or Disable and Interrupt Generation Conditions

Each switch input can be programmed to enable or disable interrupt generation upon status change by configuring registers [INT\\_EN\\_COMP1](#) to [INT\\_EN\\_COMP2](#) (for comparator inputs) and [INT\\_EN\\_CFG1](#) to [INT\\_EN\\_CFG4](#) (for ADC inputs). Interrupt generation condition can be adjusted for THRES\_COM (for IN0-IN11) by adjusting the IN\_COM\_EN bit in the [MATRIX](#) register.

The abovementioned registers can also be used to control interrupt generation condition based on the following settings:

1. **Rising edge:** an interrupt is generated if the current input measurement is above the corresponding threshold and the previous measurement was below.
2. **Falling edge:** an interrupt is generated if the current input measurement is below the corresponding threshold and the previous measurement was above.
3. **Both edges:** changes of the input voltage in either direction results in an interrupt generation.

Note interrupt generation from switch status change is disabled for all inputs by default upon device reset.

### 8.3.9.5 Detection Filter

When monitoring the switch input status, a detection filter can be configured by setting the DET\_FILTER bits in the [CONFIG](#) register to generate Switch Status Change (SSC) interrupt only if the same input status (w.r.t the threshold) is sampled consecutively. This detection filter can be useful to debounce inputs during a switch toggle event. Four different filtering schemes are available:

1. Generate an SSC interrupt, if the voltage level at an input crossed its threshold.
2. Generate an SSC interrupt, if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 2 consecutive polling cycles.
3. Generate an SSC interrupt, if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 3 consecutive polling cycles.
4. Generate an SSC interrupt, if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 4 consecutive polling cycles.

The default value of switch status is stored internally after the 1st detection cycle, even if detection filter (by configure the DET\_FILTER in the [CONFIG](#) register) is used. An example is illustrated below with the assumption that DET\_FILTER in register [CONFIG](#) is set to 11 (SSC interrupt is generated if the input crosses the threshold and the status is stable w.r.t. the threshold for at least 4 consecutive detection cycles). Assume switch status change is detected in the 3rd detection cycle and stays the same for the next 3 cycles.

| DETECTION CYCLE | 1   | 2 | 3                             | 4 | 5 | 6   |
|-----------------|---|---|-------------------------------|---|---|---|
| Event           | <ul style="list-style-type: none"> <li>• Default Switch status stored</li> <li>• INT asserted</li> <li>• SSC flagged</li> </ul> | — | Switch status change detected | — | — | <ul style="list-style-type: none"> <li>• INT asserted</li> <li>• SSC flagged</li> </ul> |

The detection filter applies to all enabled inputs regardless of their input modes (ADC or comparator) selection. The detection filter counter is reset to 0 when the TRIGGER bit in the [CONFIG](#) register is de-asserted to logic 0. Upon device reset, the default setting for the detection filter is set to generating an SSC interrupt at every threshold crossing.

Note: the detection filter does not apply to the common threshold THRES\_COM.

### 8.3.10 Temperature Monitor

When multiple switch inputs are closed and high wetting current setting is enabled, considerable power can be dissipated by the device and raise the device temperature. TIC12400-Q1 has integrated temperature monitoring and protection circuitry to put the device in low power mode to prevent damage due to overheating. Two types of temperature protection mechanisms are integrated in the device: Temperature Warning (TW) and Temperature Shutdown (TSD). The triggering temperatures and hysteresis are specified in [表 8-4](#) below:

**表 8-4. Temperature Monitoring Characteristics of TIC12400-Q1**

| PARAMETER   | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Temperature warning trigger temperature ( $T_{TW}$ )            | 130 | 140 | 155 | °C   |
| Temperature shutdown trigger temperature ( $T_{TSD}$ )          | 150 | 160 | 175 | °C   |
| Temperature hysteresis ( $T_{HYS}$ ) for $T_{TW}$ and $T_{TSD}$ |     | 15  |     | °C   |

#### 8.3.10.1 Temperature Warning (TW)

When the device temperature goes above the temperature warning trigger temperature ( $T_{TW}$ ), the TIC12400-Q1 performs the following operations:

1. Generate an interrupt by asserting the INT pin low and flag the TW bit in INT\_STAT register to logic 1. The TEMP bit in the SPI flag is also flagged to logic 1 for all SPI transactions.
2. The TW\_STAT bit of the IN\_STAT\_MISC register is flagged to logic 1.
3. If the TW\_CUR\_DIS\_CSO or TW\_CUR\_DIS\_CSO bit in [CONFIG](#) register is set to logic 0 (default), the wetting current is adjusted down to 2 mA for 10 mA or 15 mA settings. The wetting current stays at its pre-configured value if 0 mA, 1 mA, 2 mA, or 5 mA setting is used.

- Maintain the low wetting current as long as the device junction temperature stays above  $T_{TW} - T_{HYS}$ .

The  $\overline{INT}$  pin is released and the INT\_STAT register content is cleared on the rising edge of  $\overline{CS}$  provided the INT\_STAT register has been read during  $\overline{CS}$  low. The TIC12400-Q1 continues to monitor the temperature, but does not issue further interrupts if the temperature continues to stay above  $T_{TW} - T_{HYS}$ . The status bit TW\_STAT in register IN\_STAT\_MISC continues to stay at logic 1 as long as the temperature warning condition exists.

If desired, the reduction of wetting current down to 2 mA setting (from 10 mA or 15 mA) can be disabled by setting the TW\_CUR\_DIS\_CSO or TW\_CUR\_DIS\_CSI bit in the [CONFIG](#) register to 1. The interrupt is still generated ( $\overline{INT}$  asserted low and INT\_STAT interrupt register is updated) when the temperature warning event occurs but the wetting current is not reduced. This setting applies to both the polling and continuous mode operation. Note: if the feature is enabled, switch detection result might be impacted upon  $T_{TW}$  event if the wetting current is reduced to 2 mA from 10 mA or 15 mA.

When the temperature drops below  $T_{TW} - T_{HYS}$ , the  $\overline{INT}$  pin is asserted low (if released previously) to notify the microcontroller that the temperature warning condition no longer exists. The TW bit of the interrupt register INT\_STAT is flagged logic 1. The TW\_STAT bit in the IN\_STAT\_MISC register is de-asserted back to logic 0. The device resumes operation using the current programmed settings (regardless of the  $\overline{INT}$  and  $\overline{CS}$  status).

### 8.3.10.2 Temperature Shutdown (TSD)

After the device enters TW condition, if the junction temperature continues to rise and goes above the temperature shutdown threshold ( $T_{TSD}$ ), the TIC12400-Q1 enters the Temperature Shutdown (TSD) condition and performs the following operations:

- Opens all the switches connected to the current sources and sinks to prevent any further heating due to excessive current flow.
- Generate an interrupt by asserting the  $\overline{INT}$  pin (if not already asserted) low and flag the TSD bit in the INT\_STAT register to logic 1. The TEMP bit in the SPI flag is also flagged to logic 1 for all SPI transactions.
- The TSD\_STAT bit of the IN\_STAT\_MISC register is flagged to logic 1. The TW\_STAT bit also stays at logic 1.
- SPI communication stays on and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without any interruption.
- Maintain the setting as long as the junction temperature stays above  $T_{TSD} - T_{HYS}$ .

The  $\overline{INT}$  pin is released and the INT\_STAT register content is cleared on the rising edge of  $\overline{CS}$  provided the INT\_STAT register has been read during  $\overline{CS}$  low. The TIC12400-Q1 continues to monitor the temperature, but does not issue further interrupts if the temperature continues to stay above  $T_{TSD} - T_{HYS}$ . The status bit TSD\_STAT in register IN\_STAT\_MISC continues to stay at logic 1 as long as the temperature shutdown condition exists.

When the temperature drops below  $T_{TSD} - T_{HYS}$ , the  $\overline{INT}$  pin is asserted low (if released previously) to notify the microcontroller that the temperature shutdown condition no longer exists. The TSD bit of the interrupt register INT\_STAT is flagged logic 1. In the IN\_STAT\_MISC register, the TSD\_STAT bit is de-asserted back to logic 0, while the TW\_STAT bit stays at logic 1. The device resumes operation using the wetting current setting described in section [Temperature Warning](#) if the temperature stays above  $T_{TW} - T_{HYS}$ . Note: the polling restarts from the first enabled channel and the SSC interrupt is generated at the end of the first polling cycle. The detected switch status from the first polling cycle becomes the default switch status for subsequent polling.

### 8.3.11 Parity Check and Parity Generation

The TIC12400-Q1 uses parity bit check to ensure error-free data transmission from and to the SPI controller.

The device uses odd parity, for which the parity bit is set so that the total number of ones in the transmitted data on SO (including the parity bit) is an odd number (that is  $\text{Bit0} \oplus \text{Bit1} \oplus \dots \oplus \text{Bit30} \oplus \text{Bit31} \oplus \text{Parity} = 1$ ).

The device also uses odd parity check after receiving data on SI from the SPI controller. If the total number of ones in the received data (including the parity bit) is an even number the received data is discarded. The  $\overline{INT}$  will be asserted low and the PRTY\_FAIL bit in the interrupt register (INT\_STAT) is flagged to logic 1 to notify the host that transmission error occurred. The PRTY\_FAIL flag is also asserted during SPI communications.

### 8.3.12 Cyclic Redundancy Check (CRC)

The TIC12400-Q1 includes a CRC module to support redundancy checks on the configuration registers to ensure the integrity of data. The CRC calculation is based on the ITU-T X.25 implementation, and the CRC polynomial (0x1021) used is popularly known as CRC-CCITT-16 since it was initially proposed by the ITU-T (formerly CCITT) committee. The CRC calculation rule is defined in 表 8-5:

表 8-5. CRC Calculation Rule

| CRC RULE              | VALUE                               |
|-----------------------|-------------------------------------|
| CRC result width      | 16 bits                             |
| Polynomial            | $x^{16} + x^{12} + x^5 + 1$ (1021h) |
| Initial (seed) value  | FFFFh                               |
| Input data reflected  | No                                  |
| Result data reflected | No                                  |
| XOR value             | 0000h                               |

The CRC calculation is done on all the configuration registers starting from register [CONFIG](#) and ending at register [MODE](#). The device substitutes a zero for each reserved configuration register bit during the CRC calculation. The CRC calculation can be triggered by asserting the CRC\_T bit in the CONFIG register. Once completed, the CRC\_CALC interrupt bit in the INT\_STAT register is asserted and an interrupt is issued. The 16-bit CRC calculation result is stored in the register CRC. This interrupt can be disabled by de-asserting the CRC\_CALC\_EN bit in the INT\_EN\_CFG0 register. It is important to avoid writing data to the configuration registers when the device is undergoing CRC calculations to prevent false calculation results.

图 8-10 shows the block diagram of the CRC module. The module consists of 16 shift-registers and 3 exclusive-OR gates. The registers start with 1111-1111-1111-1111 (or FFFFh) and the module performs an XOR function and shifts its content until the last bit of the register string is used. The final register's content after the last data bit is the calculated CRC value of the data set and the content is stored in the CRC register.

Note the CRC\_T bit self-clears after the CRC calculation is completed. Logic 1 is used for CRC\_T bit during CRC calculation.

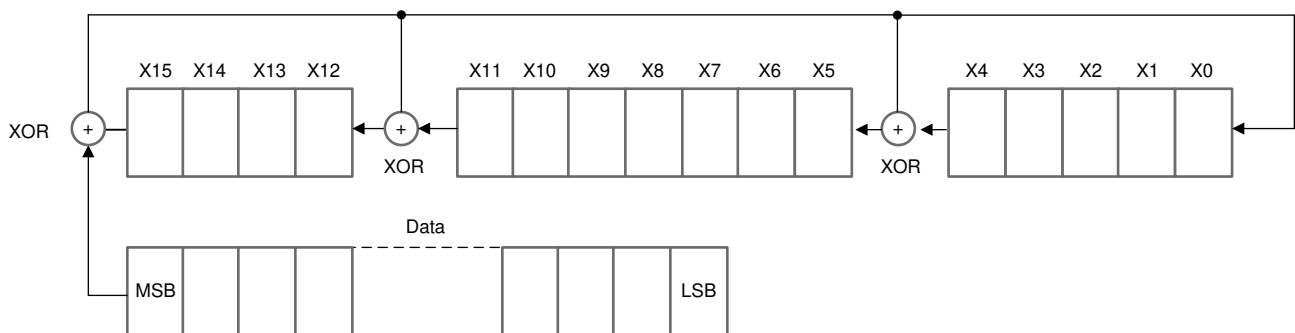


图 8-10. CCITT-16 CRC Module Block Diagram

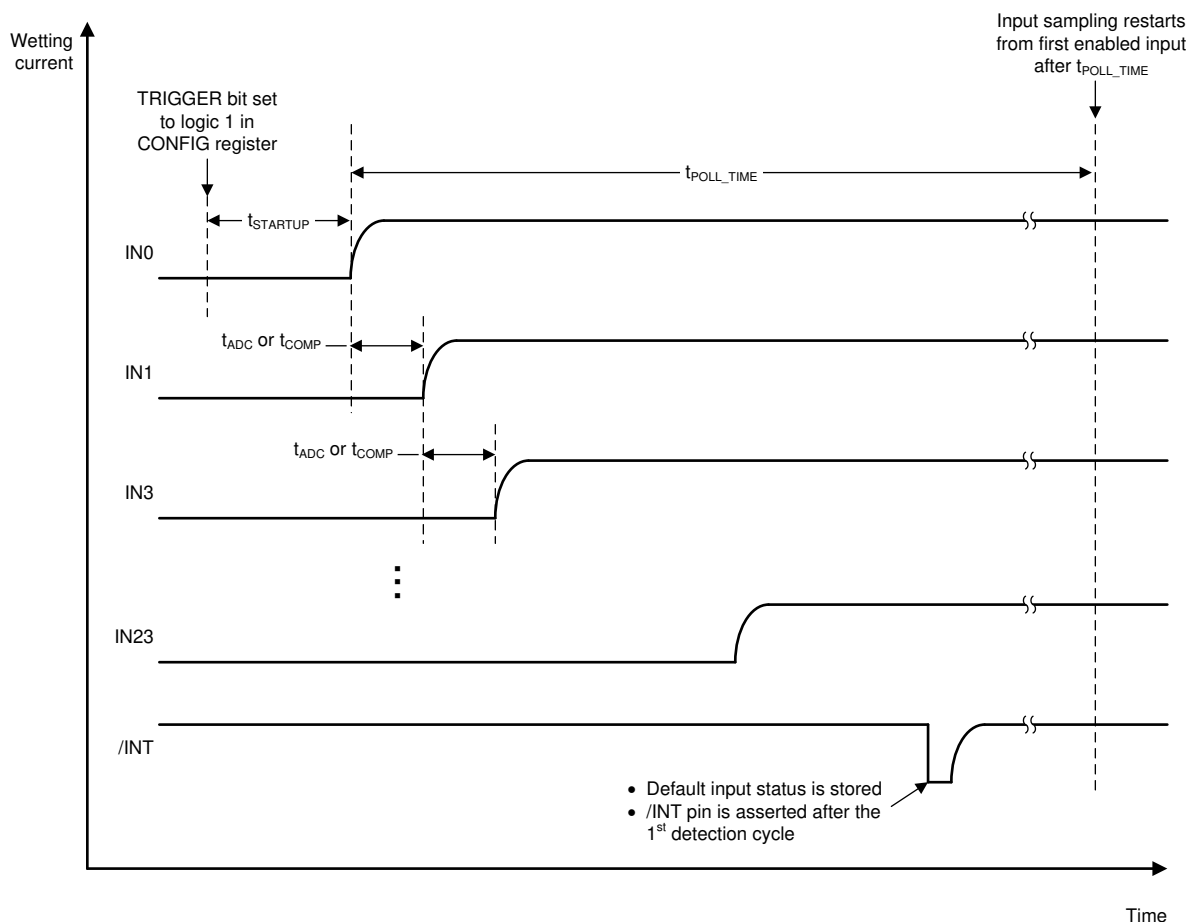
## 8.4 Device Functional Modes

The TIC12400-Q1 has 2 modes of operation: continuous mode and polling mode. The following sections describe the two operation modes in details as well as some of the advanced features that could be activated during normal operations.

### 8.4.1 Continuous Mode

In continuous mode, wetting current is continuously applied to each enabled input channel, and the status of each channel is sampled sequentially (starting from the IN0 to IN23). The TIC12400-Q1 monitors enabled inputs and issues an interrupt (if enabled) if a switch status change event is detected. The wetting current setting for each input can be individually adjusted by configuring the [WC\\_CFG0](#) and [WC\\_CFG1](#) to the 0 mA, 1 mA, 2 mA, 5 mA, 10 mA, or 15 mA setting. Each input is monitored by either a comparator or an ADC depending on the setting of the input mode in the register [MODE](#).

Figure 8-11 below illustrates an example of the timing diagram of the detection sequence in continuous mode. After the TRIGGER bit in register [CONFIG](#) is set to logic 1, it takes  $t_{STARTUP}$  to activate the wetting current for all enabled inputs. The wetting currents stay on continuously, while each input is routed to the ADC and comparator for sampling in a sequential fashion. After conversion and comparison is done for an input, the switch status (below or above detection threshold) is stored in registers ([IN\\_STAT\\_COMP](#) for comparator inputs and [IN\\_STAT\\_ADC0](#) to [IN\\_STAT\\_ADC1](#) for ADC inputs) to be used as the default state for subsequent detection cycles. The digital values (if the input is configured as ADC input mode) are stored in the registers [ANA\\_STAT0](#) to [ANA\\_STAT11](#). After the end of the first polling cycle, the  $\overline{INT}$  pin is asserted low to notify the microcontroller that the default switch status is ready to be read. The SSC bit in INT\_STAT register and the SPI status flag SSC are also asserted to logic 1. The polling cycle time ( $t_{POLL}$ ) determines how frequently each input is sampled and can be configured in the register [CONFIG](#).



**图 8-11. An Example of the Detection Sequence in Continuous Mode**



The [INT\\_STAT](#) register is cleared and  $\overline{\text{INT}}$  pin de-asserted if a SPI READ command is issued to the register. Note: the interrupt is always generated after the 1st detection cycle (after the TRIGGER bit in register [CONFIG](#) is set to logic 1). In subsequent detection cycles, the interrupt is generated only if switch status change is detected.

No wetting currents are applied to 0 mA- configured inputs, although some biasing current (as specified by  $I_{\text{IN\_LEAK\_0mA}}$ ) may still flow in and out of the input. Threshold crossing monitoring is still performed for the input using one or more of the defined thresholds. The 0 mA setting is useful for the integrated ADC or comparator to measure applied voltage on a specific input without being affected by the device wetting current.

### 8.4.2 Polling Mode

The polling mode can be activated to reduce current drawn in ignition-off condition to conserve battery charge. Unlike the continuous mode, the current sources and sinks do not stay on continuously in the polling mode. Instead, they are turned on or off sequentially from IN0 to IN23 and cycled through each individual input channel. The microcontroller can be put to sleep to reduce overall system power. If a switch status change (SSC) is detected by the TIC12400-Q1, the  $\overline{\text{INT}}$  pin (if enabled for the input channel) is asserted low (and the SSC bit in INT\_STAT register and the SPI status flag SSC are also asserted to logic 1). The  $\overline{\text{INT}}$  pin assertion can be used to wake up the system regulator which, in turn, wakes up the microcontroller as described in section [Microcontroller Wake-Up](#). The microcontroller can then use SPI communication to read the switch status information.

The polling is activated when the TRIGGER bit in the [CONFIG](#) register is set to logic 1. There are 2 different polling schemes that can be configured in TIC12400-Q1: standard polling and matrix polling.

#### 8.4.2.1 Standard Polling

In standard polling mode, wetting current is applied to each input for a pre-programmed polling active time between 64  $\mu\text{s}$  and 2048  $\mu\text{s}$ , set by the POLL\_ACT\_TIME bits in the [CONFIG](#) register. At the end of the wetting current application, the input voltage is sampled by the comparator (if input is configured as comparator input mode) or the ADC (if input is configured as ADC input mode). Each input is cycled through in sequential order from IN0 to IN23. Sampling is repeated at a frequency from 2 ms to 4096 ms, set by the POLL\_TIME bits in the [CONFIG](#) register. Wetting currents are applied to closed switches only during the polling active time; hence, the overall system current consumption can be greatly reduced.

Similar to continuous mode, after the first polling cycle, the switch status of each input (below or above detection threshold) is stored in registers ([IN\\_STAT\\_COMP](#) for comparator inputs and [IN\\_STAT\\_ADC0](#) to [IN\\_STAT\\_ADC1](#) for ADC inputs) to be used as the default state for subsequent polling cycles. The digital values (if the input is configured as ADC input mode) are stored in the registers [ANA\\_STAT0](#) to [ANA\\_STAT11](#). The  $\overline{\text{INT}}$  pin is asserted low to notify the microcontroller that the default switch status is ready to be read. The SSC bit in INT\_STAT register and the SPI status flag SSC are also asserted to logic 1. The [INT\\_STAT](#) register is cleared and  $\overline{\text{INT}}$  pin de-asserted if a SPI READ command is issued to the register. Note the interrupt is always generated after the 1st polling cycle (after the TRIGGER bit in register [CONFIG](#) is set to logic 1). In subsequent polling cycles the interrupt is generated only if switch status change is detected.

An example of the timing diagram of the polling mode operation is shown in [图 8-12](#).

**图 8-12. An Example of the Polling Sequence in Standard Polling Mode**

If the switch position changes between two active polling times, no interrupt will be generated and the status registers (*IN\_STAT\_COMP* for comparator inputs and *IN\_STAT\_ADC0* to *IN\_STAT\_ADC1* for ADC inputs) will not reflect such a change. An example is shown in 图 8-13.

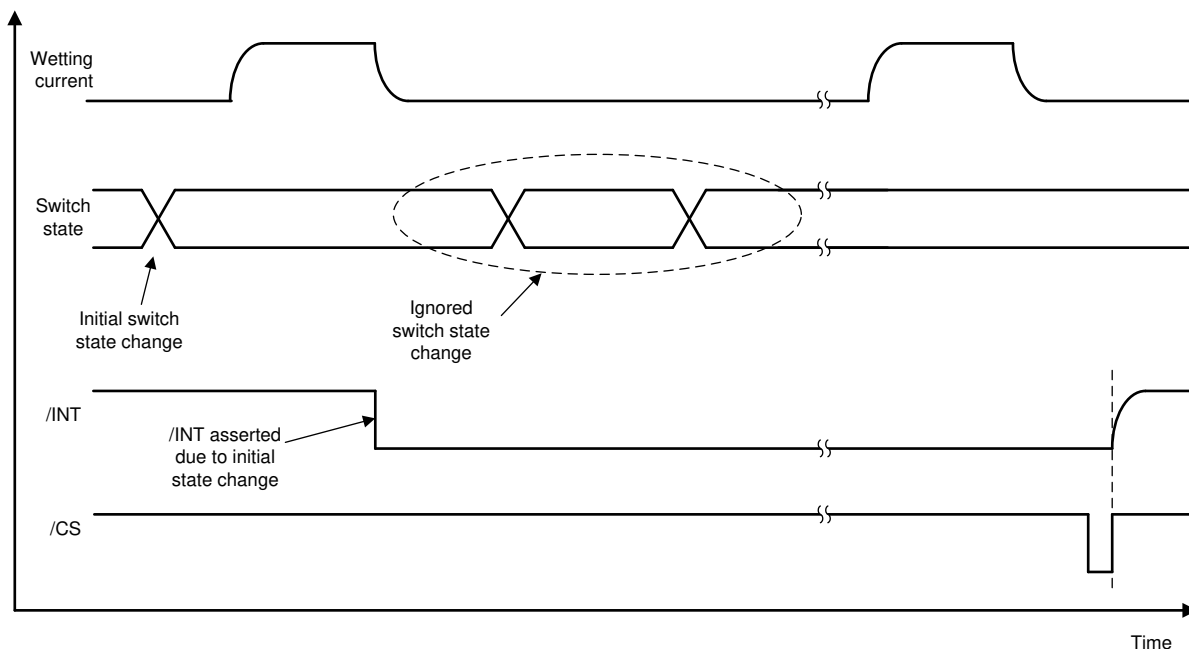
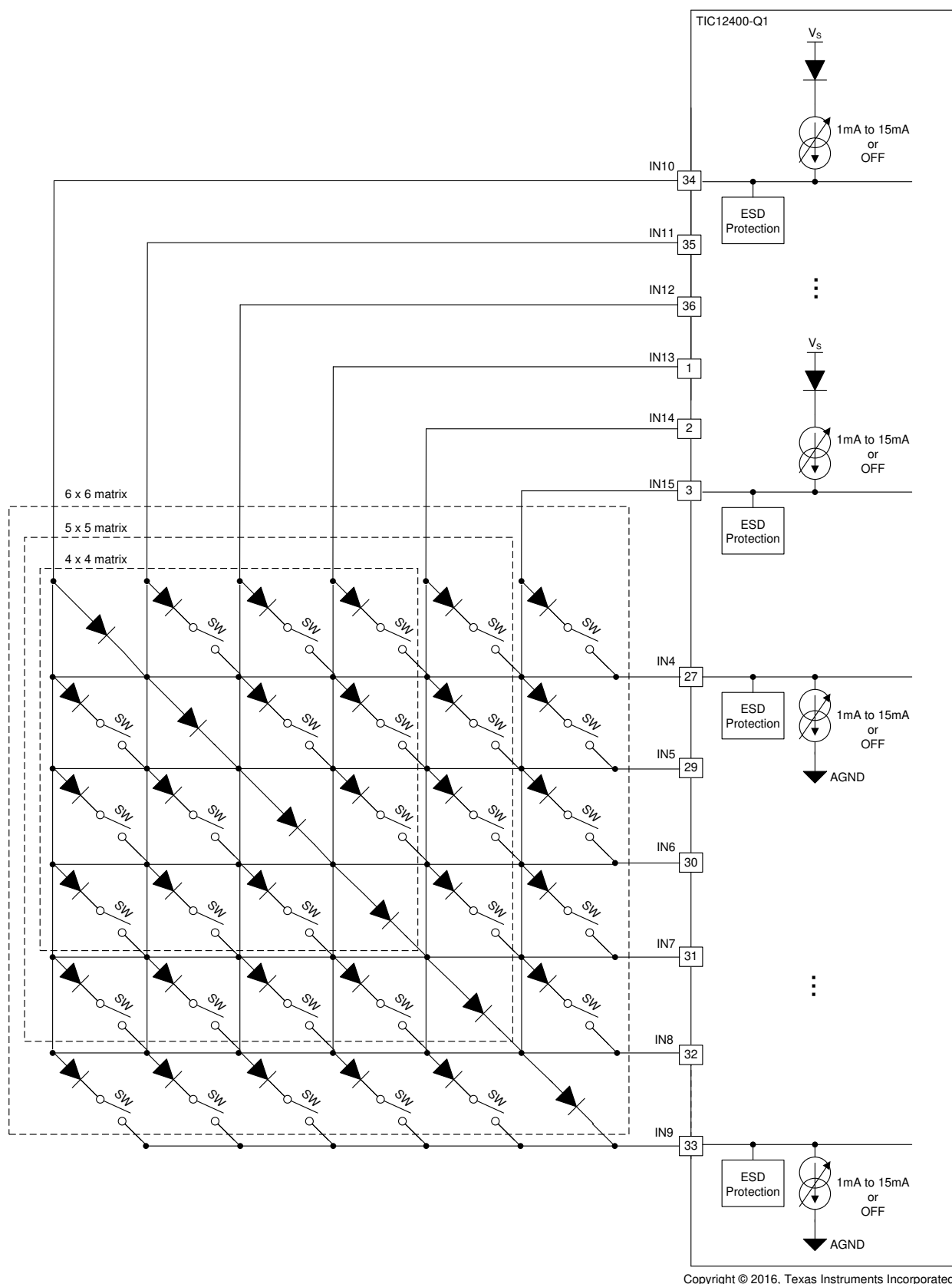


图 8-13. Example for Ignored Switch Position Change Between 2 Wetting Current Cycles

### 8.4.2.2 Matrix polling



**图 8-14. TIC12400-Q1 Matrix Configuration**

From IN4 to IN15 a special input switch matrix (see [Figure 8-14](#)) can be configured and monitored in addition to the standard switches to GND and  $V_{BAT}$ . This feature could be useful to monitor a special switch input configuration called Matrix Inputs as required by some specific OEMs.

Three different matrix configurations are possible, and are defined by MATRIX bits in the [MATRIX](#) register. If the MATRIX bits are set to '00' all inputs are treated as standard inputs with identical polling active time according to the POLL\_ACT\_TIME bits in the [CONFIG](#) register. Any settings other than '00' for MATRIX bits causes the polling active time for the matrix inputs to be configured according to POLL\_ACT\_TIME\_M bits in the [MATRIX](#) register. Inputs that are not part of the matrix configuration will be configured using the POLL\_ACT\_TIME bits in the [CONFIG](#) register.  $t_{POLL\_ACT\_TIME\_M}$  should be configured properly to allow sufficient time for the current source and sink to charge or discharge the capacitors (if any) connected to the switch inputs.

**表 8-6. TIC12400-Q1 Matrix Configuration Settings**

| Input | 4 x 4 MATRIX               |                             | 5 x 5 MATRIX               |                             | 6 x 6 MATRIX           |                             |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|-----------------------------|
|       | Current Source Or Sink     | Polling Active Time Setting | Current Source Or Sink     | Polling Active Time Setting | Current Source Or Sink | Polling Active Time Setting |
| IN4   | CSI                        | POLL_ACT_TIME_M             | CSI                        | POLL_ACT_TIME_M             | CSI                    | POLL_ACT_TIME_M             |
| IN5   | CSI                        |                             | CSI                        |                             | CSI                    |                             |
| IN6   | CSI                        |                             | CSI                        |                             | CSI                    |                             |
| IN7   | CSI                        |                             | CSI                        |                             | CSI                    |                             |
| IN8   | Configurable to CSO or CSI | POLL_ACT_TIME               | CSI                        | POLL_ACT_TIME               | CSI                    |                             |
| IN9   | Configurable to CSO or CSI |                             | Configurable to CSO or CSI |                             | CSI                    |                             |
| IN10  | CSO                        | POLL_ACT_TIME_M             | CSO                        | POLL_ACT_TIME_M             | CSO                    |                             |
| IN11  | CSO                        |                             | CSO                        |                             | CSO                    |                             |
| IN12  | CSO                        |                             | CSO                        |                             | CSO                    |                             |
| IN13  | CSO                        |                             | CSO                        |                             | CSO                    |                             |
| IN14  | CSO                        | POLL_ACT_TIME               | CSO                        | POLL_ACT_TIME               | CSO                    |                             |
| IN15  | CSO                        |                             | CSO                        |                             | CSO                    |                             |

The TIC12400-Q1 implements a different polling scheme when matrix input is configured. After the polling sequence is started (by setting TRIGGER bit in [CONFIG](#) register to logic 1), the polling takes place within the matrix input group first before the rest of the standard inputs are polled. After the matrix inputs are polled, the switch status of each input combination (below or above detection threshold) is stored internally in registers [IN\\_STAT\\_MATRIX0](#) and [IN\\_STAT\\_MATRIX1](#), and it is used as the default state for subsequent matrix polling cycles. The standard inputs follow the same polling behavior as described in section [Standard Polling](#). After the polling cycle is completed on matrix and standard inputs, the INT pin is asserted low to notify the microcontroller that the default switch status is ready to be read. The SSC bit in the [INT\\_STAT](#) register and the SPI status flag SSC are also asserted to logic 1.

The [INT\\_STAT](#) register is cleared and INT pin de-asserted if a SPI READ command is issued to the register. Note: the interrupt is always generated after the 1st complete polling cycle (after the TRIGGER bit in register [CONFIG](#) is set to logic 1). In subsequent polling cycles, the interrupt is generated only if switch status change is detected.

Note the following programming requirement when using the matrix polling:

- It is critical to program the CSO/CSI configuration for each matrix input appropriately according to 表 8-6 to avoid incorrect switch status detection.
- It is mandatory to set higher wetting current for the sinks (IN4-IN9) than the sources (IN10-IN15). The actual current flowing through the external switches will be the lesser of the two settings. If the same setting is used for both the sink and the source, the detected result might be incorrect. Because of this, the 15 mA setting shall not be used for the current sources and the 1 mA setting shall not be used for the current sinks. Depending on the type of matrix switches, the TIC12400-Q1 might require some specific wetting current settings to be able to distinguish between switch open or closed states.
- If TW\_CUR\_DIS\_CSO or TW\_CUR\_DIS\_CSI is set to logic 0 in the [CONFIG](#) register, wetting current is reduced to 2 mA for 10 mA and 15 mA settings upon TW event. Since it's mandatory to have higher wetting current for the sinks (IN4-IN9) than the sources (IN10-IN15) during matrix polling, 表 8-7 below summarizes the only possible settings if TW event is expected:

**表 8-7. Possible Wetting Current Settings for the Matrix Polling Mode if TW\_CUR\_DIS=0 and TW Event is Expected**

| CSO (IN10-IN15) | CSI (IN4-IN9)                | RESULTING WETTING CURRENT |
|-----------------|------------------------------|---------------------------|
| 1 mA            | 2 mA, 5 mA, 10 mA, and 15 mA | 1 mA                      |
| 2 mA            | 5 mA                         | 2 mA                      |

If higher wetting current is needed and TW event might be expected, the TW wetting current reduction feature needs to be disabled by setting TW\_CUR\_DIS\_CSO or TW\_CUR\_DIS\_CSI bit in the [CONFIG](#) register to 1.

- Only comparator input mode is supported for the matrix polling. Do not program the matrix inputs into ADC input mode. The comparison takes place on the source side (IN10-IN15) since the sink side is pulled to ground. Interrupt generation condition can be set by configuring the [INT\\_EN\\_COMP1](#) and [INT\\_EN\\_COMP2](#) registers for inputs IN10 to IN15.

Some programmability is removed when matrix polling mode is used, as listed below:

- To keep the polling scheme simple, the ability to disable inputs is removed for the matrix inputs. Only 3 configurations (4×4, 5×5, and 6×6) can be used for the matrix polling. Standard inputs outside the matrix input group can still be disabled, if desired.
- Detection filter (by configuring the DET\_FILTER in the [CONFIG](#) register) does not apply to the matrix inputs, but still applies to the standard inputs outside the matrix input group.
- When matrix polling is selected, continuous mode is not available to the standard inputs outside the matrix input group.

图 8-15 illustrates an example of the polling sequence for the 6×6 matrix input configuration:

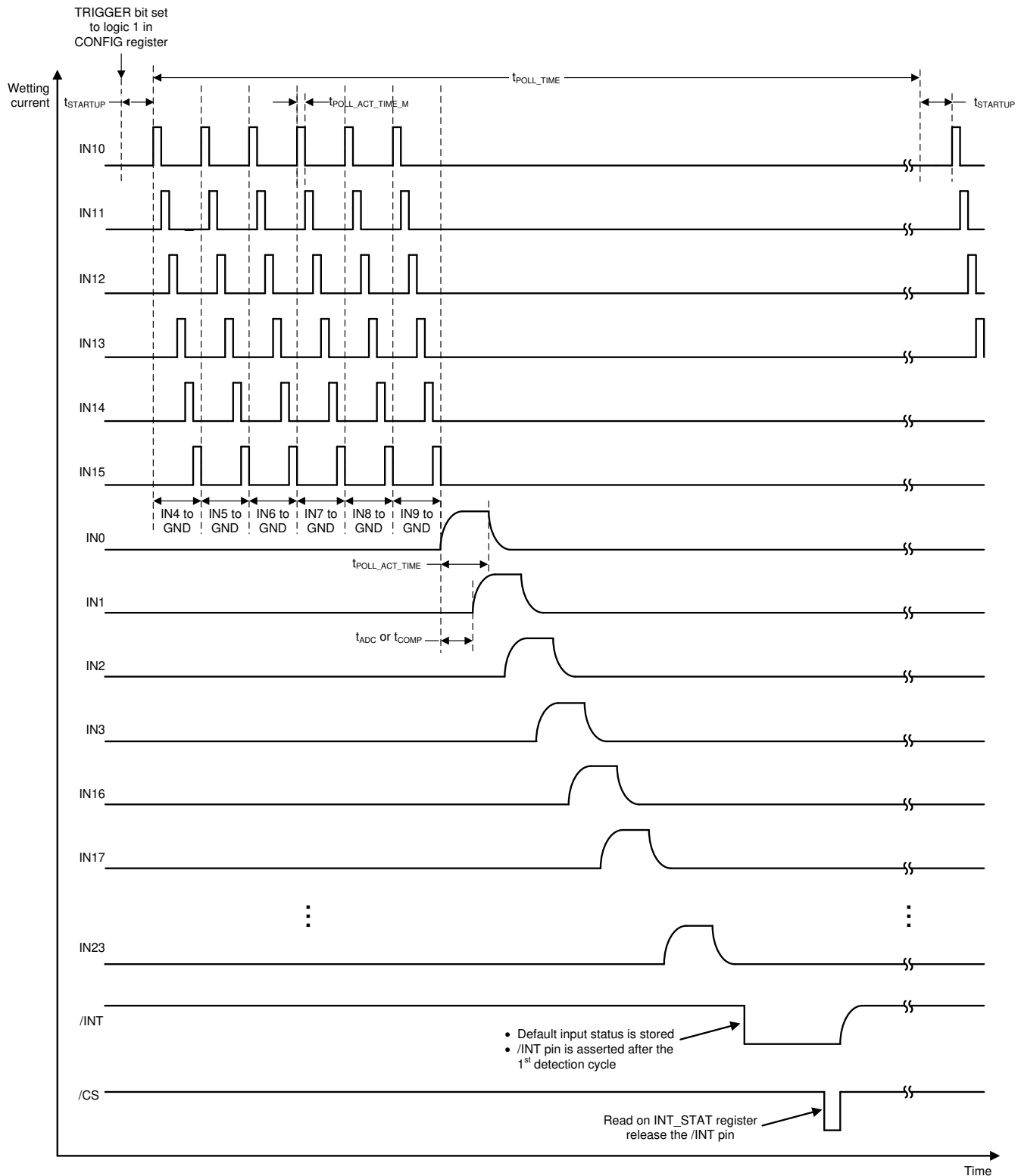


图 8-15. Polling Scheme for 6×6 Matrix Inputs



图 8-16 illustrates an example of the polling sequence for the 5×5 matrix input configuration. Note: the input IN9 and IN15 are included in the standard polling sequence.

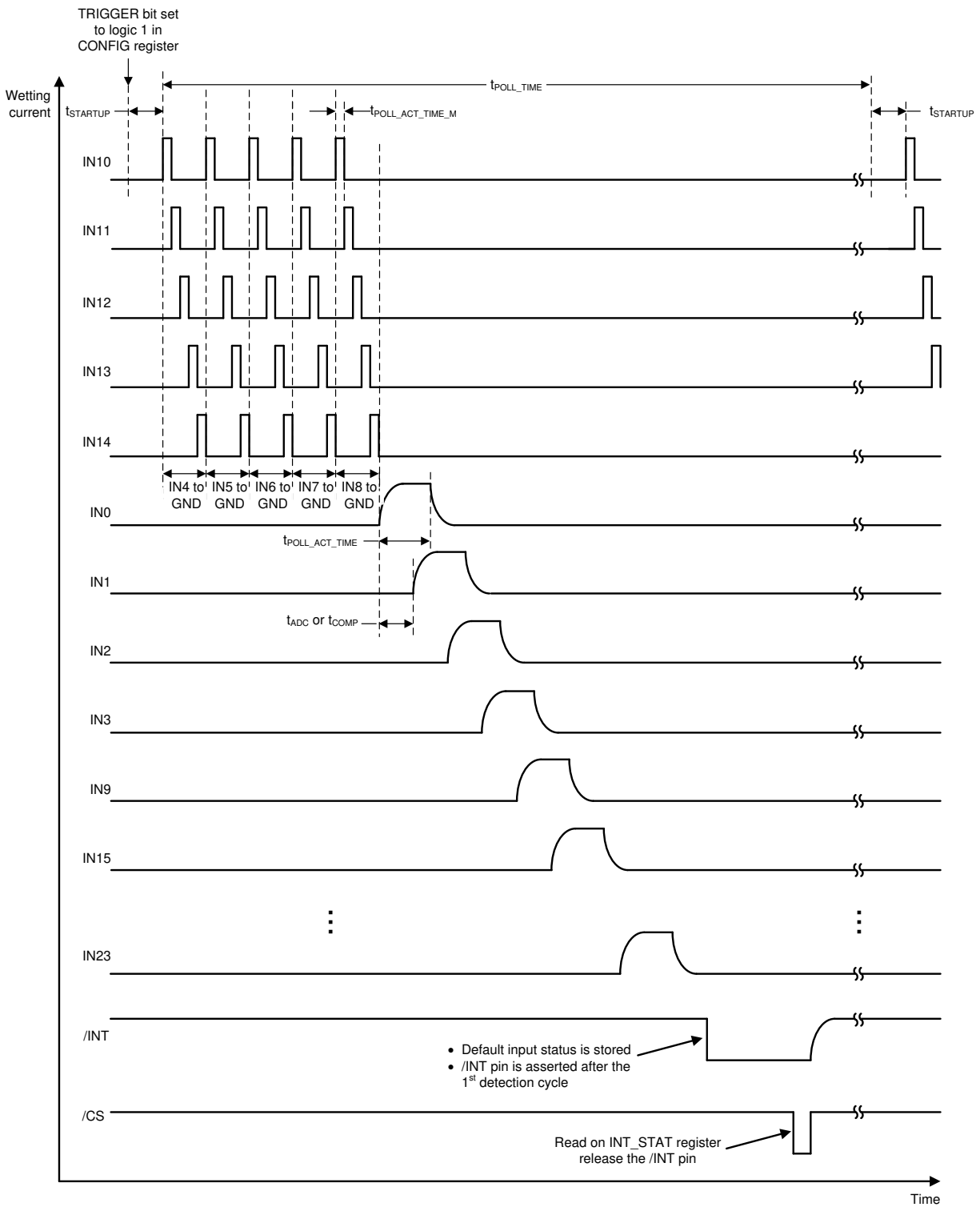


图 8-16. Polling Scheme for 5×5 Matrix Inputs

图 8-17 illustrates an example of the polling sequence for the 4×4 matrix input configuration. Note: inputs IN8, IN9, IN14, and IN15 are included in the standard polling sequence.

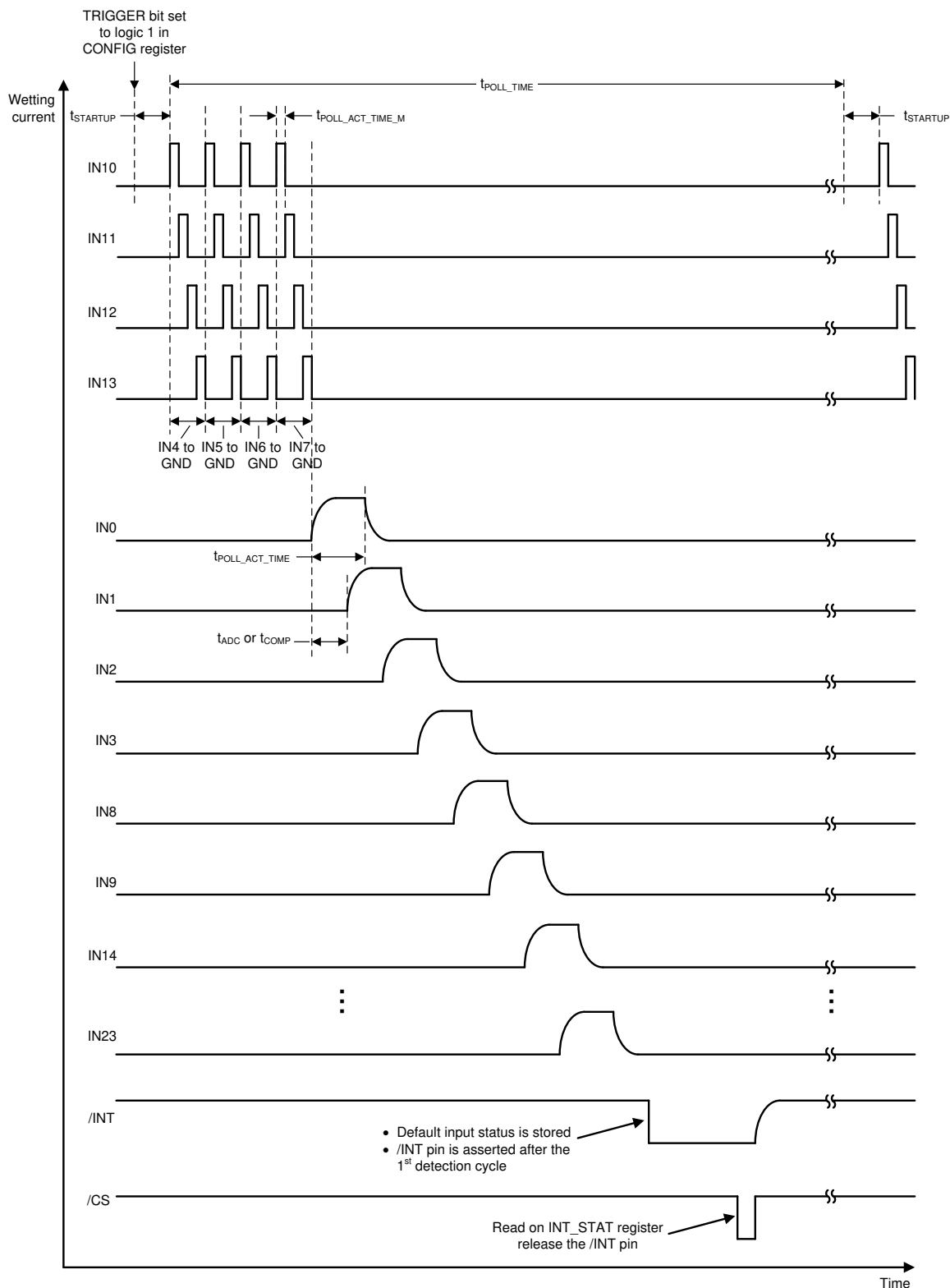


图 8-17. Polling Scheme for 4×4 Matrix Inputs

### 8.4.3 Additional Features

There are additional features that can be enabled during continuous and polling mode to increase robustness of device operation or provide more system information. These features are described in detail in the following sections.

#### 8.4.3.1 Clean Current Polling (CCP)

To detect resistor coded switches or reduce overall power consumption of the chip, a lower wetting current setting is recommended. However, certain system design requires 10 mA or higher cleaning current to clear oxide build-up on the mechanical switch contact surface when the current is applied to closed switches. A special type of polling, called the Clean Current Polling (CCP), can be used for this application.

If CCP is enabled each polling cycle consists of two wetting current activation steps. The first step uses the wetting current setting configured in the [WC\\_CFG0](#) and [WC\\_CFG1](#) registers as in the continuous mode or polling mode. The second step (cleaning cycle) is activated simultaneously for all CCP enabled inputs at a time  $t_{CCP\_TRAN}$  after the normal polling step of the last enabled input. Interrupt generation and  $\overline{INT}$  pin assertion is not impacted by the clean current pulses.

The wetting current and its active time for the cleaning cycle can be configured in the [CCP\\_CFG0](#) register. The cleaning cycle can be disabled, if desired, for each individual input by programming the [CCP\\_CFG1](#) register. CCP is available for both continuous mode and polling mode. To use the CCP feature, at least one input (standard or matrix) or the [节 8.4.3.3](#) has to be enabled.

Note: that although CCP can be enabled in Matrix polling mode, it is not an effective way to clean the matrix switch contact, since the current supplied from the TIC12400-Q1 is divided and distributed across multiple matrix channels.

图 8-18 illustrates the operation of the CCP when the device is configured to the standard polling mode.

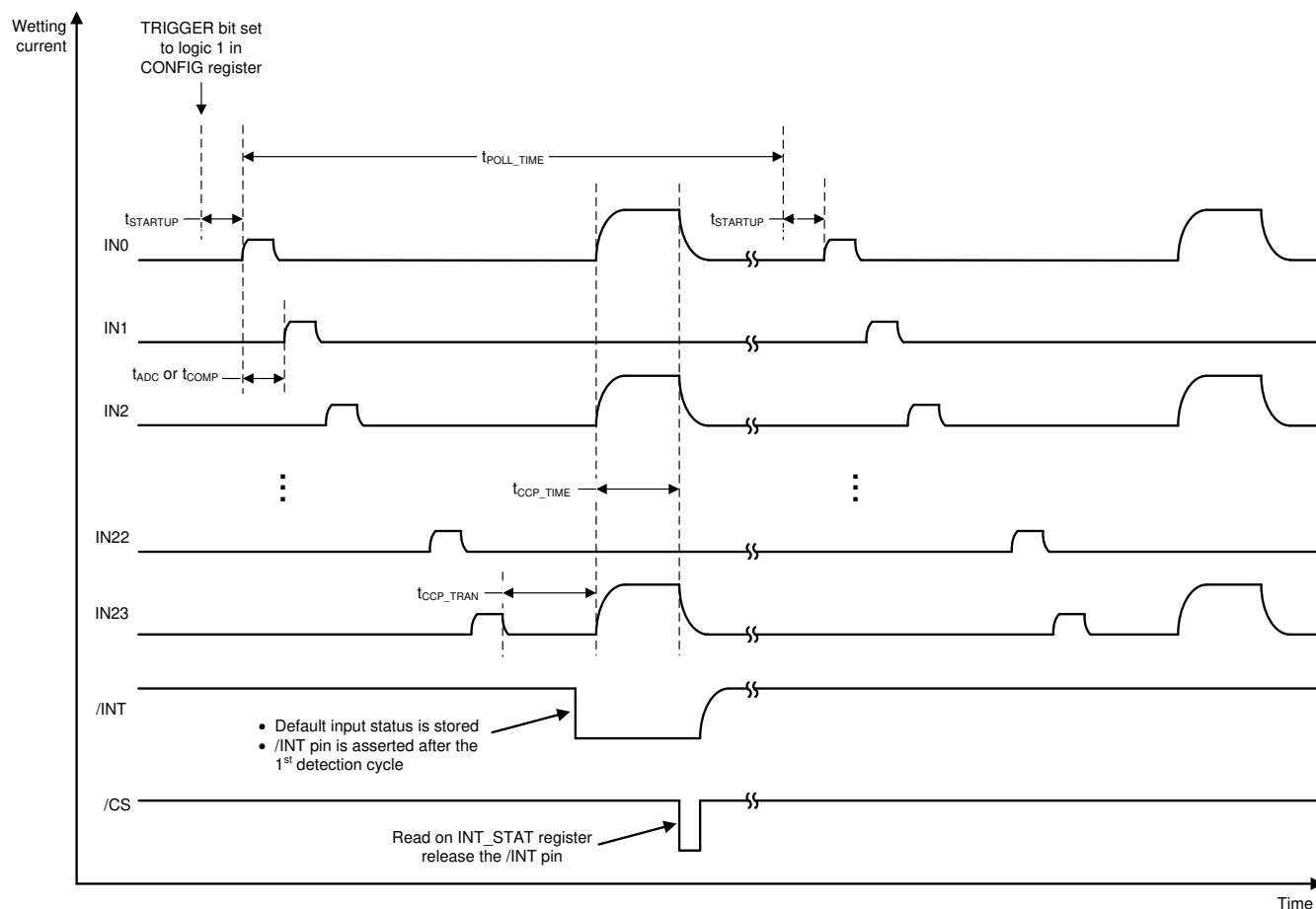


图 8-18. Standard Polling With CCP Enabled

图 8-19 illustrates the operation of the CCP when the device is configured to the continuous mode:

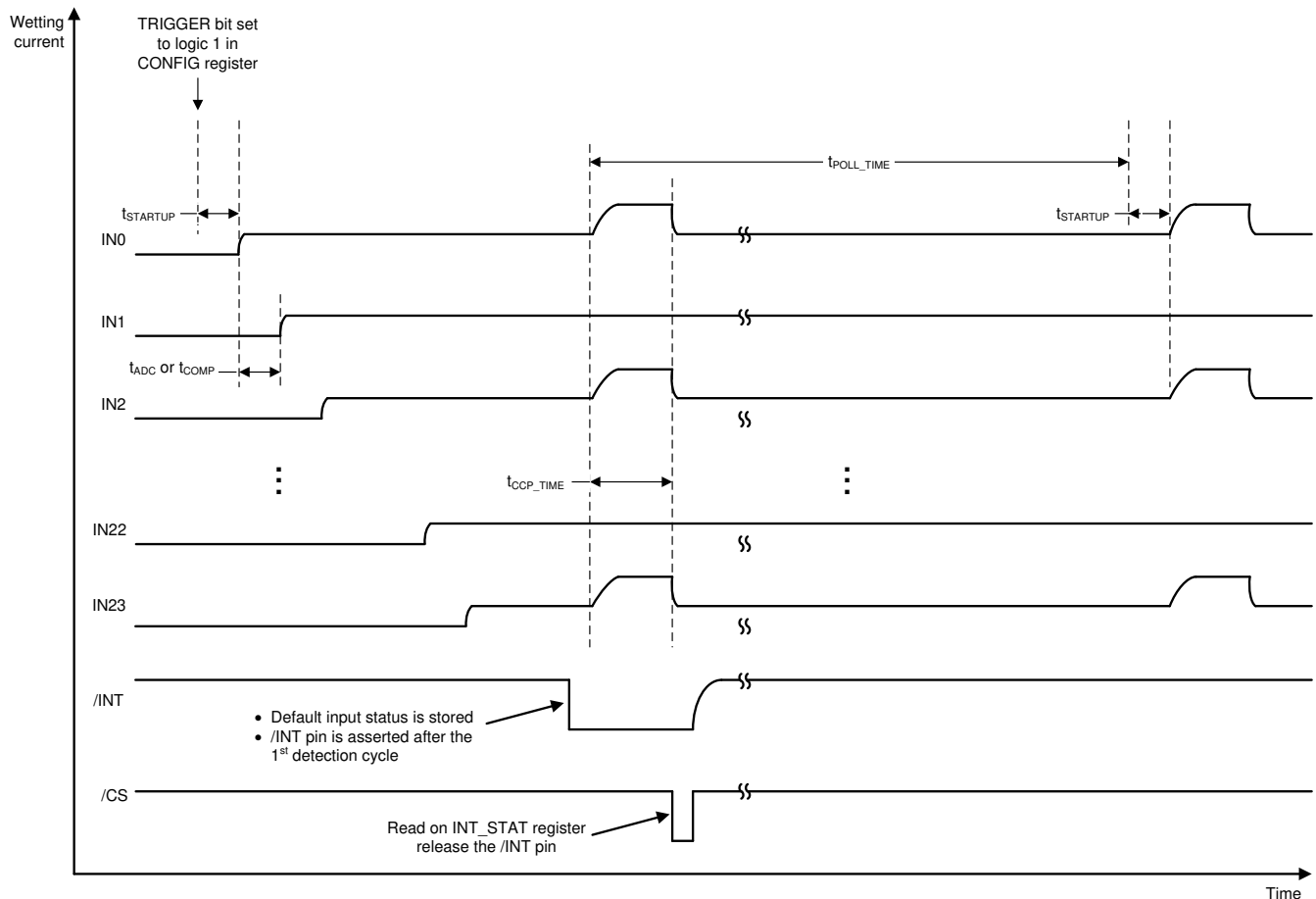


图 8-19. Continue Mode With CCP Enabled

#### 8.4.3.2 Wetting Current Auto-Scaling

The 10 mA and 15 mA wetting current settings are useful to clean oxide build-up on the mechanical switch contact surface when the switch changes state from open to close. After the switch is closed, it is undesirable to keep the wetting current level at high level if only digital switches are monitored since it results in high current consumption and could potentially heat up the device quickly if multiple inputs are monitored. The wetting current auto-scaling feature helps mitigate this issue.

When enabled (AUTO\_SCALE\_DIS\_CSO or AUTO\_SCALE\_DIS\_CSI bit = logic 0 in the [WC\\_CFG1](#) register), wetting current is reduced to 2 mA from 10 mA or 15 mA setting after switch closure is detected. The threshold used to determine a switch closure is the threshold configured in the [THRES\\_COMP](#) register for inputs configured as comparator input mode. For inputs configured as ADC input mode, the threshold used to determine a switch closure depends on the input number, as described in [表 8-8](#) below.

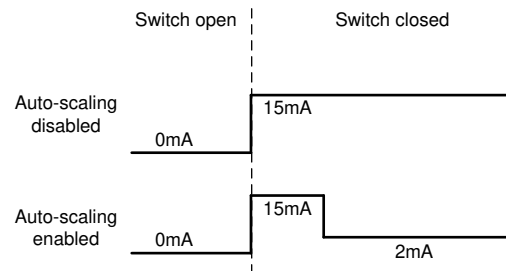
表 8-8. Threshold Used to Determine a Switch Closure for Wetting Current Auto-scaling for ADC Inputs

| INPUT        | THRESHOLD USED TO DETERMINE A SWITCH CLOSURE |
|--------------|--|
| IN0-IN11     | Mapped threshold from THRES0 to THRES7       |
| IN12 to IN17 | THRES2B                                      |
| IN18 to IN22 | THRES3C                                      |
| IN23         | THRES9                                       |

The current reduction takes place N cycles after switch closure is detected on an input, where N depends on the setting of the DET\_FILTER bits in the [CONFIG](#) register:

- DET\_FILTER= 00: wetting current is reduced immediately in the next detection cycle after a closed switch is detected.
- DET\_FILTER= 01: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 2 consecutive detection cycles.
- DET\_FILTER= 10: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 3 consecutive detection cycles.
- DET\_FILTER= 11: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 4 consecutive detection cycles.

The wetting current is adjusted back to the original setting of 10 mA or 15 mA at a time of N cycles after an open switch is detected, where N again depends on the DET\_FILTER bit setting in the [CONFIG](#) register. [图 8-20](#) depicts the behavior of the wetting current auto-scaling feature.



**图 8-20. Wetting Current Auto-scaling Behavior**

The wetting current auto-scaling only applies to 10 mA and 15 mA settings and is only available in continuous mode. If AUTO\_SCALE\_DIS\_CSO or AUTO\_SCALE\_DIS\_CSI bit is set to logic 1 in the [WC\\_CFG1](#) registers, the wetting current stays at its original setting when a closed switch is detected. Power dissipation needs to be closely monitored when wetting current auto-scaling is disabled for multiple inputs as the device could heat up quickly when high wetting current settings are used. If the auto-scaling feature is disabled in continuous mode, the total power dissipation can be approximated using [方程式 1](#).

$$P_{TOTAL} = V_S \times (I_{S\_CONT} + I_{WETT(TOTAL)}) \quad (1)$$

where  $I_{WETT(TOTAL)}$  is the sum of all wetting currents from all input channels. Increase in device junction temperature can be calculated based on  $P \times R_{\theta JA}$ . The junction temperature must be below  $T_{TSD}$  for proper device operation. An interrupt will be issued when the junction temperature exceeds  $T_{TW}$  or  $T_{TSD}$ . For detailed description of the temperature monitoring, please refer to sections [Temperature Warning \(TW\)](#) and [Temperature Shutdown \(TSD\)](#).

#### 8.4.3.3 $V_S$ Measurement

When the TIC12400-Q1 is used to monitor resistor-coded switches, the  $V_S$  supply voltage level becomes critical. If  $V_S$  is not sufficiently high, the device might not have enough headroom to produce accurate wetting currents. This could impact the accuracy of the switch status monitoring. It is imperative for the microcontroller to have knowledge of the  $V_S$  voltage on a constant basis in such a case.

Measurement of  $V_S$  voltage is a feature in TIC12400-Q1 that can be enabled by setting the VS\_MEAS\_EN bit in register [CONFIG](#) to logic 1. If enabled, at the end of every detection and polling cycle, the voltage on the  $V_S$  pin is sampled and converted by the ADC to a digital value. The conversion takes one extra  $t_{ADC}$ , and the converted value is recorded in the [ANA\\_STAT12](#) register.

The  $V_S$  measurement supports two different  $V_S$  voltage ranges that can be configured by the VS\_RATIO bit in the [CONFIG](#) register. By default (VS\_RATIO= logic 0), the supported  $V_S$  voltage range is from 4.5 V to 9 V, and  $V_S$  voltage in excess of 9 V results in a saturated ADC raw code of 1023. This setting provides better measurement resolution at lower  $V_S$  voltages. When VS\_RATIO bit is set to logic 1, the supported  $V_S$  voltage range is widened to 4.5 V to 30 V, and  $V_S$  voltage in excess of 30 V results in a saturated ADC raw code of

1023. This setting allows wider measurement range but more coarse measurement resolution. It is important to adjust the detection thresholds accordingly depending on the  $V_S$  voltage range configured.

Four different measurement thresholds can be programmed by the TIC12400-Q1:  $VS0\_THRES2A/B$  and  $VS1\_THRES2A/B$ . The value of these thresholds can be programmed by configuring registers [THRES\\_CFG0](#) to [THRES\\_CFG3](#) and the mapping can be programmed by configuring registers  $THRESMAP\_VS0\_THRES2A/B$  and  $THRESMAP\_VS1\_THRES2A/B$  bits in the register [THRESMAP\\_CFG2](#). When setting the thresholds follow the rules in [表 8-9](#) below.

**表 8-9. Proper Threshold Configuration for  $V_S$  Measurements**

| $V_S$ THRESHOLD | PROPER THRESHOLD CONFIGURATION   |
|-----------------|----------------------------------|
| VS0             | $VS0\_THRES2B \geq VS0\_THRES2A$ |
| VS1             | $VS1\_THRES2B \geq VS1\_THRES2A$ |

After the  $V_S$  measurement is enabled for the first time, the  $V_S$  measurement interrupt is always generated ( $\overline{INT}$  pin is asserted low, and the  $VS0$  or  $VS1$  bit in the [INT\\_STAT](#) register is flagged to logic 1) at the end of the first polling cycle to notify the microcontroller the initial  $V_S$  measurement result is ready to be retrieved. The  $VS0\_STAT$  and  $VS1\_STAT$  bits from register [IN\\_STAT\\_MISC](#) indicate the status of the  $V_S$  voltage with respect to the thresholds, and the [ANA\\_STAT12](#) register stores the converted digital value of the  $V_S$  voltage. The SPI status flag  $VS\_TH$  is also asserted to logic 1 during SPI communications. Note the status detected in the first polling cycle becomes the baseline value of comparison for subsequent  $V_S$  measurements and the interrupt will be generated only if threshold crossing is detected.

Similar to regular inputs, the interrupt generation conditions can be programmed by setting the  $VS\_TH0\_EN$  and  $VS\_TH1\_EN$  bits in the [INT\\_EN\\_CFG4](#) register to the following settings:

1. **Rising edge:** an interrupt is generated if the current  $V_S$  measurement is above the corresponding threshold and the previous measurement was below.
2. **Falling edge:** an interrupt is generated if the current  $V_S$  measurement is below the corresponding threshold and the previous measurement was above.
3. **Both edges:** changes of the  $V_S$  measurement status in either direction results in an interrupt generation.

Interrupt generation can also be disabled by setting  $VS\_TH0\_EN$  or  $VS\_TH1\_EN$  to logic 0 in register [INT\\_EN\\_CFG4](#). Once disabled,  $V_S$  voltage crossing does not flag the  $VS0$  or  $VS1$  bit in [INT\\_STAT](#) register and does not assert  $\overline{INT}$  pin low. To only mask the  $\overline{INT}$  pin from assertion (while keeping [INT\\_STAT](#) register updated), configure the  $VS1\_EN$  and  $VS0\_EN$  bits in register [INT\\_EN\\_CFG0](#) to logic 0.

Note the  $V_S$  measurement is only intended to be used as part of switch detection sequence to determine the validity of the switch detection states that are reported by the TIC12400-Q1. It is not intended to be used for standalone supply monitoring, such as monitoring cranking voltages, due to the potentially delayed response being part of the polling sequence. The  $V_S$  measurement result is accurate for  $V_S$  above 4.5 V.

By default, the  $V_S$  voltage measurement is disabled upon device reset.

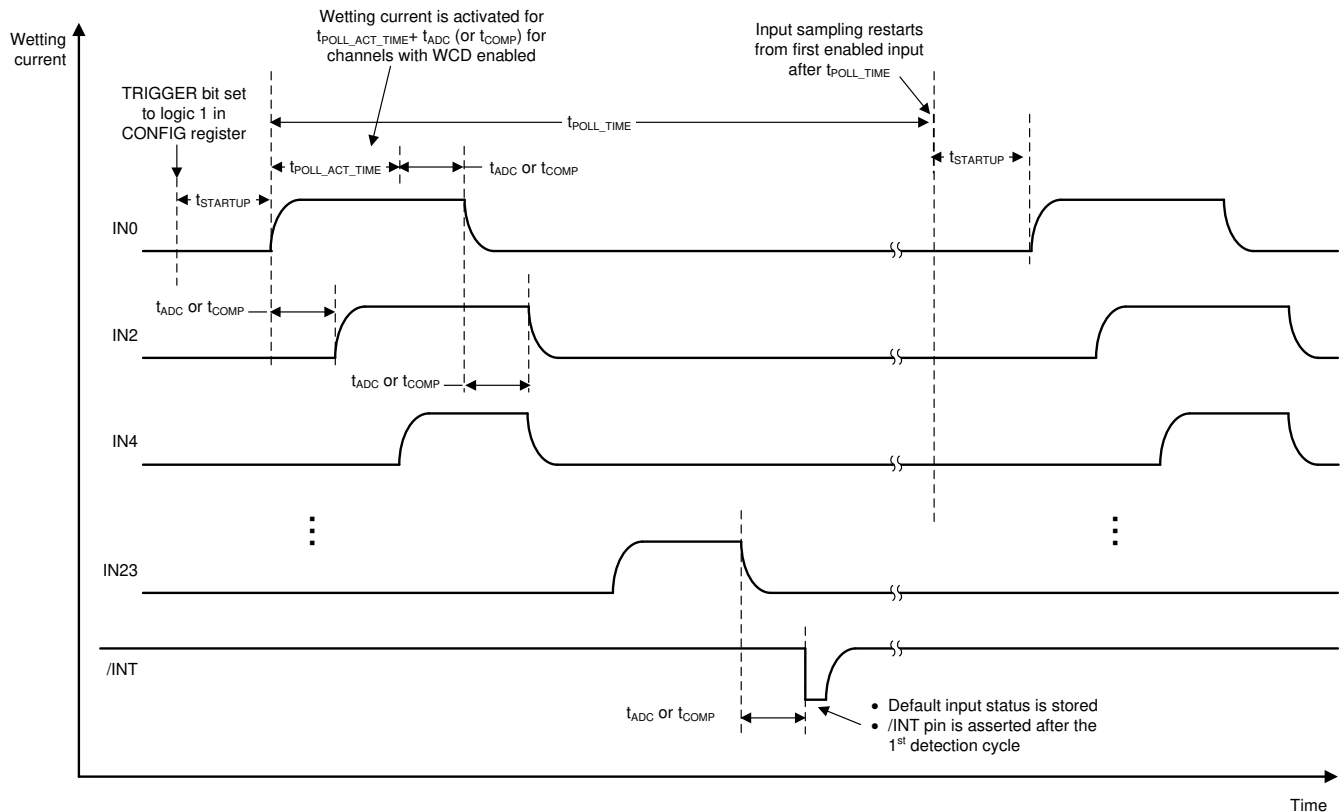
#### 8.4.3.4 Wetting Current Diagnostic

When the TIC12400-Q1 is used to monitor safety-critical switches, it may be valuable for the microcontroller to have knowledge of the operating status of the wetting current sources and sinks. This can be achieved by activating the wetting current diagnostic feature provided for inputs  $IN0$  to  $IN3$ .  $IN0$  and  $IN1$  can be diagnosed for defective wetting current sources, while  $IN2$  and  $IN3$  can be diagnosed for defective current sinks.

The wetting current diagnostic feature can be activated by setting the  $WET\_D\_INx\_EN$  bits in the [CONFIG](#) register to 1 for the desired inputs, where  $x$  can be 0, 1, 2, or 3. If activated, the TIC12400-Q1 checks the status of the wetting current sources and sinks for the configured input periodically as part of the polling sequence. If the wetting current is determined to be flawed, the TIC12400-Q1 pulls the  $\overline{INT}$  pin low to notify the host and flag the  $WET\_DIAG$  bit in the [INT\\_STAT](#) register to logic 1. The  $OI$  bit in the SPI flag is also asserted during SPI transactions. The microcontroller can then read bits  $IN0\_D$  to  $IN3\_D$  in register [IN\\_STAT\\_MISC](#) to learn more information on which wetting current source/sink is defective.

The wetting current diagnostic is not performed for inputs that are disabled (IN\_EN\_x bit = 0 in the [IN\\_EN](#) register) from polling, even if the feature is activated for those inputs. Also, it is critical to configure the current source/sink appropriately (CSO for IN0 and IN1, and CSI for IN2 and IN3) and program the input to ADC input mode before activating the wetting current diagnostic feature to prevent false interrupts from being generated. The wetting current diagnostic feature can be performed regardless of the states of external switches, and it is available in both continuous mode and polling mode.

Figure 8-21 shows an example of the feature carried out in a typical polling sequence. In this example, it can be observed that the wetting current is activated for duration of  $t_{\text{POLL\_ACT}} + t_{\text{ADC}}$  (or  $t_{\text{COMP}}$ ) for each input diagnosed (IN0 or IN2). Normal polling sequence resumes with IN4 and the wetting current is activated for  $t_{\text{POLL\_ACT}}$  for the rest of the inputs. The diagnostic is not executed on inputs IN1 and IN3 in this example since they are disabled.



**Figure 8-21. An Example of the Polling Sequence in Standard Polling Mode With Wetting Current Diagnostic Enabled**

#### 8.4.3.5 ADC Self-Diagnostic

In addition to the wetting current diagnostic, another feature – the ADC self-diagnostic, can be enabled to monitor the integrity of the internal ADC.

The ADC self-diagnostic feature is activated by setting the ADC\_DIAG\_T bit in the [CONFIG](#) register to logic 1. Once enabled, the TIC12400-Q1 periodically sends a test voltage to the ADC. The conversion result is stored in the ADC\_SELF\_ANA bits in the register [ANA\\_STAT12](#) and is compared with a pre-defined code to determine whether the conversion is performed properly. If an error is detected, the TIC12400-Q1 pulls the INT pin low to notify the host and flag the ADC\_DIAG bit in the [INT\\_STAT](#) to logic 1. The bit ADC\_D in register [IN\\_STAT\\_MISC](#) is updated with the result from the self-diagnostic. The ADC self-diagnostic feature is available in both continuous mode and polling mode.



## 8.5 Programming

The SPI interface communication consists of the 4 pins:  $\overline{CS}$ , SCLK, SI, and SO. The interface can work with SCLK frequency up to 4 MHz.

### 8.5.1 SPI Communication Interface Buses

#### 8.5.1.1 Chip Select ( $\overline{CS}$ )

The system microcontroller selects the TIC12400-Q1 to receive communication using the  $\overline{CS}$  pin. With the  $\overline{CS}$  pin in a logic LOW state, command words may be sent to the TIC12400-Q1 through the serial input (SI) pin, and the device information can be retrieved by the microcontroller via the serial output (SO) pin. The falling edge of the  $\overline{CS}$  enables the SO output and latches the content of the interrupt register INT\_STAT. The microcontroller may issue a READ command to retrieve information stored in the registers. Rising edge on the  $\overline{CS}$  pin initiates the following operations:

1. Disable the output driver and makes SO high-impedance.
2.  $\overline{INT}$  pin is reset to logic HIGH if a READ command to the INT\_STAT register was issued during  $\overline{CS}$  = LOW.

To avoid corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the  $\overline{CS}$  signal occur only when SCLK is in a logic LOW state. A clean  $\overline{CS}$  signal is needed to ensure no incomplete SPI words are sent to the device. The  $\overline{CS}$  pin should be externally pulled up to VDD by a 10 k $\Omega$  resistor.

#### 8.5.1.2 System Clock (SCLK)

The system clock (SCLK) input is used to clock the internal shift register of the TIC12400-Q1. The SI data is latched into the input shift register on the falling edge of the SCLK signal. The SO pin shifts the device stored information out on the rising edge of SCLK. The SO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to ensure validity of data and it is essential the SCLK pin be in a logic LOW state whenever  $\overline{CS}$  makes any transition. Therefore, it is recommended that the SCLK pin gets pulled to a logic LOW state as long as the device is not accessed and  $\overline{CS}$  is in a logic HIGH state. When the  $\overline{CS}$  is in a logic HIGH state, any signal on the SCLK and SI pins will be ignored and the SO pin remains as a high impedance output. Refer to [Figure 8-22](#) and [Figure 8-23](#) for examples of typical SPI read and write sequence.

#### 8.5.1.3 Slave In (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of the SCLK. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required length, the SPI\_FAIL bit of the INT\_STAT register is asserted to logic 1 and the  $\overline{INT}$  pin will be asserted low. The data received is considered invalid. Note the SPI\_FAIL bit is not flagged if SCLK is not present.

#### 8.5.1.4 Slave Out (SO)

The SO pin is the output from the internal shift register. The SO pin remains high-impedance until the  $\overline{CS}$  pin transitions to a logic LOW state. The negative transition of  $\overline{CS}$  enables the SO output driver and drives the SO output to the HIGH state (by default). The first positive transition of SCLK makes the status data bit 31 available on the SO pin. Each successive positive clock makes the next status data bit available for the microcontroller to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out scheme, with both input and output words transferring the most significant bit (MSB) first.

## 8.5.2 SPI Sequence

图 8-22 和 图 8-23 depict the SPI communication sequence during read and write operations for the TIC12400-Q1.

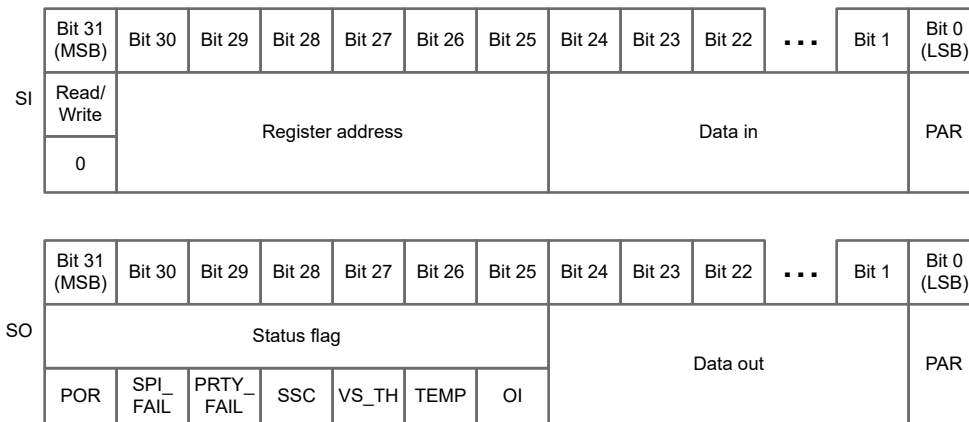


图 8-22. TIC12400-Q1 Read SPI Sequence

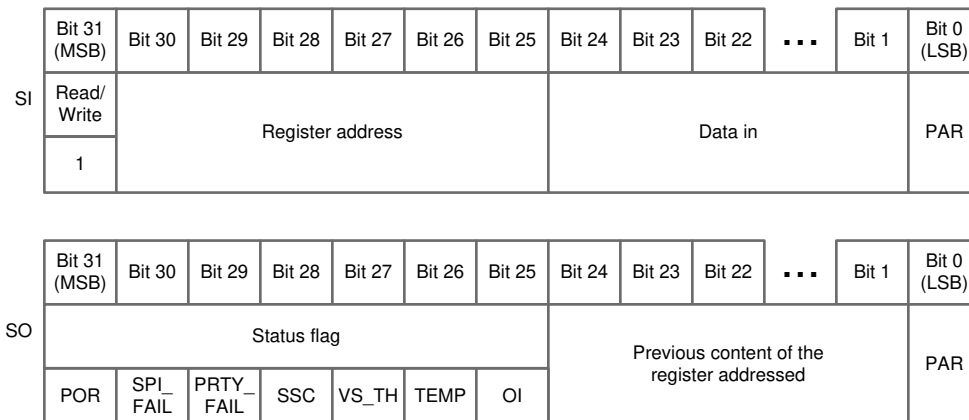


图 8-23. TIC12400-Q1 Write SPI Sequence

### 8.5.2.1 Read Operation

The Read/Write bit (bit 31) of the SI bus needs to be set to logic 0 for a READ operation. The 6-bits address of the register to be accessed follows next on the SI bus. The content from bit 24 to bit 1 does not represent a valid command for a read operation and will be ignored. The LSB (bit 0) is the parity bit used to detect communication errors.

On the SO bus, the status flags will be outputted from the TIC12400-Q1, followed by the data content in the register that was requested. The LSB is the parity bit used to detect communication errors.

Note there are several test mode registers used in the TIC12400-Q1 in addition to the normal functional registers, and a READ command to these test registers returns the register content. If a READ command is issued to an invalid register address, the TIC12400-Q1 returns all 0s.

### 8.5.2.2 Write Operation

The Read/Write bit (bit 31) on the SI bus needs to be set to 1 for a write operation. The 6-bits address of the register to be accessed follows next on the SI bus. Note: the register needs to be a writable configuration register, or otherwise the command will be ignored. The content from bit 24 to bit 1 represents the data to be written to the register. The LSB (bit 0) is the parity bit used to detect communication errors.

On the SO bus, the status flags will be output from the TIC12400-Q1, followed by the previous data content of the written register. The previous content of the register is latched after the full register address is decoded in the SI command (after bit 25 is transmitted). The new data will replace the previous data content at the end of the SPI transaction if the SI write is a valid command (valid register address and no SPI/parity error). If the write command is invalid, the new data will be ignored and the register content will remain unchanged. The LSB is the parity bit used to detect communication errors.

Note: there are several test mode registers used in the TIC12400-Q1 in addition to the normal functional registers. A WRITE command to these test registers has no effect on the register content, even though the register content is returned on the SO output. If a WRITE command is issued to an invalid register address, the SO output returns all 0s.

### 8.5.2.3 Status Flag

The status flags are output from SO during every READ or WRITE SPI transaction to indicate system conditions. These bits do not belong to an actual register, but their content is mirrored from the interrupt register INT\_STAT. A READ command executed on the INT\_STAT would clear both the bits inside the register and the status flag. The following table describes the information that can be obtained from each SPI status flag:

**表 8-10. TIC12400-Q1 SPI Status Flag Description**

| SYMBOL    | NAME                              | DESCRIPTION  |
|-----------|-----------------------------------|--|
| POR       | Power-on Reset                    | This flag mirrors the POR bit in the interrupt register INT_STAT, and it indicates, if set to 1, that a reset event has occurred. This bit is asserted after a successful power-on-reset, hardware reset, or software reset. Refer to <a href="#">§ 8.3.5</a> for more details.  |
| SPI_FAIL  | SPI Error                         | This flag mirrors the SPI_FAIL bit in the interrupt register INT_STAT and it indicates, if set to 1, that the last SPI responder in (SI) transaction is invalid. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required size, the SPI_FAIL bit, which mirrors its value to this SPI_FAIL status flag, of the interrupt register INT_STAT will be set to 1 and the INT pin will be asserted low. The data received will be considered invalid. Once the INT_STAT register is read, its content will be cleared on the rising edge of CS. The SPI_FAIL status flag, which mirrors the SPI_FAIL bit in the INT_STAT register, will also be de-asserted. Note the SPI_FAIL bit is not flagged if SCLK is not present. |
| PRTY_FAIL | Parity Fail                       | This flag mirrors the PRTY_FAIL bit in the interrupt register INT_STAT and it indicates, if set to 1, that the last SPI responder in (SI) transaction has a parity error. The device uses odd parity. If the total number of ones in the received data (including the parity bit) is an even number, the received data is discarded. The INT will be asserted low and the PRTY_FAIL bit in the interrupt register (INT_STAT) is flagged to logic 1, and the PRTY_FAIL status flag, which mirrors the PRTY_FAIL bit in the INT_STAT register, is also set to 1. Once the INT_STAT register is read, its content will be cleared on the rising edge of CS. The PRTY_FAIL status flag, which mirrors the PRTY_FAIL bit in the INT_STAT register, will also be de-asserted.  |
| SSC       | Switch State Change               | This flag mirrors the SSC bit in the interrupt register INT_STAT and it indicates, if set to 1, that one or more switch inputs crossed a threshold. To determine the origin of the state change, the microcontroller can read the content of registers IN_STAT_COMP (if input is set to comparator input mode), IN_STAT_ADC0 to IN_STAT_ADC1 (if input is set to ADC input mode), or IN_STAT_MATRIX0 to IN_STAT_MATRIX1 (if input is set to matrix input). Once the interrupt register (INT_STAT) is read, its content will be cleared on the rising edge of CS. The SSC status flag, which mirrors the SSC bit in the INT_STAT register, will also be de-asserted.  |
| VS_TH     | V <sub>S</sub> Threshold Crossing | This flag is set to 1 if either VS0 or VS1 bit in the interrupt register INT_STAT is flagged to 1. It indicates the V <sub>S</sub> voltage crosses one or more thresholds defined by VS0_THRES2A, VS0_THRES2B, VS1_THRES2A, or VS1_THRES2B. To determine the origin of the threshold crossing, the microcontroller can read register bits VS0_STAT and VS1_STAT in the register IN_STAT_MISC. Once the interrupt register (INT_STAT) is read, its content will be cleared on the rising edge of CS, and the VS_TH status flag will also be de-asserted.  |
| TEMP      | Temperature Event                 | This flag is set to 1 if either Temperature Warning (TW) or Temperature Shutdown (TSD) bit in the interrupt register INT_STAT is flagged to 1. It indicates a TW event or a TSD event has occurred. It is also flagged to 1 if a TW event or a TSD event is cleared. The interrupt register INT_STAT should be read to determine which event occurred. The SPI controller can also read the IN_STAT_MISC register to get information on the temperature status of the device. Once the interrupt register (INT_STAT) is read, its content will be cleared on the rising edge of CS, and the TEMP status flag will also be de-asserted.   |
| OI        | Other Interrupt                   | Other interrupt include interrupts such as OV, UV, CRC_CALC, WET_DIAG, ADC_DIAG and CHK_FAIL. This flag will be asserted 1 when any of the above mentioned bits is flagged in the interrupt register INT_STAT. The interrupt register INT_STAT should be read to determine which one or more events occurred. The SPI controller can also read the IN_STAT_MISC register to get information on the latest status of the device. Once the INT_STAT register is read, its content will be cleared on the rising edge of CS, and the OI status flag will also be de-asserted.   |

## 8.6 Register Maps

表 8-11 lists the memory-mapped registers for the TIC12400-Q1. All register offset addresses not listed in 表 8-11 should be considered as reserved locations and the register contents should not be modified.

**表 8-11. TIC12400-Q1 Registers**

| OFFSET   | TYPE | RESET | ACRONYM                          | REGISTER NAME  | SECTION            |
|----------|------|-------|----------------------------------|--|--------------------|
| 1h       | R    | 20h   | DEVICE_ID                        | Device ID Register                                     | <a href="#">Go</a> |
| 2h       | RC   | 1h    | INT_STAT                         | Interrupt Status Register                              | <a href="#">Go</a> |
| 3h       | R    | FFFFh | CRC                              | CRC Result Register                                    | <a href="#">Go</a> |
| 4h       | R    | 0h    | IN_STAT_MISC                     | Miscellaneous Status Register                          | <a href="#">Go</a> |
| 5h       | R    | 0h    | IN_STAT_COMP                     | Comparator Status Register                             | <a href="#">Go</a> |
| 6h-7h    | R    | 0h    | IN_STAT_ADC0, IN_STAT_ADC1       | ADC Status Register                                    | <a href="#">Go</a> |
| 8h-9h    | R    | 0h    | IN_STAT_MATRIX0, IN_STAT_MATRIX1 | Matrix Status Register                                 | <a href="#">Go</a> |
| Ah-16h   | R    | 0h    | ANA_STAT0- ANA_STAT12            | ADC Raw Code Register                                  | <a href="#">Go</a> |
| 17h-19h  | —    | —     | RESERVED                         | RESERVED   | —                  |
| 1Ah      | R/W  | 0h    | CONFIG                           | Device Global Configuration Register                   | <a href="#">Go</a> |
| 1Bh      | R/W  | 0h    | IN_EN                            | Input Enable Register                                  | <a href="#">Go</a> |
| 1Ch      | R/W  | 0h    | CS_SELECT                        | Current Source/Sink Selection Register                 | <a href="#">Go</a> |
| 1Dh-1Eh  | R/W  | 0h    | WC_CFG0, WC_CFG1                 | Wetting Current Configuration Register                 | <a href="#">Go</a> |
| 1Fh-20h  | R/W  | 0h    | CCP_CFG0, CCP_CFG1               | Clean Current Polling Register                         | <a href="#">Go</a> |
| 21h      | R/W  | 0h    | THRES_COMP                       | Comparator Threshold Control Register                  | <a href="#">Go</a> |
| 22h-23h  | R/W  | 0h    | INT_EN_COMP1, INT_EN_COMP2       | Comparator Input Interrupt Generation Control Register | <a href="#">Go</a> |
| 24h      | R/W  | 0h    | INT_EN_CFG0                      | Global Interrupt Generation Control Register           | <a href="#">Go</a> |
| 25h-28h  | R/W  | 0h    | INT_EN_CFG1- INT_EN_CFG4         | ADC Input Interrupt Generation Control Register        | <a href="#">Go</a> |
| 29h-2Dh  | R/W  | 0h    | THRES_CFG0- THRES_CFG4           | ADC Threshold Control Register                         | <a href="#">Go</a> |
| 2Eh- 30h | R/W  | 0h    | THRESMAP_CFG0- THRESMAP_CFG2     | ADC Threshold Mapping Register                         | <a href="#">Go</a> |
| 31h      | R/W  | 0h    | Matrix                           | Matrix Setting Register                                | <a href="#">Go</a> |
| 32h      | R/W  | 0h    | Mode                             | Mode Setting Register                                  | <a href="#">Go</a> |

### 8.6.1 DEVICE\_ID Register (Offset = 1h) [Reset = 20h]

DEVICE\_ID is shown in [图 8-24](#) and described in [表 8-12](#).

Return to [Summary Table](#).

This register represents the device ID of the TIC12400-Q1.

**图 8-24. DEVICE\_ID Register**

|          |       |    |    |    |    |    |    |       |    |    |    |
|----------|-------|----|----|----|----|----|----|-------|----|----|----|
| 23       | 22    | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 |
| RESERVED |       |    |    |    |    |    |    |       |    |    |    |
| R-0h     |       |    |    |    |    |    |    |       |    |    |    |
| 11       | 10    | 9  | 8  | 7  | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| RESERVED | MAJOR |    |    |    |    |    |    | MINOR |    |    |    |
| R-0h     | R-2h  |    |    |    |    |    |    | R-0h  |    |    |    |

LEGEND: R = Read only

**表 8-12. DEVICE\_ID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-11 | RESERVED | R    | 0h    | RESERVED  |
| 10-4  | MAJOR    | R    | 2h    | These 7 bits represents major revision ID. For TIC12400-Q1 the major revision ID is 2h. |
| 3-0   | MINOR    | R    | 0h    | These 4 bits represents minor revision ID. For TIC12400-Q1 the minor revision ID is 0h  |

### 8.6.2 INT\_STAT Register (Offset = 2h) [reset = 1h]

INT\_STAT is shown in 图 8-25 and described in 表 8-13.

Return to [Summary Table](#).

This register records the information of the event as it occurs in the device. A READ command executed on this register clears its content and resets the register to its default value. The  $\overline{\text{INT}}$  pin is released at the rising edge of the  $\overline{\text{CS}}$  pin from the READ command.

图 8-25. INT\_STAT Register

|          |       |          |          |          |           |          |          |
|----------|-------|----------|----------|----------|-----------|----------|----------|
| 23       | 22    | 21       | 20       | 19       | 18        | 17       | 16       |
| RESERVED |       |          |          |          |           |          |          |
| R-0h     |       |          |          |          |           |          |          |
| 15       | 14    | 13       | 12       | 11       | 10        | 9        | 8        |
| RESERVED |       | CHK_FAIL | ADC_DIAG | WET_DIAG | VS1       | VS0      | CRC_CALC |
| R-0h     |       | RC-0h    | RC-0h    | RC-0h    | RC-0h     | RC-0h    | RC-0h    |
| 7        | 6     | 5        | 4        | 3        | 2         | 1        | 0        |
| UV       | OV    | TW       | TSD      | SSC      | PRTY_FAIL | SPI_FAIL | POR      |
| RC-0h    | RC-0h | RC-0h    | RC-0h    | RC-0h    | RC-0h     | RC-0h    | RC-1h    |

LEGEND: R = Read only; RC = Read to clear

表 8-13. INT\_STAT Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-14 | RESERVED | R    | 0h    | RESERVED  |
| 13    | CHK_FAIL | RC   | 0h    | 0h = Default factory setting is successfully loaded upon device initialization or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = An error is detected when loading factory settings into the device upon device initialization.<br>During device initialization, factory settings are programmed into the device to allow proper device operation. The device performs a self-check after the device is programmed to diagnose whether correct settings are loaded. If the self-check returns an error, the CHK_FAIL bit is flagged to logic 1 along with the POR bit. The host controller is then recommended to initiate a software reset (see section <a href="#">Software Reset</a> ) to re-initialize the device and allow correct settings to be re-programmed. |
| 12    | ADC_DIAG | RC   | 0h    | 0h = No ADC self-diagnostic error is detected or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = ADC self-diagnostic error is detected.<br>The ADC Self-Diagnostic feature (see section <a href="#">ADC Self-Diagnostic</a> ) can be activated to monitor the integrity of the internal ADC. The ADC_DIAG bit is flagged to logic 1 if an ADC error is diagnosed.  |

**表 8-13. INT\_STAT Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 11  | WET_DIAG | RC   | 0h    | <p>0h = No wetting current error is detected, or the event status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Wetting current error is detected.</p> <p>The Wetting Current Diagnostic feature (see section <a href="#">Wetting Current Diagnostic</a>) can be activated to monitor the integrity of the internal current sources or sinks. The WET_DIAG bit is flagged to logic 1 if a wetting current error is diagnosed.</p>   |
| 10  | VS1      | RC   | 0h    | <p>0h = No <math>V_S</math> voltage state change occurred with respect to VS1_THRES2A or VS1_THRES2B or the status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = <math>V_S</math> voltage state change occurred with respect to VS1_THRES2A or VS1_THRES2B.</p> <p>The VS1 interrupt bit indicates whether <math>V_S</math> voltage state change occurred with respect to thresholds VS1_THRES2A and VS1_THRES2B if the <math>V_S</math> Measurement feature (see section <a href="#">VS Measurement</a>) is activated.</p> |
| 9   | VS0      | RC   | 0h    | <p>0h = No <math>V_S</math> voltage state change occurred with respect to VS0_THRES2A or VS0_THRES2B or the status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = <math>V_S</math> voltage state change occurred with respect to VS0_THRES2A or VS0_THRES2B.</p> <p>The VS0 interrupt bit indicates whether <math>V_S</math> voltage state change occurred with respect to thresholds VS0_THRES2A and VS0_THRES2B if the <math>V_S</math> Measurement feature (see section <a href="#">VS Measurement</a>) is activated.</p> |
| 8   | CRC_CALC | RC   | 0h    | <p>0h = CRC calculation is running, not started, or was acknowledged after a READ command was executed on the INT_STAT register.</p> <p>1h = CRC calculation is finished.</p> <p>CRC calculation (see section <a href="#">Cyclic Redundancy Check (CRC)</a>) can be triggered to make sure correct register values are programmed into the device. Once the calculation is completed, the CRC_CALC bit is flagged to logic 1 to indicate completion of the calculation, and the result can then be accessed from the CRC (offset = 3h) register.</p>              |
| 7   | UV       | RC   | 0h    | <p>0h = No under-voltage condition occurred or cleared on the <math>V_S</math> pin, or the event status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Under-voltage condition occurred or cleared on the <math>V_S</math> pin.</p> <p>When the UV bit is flagged to logic 1, it indicates the Under-Voltage (UV) event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the UV operation, please refer to section <a href="#">VS under-voltage (UV) condition</a>.</p>        |
| 6   | OV       | RC   | 0h    | <p>0h = No over-voltage condition occurred or cleared on the <math>V_S</math> pin, or the event status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Over-voltage condition occurred or cleared on the <math>V_S</math> pin.</p> <p>When the OV bit is flagged to logic 1, it indicates the Over-Voltage (OV) event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the OV operation, please refer to section <a href="#">VS over-voltage (OV) condition</a>.</p>            |

表 8-13. INT\_STAT Register Field Descriptions (continued)

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 5   | TW        | RC   | 0h    | <p>0h = No temperature warning event occurred or the event status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Temperature warning event occurred or cleared.</p> <p>When the TW bit is flagged to logic 1, it indicates the temperature warning event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the temperature warning operation, please refer to section <a href="#">Temperature Warning (TW)</a></p>  |
| 4   | TSD       | RC   | 0h    | <p>0h = No temperature Shutdown event occurred or the event status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Temperature Shutdown event occurred or cleared.</p> <p>When the TSD bit is flagged to logic 1, it indicates the temperature shutdown event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the temperature shutdown operation, please refer to section <a href="#">Temperature shutdown (TSD)</a></p>   |
| 3   | SSC       | RC   | 0h    | <p>0h = No switch state change occurred or the status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Switch state change occurred.</p> <p>The Switch State Change (SSC) bit indicates whether input threshold crossing has occurred from switch inputs IN0 to IN23. This bit is also flagged to logic 1 after the first polling cycle is completed after device polling is triggered.</p>  |
| 2   | PRTY_FAIL | RC   | 0h    | <p>0h = No parity error occurred in the last received SI stream or the error status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Parity error occurred.</p> <p>When the PRTY_FAIL bit is flagged to logic 1, it indicates the last SPI responder in (SI) transaction has a parity error. The device uses odd parity. If the total number of ones in the received data (including the parity bit) is an even number, the received data is discarded. The value of this register bit is mirrored to the PRTY_FLAG SPI status flag.</p>   |
| 1   | SPI_FAIL  | RC   | 0h    | <p>0h = 32 clock pulse during a <math>\overline{CS}</math> = low sequence was detected or the error status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = SPI error occurred</p> <p>When the SPI_FAIL bit is flagged to logic 1, it indicates the last SPI responder in (SI) transaction is invalid. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required length, the SPI_FAIL bit is flagged to logic 1, and the data received is considered invalid. The value of this register bit is mirrored to the SPI_FLAG SPI status flag. Note the SPI_FAIL bit is not flagged if SCLK is not present.</p> |



**表 8-13. INT\_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description   |
|-----|-------|------|-------|---|
| 0   | POR   | RC   | 1h    | <p>0h = no Power-On-Reset (POR) event occurred or the status got cleared after a READ command was executed on the INT_STAT register.</p> <p>1h = Power-On-Reset (POR) event occurred.</p> <p>The Power-On-Reset (POR) interrupt bit indicates whether a reset event has occurred. A reset event sets the registers to their default values and re-initializes the device state machine. This bit is asserted after a successful power-on-reset, hardware reset, or software reset. The value of this register bit is mirrored to the POR SPI status flag.</p> |

### 8.6.3 CRC Register (Offset = 3h) [Reset = FFFFh]

CRC is shown in 图 8-26 and described in 表 8-14.

Return to [Summary Table](#).

This register returns the CRC-16-CCCIT calculation result. The microcontroller can compare this value with its own calculated value to ensure correct register settings are programmed to the device.

**图 8-26. CRC Register**

|          |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    |    |    |    |    | CRC     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    |    |    |    |    | R-FFFFh |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-14. CRC Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-16 | RESERVED | R    | 0h    | Reserved  |
| 15-0  | CRC      | R    | FFFFh | CRC-16-CCITT calculation result: Bit1: LSB of CRC Bit16: MSB or CRC |

#### 8.6.4 IN\_STAT\_MISC Register (Offset = 4h) [Reset = 0h]

IN\_STAT\_MISC is shown in 图 8-27 and described in 表 8-15.

Return to [Summary Table](#).

This register indicates current device status unrelated to switch input monitoring.

**图 8-27. IN\_STAT\_MISC Register**

|          |    |          |       |         |         |         |          |
|----------|----|----------|-------|---------|---------|---------|----------|
| 23       | 22 | 21       | 20    | 19      | 18      | 17      | 16       |
| RESERVED |    |          |       |         |         |         |          |
| R-0h     |    |          |       |         |         |         |          |
| 15       | 14 | 13       | 12    | 11      | 10      | 9       | 8        |
| RESERVED |    |          | ADC_D | IN3_D   | IN2_D   | IN1_D   | IN0_D    |
| R-0h     |    |          | R-0h  | R-0h    | R-0h    | R-0h    | R-0h     |
| 7        | 6  | 5        | 4     | 3       | 2       | 1       | 0        |
| VS1_STAT |    | VS0_STAT |       | UV_STAT | OV_STAT | TW_STAT | TSD_STAT |
| R-0h     |    | R-0h     |       | R-0h    | R-0h    | R-0h    | R-0h     |

**表 8-15. IN\_STAT\_MISC Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-13 | RESERVED | R    | 0h    | Reserved  |
| 12    | ADC_D    | R    | 0h    | 0h = No error is identified from ADC self-diagnostic.<br>1h = An error is identified from ADC self-diagnostic.  |
| 11    | IN3_D    | R    | 0h    | 0h = Current sink on IN3 is operational.<br>1h = Current sink on IN3 is abnormal.   |
| 10    | IN2_D    | R    | 0h    | 0h = Current sink on IN2 is operational.<br>1h = Current sink on IN2 is abnormal.   |
| 9     | IN1_D    | R    | 0h    | 0h = Current source on IN1 is operational.<br>1h = Current source on IN1 is abnormal.   |
| 8     | IN0_D    | R    | 0h    | 0h = Current source on IN0 is operational.<br>1h = Current source on IN0 is abnormal.   |
| 7-6   | VS1_STAT | R    | 0h    | 0h = $V_S$ voltage is below threshold VS1_THRES2A.<br>1h = $V_S$ voltage is below threshold VS1_THRES2B and equal to or above threshold VS1_THRES2A.<br>2h = $V_S$ voltage is equal to or above threshold VS1_THRES2B.<br>3h = N/A. |
| 5-4   | VS0_STAT | R    | 0h    | 0h = $V_S$ voltage is below threshold VS0_THRES2A.<br>1h = $V_S$ voltage is below threshold VS0_THRES2B and equal to or above threshold VS0_THRES2A.<br>2h = $V_S$ voltage is equal to or above threshold VS0_THRES2B.<br>3h = N/A  |
| 3     | UV_STAT  | R    | 0h    | 0h = $V_S$ voltage is above the under-voltage condition threshold.<br>1h = $V_S$ voltage is below the under-voltage condition threshold.  |
| 2     | OV_STAT  | R    | 0h    | 0h = $V_S$ voltage is below the over-voltage condition threshold.<br>1h = $V_S$ voltage is above the over-voltage condition threshold.  |
| 1     | TW_STAT  | R    | 0h    | 0h = Device junction temperature is below the temperature warning threshold $T_{TW}$ .<br>1h = Device junction temperature is above the temperature warning threshold $T_{TW}$ .  |

表 8-15. IN\_STAT\_MISC Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 0   | TSD_STAT | R    | 0h    | 0h = Device junction temperature is below the temperature shutdown threshold $T_{TSD}$ .<br>1h = Device junction temperature is above the temperature shutdown threshold $T_{TSD}$ . |

### 8.6.5 IN\_STAT\_COMP Register (Offset = 5h) [Reset = 0h]

IN\_STAT\_COMP is shown in 图 8-28 and described in 表 8-16.

Return to [Summary Table](#).

This register indicates whether an input is below or above the comparator threshold when it is configured as comparator input mode.

**图 8-28. IN\_STAT\_COMP Register**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     |
| INC_23 | INC_22 | INC_21 | INC_20 | INC_19 | INC_18 | INC_17 | INC_16 |
| R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   |
| 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
| INC_15 | INC_14 | INC_13 | INC_12 | INC_11 | INC_10 | INC_9  | INC_8  |
| R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   |
| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| INC_7  | INC_6  | INC_5  | INC_4  | INC_3  | INC_2  | INC_1  | INC_0  |
| R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   | R-0h   |

LEGEND: R = Read only

**表 8-16. IN\_STAT\_COMP Register Field Descriptions**

| Bit | Field  | Type | Reset | Description  |
|-----|--------|------|-------|--|
| 23  | INC_23 | R    | 0h    | 0h = Input IN23 is below the comparator threshold.<br>1h = Input IN23 is above the comparator threshold. |
| 22  | INC_22 | R    | 0h    | 0h = Input IN22 is below the comparator threshold.<br>1h = Input IN22 is above the comparator threshold. |
| 21  | INC_21 | R    | 0h    | 0h = Input IN21 is below the comparator threshold.<br>1h = Input IN21 is above the comparator threshold. |
| 20  | INC_20 | R    | 0h    | 0h = Input IN20 is below the comparator threshold.<br>1h = Input IN20 is above the comparator threshold. |
| 19  | INC_19 | R    | 0h    | 0h = Input IN19 is below the comparator threshold<br>1h = Input IN19 is above the comparator threshold   |
| 18  | INC_18 | R    | 0h    | 0h = Input IN18 is below the comparator threshold<br>1h = Input IN18 is above the comparator threshold   |
| 17  | INC_17 | R    | 0h    | 0h = Input IN17 is below the comparator threshold<br>1h = Input IN17 is above the comparator threshold   |
| 16  | INC_16 | R    | 0h    | 0h = Input IN16 is below the comparator threshold<br>1h = Input IN16 is above the comparator threshold   |
| 15  | INC_15 | R    | 0h    | 0h = Input IN15 is below the comparator threshold<br>1h = Input IN15 is above the comparator threshold   |
| 14  | INC_14 | R    | 0h    | 0h = Input IN14 is below the comparator threshold<br>1h = Input IN14 is above the comparator threshold   |
| 13  | INC_13 | R    | 0h    | 0h = Input IN13 is below the comparator threshold<br>1h = Input IN13 is above the comparator threshold   |
| 12  | INC_12 | R    | 0h    | 0h = Input IN12 is below the comparator threshold<br>1h = Input IN12 is above the comparator threshold   |
| 11  | INC_11 | R    | 0h    | 0h = Input IN11 is below the comparator threshold<br>1h = Input IN11 is above the comparator threshold   |

表 8-16. IN\_STAT\_COMP Register Field Descriptions (continued)

| Bit | Field  | Type | Reset | Description  |
|-----|--------|------|-------|--|
| 10  | INC_10 | R    | 0h    | 0h = Input IN10 is below the comparator threshold<br>1h = Input IN10 is above the comparator threshold |
| 9   | INC_9  | R    | 0h    | 0h = Input IN9 is below the comparator threshold<br>1h = Input IN9 is above the comparator threshold   |
| 8   | INC_8  | R    | 0h    | 0h = Input IN8 is below the comparator threshold<br>1h = Input IN8 is above the comparator threshold   |
| 7   | INC_7  | R    | 0h    | 0h = Input IN7 is below the comparator threshold<br>1h = Input IN7 is above the comparator threshold   |
| 6   | INC_6  | R    | 0h    | 0h = Input IN6 is below the comparator threshold<br>1h = Input IN6 is above the comparator threshold   |
| 5   | INC_5  | R    | 0h    | 0h = Input IN5 is below the comparator threshold<br>1h = Input IN5 is above the comparator threshold   |
| 4   | INC_4  | R    | 0h    | 0h = Input IN4 is below the comparator threshold<br>1h = Input IN4 is above the comparator threshold   |
| 3   | INC_3  | R    | 0h    | 0h = Input IN3 is below the comparator threshold<br>1h = Input IN3 is above the comparator threshold   |
| 2   | INC_2  | R    | 0h    | 0h = Input IN2 is below the comparator threshold<br>1h = Input IN2 is above the comparator threshold   |
| 1   | INC_1  | R    | 0h    | 0h = Input IN1 is below the comparator threshold<br>1h = Input IN1 is above the comparator threshold   |
| 0   | INC_0  | R    | 0h    | 0h = Input IN0 is below the comparator threshold<br>1h = Input IN0 is above the comparator threshold   |

### 8.6.6 IN\_STAT\_ADC0 Register (Offset = 6h) [Reset = 0h]

IN\_STAT\_ADC0 is shown in [图 8-29](#) and described in [表 8-17](#).

Return to [Summary Table](#).

This register indicates whether an input is below or above the programmed threshold (for IN0-IN11) when it is configured as ADC input mode. For IN12-IN17, there are 2 thresholds and the register bits indicate whether the input is below, above or in-between the 2 thresholds.

**图 8-29. IN\_STAT\_ADC0 Register**

| 23     | 22    | 21     | 20    | 19     | 18     | 17     | 16    |
|--------|-------|--------|-------|--------|--------|--------|-------|
| INA_17 |       | INA_16 |       | INA_15 |        | INA_14 |       |
| R-0h   |       | R-0h   |       | R-0h   |        | R-0h   |       |
| 15     | 14    | 13     | 12    | 11     | 10     | 9      | 8     |
| INA_13 |       | INA_12 |       | INA_11 | INA_10 | INA_9  | INA_8 |
| R-0h   |       | R-0h   |       | R-0h   | R-0h   | R-0h   | R-0h  |
| 7      | 6     | 5      | 4     | 3      | 2      | 1      | 0     |
| INA_7  | INA_6 | INA_5  | INA_4 | INA_3  | INA_2  | INA_1  | INA_0 |
| R-0h   | R-0h  | R-0h   | R-0h  | R-0h   | R-0h   | R-0h   | R-0h  |

LEGEND: R = Read only

**表 8-17. IN\_STAT\_ADC0 Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description  |
|-------|--------|------|-------|--|
| 23-22 | INA_17 | R    | 0h    | 0h = Input IN17 is below threshold 2A<br>1h = Input IN17 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN17 is equal to or above threshold 2B<br>3h = N/A |
| 21-20 | INA_16 | R    | 0h    | 0h = Input IN16 is below threshold 2A<br>1h = Input IN16 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN16 is equal to or above threshold 2B<br>3h = N/A |
| 19-18 | INA_15 | R    | 0h    | 0h = Input IN15 is below threshold 2A<br>1h = Input IN15 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN15 is equal to or above threshold 2B<br>3h = N/A |
| 17-16 | INA_14 | R    | 0h    | 0h = Input IN14 is below threshold 2A<br>1h = Input IN14 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN14 is equal to or above threshold 2B<br>3h = N/A |
| 15-14 | INA_13 | R    | 0h    | 0h = Input IN13 is below threshold 2A<br>1h = Input IN13 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN13 is equal to or above threshold 2B<br>3h = N/A |

表 8-17. IN\_STAT\_ADC0 Register Field Descriptions (continued)

| Bit   | Field  | Type | Reset | Description  |
|-------|--------|------|-------|--|
| 13-12 | INA_12 | R    | 0h    | 0h = Input IN12 is below threshold 2A<br>1h = Input IN12 is below threshold 2B and equal to or above threshold 2A<br>2h = Input IN12 is equal to or above threshold 2B<br>3h = N/A |
| 11    | INA_11 | R    | 0h    | 0h = Input IN11 is below configured threshold<br>1h = Input IN11 is above configured threshold   |
| 10    | INA_10 | R    | 0h    | 0h = Input IN10 is below configured threshold<br>1h = Input IN10 is above configured threshold   |
| 9     | INA_9  | R    | 0h    | 0h = Input IN9 is below configured threshold<br>1h = Input IN9 is above configured threshold   |
| 8     | INA_8  | R    | 0h    | 0h = Input IN8 is below configured threshold<br>1h = Input IN8 is above configured threshold   |
| 7     | INA_7  | R    | 0h    | 0h = Input IN7 is below configured threshold<br>1h = Input IN7 is above configured threshold   |
| 6     | INA_6  | R    | 0h    | 0h = Input IN6 is below configured threshold<br>1h = Input IN6 is above configured threshold   |
| 5     | INA_5  | R    | 0h    | 0h = Input IN5 is below configured threshold<br>1h = Input IN5 is above configured threshold   |
| 4     | INA_4  | R    | 0h    | 0h = Input IN4 is below configured threshold<br>1h = Input IN4 is above configured threshold   |
| 3     | INA_3  | R    | 0h    | 0h = Input IN3 is below configured threshold<br>1h = Input IN3 is above configured threshold   |
| 2     | INA_2  | R    | 0h    | 0h = Input IN2 is below configured threshold<br>1h = Input IN2 is above configured threshold   |
| 1     | INA_1  | R    | 0h    | 0h = Input IN1 is below configured threshold<br>1h = Input IN1 is above configured threshold   |
| 0     | INA_0  | R    | 0h    | 0h = Input IN0 is below configured threshold<br>1h = Input IN0 is above configured threshold   |



### 8.6.7 IN\_STAT\_ADC1 Register (Offset = 7h) [Reset = 0h]

IN\_STAT\_ADC1 is shown in [图 8-30](#) and described in [表 8-18](#).

Return to [Summary Table](#).

This register indicates whether an input is above or below the programmed thresholds 3A, 3B, and 3C when it is configured as ADC input mode. For IN23, there are 5 thresholds that can be programmed.

**图 8-30. IN\_STAT\_ADC1 Register**

|          |    |        |    |        |    |        |    |        |    |        |        |
|----------|----|--------|----|--------|----|--------|----|--------|----|--------|--------|
| 23       | 22 | 21     | 20 | 19     | 18 | 17     | 16 | 15     | 14 | 13     | 12     |
| RESERVED |    |        |    |        |    |        |    |        |    |        | INA_23 |
| R-0h     |    |        |    |        |    |        |    |        |    |        | R-0h   |
| 11       | 10 | 9      | 8  | 7      | 6  | 5      | 4  | 3      | 2  | 1      | 0      |
| INA_23   |    | INA_22 |    | INA_21 |    | INA_20 |    | INA_19 |    | INA_18 |        |
| R-0h     |    | R-0h   |    | R-0h   |    | R-0h   |    | R-0h   |    | R-0h   |        |

LEGEND: R = Read only

**表 8-18. IN\_STAT\_ADC1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-13 | RESERVED | R    | 0h    | Reserved   |
| 12-10 | INA_23   | R    | 0h    | 0h = Input IN23 is below threshold 3A<br>1h = Input IN23 is below threshold 3B and equal to or above threshold 3A<br>2h = Input IN23 is below threshold 3C and equal to or above threshold 3B<br>3h = Input IN23 is below threshold THRES8 and equal to or above threshold 3C<br>4h = Input IN23 is below threshold THRES9 and equal to or above threshold THRES8<br>5h = Input IN23 is equal to or above threshold THRES9 |
| 9-8   | INA_22   | R    | 0h    | 0h = Input IN22 is below threshold 3A<br>1h = Input IN22 is below threshold 3B and equal to or above threshold 3A<br>2h = Input IN22 is below threshold 3C and equal to or above threshold 3B<br>3h = Input IN22 is equal to or above threshold 3C   |
| 7-6   | INA_21   | R    | 0h    | 0h = Input IN21 is below threshold 3A<br>1h = Input IN21 is below threshold 3B and equal to or above threshold 3A<br>2h = Input IN21 is below threshold 3C and equal to or above threshold 3B<br>3h = Input IN21 is equal to or above threshold 3C   |
| 5-4   | INA_20   | R    | 0h    | 0h = Input IN20 is below threshold 3A<br>1h = Input IN20 is below threshold 3B and equal to or above threshold 3A<br>2h = Input IN20 is below threshold 3C and equal to or above threshold 3B<br>3h = Input IN20 is equal to or above threshold 3C   |

表 8-18. IN\_STAT\_ADC1 Register Field Descriptions (continued)

| Bit | Field  | Type | Reset | Description  |
|-----|--------|------|-------|--|
| 3-2 | INA_19 | R    | 0h    | 0h = Input IN19 is below threshold 3A<br>1h = Input IN19 is below threshold 3B and equal to or above threshold 3A<br>2h = Input IN19 is below threshold 3C and equal to or above threshold 3B<br>3h = Input IN19 is equal to or above threshold 3C             |
| 1-0 | INA_18 | R    | 0h    | 0h = Input is IN18 is below threshold 3A<br>1h = Input is IN18 is below threshold 3B and equal to or above threshold 3A<br>2h = Input is IN18 is below threshold 3C and equal to or above threshold 3B<br>3h = Input is IN18 is equal to or above threshold 3C |

### 8.6.8 IN\_STAT\_MATRIX0 Register (Offset = 8h) [Reset = 0h]

IN\_STAT\_MATRIX0 is shown in 图 8-31 and described in 表 8-19.

Return to [Summary Table](#).

This register indicates whether an input is below or above the programmed threshold in the matrix polling mode for switches connected to IN10-IN13.

**图 8-31. IN\_STAT\_MATRIX0 Register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 23           | 22           | 21           | 20           | 19           | 18           | 17           | 16           |
| INMAT_13_IN9 | INMAT_13_IN8 | INMAT_13_IN7 | INMAT_13_IN6 | INMAT_13_IN5 | INMAT_13_IN4 | INMAT_12_IN9 | INMAT_12_IN8 |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |
| 15           | 14           | 13           | 12           | 11           | 10           | 9            | 8            |
| INMAT_12_IN7 | INMAT_12_IN6 | INMAT_12_IN5 | INMAT_12_IN4 | INMAT_11_IN9 | INMAT_11_IN8 | INMAT_11_IN7 | INMAT_11_IN6 |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| INMAT_11_IN5 | INMAT_11_IN4 | INMAT_10_IN9 | INMAT_10_IN8 | INMAT_10_IN7 | INMAT_10_IN6 | INMAT_10_IN5 | INMAT_10_IN4 |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |

LEGEND: R = Read only

**表 8-19. IN\_STAT\_MATRIX0 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 23  | INMAT_13_IN9 | R    | 0h    | 0h = Input IN13 is below threshold while IN9 pulled to GND<br>1h = Input IN13 is above threshold while IN9 pulled to GND   |
| 22  | INMAT_13_IN8 | R    | 0h    | 0h = Input IN13 is below threshold while IN8 pulled to GND<br>1h = Input IN13 is above threshold while IN8 pulled to GND   |
| 21  | INMAT_13_IN7 | R    | 0h    | 0h = Input IN13 is below threshold while IN7 pulled to GND<br>1h = Input IN13 is above threshold while IN7 pulled to GND   |
| 20  | INMAT_13_IN6 | R    | 0h    | 0h = Input IN13 is below threshold while IN6 pulled to GND<br>1h = Input IN13 is above threshold while IN6 pulled to GND   |
| 19  | INMAT_13_IN5 | R    | 0h    | 0h = Input IN13 is below threshold while IN5 pulled to GND<br>1h = Input IN13 is above threshold while IN5 pulled to GND   |
| 18  | INMAT_13_IN4 | R    | 0h    | 0h = Input IN13 is below threshold while IN4 pulled to GND<br>1h = Input IN13 is above threshold while IN4 pulled to GND   |
| 17  | INMAT_12_IN9 | R    | 0h    | 0h = Input IN12 is below threshold while IN9 pulled to GND<br>1h = Input IN12 is above threshold while IN9 pulled to GND   |
| 16  | INMAT_12_IN8 | R    | 0h    | 0h = Input IN12 is below threshold while IN8 pulled to GND.<br>1h = Input IN12 is above threshold while IN8 pulled to GND. |
| 15  | INMAT_12_IN7 | R    | 0h    | 0h = Input IN12 is below threshold while IN7 pulled to GND.<br>1h = Input IN12 is above threshold while IN7 pulled to GND. |
| 14  | INMAT_12_IN6 | R    | 0h    | 0h = Input IN12 is below threshold while IN6 pulled to GND.<br>1h = Input IN12 is above threshold while IN6 pulled to GND. |
| 13  | INMAT_12_IN5 | R    | 0h    | 0h = Input IN12 is below threshold while IN5 pulled to GND.<br>1h = Input IN12 is above threshold while IN5 pulled to GND. |
| 12  | INMAT_12_IN4 | R    | 0h    | 0h = Input IN12 is below threshold while IN4 pulled to GND.<br>1h = Input IN12 is above threshold while IN4 pulled to GND. |
| 11  | INMAT_11_IN9 | R    | 0h    | 0h = Input IN11 is below threshold while IN9 pulled to GND.<br>1h = Input IN11 is above threshold while IN9 pulled to GND. |

表 8-19. IN\_STAT\_MATRIX0 Register Field Descriptions (continued)

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 10  | INMAT_11_IN8 | R    | 0h    | 0h = Input IN11 is below threshold while IN8 pulled to GND.<br>1h = Input IN11 is above threshold while IN8 pulled to GND. |
| 9   | INMAT_11_IN7 | R    | 0h    | 0h = Input IN11 is below threshold while IN7 pulled to GND.<br>1h = Input IN11 is above threshold while IN7 pulled to GND. |
| 8   | INMAT_11_IN6 | R    | 0h    | 0h = Input IN11 is below threshold while IN6 pulled to GND.<br>1h = Input IN11 is above threshold while IN6 pulled to GND. |
| 7   | INMAT_11_IN5 | R    | 0h    | 0h = Input IN11 is below threshold while IN5 pulled to GND.<br>1h = Input IN11 is above threshold while IN5 pulled to GND. |
| 6   | INMAT_11_IN4 | R    | 0h    | 0h = Input IN11 is below threshold while IN4 pulled to GND.<br>1h = Input IN11 is above threshold while IN4 pulled to GND. |
| 5   | INMAT_10_IN9 | R    | 0h    | 0h = Input IN10 is below threshold while IN9 pulled to GND.<br>1h = Input IN10 is above threshold while IN9 pulled to GND. |
| 4   | INMAT_10_IN8 | R    | 0h    | 0h = Input IN10 is below threshold while IN8 pulled to GND.<br>1h = Input IN10 is above threshold while IN8 pulled to GND. |
| 3   | INMAT_10_IN7 | R    | 0h    | 0h = Input IN10 is below threshold while IN7 pulled to GND.<br>1h = Input IN10 is above threshold while IN7 pulled to GND. |
| 2   | INMAT_10_IN6 | R    | 0h    | 0h = Input IN10 is below threshold while IN6 pulled to GND.<br>1h = Input IN10 is above threshold while IN6 pulled to GND. |
| 1   | INMAT_10_IN5 | R    | 0h    | 0h = Input IN10 is below threshold while IN5 pulled to GND.<br>1h = Input IN10 is above threshold while IN5 pulled to GND. |
| 0   | INMAT_10_IN4 | R    | 0h    | 0h = Input IN10 is below threshold while IN4 pulled to GND.<br>1h = Input IN10 is above threshold while IN4 pulled to GND. |

### 8.6.9 IN\_STAT\_MATRIX1 Register (Offset = 9h) [Reset = 0h]

IN\_STAT\_MATRIX1 is shown in 图 8-32 and described in 表 8-20.

Return to [Summary Table](#).

This register indicates whether an input is below or above the programmed threshold in the matrix polling mode for switches connected to IN14-IN15. This register also indicates the status of IN0-IN11 with respect to the common threshold THRES\_COM.

**图 8-32. IN\_STAT\_MATRIX1 Register**

| 23           | 22           | 21           | 20           | 19           | 18           | 17           | 16           |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| IN11_COM     | IN10_COM     | IN9_COM      | IN8_COM      | IN7_COM      | IN6_COM      | IN5_COM      | IN4_COM      |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |
| 15           | 14           | 13           | 12           | 11           | 10           | 9            | 8            |
| IN3_COM      | IN2_COM      | IN1_COM      | IN0_COM      | INMAT_15_IN9 | INMAT_15_IN8 | INMAT_15_IN7 | INMAT_15_IN6 |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| INMAT_15_IN5 | INMAT_15_IN4 | INMAT_14_IN9 | INMAT_14_IN8 | INMAT_14_IN7 | INMAT_14_IN6 | INMAT_14_IN5 | INMAT_14_IN4 |
| R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         | R-0h         |

LEGEND: R = Read only

**表 8-20. IN\_STAT\_MATRIX1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 23  | IN11_COM | R    | 0h    | 0h = Input IN11 below threshold THRES_COM<br>1h = Input IN11 equal to or above threshold THRES_COM |
| 22  | IN10_COM | R    | 0h    | 0h = Input IN10 below threshold THRES_COM<br>1h = Input IN10 equal to or above threshold THRES_COM |
| 21  | IN9_COM  | R    | 0h    | 0h = Input IN9 below threshold THRES_COM<br>1h = Input IN9 equal to or above threshold THRES_COM   |
| 20  | IN8_COM  | R    | 0h    | 0h = Input IN8 below threshold THRES_COM<br>1h = Input IN8 equal to or above threshold THRES_COM   |
| 19  | IN7_COM  | R    | 0h    | 0h = Input IN7 below threshold THRES_COM<br>1h = Input IN7 equal to or above threshold THRES_COM   |
| 18  | IN6_COM  | R    | 0h    | 0h = Input IN6 below threshold THRES_COM<br>1h = Input IN6 equal to or above threshold THRES_COM   |
| 17  | IN5_COM  | R    | 0h    | 0h = Input IN5 below threshold THRES_COM<br>1h = Input IN5 equal to or above threshold THRES_COM   |
| 16  | IN4_COM  | R    | 0h    | 0h = Input IN4 below threshold THRES_COM<br>1h = Input IN4 equal to or above threshold THRES_COM   |
| 15  | IN3_COM  | R    | 0h    | 0h = Input IN3 below threshold THRES_COM<br>1h = Input IN3 equal to or above threshold THRES_COM   |
| 14  | IN2_COM  | R    | 0h    | 0h = Input IN2 below threshold THRES_COM<br>1h = Input IN2 equal to or above threshold THRES_COM   |
| 13  | IN1_COM  | R    | 0h    | 0h = Input IN1 below threshold THRES_COM<br>1h = Input IN1 equal to or above threshold THRES_COM   |
| 12  | IN0_COM  | R    | 0h    | 0h = Input IN0 below threshold THRES_COM<br>1h = Input IN0 equal to or above threshold THRES_COM   |

表 8-20. IN\_STAT\_MATRIX1 Register Field Descriptions (continued)

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 11  | INMAT_15_IN9 | R    | 0h    | 0h = Input IN15 below threshold while IN9 pulled to GND<br>1h = Input IN15 above threshold while IN9 pulled to GND |
| 10  | INMAT_15_IN8 | R    | 0h    | 0h = Input IN15 below threshold while IN8 pulled to GND<br>1h = Input IN15 above threshold while IN8 pulled to GND |
| 9   | INMAT_15_IN7 | R    | 0h    | 0h = Input IN15 below threshold while IN7 pulled to GND<br>1h = Input IN15 above threshold while IN7 pulled to GND |
| 8   | INMAT_15_IN6 | R    | 0h    | 0h = Input IN15 below threshold while IN6 pulled to GND<br>1h = Input IN15 above threshold while IN6 pulled to GND |
| 7   | INMAT_15_IN5 | R    | 0h    | 0h = Input IN15 below threshold while IN5 pulled to GND<br>1h = Input IN15 above threshold while IN5 pulled to GND |
| 6   | INMAT_15_IN4 | R    | 0h    | 0h = Input IN15 below threshold while IN4 pulled to GND<br>1h = Input IN15 above threshold while IN4 pulled to GND |
| 5   | INMAT_14_IN9 | R    | 0h    | 0h = Input IN14 below threshold while IN9 pulled to GND<br>1h = Input IN14 above threshold while IN9 pulled to GND |
| 4   | INMAT_14_IN8 | R    | 0h    | 0h = Input IN14 below threshold while IN8 pulled to GND<br>1h = Input IN14 above threshold while IN8 pulled to GND |
| 3   | INMAT_14_IN7 | R    | 0h    | 0h = Input IN14 below threshold while IN7 pulled to GND<br>1h = Input IN14 above threshold while IN7 pulled to GND |
| 2   | INMAT_14_IN6 | R    | 0h    | 0h = Input IN14 below threshold while IN6 pulled to GND<br>1h = Input IN14 above threshold while IN6 pulled to GND |
| 1   | INMAT_14_IN5 | R    | 0h    | 0h = Input IN14 below threshold while IN5 pulled to GND<br>1h = Input IN14 above threshold while IN5 pulled to GND |
| 0   | INMAT_14_IN4 | R    | 0h    | 0h = Input IN14 below threshold while IN4 pulled to GND<br>1h = Input IN14 above threshold while IN4 pulled to GND |

### 8.6.10 ANA\_STAT0 Register (Offset = Ah) [Reset = 0h]

ANA\_STAT0 is shown in 图 8-33 and described in 表 8-21.

Return to [Summary Table](#).

**图 8-33. ANA\_STAT0 Register**

|          |    |    |    |         |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|---------|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN1_ANA |    |    |    |    |    |    |    |    |    | IN0_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h    |    |    |    |    |    |    |    |    |    | R-0h    |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-21. ANA\_STAT0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-20 | RESERVED | R    | 0h    | Reserved   |
| 19-10 | IN1_ANA  | R    | 0h    | 10-bits value of IN1<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN0_ANA  | R    | 0h    | 10-bits value of IN0<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.11 ANA\_STAT1 Register (Offset = Bh) [Reset = 0h]

ANA\_STAT1 is shown in 图 8-34 and described in 表 8-22.

Return to [Summary Table](#).

**图 8-34. ANA\_STAT1 Register**

|          |    |    |    |         |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|---------|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN5_ANA |    |    |    |    |    |    |    |    |    | IN4_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h    |    |    |    |    |    |    |    |    |    | R-0h    |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-22. ANA\_STAT1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-20 | RESERVED | R    | 0h    | Reserved   |
| 19-10 | IN3_ANA  | R    | 0h    | 10-bits value of IN3<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN2_ANA  | R    | 0h    | 10-bits value of IN2<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.12 ANA\_STAT2 Register (Offset = Ch) [Reset = 0h]

ANA\_STAT2 is shown in 图 8-35 and described in 表 8-23.

Return to [Summary Table](#).

图 8-35. ANA\_STAT2 Register

|          |    |    |    |         |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|---------|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN5_ANA |    |    |    |    |    |    |    |    |    | IN4_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h    |    |    |    |    |    |    |    |    |    | R-0h    |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-23. ANA\_STAT2 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-20 | RESERVED | R    | 0h    | Reserved   |
| 19-10 | IN5_ANA  | R    | 0h    | 10-bits value of IN5<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN4_ANA  | R    | 0h    | 10-bits value of IN4<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.13 ANA\_STAT3 Register (Offset = Dh) [Reset = 0h]

ANA\_STAT3 is shown in 图 8-36 and described in 表 8-24.

Return to [Summary Table](#).

图 8-36. ANA\_STAT3 Register

|          |    |    |    |         |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|---------|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN7_ANA |    |    |    |    |    |    |    |    |    | IN6_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h    |    |    |    |    |    |    |    |    |    | R-0h    |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-24. ANA\_STAT3 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-20 | RESERVED | R    | 0h    | Reserved   |
| 19-10 | IN7_ANA  | R    | 0h    | 10-bits value of IN7<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN6_ANA  | R    | 0h    | 10-bits value of IN6<br>Bit 0: LSB<br>Bit 9: MSB   |



### 8.6.14 ANA\_STAT4 Register (Offset = Eh) [Reset = 0h]

ANA\_STAT4 is shown in 图 8-37 and described in 表 8-25.

Return to [Summary Table](#).

**图 8-37. ANA\_STAT4 Register**

|          |    |    |    |         |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|---------|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN9_ANA |    |    |    |    |    |    |    |    |    | IN8_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h    |    |    |    |    |    |    |    |    |    | R-0h    |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-25. ANA\_STAT4 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-20 | RESERVED | R    | 0h    | Reserved   |
| 19-10 | IN9_ANA  | R    | 0h    | 10-bits value of IN9<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN8_ANA  | R    | 0h    | 10-bits value of IN8<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.15 ANA\_STAT5 Register (Offset = Fh) [Reset = 0h]

ANA\_STAT5 is shown in 图 8-38 and described in 表 8-26.

Return to [Summary Table](#).

**图 8-38. ANA\_STAT5 Register**

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN11_ANA |    |    |    |    |    |    |    |    |    | IN10_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-26. ANA\_STAT5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN11_ANA | R    | 0h    | 10-bits value of IN11<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN10_ANA | R    | 0h    | 10-bits value of IN10<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.16 ANA\_STAT6 Register (Offset = 10h) [reset = 0h]

ANA\_STAT6 is shown in 图 8-39 and described in 表 8-27.

Return to [Summary Table](#).

图 8-39. ANA\_STAT6 Register

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN13_ANA |    |    |    |    |    |    |    |    |    | IN12_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-27. ANA\_STAT6 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN13_ANA | R    | 0h    | 10-bits value of IN13<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN12_ANA | R    | 0h    | 10-bits value of IN12<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.17 ANA\_STAT7 Register (Offset = 11h) [Reset = 0h]

ANA\_STAT7 is shown in 图 8-40 and described in 表 8-28.

Return to [Summary Table](#).

图 8-40. ANA\_STAT7 Register

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN15_ANA |    |    |    |    |    |    |    |    |    | IN14_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-28. ANA\_STAT7 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN15_ANA | R    | 0h    | 10-bits value of IN15<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN14_ANA | R    | 0h    | 10-bits value of IN14<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.18 ANA\_STAT8 Register (Offset = 12h) [Reset = 0h]

ANA\_STAT8 is shown in 图 8-41 and described in 表 8-29.

Return to [Summary Table](#).

**图 8-41. ANA\_STAT8 Register**

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN17_ANA |    |    |    |    |    |    |    |    |    | IN16_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-29. ANA\_STAT8 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN17_ANA | R    | 0h    | 10-bits value of IN17<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN16_ANA | R    | 0h    | 10-bits value of IN16<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.19 ANA\_STAT9 Register (Offset = 13h) [Reset = 0h]

ANA\_STAT9 is shown in 图 8-42 and described in 表 8-30.

Return to [Summary Table](#).

**图 8-42. ANA\_STAT9 Register**

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN19_ANA |    |    |    |    |    |    |    |    |    | IN18_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-30. ANA\_STAT9 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN19_ANA | R    | 0h    | 10-bits value of IN19<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN18_ANA | R    | 0h    | 10-bits value of IN18<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.20 ANA\_STAT10 Register (Offset = 14h) [Reset = 0h]

ANA\_STAT10 is shown in 图 8-43 and described in 表 8-31.

Return to [Summary Table](#).

图 8-43. ANA\_STAT10 Register

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN21_ANA |    |    |    |    |    |    |    |    |    | IN20_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-31. ANA\_STAT10 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN21_ANA | R    | 0h    | 10-bits value of IN21<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN20_ANA | R    | 0h    | 10-bits value of IN20<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.21 ANA\_STAT11 Register (Offset = 15h) [Reset = 0h]

ANA\_STAT11 is shown in 图 8-44 and described in 表 8-32.

Return to [Summary Table](#).

图 8-44. ANA\_STAT11 Register

|          |    |    |    |          |    |    |    |    |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----------|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | IN23_ANA |    |    |    |    |    |    |    |    |    | IN22_ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h     |    |    |    |    |    |    |    |    |    | R-0h     |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

表 8-32. ANA\_STAT11 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | IN23_ANA | R    | 0h    | 10-bits value of IN23<br>Bit 10: LSB<br>Bit 19: MSB |
| 9-0   | IN22_ANA | R    | 0h    | 10-bits value of IN22<br>Bit 0: LSB<br>Bit 9: MSB   |

### 8.6.22 ANA\_STAT12 Register (Offset = 16h) [Reset = 0h]

ANA\_STAT12 is shown in 图 8-45 and described in 表 8-33.

Return to [Summary Table](#).

**图 8-45. ANA\_STAT12 Register**

|          |    |    |    |              |    |    |    |    |    |    |    |    |    |                     |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|--------------|----|----|----|----|----|----|----|----|----|---------------------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19           | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9                   | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | ADC_SELF_ANA |    |    |    |    |    |    |    |    |    | V <sub>S</sub> _ANA |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h         |    |    |    |    |    |    |    |    |    | R-0h                |   |   |   |   |   |   |   |   |   |

LEGEND: R = Read only

**表 8-33. ANA\_STAT12 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description   |
|-------|---------------------|------|-------|---|
| 23-20 | RESERVED            | R    | 0h    | Reserved  |
| 19-10 | ADC_SELF_ANA        | R    | 0h    | 10-bits value of the ADC self-diagnosis<br>Bit 10: LSB<br>Bit 19: MSB   |
| 9-0   | V <sub>S</sub> _ANA | R    | 0h    | 10-bits value of V <sub>S</sub> measurement<br>Bit 0: LSB<br>Bit 9: MSB |

### 8.6.23 CONFIG Register (Offset = 1Ah) [Reset = 0h]

CONFIG is shown in 图 8-46 and described in 表 8-34.

Return to [Summary Table](#).

图 8-46. CONFIG Register

| 23            | 22         | 21             | 20           | 19           | 18           | 17         | 16             |
|---------------|------------|----------------|--------------|--------------|--------------|------------|----------------|
| VS_RATIO      | ADC_DIAG_T | WET_D_IN3_EN   | WET_D_IN2_EN | WET_D_IN1_EN | WET_D_IN0_EN | VS_MEAS_EN | TW_CUR_DIS_CSI |
| R/W-0h        | R/W-0h     | R/W-0h         | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h     | R/W-0h         |
| 15            | 14         | 13             | 12           | 11           | 10           | 9          | 8              |
| DET_FILTER    |            | TW_CUR_DIS_CSO | INT_CONFIG   | TRIGGER      | POLL_EN      | CRC_T      | POLL_ACT_TIME  |
| R/W-0h        |            | R/W-0h         | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h     | R/W-0h         |
| 7             | 6          | 5              | 4            | 3            | 2            | 1          | 0              |
| POLL_ACT_TIME |            |                |              | POLL_TIME    |              |            | RESET          |
| R/W-0h        |            |                |              | R/W-0h       |              |            | R/W-0h         |

LEGEND: R/W = Read/Write

表 8-34. CONFIG Register Field Descriptions

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 23    | VS_RATIO       | R/W  | 0h    | 0h = Use voltage divider factor of 3 for the $V_S$ measurement<br>1h = Use voltage divider factor of 10 for the $V_S$ measurement  |
| 22    | ADC_DIAG_T     | R/W  | 0h    | For detailed descriptions for the ADC self-diagnostic feature, refer to section <a href="#">ADC Self-Diagnostic</a><br>0h = Disable ADC self-diagnostic feature<br>1h = Enable ADC self-diagnostic feature   |
| 21    | WET_D_IN3_EN   | R/W  | 0h    | 0h = Disable wetting current diagnostic for input IN3<br>1h = Enable wetting current diagnostic for input IN3  |
| 20    | WET_D_IN2_EN   | R/W  | 0h    | 0h = Disable wetting current diagnostic for input IN2<br>1h = Enable wetting current diagnostic for input IN2  |
| 19    | WET_D_IN1_EN   | R/W  | 0h    | 0h = Disable wetting current diagnostic for input IN1<br>1h = Enable wetting current diagnostic for input IN1  |
| 18    | WET_D_IN0_EN   | R/W  | 0h    | 0h = Disable wetting current diagnostic for input IN0<br>1h = Enable wetting current diagnostic for input IN0  |
| 17    | VS_MEAS_EN     | R/W  | 0h    | For detailed descriptions for the $V_S$ measurement, refer to section <a href="#">VS Measurement</a> .<br>0h = Disable $V_S$ measurement at the end of every polling cycle<br>1h = Enable $V_S$ measurement at the end of every polling cycle  |
| 16    | TW_CUR_DIS_CSI | R/W  | 0h    | 0h = Enable wetting current reduction (to 2 mA) for 10 mA and 15 mA settings upon TW event for all inputs enabled with CSI.<br>1h = Disable wetting current reduction (to 2 mA) for 10 mA and 15 mA settings upon TW event for all inputs enabled with CSI.  |
| 15-14 | DET_FILTER     | R/W  | 0h    | For detailed descriptions for the detection filter, refer to section <a href="#">Detection Filter</a> .<br>0h = every sample is valid and taken for threshold evaluation<br>1h = 2 consecutive and equal samples required to be valid data<br>2h = 3 consecutive and equal samples required to be valid data<br>3h = 4 consecutive and equal samples required to be valid data |

表 8-34. CONFIG Register Field Descriptions (continued)

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 13  | TW_CUR_DIS_CSO | R/W  | 0h    | 0h = Enable wetting current reduction (to 2 mA) for 10 mA and 15 mA settings upon TW event for all inputs enabled with CSO.<br>1h = Disable wetting current reduction (to 2 mA) for 10 mA and 15 mA settings upon TW event for all inputs enabled with CSO.  |
| 12  | INT_CONFIG     | R/W  | 0h    | For detailed descriptions for the INT pin assertion scheme, refer to section <a href="#">Interrupt Generation and /INT Assertion</a> .<br>0h = INT pin assertion scheme set to static<br>1h = INT pin assertion scheme set to dynamic  |
| 11  | TRIGGER        | R/W  | 0h    | When the TRIGGER bit is set to logic 1, normal device operation (wetting current activation and polling) starts. To stop device operation and keep the device in an idle state, de-assert this bit to 0. After device normal operation is triggered, if at any time the device setting needs to be re-configured, the microcontroller is required to first set the bit TRIGGER to logic 0 to stop device operation. Once the re-configuration is completed, the microcontroller can set the TRIGGER bit back to logic 1 to re-start device operation. If re-configuration is done on the fly without first stopping the device operation, false switch status could be reported and accidental interrupt might be issued. The following register bits are the exception and can be configured when TRIGGER bit is set to logic 1: <ul style="list-style-type: none"> <li>• TRIGGER (bit 11 of the CONFIG register)</li> <li>• CRC_T (bit 9 of the CONFIG register)</li> <li>• RESET (bit 0 of the CONFIG register)</li> <li>• The CCP_CFG1 register</li> </ul> 0h = Stop TIC12400-Q1 from normal operation.<br>1h = Trigger TIC12400-Q1 from normal operation. |
| 10  | POLL_EN        | R/W  | 0h    | 0h = Polling disabled. Device operates in continuous mode.<br>1h = Polling enabled and the device operates in one of the polling modes.  |
| 9   | CRC_T          | R/W  | 0h    | Set this bit to 1 to trigger a CRC calculation on all the configuration register bits. Once triggered, it is strongly recommended the SPI controller does not change the content of the configuration registers until the CRC calculation is completed to avoid erroneous CRC calculation result. The TIC12400-Q1 sets the CRC_CALC interrupt bit and asserts the $\overline{\text{INT}}$ pin low when the CRC calculation is completed. The calculated result will be available in the CRC register. This bit self-clears back to 0 after CRC calculation is executed.<br>0h = no CRC calculation triggered.<br>1h = trigger CRC calculation.   |

表 8-34. CONFIG Register Field Descriptions (continued)

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 8-5 | POLL_ACT_TIME | R/W  | 0h    | 0h = 64 $\mu$ s<br>1h = 128 $\mu$ s<br>2h = 192 $\mu$ s<br>3h = 256 $\mu$ s<br>4h = 320 $\mu$ s<br>5h = 384 $\mu$ s<br>6h = 448 $\mu$ s<br>7h = 512 $\mu$ s<br>8h = 640 $\mu$ s<br>9h = 768 $\mu$ s<br>Ah = 896 $\mu$ s<br>Bh = 1024 $\mu$ s<br>Ch = 2048 $\mu$ s<br>Dh-15h = 512 $\mu$ s (most frequently-used setting) |
| 4-1 | POLL_TIME     | R/W  | 0h    | 0h = 2 ms<br>1h = 4 ms<br>2h = 8 ms<br>3h = 16 ms<br>4h = 32 ms<br>5h = 48 ms<br>6h = 64 ms<br>7h = 128 ms<br>8h = 256 ms<br>9h = 512 ms<br>Ah = 1024 ms<br>Bh = 2048 ms<br>Ch = 4096 ms<br>Dh-15h = 8 ms (most frequently-used setting)   |
| 0   | RESET         | R/W  | 0h    | 0h = No reset.<br>1h = Trigger software reset of the device.   |



### 8.6.24 IN\_EN Register (Offset = 1Bh) [Reset = 0h]

IN\_EN is shown in 图 8-47 and described in 表 8-35.

Return to [Summary Table](#).

**图 8-47. IN\_EN Register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
| IN_EN_23 | IN_EN_22 | IN_EN_21 | IN_EN_20 | IN_EN_19 | IN_EN_18 | IN_EN_17 | IN_EN_16 |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| IN_EN_15 | IN_EN_14 | IN_EN_13 | IN_EN_12 | IN_EN_11 | IN_EN_10 | IN_EN_9  | IN_EN_8  |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| IN_EN_7  | IN_EN_6  | IN_EN_5  | IN_EN_4  | IN_EN_3  | IN_EN_2  | IN_EN_1  | IN_EN_0  |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |

LEGEND: R/W = Read/Write

**表 8-35. IN\_EN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 23  | IN_EN_23 | R/W  | 0h    | 0h = Input channel IN23 disabled. Polling sequence skips this channel<br>1h = Input channel IN23 enabled. |
| 22  | IN_EN_22 | R/W  | 0h    | 0h = Input channel IN22 disabled. Polling sequence skips this channel<br>1h = Input channel IN22 enabled. |
| 21  | IN_EN_21 | R/W  | 0h    | 0h = Input channel IN21 disabled. Polling sequence skips this channel<br>1h = Input channel IN21 enabled. |
| 20  | IN_EN_20 | R/W  | 0h    | 0h = Input channel IN20 disabled. Polling sequence skips this channel<br>1h = Input channel IN20 enabled. |
| 19  | IN_EN_19 | R/W  | 0h    | 0h = Input channel IN19 disabled. Polling sequence skips this channel<br>1h = Input channel IN19 enabled. |
| 18  | IN_EN_18 | R/W  | 0h    | 0h = Input channel IN18 disabled. Polling sequence skips this channel<br>1h = Input channel IN18 enabled. |
| 17  | IN_EN_17 | R/W  | 0h    | 0h = Input channel IN17 disabled. Polling sequence skips this channel<br>1h = Input channel IN17 enabled. |
| 16  | IN_EN_16 | R/W  | 0h    | 0h = Input channel IN16 disabled. Polling sequence skips this channel<br>1h = Input channel IN16 enabled. |
| 15  | IN_EN_15 | R/W  | 0h    | 0h = Input channel IN15 disabled. Polling sequence skips this channel<br>1h = Input channel IN15 enabled. |

表 8-35. IN\_EN Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 14  | IN_EN_14 | R/W  | 0h    | 0h = Input channel IN14 disabled. Polling sequence skips this channel<br>1h = Input channel IN14 enabled. |
| 13  | IN_EN_13 | R/W  | 0h    | 0h = Input channel IN13 disabled. Polling sequence skips this channel<br>1h = Input channel IN13 enabled. |
| 12  | IN_EN_12 | R/W  | 0h    | 0h = Input channel IN12 disabled. Polling sequence skips this channel<br>1h = Input channel IN12 enabled. |
| 11  | IN_EN_11 | R/W  | 0h    | 0h = Input channel IN11 disabled. Polling sequence skips this channel<br>1h = Input channel IN11 enabled. |
| 10  | IN_EN_10 | R/W  | 0h    | 0h = Input channel IN10 disabled. Polling sequence skips this channel<br>1h = Input channel IN10 enabled. |
| 9   | IN_EN_9  | R/W  | 0h    | 0h = Input channel IN9 disabled. Polling sequence skips this channel<br>1h = Input channel IN9 enabled.   |
| 8   | IN_EN_8  | R/W  | 0h    | 0h = Input channel IN8 disabled. Polling sequence skips this channel<br>1h = Input channel IN8 enabled.   |
| 7   | IN_EN_7  | R/W  | 0h    | 0h = Input channel IN7 disabled. Polling sequence skips this channel<br>1h = Input channel IN7 enabled.   |
| 6   | IN_EN_6  | R/W  | 0h    | 0h = Input channel IN6 disabled. Polling sequence skips this channel<br>1h = Input channel IN6 enabled.   |
| 5   | IN_EN_5  | R/W  | 0h    | 0h = Input channel IN5 disabled. Polling sequence skips this channel<br>1h = Input channel IN5 enabled.   |
| 4   | IN_EN_4  | R/W  | 0h    | 0h = Input channel IN4 disabled. Polling sequence skips this channel<br>1h = Input channel IN4 enabled.   |
| 3   | IN_EN_3  | R/W  | 0h    | 0h = Input channel IN3 disabled. Polling sequence skips this channel<br>1h = Input channel IN3 enabled.   |
| 2   | IN_EN_2  | R/W  | 0h    | 0h = Input channel IN2 disabled. Polling sequence skips this channel<br>1h = Input channel IN2 enabled.   |
| 1   | IN_EN_1  | R/W  | 0h    | 0h = Input channel IN1 disabled. Polling sequence skips this channel<br>1h = Input channel IN1 enabled.   |
| 0   | IN_EN_0  | R/W  | 0h    | 0h = Input channel IN0 disabled. Polling sequence skips this channel<br>1h = Input channel IN0 enabled.   |

### 8.6.25 CS\_SELECT Register (Offset = 1Ch) [Reset = 0h]

CS\_SELECT is shown in 图 8-48 and described in 表 8-36.

Return to [Summary Table](#).

**图 8-48. CS\_SELECT Register**

|          |        |        |        |        |        |        |        |        |        |        |        |
|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 23       | 22     | 21     | 20     | 19     | 18     | 17     | 16     | 15     | 14     | 13     | 12     |
| RESERVED |        |        |        |        |        |        |        |        |        |        |        |
| R-0h     |        |        |        |        |        |        |        |        |        |        |        |
| 11       | 10     | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| RESERVED | CS_IN9 | CS_IN8 | CS_IN7 | CS_IN6 | CS_IN5 | CS_IN4 | CS_IN3 | CS_IN2 | CS_IN1 | CS_IN0 |        |
| R-0h     | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only

**表 8-36. CS\_SELECT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23-10 | RESERVED | R    | 0h    | Reserved   |
| 9     | CS_IN9   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 8     | CS_IN8   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 7     | CS_IN7   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 6     | CS_IN6   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 5     | CS_IN5   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 4     | CS_IN4   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 3     | CS_IN3   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 2     | CS_IN2   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 1     | CS_IN1   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 0     | CS_IN0   | R/W  | 0h    | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |

### 8.6.26 WC\_CFG0 Register (Offset = 1Dh) [Reset = 0h]

WC\_CFG0 is shown in 图 8-49 and described in 表 8-37.

Return to [Summary Table](#).

图 8-49. WC\_CFG0 Register

|         |    |    |    |         |    |    |    |            |    |    |    |
|---------|----|----|----|---------|----|----|----|------------|----|----|----|
| 23      | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15         | 14 | 13 | 12 |
| WC_IN11 |    |    |    | WC_IN10 |    |    |    | WC_IN8_IN9 |    |    |    |
| R/W-0h  |    |    |    | R/W-0h  |    |    |    | R/W-0h     |    |    |    |
| 11      | 10 | 9  | 8  | 7       | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| WC_IN5  |    |    |    | WC_IN4  |    |    |    | WC_IN2_IN3 |    |    |    |
| R/W-0h  |    |    |    | R/W-0h  |    |    |    | R/W-0h     |    |    |    |

LEGEND: R/W = Read/Write

表 8-37. WC\_CFG0 Register Field Descriptions

| Bit   | Field      | Type | Reset | Description   |
|-------|------------|------|-------|---|
| 23-21 | WC_IN11    | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 20-18 | WC_IN10    | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 17-15 | WC_IN8_IN9 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 14-12 | WC_IN6_IN7 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 11-9  | WC_IN5     | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |

**表 8-37. WC\_CFG0 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 8-6 | WC_IN4     | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 5-3 | WC_IN2_IN3 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 2-0 | WC_IN0_IN1 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |

### 8.6.27 WC\_CFG1 Register (Offset = 1Eh) [Reset = 0h]

WC\_CFG1 is shown in 图 8-50 and described in 表 8-38.

Return to [Summary Table](#).

图 8-50. WC\_CFG1 Register

| 23           | 22                 | 21                 | 20           | 19 | 18      | 17           | 16 | 15           | 14           | 13 | 12 |
|--------------|--------------------|--------------------|--------------|----|---------|--------------|----|--------------|--------------|----|----|
| RESERVED     | AUTO_SCALE_DIS_CSI | AUTO_SCALE_DIS_CSO | WC_IN23      |    | WC_IN22 |              |    | WC_IN20_IN21 |              |    |    |
| R-0h         | R/W-0h             | R/W-0h             | R/W-0h       |    | R/W-0h  |              |    | R/W-0h       |              |    |    |
| 11           | 10                 | 9                  | 8            | 7  | 6       | 5            | 4  | 3            | 2            | 1  | 0  |
| WC_IN18_IN19 |                    |                    | WC_IN16_IN17 |    |         | WC_IN14_IN15 |    |              | WC_IN12_IN13 |    |    |
| R/W-0h       |                    |                    | R/W-0h       |    |         | R/W-0h       |    |              | R/W-0h       |    |    |

LEGEND: R/W = Read/Write; R = Read only

表 8-38. WC\_CFG1 Register Field Descriptions

| Bit   | Field              | Type | Reset | Description  |
|-------|--------------------|------|-------|--|
| 23    | RESERVED           | R    | 0h    | Reserved   |
| 22    | AUTO_SCALE_DIS_CSI | R/W  | 0h    | 0h = Enable wetting current auto-scaling (to 2 mA) in continuous mode for 10 mA and 15 mA settings upon switch closure for all inputs enabled with CSI<br>1h = Disable wetting current auto-scaling (to 2 mA) in continuous mode for 10 mA and 15 mA settings upon switch closure for all inputs enabled with CS<br>For detailed descriptions for the wetting current auto-scaling, refer to section <a href="#">Wetting Current Auto-Scaling</a> .  |
| 21    | AUTO_SCALE_DIS_CSO | R/W  | 0h    | 0h = Enable wetting current auto-scaling (to 2 mA) in continuous mode for 10 mA and 15 mA settings upon switch closure for all inputs enabled with CSO<br>1h = Disable wetting current auto-scaling (to 2 mA) in continuous mode for 10 mA and 15 mA settings upon switch closure for all inputs enabled with CSO<br>For detailed descriptions for the wetting current auto-scaling, refer to section <a href="#">Wetting Current Auto-Scaling</a> . |
| 20-18 | WC_IN23            | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current  |
| 17-15 | WC_IN22            | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current  |

**表 8-38. WC\_CFG1 Register Field Descriptions (continued)**

| Bit   | Field        | Type | Reset | Description   |
|-------|--------------|------|-------|---|
| 14-12 | WC_IN20_IN21 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 11-9  | WC_IN18_IN19 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 8-6   | WC_IN16_IN17 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 5-3   | WC_IN14_IN15 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |
| 2-0   | WC_IN12_IN13 | R/W  | 0h    | 0h = no wetting current<br>1h = 1 mA (typical) wetting current<br>2h = 2 mA (typical) wetting current<br>3h = 5 mA (typical) wetting current<br>4h = 10 mA (typical) wetting current<br>5h-7h = 15 mA (typical) wetting current |

### 8.6.28 CCP\_CFG0 Register (Offset = 1Fh) [Reset = 0h]

CCP\_CFG0 is shown in 图 8-51 and described in 表 8-39.

Return to [Summary Table](#).

图 8-51. CCP\_CFG0 Register

|          |    |    |    |          |    |    |    |                     |                     |                     |                     |
|----------|----|----|----|----------|----|----|----|---------------------|---------------------|---------------------|---------------------|
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15                  | 14                  | 13                  | 12                  |
| RESERVED |    |    |    |          |    |    |    |                     |                     |                     |                     |
| R-0h     |    |    |    |          |    |    |    |                     |                     |                     |                     |
| 11       | 10 | 9  | 8  | 7        | 6  | 5  | 4  | 3                   | 2                   | 1                   | 0                   |
| RESERVED |    |    |    | CCP_TIME |    |    |    | WC_CCP <sub>3</sub> | WC_CCP <sub>2</sub> | WC_CCP <sub>1</sub> | WC_CCP <sub>0</sub> |
| R-0h     |    |    |    | R-0h     |    |    |    | R-0h                | R-0h                | R-0h                | R-0h                |

LEGEND: R/W = Read/Write; R = Read only

表 8-39. CCP\_CFG0 Register Field Descriptions

| Bit  | Field    | Type | Reset | Description  |
|------|----------|------|-------|--|
| 23-7 | RESERVED | R    | 0h    | Reserved   |
| 6-4  | CCP_TIME | R/W  | 0h    | Wetting current activation time in CCP mode<br>0h = 64 $\mu$ s<br>1h = 128 $\mu$ s<br>2h = 192 $\mu$ s<br>3h = 256 $\mu$ s<br>4h = 320 $\mu$ s<br>5h = 384 $\mu$ s<br>6h = 448 $\mu$ s<br>7h = 512 $\mu$ s |
| 3    | WC_CCP3  | R/W  | 0h    | Wetting current setting for IN18 to IN23 in CCP mode<br>0h = 10 mA (typical) wetting current<br>1h = 15 mA (typical) wetting current   |
| 2    | WC_CCP2  | R/W  | 0h    | Wetting current setting for IN12 to IN17 in CCP mode<br>0h = 10 mA (typical) wetting current<br>1h = 15 mA (typical) wetting current   |
| 1    | WC_CCP1  | R/W  | 0h    | Wetting current setting for IN6 to IN11 in CCP mode<br>0h = 10 mA (typical) wetting current<br>1h = 15 mA (typical) wetting current  |
| 0    | WC_CCP0  | R/W  | 0h    | Wetting current setting for IN0 to IN5 in CCP mode<br>0h = 10 mA (typical) wetting current<br>1h = 15 mA (typical) wetting current   |



### 8.6.29 CCP\_CFG1 Register (Offset = 20h) [Reset = 0h]

CCP\_CFG1 is shown in 图 8-52 and described in 表 8-40.

Return to [Summary Table](#).

**图 8-52. CCP\_CFG1 Register**

| 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
|----------|----------|----------|----------|----------|----------|----------|----------|
| CCP_IN23 | CCP_IN22 | CCP_IN21 | CCP_IN20 | CCP_IN19 | CCP_IN18 | CCP_IN17 | CCP_IN16 |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| CCP_IN15 | CCP_IN14 | CCP_IN13 | CCP_IN12 | CCP_IN11 | CCP_IN10 | CCP_IN9  | CCP_IN8  |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| CCP_IN7  | CCP_IN6  | CCP_IN5  | CCP_IN4  | CCP_IN3  | CCP_IN2  | CCP_IN1  | CCP_IN0  |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   |

LEGEND: R/W = Read/Write

**表 8-40. CCP\_CFG1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 23  | CCP_IN23 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 22  | CCP_IN22 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 21  | CCP_IN21 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 20  | CCP_IN20 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 19  | CCP_IN19 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 18  | CCP_IN18 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 17  | CCP_IN17 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 16  | CCP_IN16 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 15  | CCP_IN15 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 14  | CCP_IN14 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 13  | CCP_IN13 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 12  | CCP_IN12 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 11  | CCP_IN11 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 10  | CCP_IN10 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |

表 8-40. CCP\_CFG1 Register Field Descriptions (continued)

| Bit | Field   | Type | Reset | Description   |
|-----|---------|------|-------|---|
| 9   | CCP_IN9 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 8   | CCP_IN8 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 7   | CCP_IN7 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 6   | CCP_IN6 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 5   | CCP_IN5 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 4   | CCP_IN4 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 3   | CCP_IN3 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 2   | CCP_IN2 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 1   | CCP_IN1 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 0   | CCP_IN0 | R/W  | 0h    | 0h = no CCP wetting current<br>1h = CCP wetting current activated |

### 8.6.30 THRES\_COMP Register (Offset = 21h) [Reset = 0h]

THRES\_COMP is shown in 图 8-53 and described in 表 8-41.

Return to [Summary Table](#).

**图 8-53. THRES\_COMP Register**

|                      |    |                     |    |                      |    |                      |    |
|----------------------|----|---------------------|----|----------------------|----|----------------------|----|
| 23                   | 22 | 21                  | 20 | 19                   | 18 | 17                   | 16 |
| RESERVED             |    |                     |    |                      |    |                      |    |
| R-0h                 |    |                     |    |                      |    |                      |    |
| 15                   | 14 | 13                  | 12 | 11                   | 10 | 9                    | 8  |
| RESERVED             |    |                     |    | THRES_COMP_IN20_IN23 |    | THRES_COMP_IN16_IN19 |    |
| R-0h                 |    |                     |    | R/W-0h               |    | R/W-0h               |    |
| 7                    | 6  | 5                   | 4  | 3                    | 2  | 1                    | 0  |
| THRES_COMP_IN12_IN15 |    | THRES_COMP_IN8_IN11 |    | THRES_COMP_IN4_IN7   |    | THRES_COMP_IN0_IN3   |    |
| R/W-0h               |    | R/W-0h              |    | R/W-0h               |    | R/W-0h               |    |

LEGEND: R/W = Read/Write; R = Read only

**表 8-41. THRES\_COMP Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 23-12 | RESERVED             | R    | 0h    | Reserved  |
| 11-10 | THRES_COMP_IN20_IN23 | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN20 to IN23.<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V |
| 9-8   | THRES_COMP_IN16_IN19 | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN16 to IN19.<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V |
| 7-6   | THRES_COMP_IN12_IN15 | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN12 to IN15.<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V |
| 5-4   | THRES_COMP_IN8_IN11  | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN8 to IN11.<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V  |
| 3-2   | THRES_COMP_IN4_IN7   | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN4 to IN7.<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V   |

表 8-41. THRES\_COMP Register Field Descriptions (continued)

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 1-0 | THRES_COMP_IN0_IN3 | R/W  | 0h    | These 2 bits configure the comparator thresholds for input channels IN0 to IN3<br>0h = comparator threshold set to 2 V<br>1h = comparator threshold set to 2.7 V<br>2h = comparator threshold set to 3 V<br>3h = comparator threshold set to 4 V |

### 8.6.31 INT\_EN\_COMP1 Register (Offset = 22h) [Reset = 0h]

INT\_EN\_COMP1 is shown in 图 8-54 and described in 表 8-42.

Return to [Summary Table](#).

**图 8-54. INT\_EN\_COMP1 Register**

|           |    |           |    |          |    |          |    |          |    |          |    |
|-----------|----|-----------|----|----------|----|----------|----|----------|----|----------|----|
| 23        | 22 | 21        | 20 | 19       | 18 | 17       | 16 | 15       | 14 | 13       | 12 |
| INC_EN_11 |    | INC_EN_10 |    | INC_EN_9 |    | INC_EN_8 |    | INC_EN_7 |    | INC_EN_6 |    |
| R/W-0h    |    | R/W-0h    |    | R/W-0h   |    | R/W-0h   |    | R/W-0h   |    | R/W-0h   |    |
| 11        | 10 | 9         | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| INC_EN_5  |    | INC_EN_4  |    | INC_EN_3 |    | INC_EN_2 |    | INC_EN_1 |    | INC_EN_0 |    |
| R/W-0h    |    | R/W-0h    |    | R/W-0h   |    | R/W-0h   |    | R/W-0h   |    | R/W-0h   |    |

LEGEND: R/W = Read/Write

**表 8-42. INT\_EN\_COMP1 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 23-22 | INC_EN_11 | R/W  | 0h    | 0h = no interrupt generation for IN11.<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN11.<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN11.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN11. |
| 21-20 | INC_EN_10 | R/W  | 0h    | 0h = no interrupt generation for IN10<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN10.<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN10.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN10.  |
| 19-18 | INC_EN_9  | R/W  | 0h    | 0h = no interrupt generation for IN9.<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN9.<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN9.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN9.     |
| 17-16 | INC_EN_8  | R/W  | 0h    | 0h = no interrupt generation for IN8.<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN8.<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN8.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN8.     |
| 15-14 | INC_EN_7  | R/W  | 0h    | 0h = no interrupt generation for IN7.<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN7.<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN7.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN7.        |

表 8-42. INT\_EN\_COMP1 Register Field Descriptions (continued)

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 13-12 | INC_EN_6 | R/W  | 0h    | 0h = no interrupt generation for IN6.<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN6.<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN6.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN6. |
| 11-10 | INC_EN_5 | R/W  | 0h    | 0h = no interrupt generation for IN5.<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN5.<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN5.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN5. |
| 9-8   | INC_EN_4 | R/W  | 0h    | 0h = no interrupt generation for IN4.<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN4.<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN4.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN4. |
| 7-6   | INC_EN_3 | R/W  | 0h    | 0h = no interrupt generation for IN3.<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN3.<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN3.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN3. |
| 5-4   | INC_EN_2 | R/W  | 0h    | 0h = no interrupt generation for IN2.<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN2.<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN2.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN2. |
| 3-2   | INC_EN_1 | R/W  | 0h    | 0h = no interrupt generation for IN1.<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN1.<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN1.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN1. |
| 1-0   | INC_EN_0 | R/W  | 0h    | 0h = no interrupt generation for IN0.<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN0.<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN0.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN0. |

### 8.6.32 INT\_EN\_COMP2 Register (Offset = 23h) [Reset = 0h]

INT\_EN\_COMP2 is shown in 图 8-55 and described in 表 8-43.

Return to [Summary Table](#).

**图 8-55. INT\_EN\_COMP2 Register**

|           |    |           |    |           |    |           |    |           |    |           |    |
|-----------|----|-----------|----|-----------|----|-----------|----|-----------|----|-----------|----|
| 23        | 22 | 21        | 20 | 19        | 18 | 17        | 16 | 15        | 14 | 13        | 12 |
| INC_EN_23 |    | INC_EN_22 |    | INC_EN_21 |    | INC_EN_20 |    | INC_EN_19 |    | INC_EN_18 |    |
| R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    |
| 11        | 10 | 9         | 8  | 7         | 6  | 5         | 4  | 3         | 2  | 1         | 0  |
| INC_EN_17 |    | INC_EN_16 |    | INC_EN_15 |    | INC_EN_14 |    | INC_EN_13 |    | INC_EN_12 |    |
| R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    | R/W-0h    |    |

LEGEND: R/W = Read/Write

**表 8-43. INT\_EN\_COMP2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description   |
|-------|-----------|------|-------|---|
| 23-22 | INC_EN_23 | R/W  | 0h    | 0h = no interrupt generation for IN23.<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN23.<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN23.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN23. |
| 21-20 | INC_EN_22 | R/W  | 0h    | 0h = no interrupt generation for IN22.<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN22.<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN22.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN22. |
| 19-18 | INC_EN_21 | R/W  | 0h    | 0h = no interrupt generation for IN21.<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN21.<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN21.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN21. |
| 17-16 | INC_EN_20 | R/W  | 0h    | 0h = no interrupt generation for IN20.<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN20.<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN20.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN20. |
| 15-14 | INC_EN_19 | R/W  | 0h    | 0h = no interrupt generation for IN19.<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN19.<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN19.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN19. |

表 8-43. INT\_EN\_COMP2 Register Field Descriptions (continued)

| Bit   | Field     | Type | Reset | Description   |
|-------|-----------|------|-------|---|
| 13-12 | INC_EN_18 | R/W  | 0h    | 0h = no interrupt generation for IN18.<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN18.<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN18.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN18. |
| 11-10 | INC_EN_17 | R/W  | 0h    | 0h = no interrupt generation for IN17.<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN17.<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN17.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN17. |
| 9-8   | INC_EN_16 | R/W  | 0h    | 0h = no interrupt generation for IN16.<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN16.<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN16.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN16. |
| 7-6   | INC_EN_15 | R/W  | 0h    | 0h = no interrupt generation for IN15.<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN15.<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN15.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN15. |
| 5-4   | INC_EN_14 | R/W  | 0h    | 0h = no interrupt generation for IN14.<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN14.<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN14.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN14. |
| 3-2   | INC_EN_13 | R/W  | 0h    | 0h = no interrupt generation for IN13.<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN13.<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN13.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN13. |
| 1-0   | INC_EN_12 | R/W  | 0h    | 0h = no interrupt generation for IN12.<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN12.<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN12.<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN12. |



### 8.6.33 INT\_EN\_CFG0 Register (Offset = 24h) [Reset = 0h]

INT\_EN\_CFG0 is shown in 图 8-56 and described in 表 8-44.

Return to [Summary Table](#).

**图 8-56. INT\_EN\_CFG0 Register**

|             |        |        |        |             |             |              |             |
|-------------|--------|--------|--------|-------------|-------------|--------------|-------------|
| 23          | 22     | 21     | 20     | 19          | 18          | 17           | 16          |
| RESERVED    |        |        |        |             |             |              |             |
| R-0h        |        |        |        |             |             |              |             |
| 15          | 14     | 13     | 12     | 11          | 10          | 9            | 8           |
| RESERVED    |        |        |        | ADC_DIAG_EN | WET_DIAG_EN | VS1_EN       | VS0_EN      |
| R-0h        |        |        |        | R/W-0h      | R/W-0h      | R/W-0h       | R/W-0h      |
| 7           | 6      | 5      | 4      | 3           | 2           | 1            | 0           |
| CRC_CALC_EN | UV_EN  | OV_EN  | TW_EN  | TSD_EN      | SSC_EN      | PRTY_FAIL_EN | SPI_FAIL_EN |
| R/W-0h      | R/W-0h | R/W-0h | R/W-0h | R/W-0h      | R/W-0h      | R/W-0h       | R/W-0h      |

LEGEND: R/W = Read/Write; R = Read only

**表 8-44. INT\_EN\_CFG0 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description   |
|-------|--------------|------|-------|---|
| 23-12 | RESERVED     | R    | 0h    | Reserved  |
| 11    | ADC_DIAG_EN  | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to ADC error disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to ADC error enabled.                                   |
| 10    | WET_DIAG_EN  | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to wetting current error disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to wetting current error enabled.           |
| 9     | VS1_EN       | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to VS1 threshold crossing disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to VS1 threshold crossing enabled.         |
| 8     | VS0_EN       | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to VS0 threshold crossing disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to VS0 threshold crossing enabled.         |
| 7     | CRC_CALC_EN  | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to CRC calculation completion disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to CRC calculation completion enabled. |
| 6     | UV_EN        | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to UV event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to UV event enabled.                                     |
| 5     | OV_EN        | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to OV event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to OV event enabled.                                     |
| 4     | TW_EN        | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to TW event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to TW event enabled.                                     |
| 3     | TSD_EN       | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to TSD event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to TSD event enabled.                                   |
| 2     | SSC_EN       | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to SSC event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to SSC event enabled.                                   |
| 1     | PRTY_FAIL_EN | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to parity fail event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to parity fail event enabled.                   |
| 0     | SPI_FAIL_EN  | R/W  | 0h    | 0h = $\overline{\text{INT}}$ pin assertion due to SPI fail event disabled.<br>1h = $\overline{\text{INT}}$ pin assertion due to SPI fail event enabled.                         |

### 8.6.34 INT\_EN\_CFG1 Register (Offset = 25h) [Reset = 0h]

INT\_EN\_CFG1 is shown in 图 8-57 and described in 表 8-45.

Return to [Summary Table](#).

图 8-57. INT\_EN\_CFG1 Register

|         |    |         |    |        |    |        |    |        |    |        |    |
|---------|----|---------|----|--------|----|--------|----|--------|----|--------|----|
| 23      | 22 | 21      | 20 | 19     | 18 | 17     | 16 | 15     | 14 | 13     | 12 |
| IN11_EN |    | IN10_EN |    | IN9_EN |    | IN8_EN |    | IN7_EN |    | IN6_EN |    |
| R/W-0h  |    | R/W-0h  |    | R/W-0h |    | R/W-0h |    | R/W-0h |    | R/W-0h |    |
| 11      | 10 | 9       | 8  | 7      | 6  | 5      | 4  | 3      | 2  | 1      | 0  |
| IN5_EN  |    | IN4_EN  |    | IN3_EN |    | IN2_EN |    | IN1_EN |    | IN0_EN |    |
| R/W-0h  |    | R/W-0h  |    | R/W-0h |    | R/W-0h |    | R/W-0h |    | R/W-0h |    |

LEGEND: R/W = Read/Write

表 8-45. INT\_EN\_CFG1 Register Field Descriptions

| Bit   | Field   | Type | Reset | Description   |
|-------|---------|------|-------|---|
| 23-22 | IN11_EN | R/W  | 0h    | 0h = no interrupt generation for IN11.<br>1h = interrupt generation on rising edge above THRESx for IN11.<br>2h = interrupt generation on falling edge below THRESx for IN11.<br>3h = interrupt generation on falling and rising edge of THRESx for IN11. |
| 21-20 | IN10_EN | R/W  | 0h    | 0h = no interrupt generation for IN10.<br>1h = interrupt generation on rising edge above THRESx for IN10.<br>2h = interrupt generation on falling edge below THRESx for IN10.<br>3h = interrupt generation on falling and rising edge of THRESx for IN10. |
| 19-18 | IN9_EN  | R/W  | 0h    | 0h = no interrupt generation for IN9.<br>1h = interrupt generation on rising edge above THRESx for IN9.<br>2h = interrupt generation on falling edge below THRESx for IN9.<br>3h = interrupt generation on falling and rising edge of THRESx for IN9.     |
| 17-16 | IN8_EN  | R/W  | 0h    | 0h = no interrupt generation for IN8.<br>1h = interrupt generation on rising edge above THRESx for IN8.<br>2h = interrupt generation on falling edge below THRESx for IN8.<br>3h = interrupt generation on falling and rising edge of THRESx for IN8.     |
| 15-14 | IN7_EN  | R/W  | 0h    | 0h = no interrupt generation for IN7.<br>1h = interrupt generation on rising edge above THRESx for IN7.<br>2h = interrupt generation on falling edge below THRESx for IN7.<br>3h = interrupt generation on falling and rising edge of THRESx for IN7.     |
| 13-12 | IN6_EN  | R/W  | 0h    | 0h = no interrupt generation for IN6.<br>1h = interrupt generation on rising edge above THRESx for IN6.<br>2h = interrupt generation on falling edge below THRESx for IN6.<br>3h = interrupt generation on falling and rising edge of THRESx for IN6.     |
| 11-10 | IN5_EN  | R/W  | 0h    | 0h = no interrupt generation for IN5.<br>1h = interrupt generation on rising edge above THRESx for IN5.<br>2h = interrupt generation on falling edge below THRESx for IN5.<br>3h = interrupt generation on falling and rising edge of THRESx for IN5.     |

**表 8-45. INT\_EN\_CFG1 Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description   |
|-----|--------|------|-------|---|
| 9-8 | IN4_EN | R/W  | 0h    | 0h = no interrupt generation for IN4.<br>1h = interrupt generation on rising edge above THRESx for IN4.<br>2h = interrupt generation on falling edge below THRESx for IN4.<br>3h = interrupt generation on falling and rising edge of THRESx for IN4. |
| 7-6 | IN3_EN | R/W  | 0h    | 0h = no interrupt generation for IN3.<br>1h = interrupt generation on rising edge above THRESx for IN3.<br>2h = interrupt generation on falling edge below THRESx for IN3.<br>3h = interrupt generation on falling and rising edge of THRESx for IN3. |
| 5-4 | IN2_EN | R/W  | 0h    | 0h = no interrupt generation for IN2.<br>1h = interrupt generation on rising edge above THRESx for IN2.<br>2h = interrupt generation on falling edge below THRESx for IN2.<br>3h = interrupt generation on falling and rising edge of THRESx for IN2. |
| 3-2 | IN1_EN | R/W  | 0h    | 0h = no interrupt generation for IN1.<br>1h = interrupt generation on rising edge above THRESx for IN1.<br>2h = interrupt generation on falling edge below THRESx for IN1.<br>3h = interrupt generation on falling and rising edge of THRESx for IN1. |
| 1-0 | IN0_EN | R/W  | 0h    | 0h = no interrupt generation for IN0.<br>1h = interrupt generation on rising edge above THRESx for IN0.<br>2h = interrupt generation on falling edge below THRESx for IN0.<br>3h = interrupt generation on falling and rising edge of THRESx for IN0. |

### 8.6.35 INT\_EN\_CFG2 Register (Offset = 26h) [Reset = 0h]

INT\_EN\_CFG2 is shown in 图 8-58 and described in 表 8-46.

Return to [Summary Table](#).

图 8-58. INT\_EN\_CFG2 Register

|         |    |    |    |         |    |    |    |         |    |    |    |
|---------|----|----|----|---------|----|----|----|---------|----|----|----|
| 23      | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15      | 14 | 13 | 12 |
| IN17_EN |    |    |    | IN16_EN |    |    |    | IN15_EN |    |    |    |
| R/W-0h  |    |    |    | R/W-0h  |    |    |    | R/W-0h  |    |    |    |
| 11      | 10 | 9  | 8  | 7       | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| IN14_EN |    |    |    | IN13_EN |    |    |    | IN12_EN |    |    |    |
| R/W-0h  |    |    |    | R/W-0h  |    |    |    | R/W-0h  |    |    |    |

LEGEND: R/W = Read/Write

表 8-46. INT\_EN\_CFG2 Register Field Descriptions

| Bit   | Field   | Type | Reset | Description  |
|-------|---------|------|-------|--|
| 23-20 | IN17_EN | R/W  | 0h    | xx00: no interrupt generation for IN17 w.r.t. THRES2A.<br>xx01: interrupt generation on rising edge above THRES2A for IN17.<br>xx10: interrupt generation on falling edge below THRES2A for IN17.<br>xx11: interrupt generation on falling and rising edge of THRES2A for IN17.<br>00xx: no interrupt generation for IN17 w.r.t. THRES2B.<br>01xx: interrupt generation on rising edge above THRES2B for IN17.<br>10xx: interrupt generation on falling edge below THRES2B for IN17.<br>11xx: interrupt generation on falling and rising edge of THRES2B for IN17. |
| 19-16 | IN16_EN | R/W  | 0h    | xx00: no interrupt generation for IN16 w.r.t. THRES2A.<br>xx01: interrupt generation on rising edge above THRES2A for IN16.<br>xx10: interrupt generation on falling edge below THRES2A for IN16.<br>xx11: interrupt generation on falling and rising edge of THRES2A for IN16.<br>00xx: no interrupt generation for IN16 w.r.t. THRES2B.<br>01xx: interrupt generation on rising edge above THRES2B for IN16.<br>10xx: interrupt generation on falling edge below THRES2B for IN16.<br>11xx: interrupt generation on falling and rising edge of THRES2B for IN16. |
| 15-12 | IN15_EN | R/W  | 0h    | xx00: no interrupt generation for IN15 w.r.t. THRES2A.<br>xx01: interrupt generation on rising edge above THRES2A for IN15.<br>xx10: interrupt generation on falling edge below THRES2A for IN15.<br>xx11: interrupt generation on falling and rising edge of THRES2A for IN15.<br>00xx: no interrupt generation for IN15 w.r.t. THRES2B.<br>01xx: interrupt generation on rising edge above THRES2B for IN15.<br>10xx: interrupt generation on falling edge below THRES2B for IN15.<br>11xx: interrupt generation on falling and rising edge of THRES2B for IN15. |

**表 8-46. INT\_EN\_CFG2 Register Field Descriptions (continued)**

| Bit  | Field   | Type | Reset | Description   |
|------|---------|------|-------|---|
| 11-8 | IN14_EN | R/W  | 0h    | <p>xx00: no interrupt generation for IN14 w.r.t. THRES2A.<br/> xx01: interrupt generation on rising edge above THRES2A for IN14.<br/> xx10: interrupt generation on falling edge below THRES2A for IN14.<br/> xx11: interrupt generation on falling and rising edge of THRES2A for IN14.<br/> 00xx: no interrupt generation for IN14 w.r.t. THRES2B.<br/> 01xx: interrupt generation on rising edge above THRES2B for IN14.<br/> 10xx: interrupt generation on falling edge below THRES2B for IN14.<br/> 11xx: interrupt generation on falling and rising edge of THRES2B for IN14.</p> |
| 7-4  | IN13_EN | R/W  | 0h    | <p>xx00: no interrupt generation for IN13 w.r.t. THRES2A.<br/> xx01: interrupt generation on rising edge above THRES2A for IN13.<br/> xx10: interrupt generation on falling edge below THRES2A for IN13.<br/> xx11: interrupt generation on falling and rising edge of THRES2A for IN13.<br/> 00xx: no interrupt generation for IN13 w.r.t. THRES2B.<br/> 01xx: interrupt generation on rising edge above THRES2B for IN13.<br/> 10xx: interrupt generation on falling edge below THRES2B for IN13.<br/> 11xx: interrupt generation on falling and rising edge of THRES2B for IN13.</p> |
| 3-0  | IN12_EN | R/W  | 0h    | <p>xx00: no interrupt generation for IN12 w.r.t. THRES2A.<br/> xx01: interrupt generation on rising edge above THRES2A for IN12.<br/> xx10: interrupt generation on falling edge below THRES2A for IN12.<br/> xx11: interrupt generation on falling and rising edge of THRES2A for IN12.<br/> 00xx: no interrupt generation for IN12 w.r.t. THRES2B.<br/> 01xx: interrupt generation on rising edge above THRES2B for IN12.<br/> 10xx: interrupt generation on falling edge below THRES2B for IN12.<br/> 11xx: interrupt generation on falling and rising edge of THRES2B for IN12.</p> |

### 8.6.36 INT\_EN\_CFG3 Register (Offset = 27h) [Reset = 0h]

INT\_EN\_CFG3 is shown in 图 8-59 and described in 表 8-47.

Return to [Summary Table](#).

图 8-59. INT\_EN\_CFG3 Register

|         |    |    |    |    |    |    |    |         |    |    |    |
|---------|----|----|----|----|----|----|----|---------|----|----|----|
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 |
| IN21_EN |    |    |    |    |    |    |    | IN20_EN |    |    |    |
| R/W-0h  |    |    |    |    |    |    |    | R/W-0h  |    |    |    |
| 11      | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| IN19_EN |    |    |    |    |    |    |    | IN18_EN |    |    |    |
| R/W-0h  |    |    |    |    |    |    |    | R/W-0h  |    |    |    |

LEGEND: R/W = Read/Write

表 8-47. INT\_EN\_CFG3 Register Field Descriptions

| Bit   | Field   | Type | Reset | Description   |
|-------|---------|------|-------|---|
| 23-18 | IN21_EN | R/W  | 0h    | xxxx00: no interrupt generation for IN21 w.r.t. THRES3A<br>xxxx01: interrupt generation on rising edge above THRES3A for IN21<br>xxxx10: interrupt generation on falling edge below THRES3A for IN21<br>xxxx11: interrupt generation on falling and rising edge of THRES3A for IN21<br>xx00xx: no interrupt generation for IN21 w.r.t. THRES3B<br>xx01xx: interrupt generation on rising edge above THRES3B for IN21<br>xx10xx: interrupt generation on falling edge below THRES3B for IN21<br>xx11xx: interrupt generation on falling and rising edge of THRES3B for IN21<br>00xxxx: no interrupt generation for IN21 w.r.t. THRES3C<br>01xxxx: interrupt generation on rising edge above THRES3C for IN21<br>10xxxx: interrupt generation on falling edge below THRES3C for IN21<br>11xxxx: interrupt generation on falling and rising edge of THRES3C for IN21 |

**表 8-47. INT\_EN\_CFG3 Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description  |
|-------|---------|------|-------|--|
| 17-12 | IN20_EN | R/W  | 0h    | <p>xxxx00: no interrupt generation for IN20 w.r.t. THRES3A</p> <p>xxxx01: interrupt generation on rising edge above THRES3A for IN20</p> <p>xxxx10: interrupt generation on falling edge below THRES3A for IN20</p> <p>xxxx11: interrupt generation on falling and rising edge of THRES3A for IN20</p> <p>xx00xx: no interrupt generation for IN20 w.r.t. THRES3B</p> <p>xx01xx: interrupt generation on rising edge above THRES3B for IN20</p> <p>xx10xx: interrupt generation on falling edge below THRES3B for IN20</p> <p>xx11xx: interrupt generation on falling and rising edge of THRES3B for IN20</p> <p>00xxxx: no interrupt generation for IN20 w.r.t. THRES3C</p> <p>01xxxx: interrupt generation on rising edge above THRES3C for IN20</p> <p>10xxxx: interrupt generation on falling edge below THRES3C for IN20</p> <p>11xxxx: interrupt generation on falling and rising edge of THRES3C for IN20</p> |
| 11-6  | IN19_EN | R/W  | 0h    | <p>xxxx00: no interrupt generation for IN19 w.r.t. THRES3A</p> <p>xxxx01: interrupt generation on rising edge above THRES3A for IN19</p> <p>xxxx10: interrupt generation on falling edge below THRES3A for IN19</p> <p>xxxx11: interrupt generation on falling and rising edge of THRES3A for IN19</p> <p>xx00xx: no interrupt generation for IN19 w.r.t. THRES3B</p> <p>xx01xx: interrupt generation on rising edge above THRES3B for IN19</p> <p>xx10xx: interrupt generation on falling edge below THRES3B for IN19</p> <p>xx11xx: interrupt generation on falling and rising edge of THRES3B for IN19</p> <p>00xxxx: no interrupt generation for IN19 w.r.t. THRES3C</p> <p>01xxxx: interrupt generation on rising edge above THRES3C for IN19</p> <p>10xxxx: interrupt generation on falling edge below THRES3C for IN19</p> <p>11xxxx: interrupt generation on falling and rising edge of THRES3C for IN19</p> |

表 8-47. INT\_EN\_CFG3 Register Field Descriptions (continued)

| Bit | Field   | Type | Reset | Description   |
|-----|---------|------|-------|---|
| 5-0 | IN18_EN | R/W  | 0h    | xxxx00: no interrupt generation for IN18 w.r.t. THRES3A<br>xxxx01: interrupt generation on rising edge above THRES3A for IN18<br>xxxx10: interrupt generation on falling edge below THRES3A for IN18<br>xxxx11: interrupt generation on falling and rising edge of THRES3A for IN18<br>xx00xx: no interrupt generation for IN18 w.r.t. THRES3B<br>xx01xx: interrupt generation on rising edge above THRES3B for IN18<br>xx10xx: interrupt generation on falling edge below THRES3B for IN18<br>xx11xx: interrupt generation on falling and rising edge of THRES3B for IN18<br>00xxxx: no interrupt generation for IN18 w.r.t. THRES3C<br>01xxxx: interrupt generation on rising edge above THRES3C for IN18<br>10xxxx: interrupt generation on falling edge below THRES3C for IN18<br>11xxxx: interrupt generation on falling and rising edge of THRES3C for IN18 |



### 8.6.37 INT\_EN\_CFG4 Register (Offset = 28h) [Reset = 0h]

INT\_EN\_CFG4 is shown in 图 8-60 and described in 表 8-48.

Return to [Summary Table](#).

**图 8-60. INT\_EN\_CFG4 Register**

|           |    |    |    |           |    |         |    |         |    |    |    |
|-----------|----|----|----|-----------|----|---------|----|---------|----|----|----|
| 23        | 22 | 21 | 20 | 19        | 18 | 17      | 16 | 15      | 14 | 13 | 12 |
| VS_TH1_EN |    |    |    | VS_TH0_EN |    |         |    | IN23_EN |    |    |    |
| R/W-0h    |    |    |    | R/W-0h    |    |         |    | R/W-0h  |    |    |    |
| 11        | 10 | 9  | 8  | 7         | 6  | 5       | 4  | 3       | 2  | 1  | 0  |
| IN23_EN   |    |    |    |           |    | IN22_EN |    |         |    |    |    |
| R/W-0h    |    |    |    |           |    | R/W-0h  |    |         |    |    |    |

LEGEND: R/W = Read/Write

**表 8-48. INT\_EN\_CFG4 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 23-20 | VS_TH1_EN | R/W  | 0h    | xx00: no interrupt generation for $V_S$ w.r.t. VS1_THRES2A.<br>xx01: interrupt generation on rising edge above VS1_THRES2A for $V_S$ .<br>xx10: interrupt generation on falling edge below VS1_THRES2A for $V_S$ .<br>xx11: interrupt generation on falling and rising edge of VS1_THRES2A for $V_S$ .<br>00xx: no interrupt generation for $V_S$ w.r.t. VS1_THRES2B.<br>01xx: interrupt generation on rising edge above VS1_THRES2B for $V_S$ .<br>10xx: interrupt generation on falling edge below VS1_THRES2B for $V_S$ .<br>11xx: interrupt generation on falling and rising edge of VS1_THRES2B for $V_S$ . |
| 19-16 | VS_TH0_EN | R/W  | 0h    | xx00: no interrupt generation for $V_S$ w.r.t. VS0_THRES2A.<br>xx01: interrupt generation on rising edge above VS0_THRES2A for $V_S$ .<br>xx10: interrupt generation on falling edge below VS0_THRES2A for $V_S$ .<br>xx11: interrupt generation on falling and rising edge of VS0_THRES2A for $V_S$ .<br>00xx: no interrupt generation for $V_S$ w.r.t. VS0_THRES2B.<br>01xx: interrupt generation on rising edge above VS0_THRES2B for $V_S$ .<br>10xx: interrupt generation on falling edge below VS0_THRES2B for $V_S$ .<br>11xx: interrupt generation on falling and rising edge of VS0_THRES2B for $V_S$ . |

表 8-48. INT\_EN\_CFG4 Register Field Descriptions (continued)

| Bit  | Field   | Type | Reset | Description  |
|------|---------|------|-------|--|
| 15-6 | IN23_EN | R/W  | 0h    | <p>xxxxxxx00: no interrupt generation for IN23 w.r.t. THRES3A.</p> <p>xxxxxxx01: interrupt generation on rising edge above THRES3A for IN23.</p> <p>xxxxxxx10: interrupt generation on falling edge below THRES3A for IN23.</p> <p>xxxxxxx11: interrupt generation on falling and rising edge of THRES3A for IN23.</p> <p>xxxxx00xx: no interrupt generation for IN23 w.r.t. THRES3B.</p> <p>xxxxx01xx: interrupt generation on rising edge above THRES3B for IN23.</p> <p>xxxxx10xx: interrupt generation on falling edge below THRES3B for IN23.</p> <p>xxxxx11xx: interrupt generation on falling and rising edge of THRES3B for IN23.</p> <p>xxx00xxxx: no interrupt generation for IN23 w.r.t. THRES3C.</p> <p>xxx01xxxx: interrupt generation on rising edge above THRES3C for IN23.</p> <p>xxx10xxxx: interrupt generation on falling edge below THRES3C for IN23.</p> <p>xxx11xxxx: interrupt generation on falling and rising edge of THRES3C for IN23.</p> <p>xx00xxxxx: no interrupt generation for IN23 w.r.t. THRES8.</p> <p>xx01xxxxx: interrupt generation on rising edge above THRES8 for IN23.</p> <p>xx10xxxxx: interrupt generation on falling edge below THRES8 for IN23.</p> <p>xx11xxxxx: interrupt generation on falling and rising edge of THRES8 for IN23.</p> <p>00xxxxxxx: no interrupt generation for IN23 w.r.t. THRES9.</p> <p>01xxxxxxx: interrupt generation on rising edge above THRES9 for IN23.</p> <p>10xxxxxxx: interrupt generation on falling edge below THRES9 for IN23.</p> <p>11xxxxxxx: interrupt generation on falling and rising edge of THRES9 for IN23.</p> |

**表 8-48. INT\_EN\_CFG4 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description  |
|-----|---------|------|-------|--|
| 5-0 | IN22_EN | R/W  | 0h    | <p>xxxx00: no interrupt generation for IN22 w.r.t. THRES3A.</p> <p>xxxx01: interrupt generation on rising edge above THRES3A for IN22.</p> <p>xxxx10: interrupt generation on falling edge below THRES3A for IN22.</p> <p>xxxx11: interrupt generation on falling and rising edge of THRES3A for IN22.</p> <p>xx00xx: no interrupt generation for IN22 w.r.t. THRES3B.</p> <p>xx01xx: interrupt generation on rising edge above THRES3B for IN22.</p> <p>xx10xx: interrupt generation on falling edge below THRES3B for IN22.</p> <p>xx11xx: interrupt generation on falling and rising edge of THRES3B for IN22.</p> <p>00xxxx: no interrupt generation for IN22 w.r.t. THRES3C.</p> <p>01xxxx: interrupt generation on rising edge above THRES3C for IN22.</p> <p>10xxxx: interrupt generation on falling edge below THRES3C for IN22.</p> <p>11xxxx: interrupt generation on falling and rising edge of THRES3C for IN22.</p> |

### 8.6.38 THRES\_CFG0 Register (Offset = 29h) [Reset = 0h]

THRES\_CFG0 is shown in 图 8-61 and described in 表 8-49.

Return to [Summary Table](#).

图 8-61. THRES\_CFG0 Register

| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| RESERVED |    |    |    | THRES1 |    |    |    |    |    |    |    |    |    | THRES0 |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h   |    |    |    |    |    |    |    |    |    | R-0h   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only

表 8-49. THRES\_CFG0 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | THRES1   | R/W  | 0h    | 10-bits value of threshold 1:<br>Bit10: LSB<br>Bit19: MSB |
| 9-0   | THRES0   | R/W  | 0h    | 10-bits value of threshold 0<br>Bit0: LSB<br>Bit9: MSB    |

### 8.6.39 THRES\_CFG1 Register (Offset = 2Ah) [Reset = 0h]

THRES\_CFG1 is shown in 图 8-62 and described in 表 8-50.

Return to [Summary Table](#).

图 8-62. THRES\_CFG1 Register

| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| RESERVED |    |    |    | THRES3 |    |    |    |    |    |    |    |    |    | THRES2 |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h   |    |    |    |    |    |    |    |    |    | R-0h   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only

表 8-50. THRES\_CFG1 Register Field Descriptions

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | THRES3   | R/W  | 0h    | 10-bits value of threshold 3:<br>Bit10: LSB<br>Bit19: MSB |
| 9-0   | THRES2   | R/W  | 0h    | 10-bits value of threshold 2<br>Bit0: LSB<br>Bit9: MSB    |

#### 8.6.40 THRES\_CFG2 Register (Offset = 2Bh) [Reset = 0h]

THRES\_CFG2 is shown in [图 8-63](#) and described in [表 8-51](#).

Return to [Summary Table](#).

**图 8-63. THRES\_CFG2 Register**

|          |    |    |    |        |    |    |    |    |    |    |    |    |    |        |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | THRES5 |    |    |    |    |    |    |    |    |    | THRES4 |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h   |    |    |    |    |    |    |    |    |    | R-0h   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only

**表 8-51. THRES\_CFG2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | THRES5   | R/W  | 0h    | 10-bits value of threshold 5:<br>Bit10: LSB<br>Bit19: MSB |
| 10-1  | THRES4   | R/W  | 0h    | 10-bits value of threshold 4:<br>Bit0: LSB<br>Bit9: MSB   |

#### 8.6.41 THRES\_CFG3 Register (Offset = 2Ch) [Reset = X]

THRES\_CFG3 is shown in [图 8-64](#) and described in [表 8-52](#).

Return to [Summary Table](#).

**图 8-64. THRES\_CFG3 Register**

|          |    |    |    |        |    |    |    |    |    |    |    |    |    |        |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | THRES6 |    |    |    |    |    |    |    |    |    | THRES7 |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h   |    |    |    |    |    |    |    |    |    | R-0h   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only

**表 8-52. THRES\_CFG3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | THRES7   | R/W  | 0h    | 10-bits value of threshold 7:<br>Bit10: LSB<br>Bit19: MSB |
| 9-0   | THRES6   | R/W  | 0h    | 10-bits value of threshold 6:<br>Bit0: LSB<br>Bit9: MSB   |

### 8.6.42 THRES\_CFG4 Register (Offset = 2Dh) [Reset = X]

THRES\_CFG4 is shown in [图 8-65](#) and described in [表 8-53](#).

Return to [Summary Table](#).

**图 8-65. THRES\_CFG4 Register**

|          |    |    |    |        |    |    |    |    |    |    |    |    |    |        |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | THRES9 |    |    |    |    |    |    |    |    |    | THRES8 |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    | R-0h   |    |    |    |    |    |    |    |    |    | R-0h   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only

**表 8-53. THRES\_CFG4 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 23-20 | RESERVED | R    | 0h    | Reserved  |
| 19-10 | THRES9   | R/W  | 0h    | 10-bits value of threshold 9:<br>Bit10: LSB<br>Bit19: MSB |
| 9-0   | THRES8   | R/W  | 0h    | 10-bits value of threshold 8:<br>Bit0: LSB<br>Bit9: MSB   |

### 8.6.43 THRESMAP\_CFG0 Register (Offset = 2Eh) [Reset = 0h]

THRESMAP\_CFG0 is shown in 图 8-66 and described in 表 8-54.

Return to [Summary Table](#).

**图 8-66. THRESMAP\_CFG0 Register**

|              |    |    |    |              |    |    |    |              |    |    |    |
|--------------|----|----|----|--------------|----|----|----|--------------|----|----|----|
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16 | 15           | 14 | 13 | 12 |
| THRESMAP_IN7 |    |    |    | THRESMAP_IN6 |    |    |    | THRESMAP_IN5 |    |    |    |
| R/W-0h       |    |    |    | R/W-0h       |    |    |    | R/W-0h       |    |    |    |
| 11           | 10 | 9  | 8  | 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| THRESMAP_IN3 |    |    |    | THRESMAP_IN2 |    |    |    | THRESMAP_IN1 |    |    |    |
| R/W-0h       |    |    |    | R/W-0h       |    |    |    | R/W-0h       |    |    |    |

LEGEND: R/W = Read/Write

**表 8-54. THRESMAP\_CFG0 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description  |
|-------|--------------|------|-------|--|
| 23-21 | THRESMAP_IN7 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 20-18 | THRESMAP_IN6 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 17-15 | THRESMAP_IN5 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 14-12 | THRESMAP_IN4 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |

表 8-54. THRESMAP\_CFG0 Register Field Descriptions (continued)

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--|
| 11-9 | THRESMAP_IN3 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 8-6  | THRESMAP_IN2 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 5-3  | THRESMAP_IN1 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 2-0  | THRESMAP_IN0 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |



### 8.6.44 THRESMAP\_CFG1 Register (Offset = 2Fh) [Reset = 0h]

THRESMAP\_CFG1 is shown in [图 8-67](#) and described in [表 8-55](#).

Return to [Summary Table](#).

**图 8-67. THRESMAP\_CFG1 Register**

|               |    |    |               |    |    |                            |    |    |                            |    |    |
|---------------|----|----|---------------|----|----|----------------------------|----|----|----------------------------|----|----|
| 23            | 22 | 21 | 20            | 19 | 18 | 17                         | 16 | 15 | 14                         | 13 | 12 |
| RESERVED      |    |    |               |    |    | THRESMAP_IN12_IN17_THRES2B |    |    | THRESMAP_IN12_IN17_THRES2A |    |    |
| R/W-0h        |    |    |               |    |    | R/W-0h                     |    |    | R/W-0h                     |    |    |
| 11            | 10 | 9  | 8             | 7  | 6  | 5                          | 4  | 3  | 2                          | 1  | 0  |
| THRESMAP_IN11 |    |    | THRESMAP_IN10 |    |    | THRESMAP_IN9               |    |    | THRESMAP_IN8               |    |    |
| R/W-0h        |    |    | R/W-0h        |    |    | R/W-0h                     |    |    | R/W-0h                     |    |    |

LEGEND: R/W = Read/Write; R = Read only

**表 8-55. THRESMAP\_CFG1 Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description  |
|-------|----------------------------|------|-------|--|
| 23-18 | RESERVED                   | R    | 0h    | Reserved   |
| 17-15 | THRESMAP_IN12_IN17_THRES2B | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 14-12 | THRESMAP_IN12_IN17_THRES2A | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 11-9  | THRESMAP_IN11              | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 8-6   | THRESMAP_IN10              | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |

表 8-55. THRESMAP\_CFG1 Register Field Descriptions (continued)

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 5-3 | THRESMAP_IN9 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 2-0 | THRESMAP_IN8 | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |

### 8.6.45 THRESMAP\_CFG2 Register (Offset = 30h) [Reset = 0h]

THRESMAP\_CFG2 is shown in 图 8-68 and described in 表 8-56.

Return to [Summary Table](#).

**图 8-68. THRESMAP\_CFG2 Register**

|                      |    |    |    |                            |    |    |    |                            |    |    |    |
|----------------------|----|----|----|----------------------------|----|----|----|----------------------------|----|----|----|
| 23                   | 22 | 21 | 20 | 19                         | 18 | 17 | 16 | 15                         | 14 | 13 | 12 |
| RESERVED             |    |    |    | THRESMAP_VS1_THRES2B       |    |    |    | THRESMAP_VS1_THRES2A       |    |    |    |
| R-0h                 |    |    |    | R/W-0h                     |    |    |    | R/W-0h                     |    |    |    |
| 11                   | 10 | 9  | 8  | 7                          | 6  | 5  | 4  | 3                          | 2  | 1  | 0  |
| THRESMAP_VS0_THRES2A |    |    |    | THRESMAP_IN18_IN23_THRES3C |    |    |    | THRESMAP_IN18_IN23_THRES3B |    |    |    |
| R/W-0h               |    |    |    | R/W-0h                     |    |    |    | R/W-0h                     |    |    |    |

LEGEND: R/W = Read/Write; R = Read only

**表 8-56. THRESMAP\_CFG2 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description  |
|-------|----------------------|------|-------|--|
| 23-21 | RESERVED             | R    | 0h    | Reserved   |
| 20-18 | THRESMAP_VS1_THRES2B | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 17-15 | THRESMAP_VS1_THRES2A | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 14-12 | THRESMAP_VS0_THRES2B | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 11-9  | THRESMAP_VS0_THRES2A | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |

表 8-56. THRESMAP\_CFG2 Register Field Descriptions (continued)

| Bit | Field                      | Type | Reset | Description  |
|-----|----------------------------|------|-------|--|
| 8-6 | THRESMAP_IN18_IN23_THRES3C | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 5-3 | THRESMAP_IN18_IN23_THRES3B | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |
| 2-0 | THRESMAP_IN18_IN23_THRES3A | R/W  | 0h    | 0h = THRES0<br>1h = THRES1<br>2h = THRES2<br>3h = THRES3<br>4h = THRES4<br>5h = THRES5<br>6h = THRES6<br>7h = THRES7 |

### 8.6.46 Matrix Register (Offset = 31h) [Reset = 0h]

Matrix is shown in 图 8-69 and described in 表 8-57.

Return to [Summary Table](#).

**图 8-69. Matrix Register**

|           |    |    |    |    |    |    |           |    |                 |    |    |
|-----------|----|----|----|----|----|----|-----------|----|-----------------|----|----|
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16        | 15 | 14              | 13 | 12 |
| RESERVED  |    |    |    |    |    |    | IN_COM_EN |    | THRES_COM       |    |    |
| R-0h      |    |    |    |    |    |    | R/W-0h    |    | R/W-0h          |    |    |
| 11        | 10 | 9  | 8  | 7  | 6  | 5  | 4         | 3  | 2               | 1  | 0  |
| THRES_COM |    |    |    |    |    |    | MATRIX    |    | POLL_ACT_TIME_M |    |    |
| R/W-0h    |    |    |    |    |    |    | R/W-0h    |    | R/W-0h          |    |    |

LEGEND: R/W = Read/Write; R = Read only

**表 8-57. Matrix Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description   |
|-------|-----------------|------|-------|---|
| 23-17 | RESERVED        | R    | 0h    | Reserved  |
| 16-15 | IN_COM_EN       | R/W  | 0h    | 0h = no interrupt generation for w.r.t. threshold THRES_COM<br>1h = interrupt generation on rising edge above threshold THRES_COM<br>2h = interrupt generation on falling edge below threshold THRES_COM<br>3h = interrupt generation on falling and rising edge of threshold THRES_COM |
| 14-5  | THRES_COM       | R/W  | 0h    | 10-bits value of threshold THRES_COM:<br>Bit5: LSB<br>Bit14: MSB  |
| 4-3   | MATRIX          | R/W  | 0h    | 0h = no matrix, regular inputs only<br>1h = 4×4 matrix<br>2h = 5×5 matrix<br>3h = 6×6 matrix  |
| 2-0   | POLL_ACT_TIME_M | R/W  | 0h    | Polling active time setting for the matrix inputs:<br>0h = 64 μs<br>1h = 128 μs<br>2h = 256 μs<br>3h = 384 μs<br>4h = 512 μs<br>5h = 768 μs<br>6h = 1024 μs<br>7h = 1360 μs   |

### 8.6.47 Mode Register (Offset = 32h) [Reset = 0h]

Mode is shown in 图 8-70 and described in 表 8-58.

Return to [Summary Table](#).

图 8-70. Mode Register

| 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     | 15     | 14     | 13     | 12     |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| M_IN23 | M_IN22 | M_IN21 | M_IN20 | M_IN19 | M_IN18 | M_IN17 | M_IN16 | M_IN15 | M_IN14 | M_IN13 | M_IN12 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 11     | 10     | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| M_IN11 | M_IN10 | M_IN9  | M_IN8  | M_IN7  | M_IN6  | M_IN5  | M_IN4  | M_IN3  | M_IN2  | M_IN1  | M_IN0  |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write

表 8-58. Mode Register Field Descriptions

| Bit | Field  | Type | Reset | Description   |
|-----|--------|------|-------|---|
| 23  | M_IN23 | R/W  | 0h    | 0h = comparator mode for IN23<br>1h = ADC mode for IN23 |
| 22  | M_IN22 | R/W  | 0h    | 0h = comparator mode for IN22<br>1h = ADC mode for IN22 |
| 21  | M_IN21 | R/W  | 0h    | 0h = comparator mode for IN21<br>1h = ADC mode for IN21 |
| 20  | M_IN20 | R/W  | 0h    | 0h = comparator mode for IN20<br>1h = ADC mode for IN20 |
| 19  | M_IN19 | R/W  | 0h    | 0h = comparator mode for IN19<br>1h = ADC mode for IN19 |
| 18  | M_IN18 | R/W  | 0h    | 0h = comparator mode for IN18<br>1h = ADC mode for IN18 |
| 17  | M_IN17 | R/W  | 0h    | 0h = comparator mode for IN17<br>1h = ADC mode for IN17 |
| 16  | M_IN16 | R/W  | 0h    | 0h = comparator mode for IN16<br>1h = ADC mode for IN16 |
| 15  | M_IN15 | R/W  | 0h    | 0h = comparator mode for IN15<br>1h = ADC mode for IN15 |
| 14  | M_IN14 | R/W  | 0h    | 0h = comparator mode for IN14<br>1h = ADC mode for IN14 |
| 13  | M_IN13 | R/W  | 0h    | 0h = comparator mode for IN13<br>1h = ADC mode for IN13 |
| 12  | M_IN12 | R/W  | 0h    | 0h = comparator mode for IN12<br>1h = ADC mode for IN12 |
| 11  | M_IN11 | R/W  | 0h    | 0h = comparator mode for IN11<br>1h = ADC mode for IN11 |
| 10  | M_IN10 | R/W  | 0h    | 0h = comparator mode for IN10<br>1h = ADC mode for IN10 |
| 9   | M_IN9  | R/W  | 0h    | 0h = comparator mode for IN9<br>1h = ADC mode for IN9   |
| 8   | M_IN8  | R/W  | 0h    | 0h = comparator mode for IN8<br>1h = ADC mode for IN8   |

**表 8-58. Mode Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description   |
|-----|-------|------|-------|---|
| 7   | M_IN7 | R/W  | 0h    | 0h = comparator mode for IN7<br>1h = ADC mode for IN7 |
| 6   | M_IN6 | R/W  | 0h    | 0h = comparator mode for IN6<br>1h = ADC mode for IN6 |
| 5   | M_IN5 | R/W  | 0h    | 0h = comparator mode for IN5<br>1h = ADC mode for IN5 |
| 4   | M_IN4 | R/W  | 0h    | 0h = comparator mode for IN4<br>1h = ADC mode for IN4 |
| 3   | M_IN3 | R/W  | 0h    | 0h = comparator mode for IN3<br>1h = ADC mode for IN1 |
| 2   | M_IN2 | R/W  | 0h    | 0h = comparator mode for IN2<br>1h = ADC mode for IN0 |
| 1   | M_IN1 | R/W  | 0h    | 0h = comparator mode for IN1<br>1h = ADC mode for IN1 |
| 0   | M_IN0 | R/W  | 0h    | 0h = comparator mode for IN0<br>1h = ADC mode for IN0 |

## 8.7 Programming Guidelines

When configuring the TIC12400-Q1, it is critical to follow the programming guideline summarized below (see [表 8-59](#)) to ensure proper behavior of the device:

**表 8-59. TIC12400-Q1 Programming Guidelines**

| Category   | Programming requirement  |
|--|--|
| Threshold setup:<br><ul style="list-style-type: none"> <li>Continuous mode</li> <li>Regular polling mode</li> <li>Matrix mode (non-matrix inputs)</li> </ul> | <ul style="list-style-type: none"> <li><math>THRES2B \geq THRES2A</math> (for IN12 to IN17)</li> <li><math>THRES3C \geq THRES3B \geq THRES3A</math> (for IN18 to IN22)</li> <li><math>THRES9 \geq THRES8 \geq THRES3C \geq THRES3B \geq THRES3A</math> (for IN23)</li> </ul> |
| Threshold setup:<br><ul style="list-style-type: none"> <li><math>V_S</math> measurement</li> </ul>   | <ul style="list-style-type: none"> <li><math>VS0\_THRES2B \geq VS0\_THRES2A</math></li> <li><math>VS1\_THRES2B \geq VS1\_THRES2A</math></li> </ul>   |

表 8-59. TIC12400-Q1 Programming Guidelines (continued)

| Category                               | Programming requirement   |
|--|---|
| 4×4 Matrix mode (MATRIX [4:3] = 2'b01) | <ul style="list-style-type: none"> <li>POLL_EN=1</li> <li>IN_EN[7:4]=4' b1111; IN_EN[13:10]= 4' b1111</li> <li>MODE[7:4] = 4' b0000; MODE[13:10] = 4' b0000</li> <li>CS_SELECT[7:4]= 4' b1111; CS_SELECT[13:10]= 4' b0000</li> <li>IWETT(CSI) &gt; IWETT (CSO): <ol style="list-style-type: none"> <li>WC_CFG0[20:18] &lt; WC_CFG0[8:6]</li> <li>WC_CFG0[23:21] &lt; WC_CFG0[11:9]</li> <li>WC_CFG1[2:0] &gt; WC_CFG0[14:12]</li> </ol> </li> <li>If TW event is expected, CSO can only be set to 1 mA or 2 mA: <ol style="list-style-type: none"> <li>If WC_CFG0[8:6]= 3' b001: WC_CFG0[20:18]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[8:6]= 3' b010: WC_CFG0[20:18] = 3' b011</li> <li>If WC_CFG0[11:9]= 3' b001: WC_CFG0[23:21]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[11:9]= 3' b010: WC_CFG0[23:21] = 3' b011</li> <li>If WC_CFG1[2:0]= 3' b001: WC_CFG0[14:12]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG1[2:0]= 3' b010: WC_CFG0[14:12] = 3' b011</li> </ol> </li> </ul>   |
| 5×5 Matrix mode (MATRIX [4:3] = 2'b10) | <ul style="list-style-type: none"> <li>POLL_EN=1</li> <li>IN_EN[8:4]= 5' b11111; IN_EN[14:10]= 5' b11111</li> <li>MODE[8:4] = 5' b00000; MODE[14:10] = 5' b00000</li> <li>CS_SELECT[8:4]= 5' b11111; CS_SELECT[14:10]= 5' b00000</li> <li>IWETT(CSI) &gt; IWETT (CSO): <ol style="list-style-type: none"> <li>WC_CFG0[20:18] &lt; WC_CFG0[8:6]</li> <li>WC_CFG0[23:21] &lt; WC_CFG0[11:9]</li> <li>WC_CFG1[2:0] &gt; WC_CFG0[14:12]</li> <li>WC_CFG1[5:3] &gt; WC_CFG0[17:15]</li> </ol> </li> <li>If TW event is expected, CSO can only be set to 1 mA or 2 mA: <ol style="list-style-type: none"> <li>If WC_CFG0[8:6]= 3' b001: WC_CFG0[20:18]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[8:6]= 3' b010: WC_CFG0[20:18] = 3' b011</li> <li>If WC_CFG0[11:9]= 3' b001: WC_CFG0[23:21]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[11:9]= 3' b010: WC_CFG0[23:21] = 3' b011</li> <li>If WC_CFG1[2:0]= 3' b001: WC_CFG0[14:12]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG1[2:0]= 3' b010: WC_CFG0[14:12] = 3' b011</li> <li>If WC_CFG1[5:3]= 3' b001: WC_CFG0[17:15]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG1[5:3]= 3' b010: WC_CFG0[17:15] = 3' b011</li> </ol> </li> </ul> |



**表 8-59. TIC12400-Q1 Programming Guidelines (continued)**

| Category   | Programming requirement   |
|--|---|
| 6×6 Matrix mode (MATRIX [4:3]= 2' b11)   | <ul style="list-style-type: none"> <li>POLL_EN=1</li> <li>IN_EN[9:4]= 6' b111111; IN_EN[15:10]= 6' b111111</li> <li>MODE[9:4]= 6' b000000; MODE[15:10]= 6' b000000</li> <li>CS_SELECT[9:4]= 6' b111111; CS_SELECT[15:10]= 6' b000000</li> <li>IWETT(CSI) &gt; IWETT (CSO):               <ol style="list-style-type: none"> <li>WC_CFG0[20:18] &lt; WC_CFG0[8:6]</li> <li>WC_CFG0[23:21] &lt; WC_CFG0[11:9]</li> <li>WC_CFG1[2:0] &gt; WC_CFG0[14:12]</li> <li>WC_CFG1[5:3] &gt; WC_CFG0[17:15]</li> </ol> </li> <li>If TW event is expected, CSO can only be set to 1 mA or 2 mA:               <ol style="list-style-type: none"> <li>If WC_CFG0[8:6]= 3' b001: WC_CFG0[20:18]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[8:6]= 3' b010: WC_CFG0[20:18]= 3' b011</li> <li>If WC_CFG0[11:9]= 3' b001: WC_CFG0[23:21]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG0[11:9]= 3' b010: WC_CFG0[23:21]= 3' b011</li> <li>If WC_CFG1[2:0]= 3' b001: WC_CFG0[14:12]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG1[2:0]= 3' b010: WC_CFG0[14:12]= 3' b011</li> <li>If WC_CFG1[5:3]= 3' b001: WC_CFG0[17:15]= 3' b010, 3' b011, 3' b100, 3' b101, 3' b110, or 3' b111; If WC_CFG1[5:3]= 3' b010: WC_CFG0[17:15]= 3' b011</li> </ol> </li> </ul> |
| Clean Current Polling (if CCP_INx= 1 in the CCP_CFG1 register)                                   | At least one input (standard or matrix) or the VS measurement has to be enabled: IN_EN_x= 1 in the IN_EN register or CONFIG [16]= 1' b1 <sup>(1)</sup>  |
| Wetting current auto-scaling (if WC_CFG1 [22:21] != 2b' 11)                                      | <ul style="list-style-type: none"> <li>The wetting current auto-scaling feature is only activated in the continuous mode: POLL_EN= 0<sup>(2)</sup></li> <li>The wetting current auto-scaling only applies to 10 mA or 15 mA wetting currents: WC_INx bits = 3' b100, 3' b101, 3' b110, or 3' b111 in the WC_CFG0 and WC_CFG1 registers.<sup>(2)</sup></li> </ul>  |
| Wetting current diagnostic (If CONFIG [21:18] != 4b' 0000)                                       | <ul style="list-style-type: none"> <li>At least one channel has to be enabled from IN0 to IN3 (IN_EN[3:0] != 4b' 0000)</li> <li>Inputs IN0 to IN3 need to be configured to ADC input mode: MODE[3:0]= 4' b1111</li> <li>Inputs IN0 and IN1 need to be configured to CSO: CS_SELECT [1:0]= 2b' 00</li> <li>Inputs IN2 and IN3 need to be configured to CSI: CS_SELECT [3:2]= 2b' 11</li> </ul>   |
| <ul style="list-style-type: none"> <li>Continuous mode</li> <li>Standard polling mode</li> </ul> | <p>t<sub>POLL_TIME</sub> and t<sub>POLL_ACT_TIME</sub> settings have to meet the below requirement: t<sub>POLL_TIME</sub> ≥ 1.3 × [ t<sub>POLL_ACT_TIME</sub> + n × 24 μs + 10 μs ]<sup>(3) (4)</sup></p> <ul style="list-style-type: none"> <li>n: the number of enabled channels configured in register IN_EN</li> <li>t<sub>POLL_TIME</sub>: timing setting configured in CONFIG[4:1]</li> <li>t<sub>POLL_ACT_TIME</sub>: timing setting configured in CONFIG[8:5]</li> </ul>  |
| Matrix polling mode  | <p>t<sub>POLL_TIME</sub>, t<sub>POLL_ACT_TIME</sub>, and t<sub>POLL_ACT_TIME_M</sub> settings have to meet the below requirement: t<sub>POLL_TIME</sub> &gt; 1.3 × [ m × t<sub>POLL_ACT_TIME_M</sub> + t<sub>POLL_ACT_TIME</sub> + n × 24 μs + 10 μs ]<sup>(3) (4)</sup></p> <ul style="list-style-type: none"> <li>n: the number of enabled channels configured in register IN_EN</li> <li>m: 16 for 4×4 matrix; 25 for 5×5 matrix; 36 for 6×6 matrix</li> <li>t<sub>POLL_TIME</sub>: timing setting configured in CONFIG[4:1]</li> <li>t<sub>POLL_ACT_TIME_M</sub>: timing setting configured in MATRIX[2:0]</li> <li>t<sub>POLL_ACT_TIME</sub>: timing setting configured in CONFIG[8:5]</li> </ul>  |

(1) This is a soft requirement to take advantage of the clean current polling feature. The feature takes no effect otherwise.

- (2) These are soft requirements to take advantage of the wetting current auto-scaling feature. The feature takes no effect otherwise.
- (3) If WCD is enabled, add additional 96  $\mu$ s
- (4) If CCP is enabled, add tCCP\_TRAN + tCCP\_TIME, where tCCP\_TIME is the timing setting configured in CCP\_CFG0[6:4]

## 9 Application Information Disclaimer

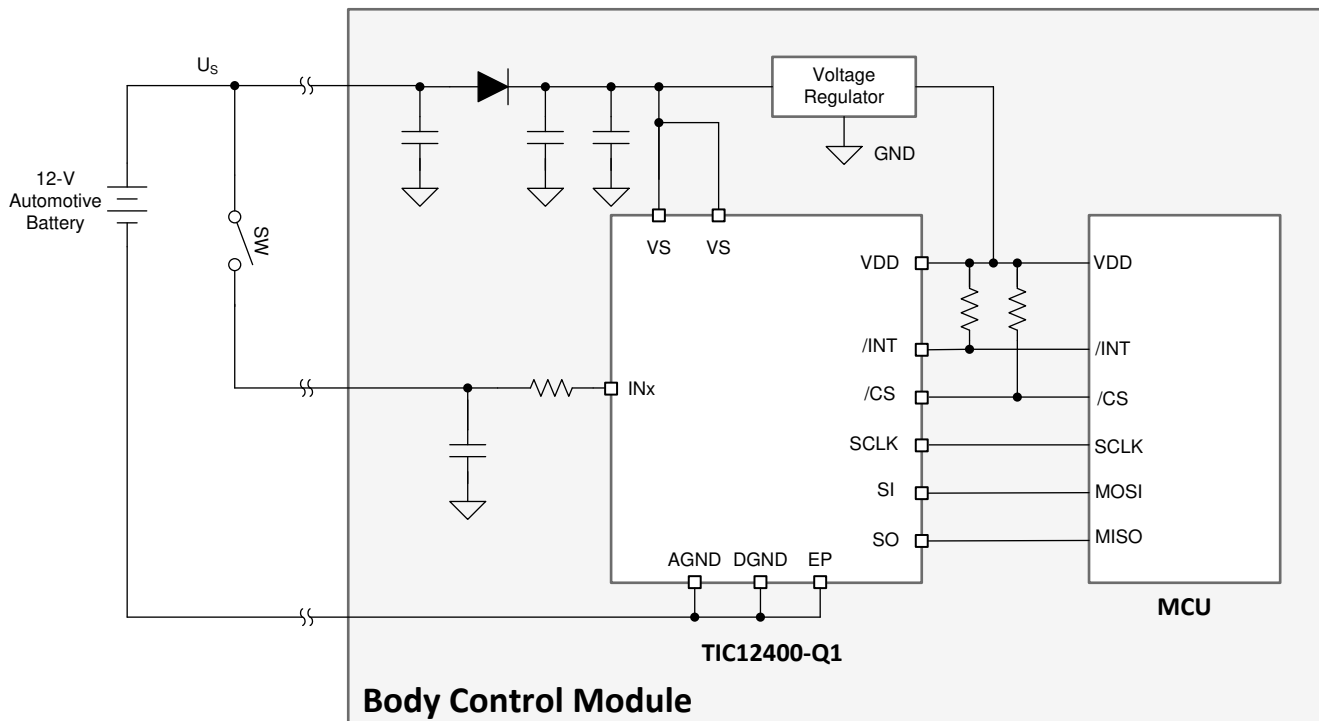
### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TIC12400-Q1 is an advanced 24-input Multiple Switch Detection Interface (MSDI) device designed to detect external mechanical switch status in a 12-V automotive system by acting as an interface between the switches and the low-voltage microcontroller. The device offers a number of unique features to replace systems implemented with discrete components, saving board space and reducing the bill of materials (BOM). The device can also be configured into low-power polling mode, which provides significant savings on system power consumption.

### 9.2 Using TIC12400-Q1 in a 12 V Automotive System



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**图 9-1. Typical System Diagram of Battery Connections for TIC12400-Q1**

The TIC12400-Q1 is designed to operate with a 12 V automotive system. 图 9-1 depicts a typical system diagram to show how the device is connected to the battery. Remember to be careful when connecting the battery directly to the device on the VS supply pin (through a reverse-blocking diode) or the input (INx) pins since an automotive battery can be subjected to various transient and over-voltage events. Manufacturers have independently created standards and test procedures in an effort to prevent sensitive electronics from failing due to these events. Recently, combined efforts are made with ISO to develop the ISO 16750-2 standard (Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 2: Electrical loads), which describe the possible transients that could occur to an automotive battery and specify test methods to simulate them.

It shall be noted that the TIC12400-Q1 is designed and tested according to the ISO 16750-2 standard. A few voltage stress tests and their test conditions are listed below. Exposing the device to more severe transient events than described by the standard could potentially causes performance degradation and long-term damage to the device.

- Direct current supply voltage:  $V_{BAT, min} = 6\text{ V}$ ;  $V_{BAT, max} = 16\text{ V}$
- To emulate a jump start event, voltage profile described in 图 9-2 is used.

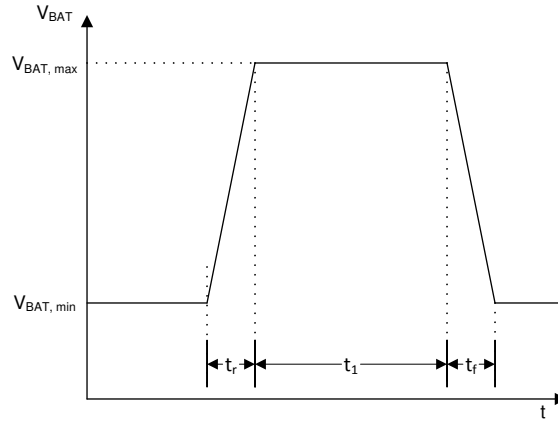


图 9-2. Voltage Profile to Test a Jump Start Event

表 9-1. Voltage Profile Parameters to Test a Jump Start Event

| Parameter        | Value          |
|------------------|----------------|
| $V_{BAT, min}$   | 10.8 V         |
| $V_{BAT, max}$   | 24 V           |
| $t_r$            | < 10 ms        |
| $t_1$            | 60 s $\pm$ 6 s |
| $t_f$            | < 10 ms        |
| Number of cycles | 1              |

- To emulate a load dump event for an alternator with centralized load dump suppression, voltage profile described below is used.  $U_A$  and  $U_S^*$  are applied directly to  $V_{BAT}$ .

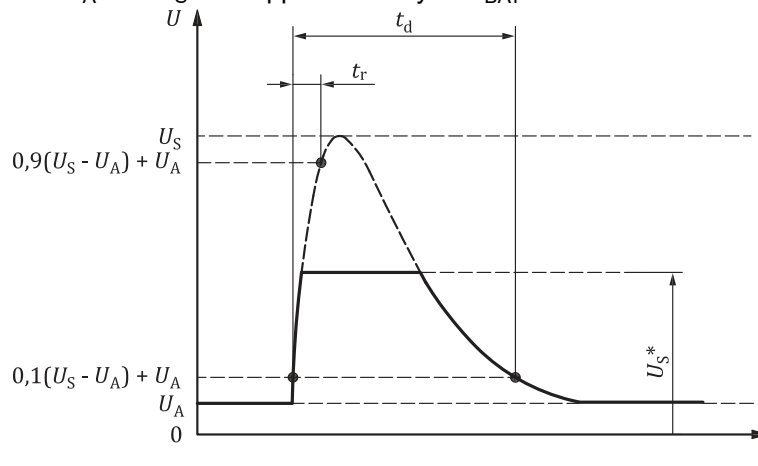


图 9-3. Voltage Profile to Test a Load Dump Event with Centralized Load Dump Suppression

- To emulate a cranking event, voltage profile describe below is used.  $U_S$ ,  $U_{S6}$ , and  $U_A$  are applied directly to  $V_{BAT}$ .



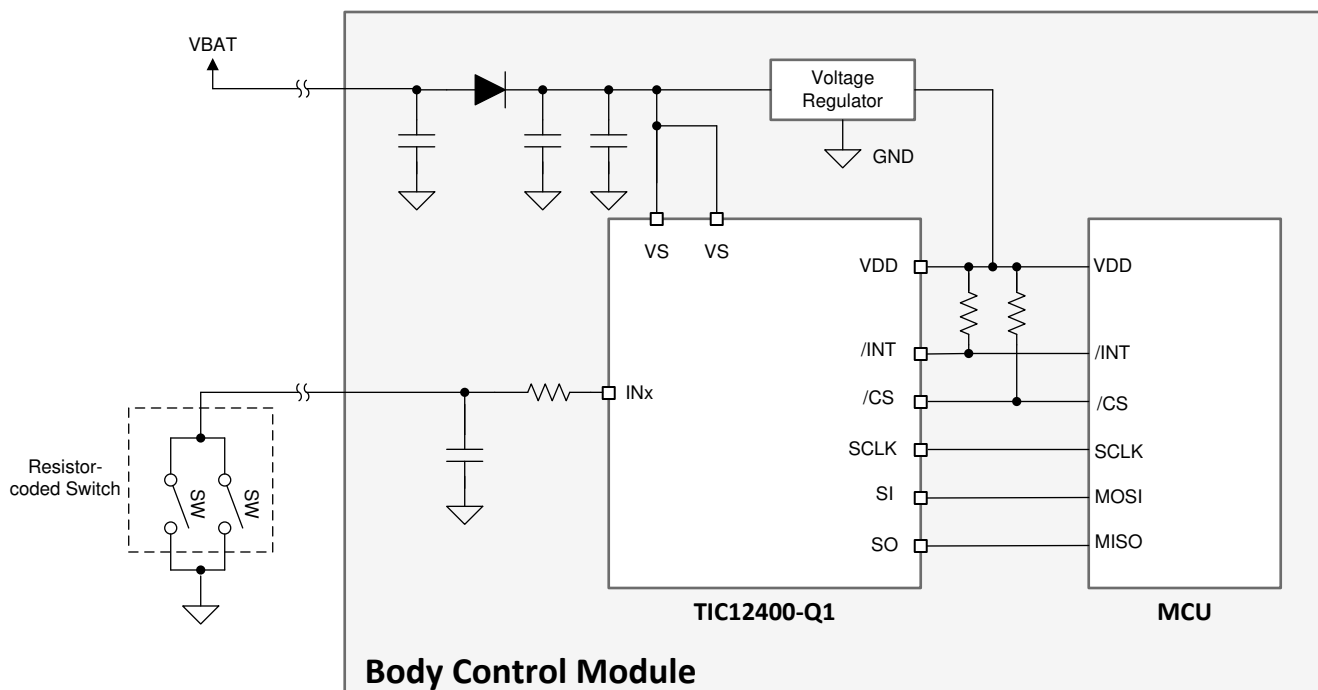
### 表 9-3. Voltage Profile Used to Test a Cranking Event

### 9.3 Resistor-coded Switches Detection in Automotive Body Control Module

The body control module (BCM) is an electronic control unit responsible for monitoring and controlling various electronic accessories in a vehicle's body. Detection of various mechanical switches status in a vehicle is one important task handled by the BCM. Besides the typical on-and-off (or digital) type of switch, more sophisticated type of switches, called resistor-coded switches, can also be present in an automotive body control system.

Resistor-coded switches have more than 2 unique switch states, and are often used for implementation of wiper, illumination, and signal control arms in a vehicle. Due to various voltage potentials generated by different positions of a resistor-coded switch, an ADC, typically inside the microcontroller, is used to detect the different

states of the switch. The TIC12400-Q1 can natively support monitoring of a resistor-coded switch with its integrated 10-bit ADC and configurable thresholds. The following application diagram depicts how the TIC12400-Q1 is used in a BCM to detect external mechanical resistor-coded switches and a detailed design example is shown in the following sections.



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图 9-5. Using TIC12400-Q1 to Monitor a Resistor-Coded Switch in Body Control Module Application

### 9.3.1 Design Requirements

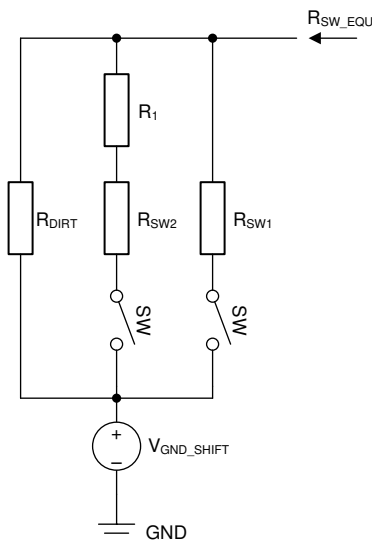


图 9-6. Example 3-state Resistor-Coded Switch

表 9-4. Example Resistor-Coded Switch Specification

|           | SPECIFICATION                              | MIN            | MAX            |
|-----------|--|----------------|----------------|
| $V_{BAT}$ | $9\text{ V} \leq V_{BAT} \leq 16\text{ V}$ | 9 V            | 16 V           |
| $R_1$     | $680\ \Omega \pm 8\%$                      | 625.6 $\Omega$ | 734.4 $\Omega$ |

**表 9-4. Example Resistor-Coded Switch Specification (continued)**

|                        | SPECIFICATION        | MIN    | MAX  |
|------------------------|----------------------|--------|------|
| R <sub>SW1</sub>       | 50 Ω Max when closed | 0 Ω    | 50 Ω |
| R <sub>SW2</sub>       | 50 Ω Max when closed | 0 Ω    | 50 Ω |
| R <sub>DIRT</sub>      | 5000 Ω Min           | 5000 Ω | ∞    |
| V <sub>GND_SHIFT</sub> | ±1 V                 | -1 Ω   | +1 Ω |

An example of a 3-state resistor-coded switch is shown in 图 9-6, with 表 9-4 summarizing its detailed specification. The goal of this design is to utilize the TIC12400-Q1's integrated ADC to detect and differentiate the 3 switch states:

1. State 1: Both SW1 and SW2 open.
2. State 2: SW1 open and SW2 close.
3. State 3: SW1 close and SW2 open.

To mimic real automotive systems, the battery is assumed to be fluctuating between 9 V and 16 V. R<sub>DIRT</sub> is introduced to model the small leakage flowing across the switch in open state. There is also a ±1 V ground shift present in the system, meaning there could be up to ±1 V of potential difference between the switch reference point and the ground reference of the TIC12400-Q1. When the switch changes position and the switch state changes from one to another, the TIC12400-Q1 is required to correctly detect the state transition and issue an interrupt to alert the microcontroller. The switch information needs to be stored in the status registers for the microcontroller to retrieve.

### 9.3.2 Detailed Design Procedure

**表 9-5. Detailed Design Procedure**

|                                  | STEP 1                          |        | STEP 2               |       | STEP 3  |       | STEP 4          |     | STEP 5    |
|----------------------------------|---------------------------------|--------|----------------------|-------|---|-------|-----------------|-----|-----------|
|                                  | Equivalent Resistance Value (Ω) |        | V <sub>INX</sub> (V) |       | V <sub>INX</sub> + V <sub>GND_SHIFT</sub> (V) |       | ADC Code Spread |     | Threshold |
|                                  | MIN                             | MAX    | MIN                  | MAX   | MIN   | MAX   | MIN             | MAX |           |
| State 1: Both SW1 and SW2 open   | 5000                            | ∞      | > 6 V                | -     | >6 V  | -     | 1023            | -   |           |
| State 2: SW1 open and SW2 closed | 555.95                          | 678.03 | 2.502                | 3.729 | 1.502   | 4.729 | 256             | 806 | 915       |
| State 3: SW1 closed and SW2 open | 0                               | 49.5   | 0                    | 0.272 | 0   | 1.272 | 0               | 217 | 237       |

use the following procedures to calculate thresholds to program to the TIC12400-Q1 for proper switch detection:

1. Calculate the equivalent resistance values at different switch states, taking into account R<sub>DIRT</sub> and the 8% resistance variation.
2. Estimate the voltage established when wetting current flows through the switch by utilizing the relationship  $V_{INX} = R_{SW\_EQU} \times I_{WETT\_ACT}$ , where R<sub>SW\_EQU</sub> is the equivalent switch resistance value and I<sub>WETT\_ACT</sub> is the actual wetting current flowing through the switch. The 5 mA wetting current setting is selected in this design, because it best uses the dynamic range of the ADC (from 0 to 6 V). The wetting current, however, can vary depending on manufacturing process variation and operating temperature, and needs to be taken into account. Referring to the electrical table of the TIC12400-Q1 and assuming enough headroom for the current source (CSO) to operate, the 5 mA wetting current setting produces current ranging between 4.5 mA and 5.5 mA (for V<sub>S</sub> - I<sub>Nx</sub> ≥ 3 V condition). The voltage established on the TIC12400-Q1 input pin (V<sub>INX</sub>) can be calculated accordingly.
3. Take the ground shift non-ideality into account. As defined in 节 9.3.1, the ground shift can vary between ±1 V. Therefore, effectively, the actual voltage seen at the TIC12400-Q1 can also vary up to ±1 V.
4. Convert the voltage established on the INx pin into equivalent ADC code. The full-scale range of the 10-bit ADC is from 0 V to 6 V, with 6 V corresponding to the max code of 1023. Therefore, the ADC code spread for each of the 3 different switch states can be calculated accordingly.

5. After the ADC code spread for each switch state is calculated, the detection threshold can be chosen to be the mid-point between the upper and lower codes of two neighboring states to give best margin for detection.

### 9.3.3 Application Curves

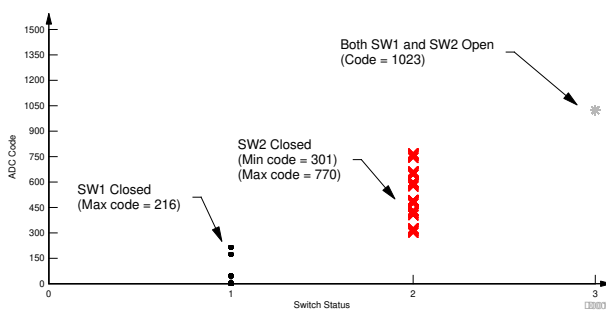


图 9-7. Measured ADC Code Distribution for the 3 Switch States



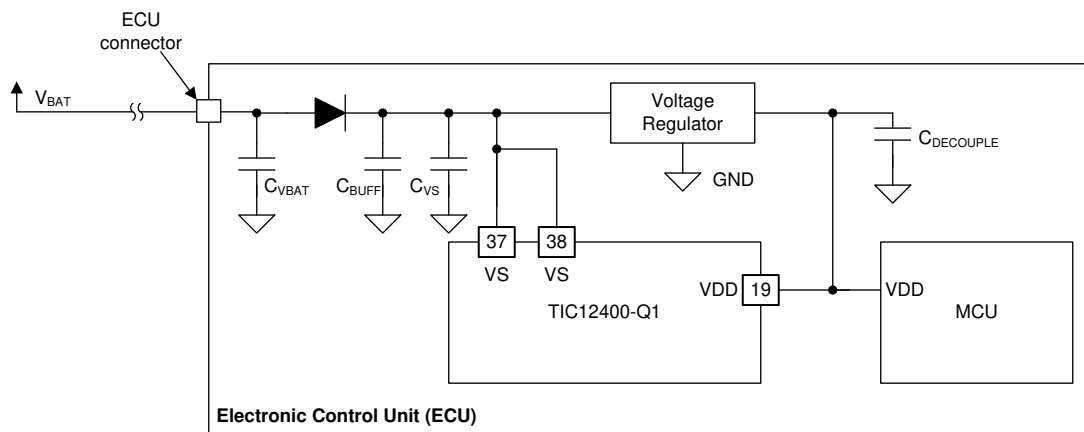
## 10 Power Supply Recommendations

There are two supply input pins for the TIC12400-Q1:  $V_S$  and  $V_{DD}$ .  $V_S$  is the main power supply for the entire chip and is essential for all critical functions of the device. The  $V_S$  supply is designed to be connected to a 12-V automotive battery (through a reverse blocking diode) with nominal operating voltage no greater than 16 V. The  $V_{DD}$  supply is used to determine the logic level on the SPI communication interface, source the current for the SO driver, and sets the pull-up voltage for the /CS pin. It can also be used as a possible external pull-up supply for the /INT pin as an alternative to the  $V_S$  supply and it shall be connected to a 3 V to 5.5 V logic supply. Removing  $V_{DD}$  from the device disables SPI communications, but does not impact normal operation of the device.

To improve stability of the supply inputs, some decoupling capacitors are recommended on the PCB. 图 10-1 shows an example on the on-board power supply decoupling scheme. The battery voltage ( $V_{BAT}$ ) is decoupled on the Electronic Control Unit (ECU) board using a large decoupling capacitor ( $C_{BUFF}$ ). The diode is installed to prevent damage to the internal system under reversed battery condition.  $C_{VS}$  shall be installed close to the TIC12400-Q1 for best decoupling performance. The voltage regulator provides a regulated voltage for the digital portion of the device and for the local microcontroller and its output is decoupled with  $C_{DECOUPLE}$ . 表 10-1 lists recommended values for each individual decoupling capacitor shown in the system diagram.

**表 10-1. Decoupling Capacitor Recommendations**

| CRC RULE       | VALUE                               |
|----------------|-------------------------------------|
| $C_{BUFF}$     | 100 $\mu$ F, 50 V rated, $\pm 20\%$ |
| $C_{VBAT}$     | 100 nF, 50V rated, $\pm 10\%$ ; X7R |
| $C_{VS}$       | 100 nF, 50 V rated                  |
| $C_{DECOUPLE}$ | 100 nF $\approx$ 1 $\mu$ F          |




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**图 10-1. Recommended Power Supply Decoupling**

## 11 Layout

### 11.1 Layout Guidelines

1.  11-1 illustrates an example of a PCB layout with the TIC12400-Q1. Some key considerations are:
2. Decouple the  $V_S$  and  $V_{DD}$  pins with capacitor using recommended values from section [Power Supply Recommendations](#) and place them as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the  $V_S$  and  $V_{DD}$  supplies.
3. Keep the input lines as short as possible.
4. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
5. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
6. To achieve good thermal performance, the exposed thermal pad underneath the device must be soldered to the board and flooded with vias to ground planes. For simple double-sided PCBs where there are no internal layers, the surface layers can be used to remove heat. For multilayer PCBs, internal ground planes can be used for heat removal.
7. Minimize the inductive parasitic between the INx input capacitors and the thermal pad ground return.



## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TIC12400QDCPRQ1</a> | Active        | Production           | HTSSOP (DCP)   38 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | TIC12400Q           |
| TIC12400QDCPRQ1.A               | Active        | Production           | HTSSOP (DCP)   38 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | TIC12400Q           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF TIC12400-Q1 :

- Catalog : [TIC12400](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TIC12400QDCPRQ1 | HTSSOP       | DCP             | 38   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TIC12400QDCPRQ1 | HTSSOP       | DCP             | 38   | 2000 | 350.0       | 350.0      | 43.0        |



## GENERIC PACKAGE VIEW

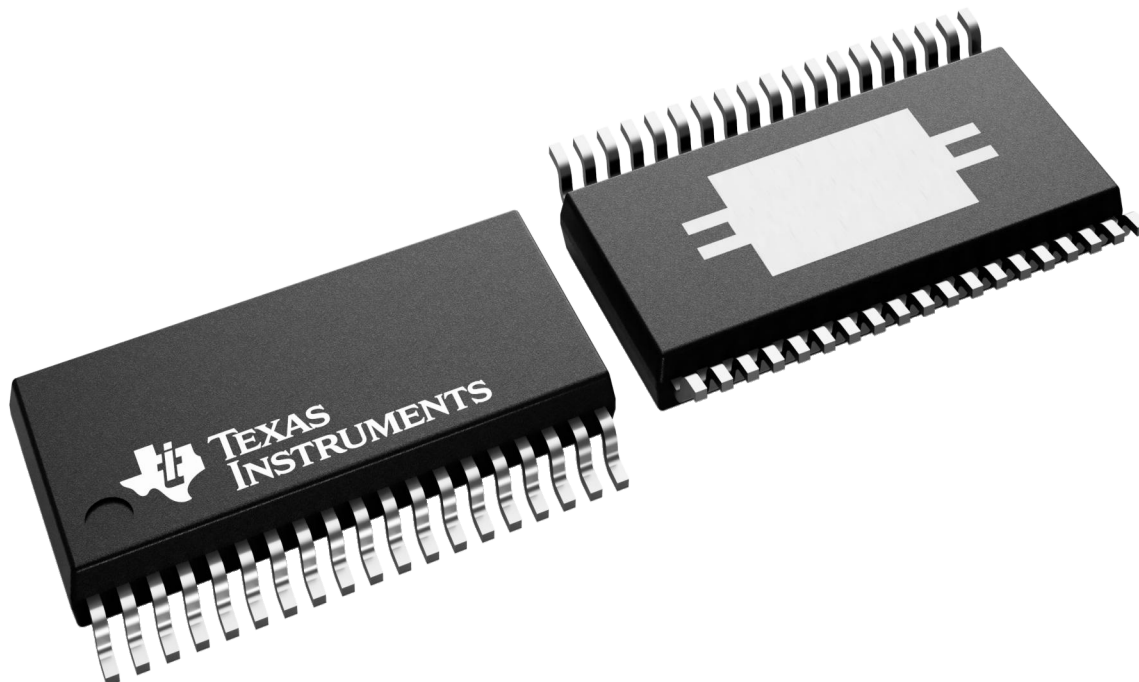
**DCP 38**

**PowerPAD TSSOP - 1.2 mm max height**

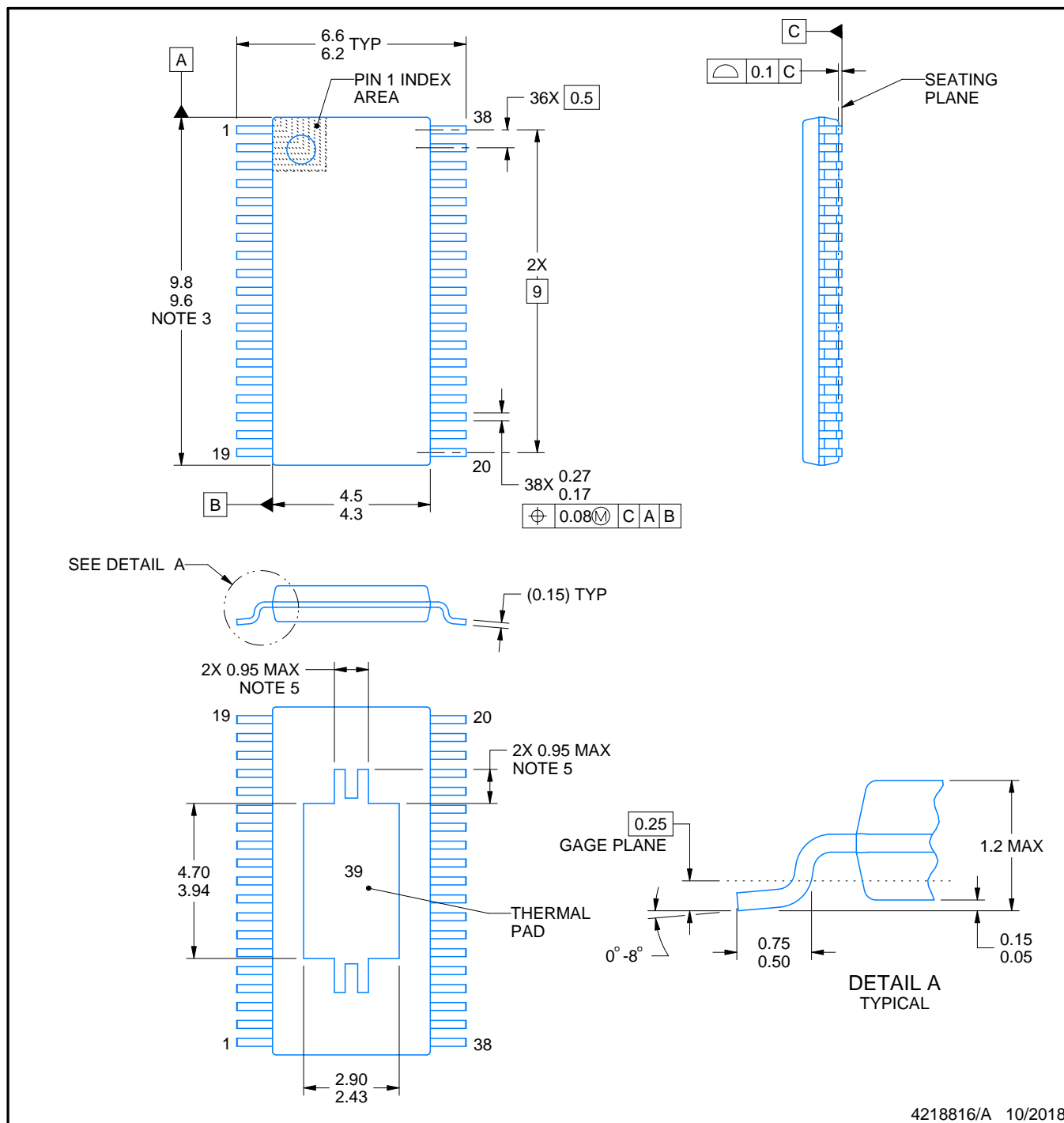
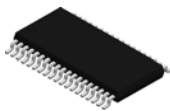
4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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**NOTES:**

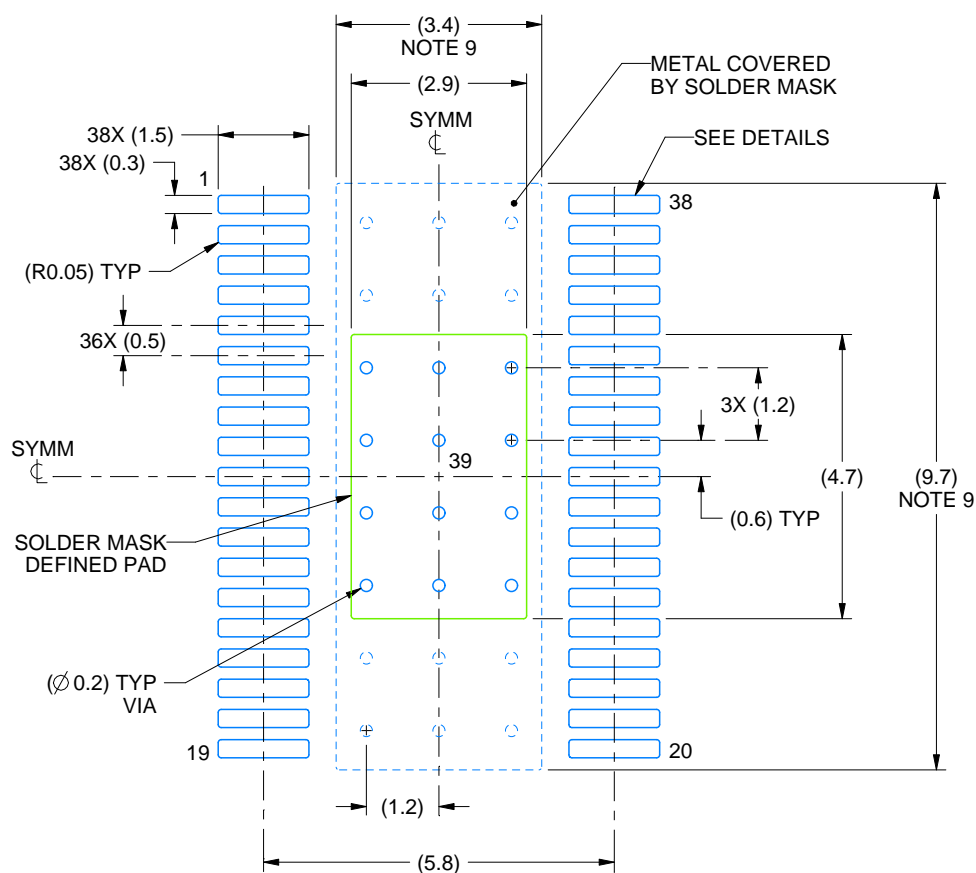
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

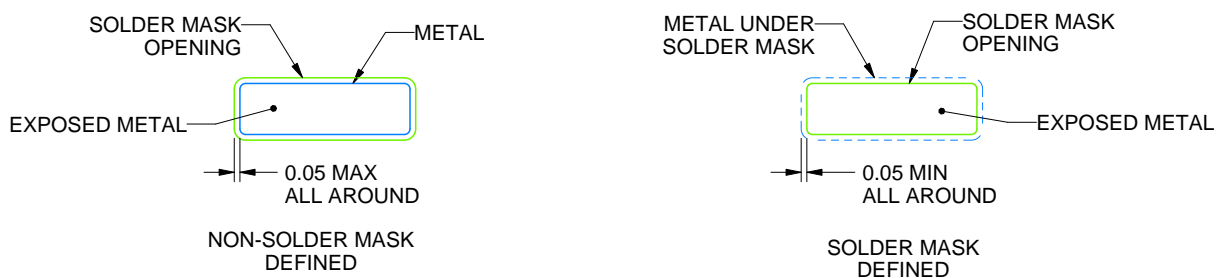
**DCP0038A**

## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



## SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

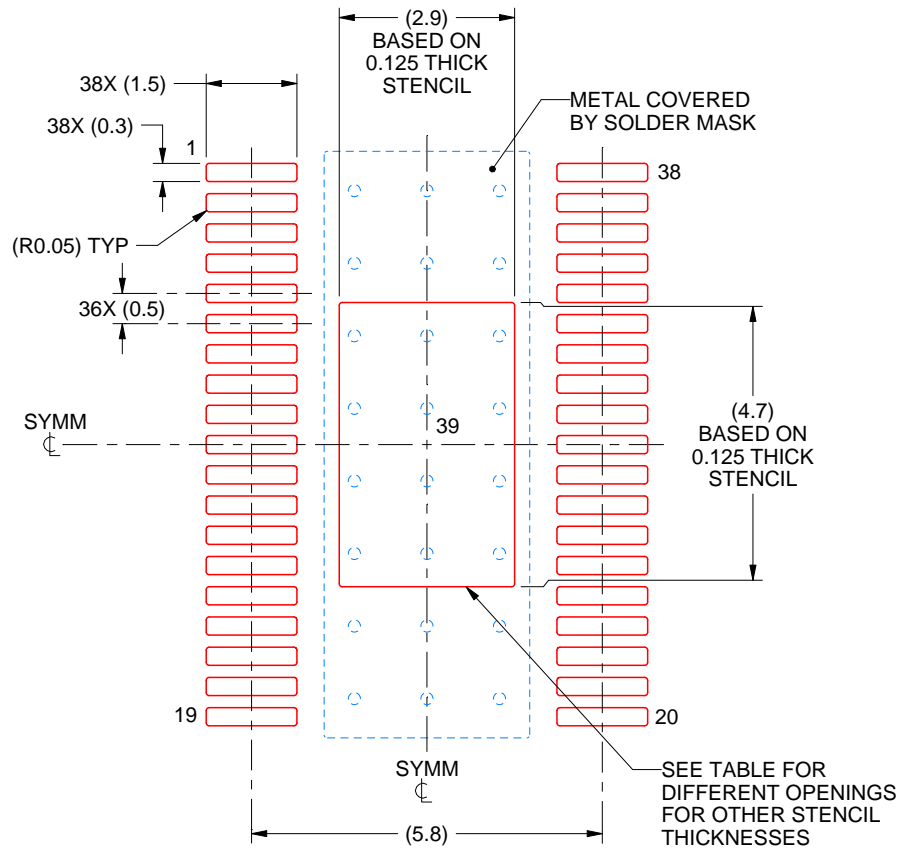
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.24 X 5.25            |
| 0.125             | 2.90 X 4.70 (SHOWN)    |
| 0.15              | 2.65 X 4.29            |
| 0.175             | 2.45 X 3.97            |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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