RF430CL330H 动态近场通信 (NFC) 接口应答器

1 器件概述

1.1 特性

- NFC 标签类型 4
- 符合 ISO14443B 标准的 13.56MHz (RF) 接口支持高达 848kbps
- 串行外设接口 (SPI) 或 I^2C 接口将近场通信数据交换格式 (NDEF) 消息写入内部 SRAM 并从中读取此消息
- 为 NDEF 消息提供 3KB SRAM
- NDEF 结构的自动校验
- 中断寄存器和输出引脚以表示 NDEF 读取或写入完成

1.2 应用

- *Bluetooth*® 配对
- Wi-Fi® 配置
- 诊断接口
- 传感器接口

1.3 说明

德州仪器 (TI) 动态 NFC 接口应答器 RF430CL330H 是一款 NFC 标签类型 4 器件，可结合一个无线 NFC 接口和一个有线 SPI 或 I^2C 接口将器件连接到主机。 SRAM 中的 NDEF 消息可通过集成的 SPI 或 I^2C 串行通信接口读写，也可通过支持高达 848kbps 速率的集成 ISO14443B 标准射频接口无线访问或更新。

这种工作方式可以直观地简化备用载波的 NFC 连接切换，例如，只需轻轻点击即可完成*蓝牙*、低功耗*蓝牙* (BLE) 和 Wi-Fi 配对过程或验证过程。 作为一个常见 NFC 接口，RF430CL330H 使得终端设备能够与启用 NFC 的智能手机、平板电脑和笔记本电脑这类快速增长的基础设施进行通信。

表 **1-1.** 器件信息(1)

器件型号	封装	封装尺寸(2)
RF430CL330HPW	TSSOP (14)	5mm x 4.4mm
RF430CL330HRGT	VQFN (16)	3mm x 3mm

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见节 7中的*封装选项附录*或浏览 TI 网站 www.ti.com.cn。

(2) 这里显示的尺寸为近似值。 要获得包含误差值的封装尺寸，请参见节 7中的*机械数据*。

1.4 典型应用图

图 1-1 显示了 RF430CL330H 器件的典型应用图。

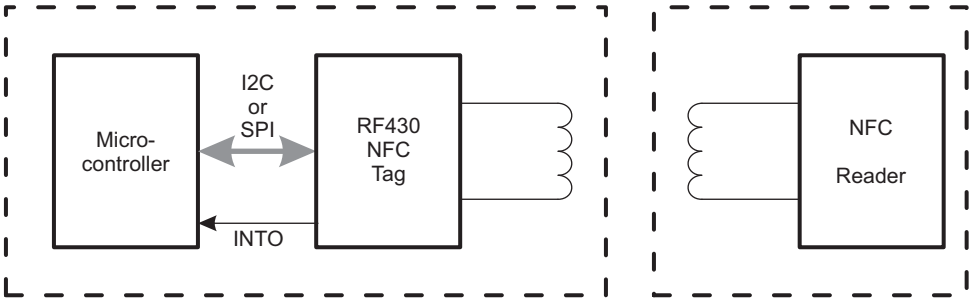


图 **1-1.** 典型应用

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

内容

1 器件概述 **1**
1.1 特性 1
1.2 应用 1
1.3 说明 1
1.4 典型应用图 1
2 修订历史记录 **2**
3 **Terminal Configuration and Functions** **3**
4 **Specifications** **6**
4.1 Absolute Maximum Ratings 6
4.2 Handling Ratings 6
4.3 Recommended Operating Conditions 6
4.4 Recommended Operating Conditions, Resonant Circuit 6
4.5 Supply Currents 7
4.6 Digital Inputs 7
4.7 Digital Outputs 7
4.8 Thermal Characteristics 8
4.9 Serial Communication Protocol Timings 9
4.10 I^2C Interface 9
4.11 SPI Interface 10
4.12 RF143B, Recommended Operating Conditions 11
4.13 RF143B, ISO14443B ASK Demodulator 11
4.14 RF143B, ISO14443B-Compliant Load Modulator 11
4.15 RF143B, Power Supply 11
5 **Detailed Description** **12**
5.1 Functional Block Diagram 12
5.2 Serial Communication Interface 12
5.3 SPI or I^2C Mode Selection 12
5.4 Communication Protocol 13
5.5 I^2C Protocol 14
5.6 SPI Protocol 17
5.7 Registers 23
5.8 NFC Type-4 Tag Functionality 29
5.9 NDEF Memory 33
5.10 Typical Usage Scenario 36
5.11 References 36
6 器件和文档支持 **37**
6.1 器件支持 37
6.2 文档支持 38
6.3 社区资源 38
6.4 商标 39
6.5 静电放电警告 39
6.6 术语表 39
7 机械封装和可订购信息 **39**
7.1 封装信息 39

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2014) to Revision C	Page
• 已在器件信息表中添加 RGT 封装	1
• Added RGT package pinout	3
• Added RGT package to Table 3-1	4
• Added Section 4.8	8

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3 Terminal Configuration and Functions

Figure 3-1 shows the pin assignments for the PW package.

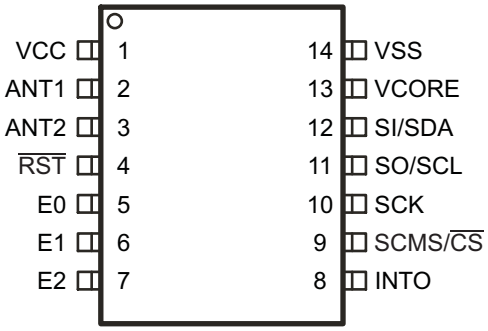


Figure 3-1. 14-Pin PW Package (Top View)

Figure 3-2 shows the pin assignments for the RGT package.

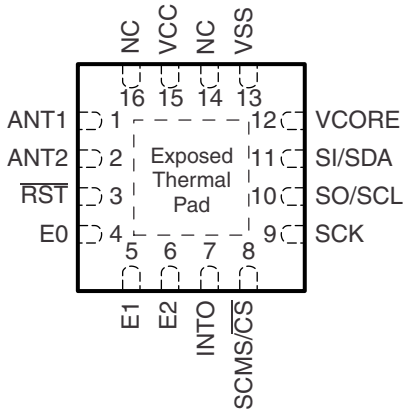


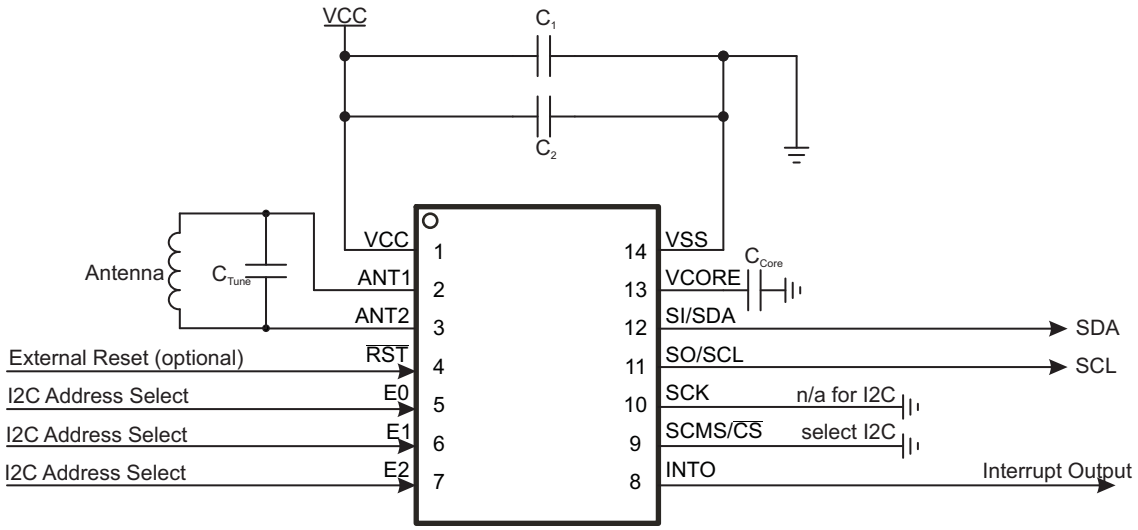
Figure 3-2. 16-Pin RGT Package (Top View)

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Table 3-1. Terminal Functions

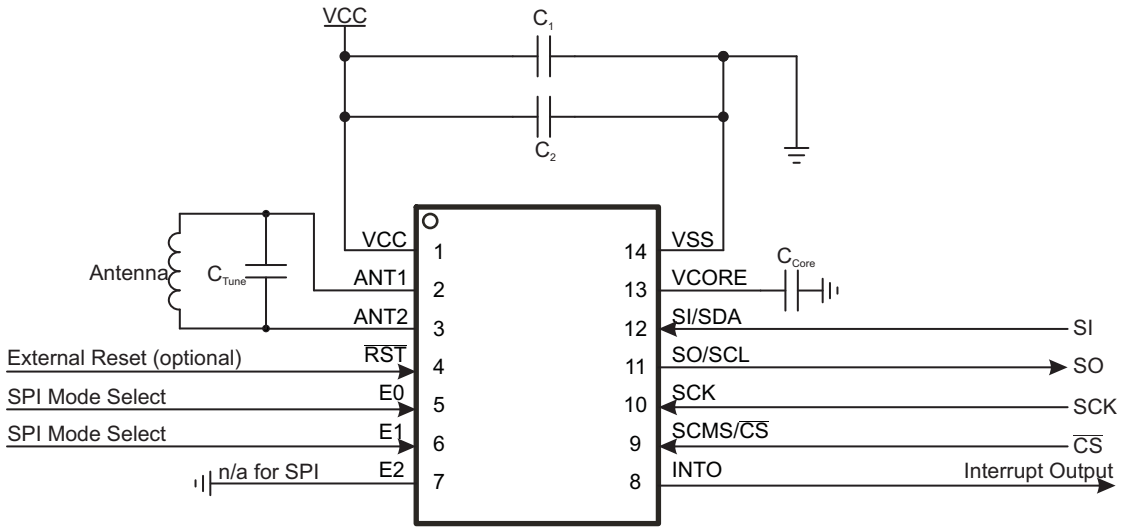
TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PW	RGT		
VCC	1	15	PWR	3.3-V power supply
ANT1	2	1	RF	Antenna input 1
ANT2	3	2	RF	Antenna input 2
$\overline{RST}$	4	3	I	Reset input (active low)
E0 (TMS)	5	4	I	I^2C address select 0 SPI mode select 0 (JTAG test mode select)
E1 (TDO)	6	5	I (O)	I^2C address select 1 SPI mode select 1 (JTAG test data output)
E2 (TDI)	7	6	I	I^2C address select 2 (JTAG test data in)
INTO (TCK)	8	7	O	Interrupt output (JTAG test clock)
SCMS/ $\overline{CS}$	9	8	I	Serial Communication Mode Select (during device initialization) Chip select (in SPI mode)
SCK	10	9	I	SPI clock input (SPI mode)
SO/SCL	11	10	I/O	SPI slave out (SPI mode) I^2C clock (I^2C mode)
SI/SDA	12	11	I/O	SPI slave in (SPI mode) I^2C data (I^2C mode)
VCORE	13	12	PWR	Regulated core supply voltage
VSS	14	13	PWR	Ground supply
NC	-	14, 16		Leave open, No connection

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NOTE: For recommended capacitance values, see Recommended Operating Conditions.

Figure 3-3. Example Application Diagram (I^2C Operation) (PW Package Shown)



NOTE: For recommended capacitance values, see Recommended Operating Conditions.

Figure 3-4. Example Application Diagram (SPI Operation) (PW Package Shown)

4 Specifications

4.1 Absolute Maximum Ratings(1) (2)

	MIN	MAX	UNIT
Voltage applied at V_{CC} referenced to V_{SS} (V_{AMR})	-0.3	4.1	V
Voltage applied at V_{ANT} referenced to V_{SS} (V_{AMR})	-0.3	4.1	V
Voltage applied to any pin (references to V_{SS})	-0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to VSS.

4.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range(1)	-40	125	°C

(1) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

4.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution no RF field present	3.0	3.3	3.6	V
	Supply voltage during program execution with RF field present	2.0	3.3	3.6	V
V_{SS}	Supply voltage (GND reference)		0		V
T_A	Operating free-air temperature	-40		85	°C
C_1	Decoupling capacitor on V_{CC} (1)		0.1		µF
C_2	Decoupling capacitor on V_{CC} (1)		1		µF
C_{VCORE}	Capacitor on V_{CORE} (1)	0.1	0.47	1	µF

(1) Low equivalent series resistance (ESR) capacitor

4.4 Recommended Operating Conditions, Resonant Circuit

		MIN	NOM	MAX	UNIT
f_c	Carrier frequency		13.56		MHz
V_{ANT_peak}	Antenna input voltage			3.6	V
Z	Impedance of LC circuit	6.5		15.5	kΩ
L_{RES}	Coil inductance(1)		2.66		µH
C_{RES}	Total resonance capacitance(1) $C_{RES} = C_{IN}+C_{Tune}$		51.8		pF
C_{Tune}	External resonance capacitance		$C_{RES} - C_{IN}$(2)		pF
QT	Tank quality factor		30		

(1) The coil inductance of the antenna L_{RES} together with the external capacitance C_{Tune} plus the device internal capacitance C_{IN} is a resonant circuit. The resonant frequency of this LC circuit must be close to the carrier frequency f_c:
$f_{RES} = 1 / [2\pi(L_{RES}C_{RES})^{1/2}] = 1 / [2\pi(L_{RES}(C_{IN} + C_{Tune}))^{1/2}] \approx f_c$
(2) For C_{IN} refer to Section 4.12.

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4.5 Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{CC(SPI)}$	SPI, $f_{SCK,MAX}$, SO = Open, Writing into NDEF memory		3.3 V		250		µA
$I_{CC(I2C)}$	I^2C, 400 kHz, Writing into NDEF memory		3.3 V		250		µA
$I_{CC(RF\ enabled)}$	RF enabled, no RF field present		3.3 V		40		µA
$I_{CC(Inactive)}$	Standby enable = 0, RF disabled, no serial communication		3.3 V		15		µA
$I_{CC(Standby)}$	Standby enable = 1, RF disabled, no serial communication		3.3 V		10	45	µA
$\Delta I_{CC(StrongRF)}$	Additional current consumption with strong RF field present		3.0 V to 3.6 V			160	µA
$I_{CC(RF,lowVCC)}$	Current drawn from VCC < 3.0 V with RF field present (passive operation)		2.0 V to 3.0 V			0	µA

4.6 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.3× V_{CC}	V
V_{IH}	High-level input voltage			0.7× V_{CC}			V
V_{HYS}	Input hysteresis			0.1× V_{CC}			V
I_L	High-impedance leakage current		3.3 V	-50		50	nA
$R_{PU(RST)}$	Integrated $\overline{RST}$ pullup resistor			20	35	50	kΩ
$R_{PU(CS)}$	Integrated SCMS/$\overline{CS}$ pullup resistor (only active during initialization)			20	35	50	kΩ

4.7 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	I_{OL} = 3 mA	3 V			0.4	V
			3.3 V			0.4	
			3.6 V			0.4	
V_{OH}	Output high voltage	I_{OH} = -3 mA	3 V	2.6			V
			3.3 V	2.9			
			3.6 V	3.2			

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4.8 Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	TSSOP-14 (PW)	116.0	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		45.1	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		57.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		57.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		4.6	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	VQFN-16 (RGT)	48.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		60.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		21.9	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		21.9	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		1.5	°C/W
$\theta_{JC(BOT)}$	Junction-to-case (bottom) thermal resistance(4)		7.1	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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4.9 Serial Communication Protocol Timings

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{SPIvsI2C}$	Time after power-up or reset until SCMS/$\overline{CS}$ is sampled for SPI or I^2C decision(1)	1		10	ms
t_{Ready}	Time after power-up or reset until device is ready to communicate using SPI or I^2C(2)			20	ms

(1) The SCMS/$\overline{CS}$ pin is sampled after $t_{SPIvsI2C}$(MIN) at the earliest and after $t_{SPIvsI2C}$(MAX) at the latest.
(2) The device is ready to communicate after t_{Ready}(MAX) at the latest.

4.10 I^2C Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4-1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency (with Master supporting clock stretching according to I^2C standard, or when the device is not being addressed)		3.3 V	0		400	kHz
	SCL clock frequency (device being addressed by Master not supporting clock stretching)	write	3.3 V	0		120	kHz
		read	3.3 V	0		100	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	3.3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	3.3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		3.3 V	0			ns
$t_{SU,DAT}$	Data setup time		3.3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		3.3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		3.3 V	6.25		75	ns

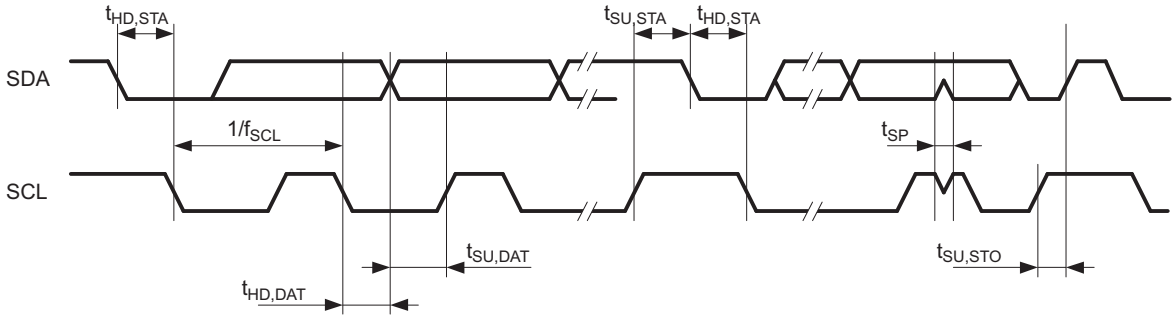


Figure 4-1. I^2C Mode Timing

4.11 SPI Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCK}	SCK clock frequency	write	3.3 V	0		100	kHz
		read	3.3 V	0		110	kHz
$t_{HIGH,CS}$	$\overline{CS}$ high time		3.3 V	50			µs
$t_{SU,CS}$	$\overline{CS}$ setup time		3.3 V	25			µs
$t_{HD,CS}$	$\overline{CS}$ hold time		3.3 V	100			ns
t_{HIGH}	SCK high time		3.3 V	100			ns
t_{LOW}	SCK low time		3.3 V	100			ns
$t_{SU,SI}$	Data In (SI) setup time		3.3 V	50			ns
$t_{HD,SI}$	Data In (SI) hold time		3.3 V	50			ns
$t_{VALID,SO}$	Output (SO) valid		3.3 V	0		50	ns
$t_{HOLD,SO}$	Output (SO) hold time		3.3 V	0			ns

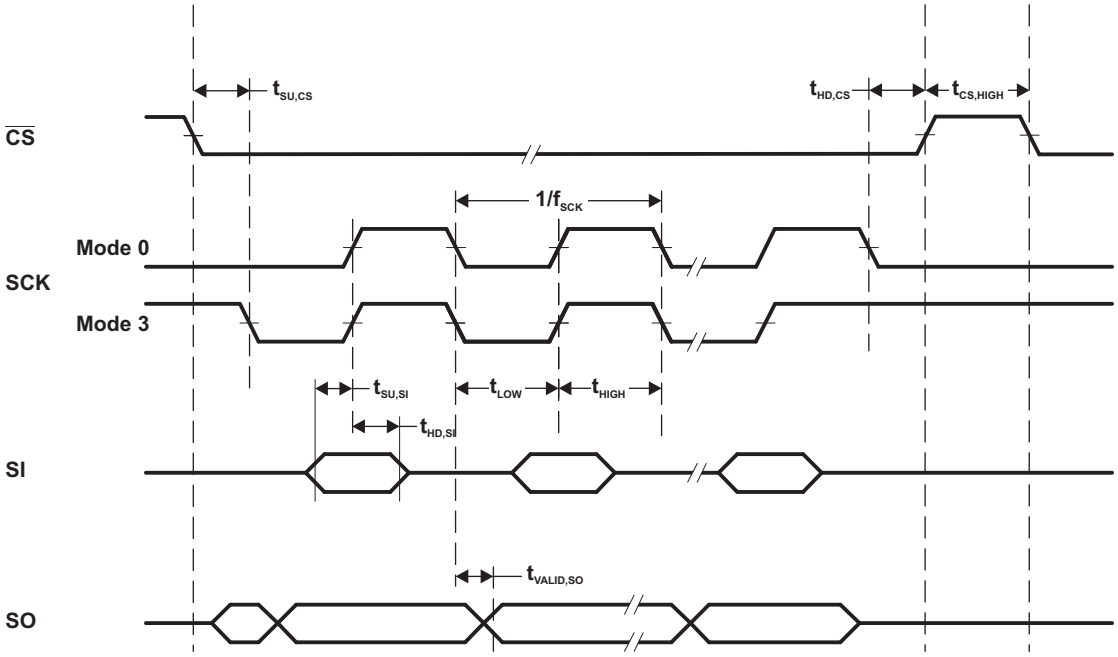


Figure 4-2. SPI Mode Timing

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4.12 RF143B, Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDH}	Antenna rectified voltage	Peak voltage limited by antenna limiter	3.0	3.3	3.6	V
I_{DDH}	Antenna load current	RMS, without limiter current			100	µA
C_{IN}	Input capacitance	ANT1 to ANT2, 2 V RMS	31.5	35	38.5	pF

4.13 RF143B, ISO14443B ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR_{10}	Input signal data rate 10% downlink modulation, 7% to 30% ASK, ISO1443B		106	848	kbps
m10	Modulation depth 10%, tested as defined in ISO10373	7		30	%

4.14 RF143B, ISO14443B-Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{PICC}	Uplink subcarrier modulation frequency	0.2		1	MHz
V_{A_MOD}	Modulated antenna voltage, V_{A_unmod} = 2.3 V	0.5			V
V_{SUB14}	Uplink modulation subcarrier level, ISO14443B: H = 1.5 to 7.5 A/m	$22/H^{0.5}$			mV

4.15 RF143B, Power Supply

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LIM}	Limiter clamping voltage	I_{LIM} ≤ 70 mA RMS, f = 13.56 MHz	3.0		3.6	V_{pk}
$I_{LIM,MAX}$	Maximum limiter current				70	mA

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5 Detailed Description

5.1 Functional Block Diagram

图 5-1 shows the functional block diagram.

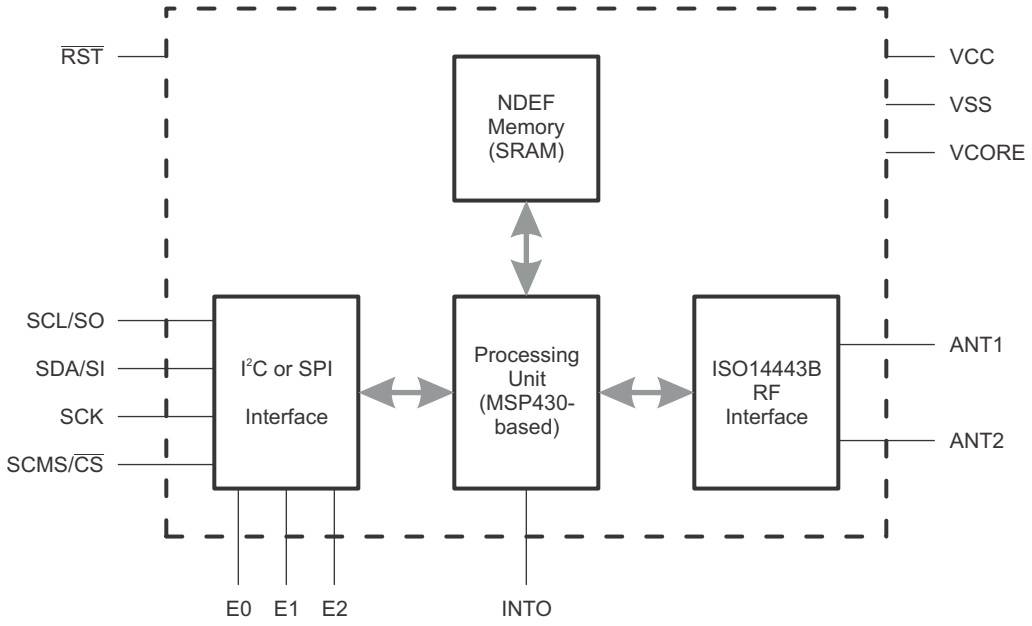


图 5-1. Functional Block Diagram

5.2 Serial Communication Interface

A "dual-mode" serial communication interface supports either SPI or I^2C communication. The serial interface allows writing and reading the internal NDEF memory as well as configuring the device operation.

5.3 SPI or I^2C Mode Selection

The selection between I^2C or SPI mode takes place during the power-up and initialization phase of the device based on the input level at pin SCMS/$\overline{CS}$ (see 表 5-1).

表 5-1. SPI or I^2C Mode Selection

Input Level at SCMS/$\overline{CS}$ During Initialization	Selected Serial Interface
0	I^2C
1	SPI

During initialization, an integrated pullup resistor pulls SCMS/$\overline{CS}$ high, which makes SPI the default interface. To enable I^2C, this pin must be tied low externally. The pullup resistor is disabled after initialization to avoid any current through the resistor during normal operation. In SPI mode, the pin reverts to its $\overline{CS}$ functionality after initialization.

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5.4 Communication Protocol

The tag is programmed and controlled by writing data into and reading data from the address map shown in 表 5-2 via the serial interface (SPI or I^2C).

表 5-2. User Address Map

Range	Address	Size	Description
Registers	0xFFFE	2B	Control Register
	0xFFFC	2B	Status Register
	0xFFFA	2B	Interrupt Enable
	0xFFF8	2B	Interrupt Flags
	0xFFF6	2B	CRC Result (16-bit CCITT)
	0xFFF4	2B	CRC Length
	0xFFF2	2B	CRC Start Address
	0xFFF0	2B	Communication Watchdog Control Register
	0xFFEE	2B	Version
	0xFFEC	2B	Reserved
	0xFFEA	2B	Reserved
	0xFFE8	2B	Reserved
	0xFFE6	2B	Reserved
	0xFFE4	2B	Reserved
	0xFFE2	2B	Reserved
	0xFFE0	2B	Reserved
Reserved	0x4000 to 0xFFDF		Reserved
	0x0C00 to 0x3FFF	13KB	Reserved (for example, future extension of NDEF Memory size)
NDEF	0x0000 to 0x0BFF	3KB	NDEF Memory

注

Crossing Range Boundaries

Crossing range boundaries causes writes to be ignored and reads to return undefined data.

5.5 I²C Protocol

A command is always initiated by the master by addressing the device using the specified I²C device address. The device address is a 7-bit I²C address. The upper 4 bits are hard-coded, and the lower 3 bits are programmable by the input pins E0 through E2.

表 5-3. I²C Device Address

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	E2	E1	E0
MSB						LSB

To write data, the device is addressed using the specified I²C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be written and the lower 8 bits of that address. Next (without a repeated start), the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by the STOP condition on the I²C bus.

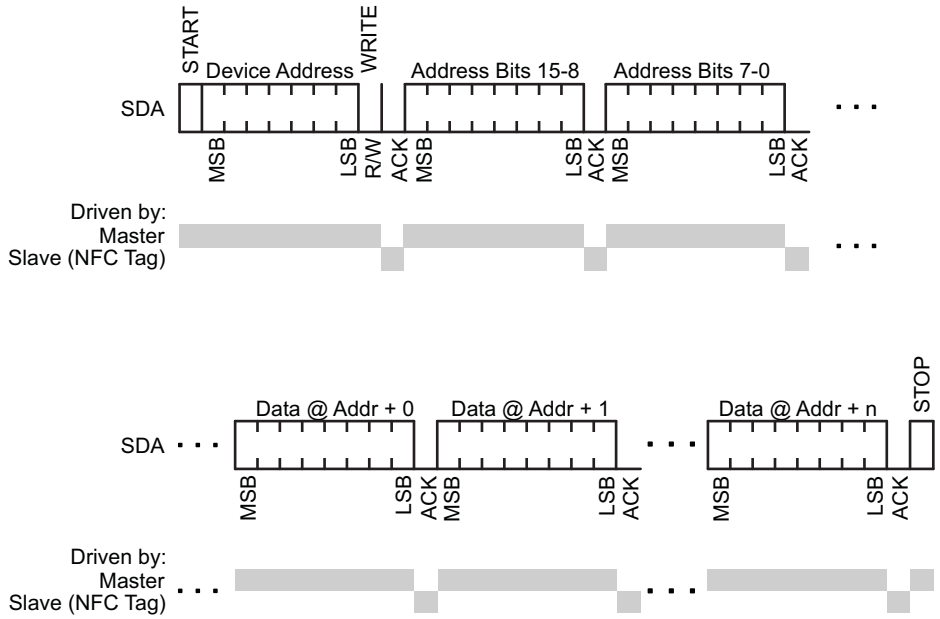


图 5-2. I²C Write Access

To read data, the device is addressed using the specified I²C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be read and then the lower 8 bits of that address. Next, a repeated start condition is expected with the I²C device address and R/$\overline{W}$ = 1. The device then transmit data starting at the specified address until a non-acknowledgment and a STOP condition is received.

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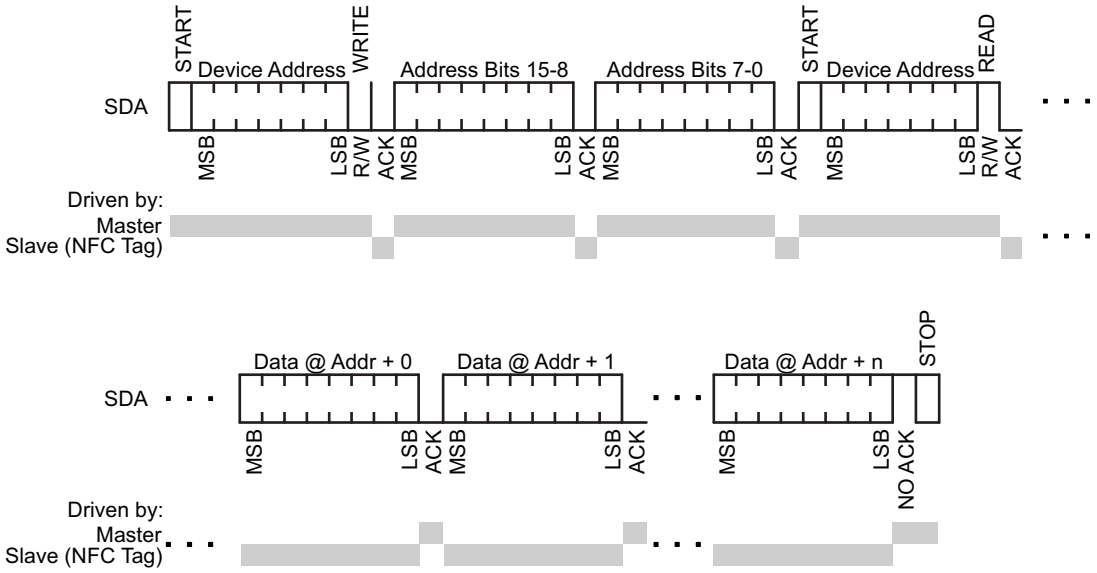


图 5-3. I²C Read Access

The following figures show examples of I²C accesses to the Control register at address 0xFFFE.

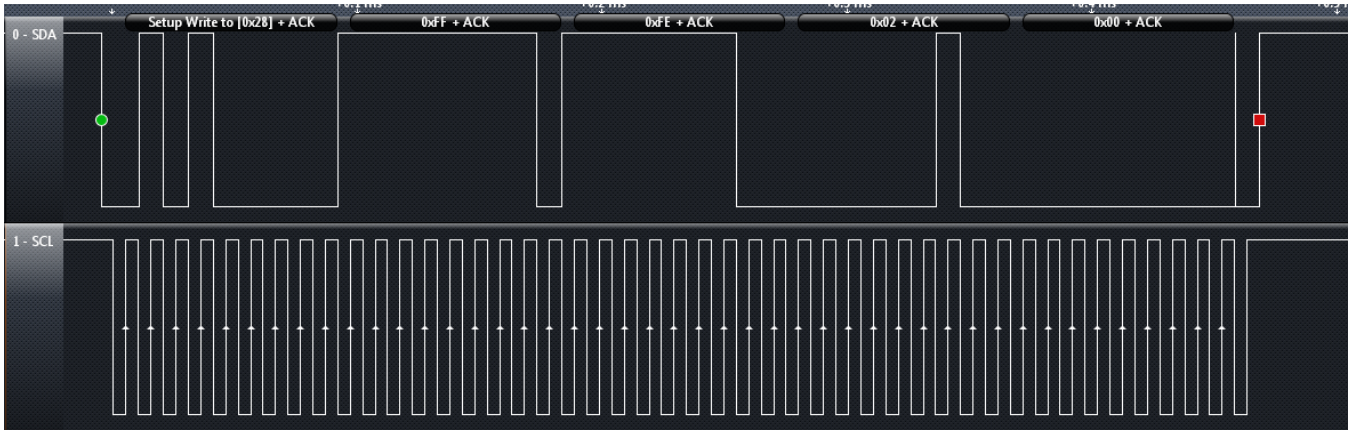


图 5-4. I²C Access Example: Write of the Control Register at Address 0xFFFE With 0x00, 0x02 (RF Enable = 1)

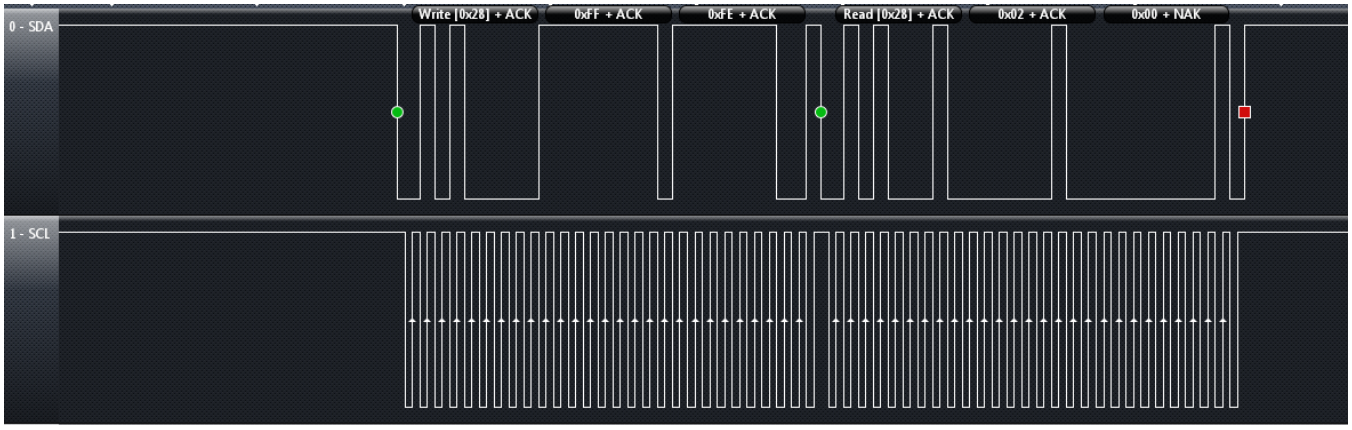


图 5-5. I²C Access Example: Read of the Control Register at Address 0xFFFE, Responds With 0x00, 0x02 (RF Enable = 1)

5.5.1 BIP-8 Communication Mode With I^2C

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

表 5-4. Write Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
Slave	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the I^2C device address).

表 5-5. Read Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	n/a	n/a	n/a
Slave	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access, the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address and the 2 transmitted data bytes, and it is transmitted back to the master. The BIP-8 does not include the device address.

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5.6 SPI Protocol

The SPI communication mode (SCK idle state and clock phase) is selected by tying E0 and E1 to VSS or VCC according to 表 5-6.

表 5-6. SPI Mode Selection

E1	E0	SPI Mode
0	0	**SPI Mode 0** with CPOL = 0 and CPHA = 0 SCK idle state: 0 SI capture starts on the first edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.
0	1	**SPI Mode 1** with CPOL = 0 and CPHA = 1 SCK idle state: 0 SI capture starts on the second edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	0	**SPI Mode 2** with CPOL = 1 and CPHA = 0 SCK idle state: 1 SI capture starts on the first edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	1	**SPI Mode 3** with CPOL = 1 and CPHA = 1 SCK idle state: 1 SI capture starts on the second edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.

An SPI communication is always initiated by the master by pulling the $\overline{CS}$ pin low.

To write data into the device, this is followed by the master sending a write command (0x02) followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by pulling the $\overline{CS}$ pin high.

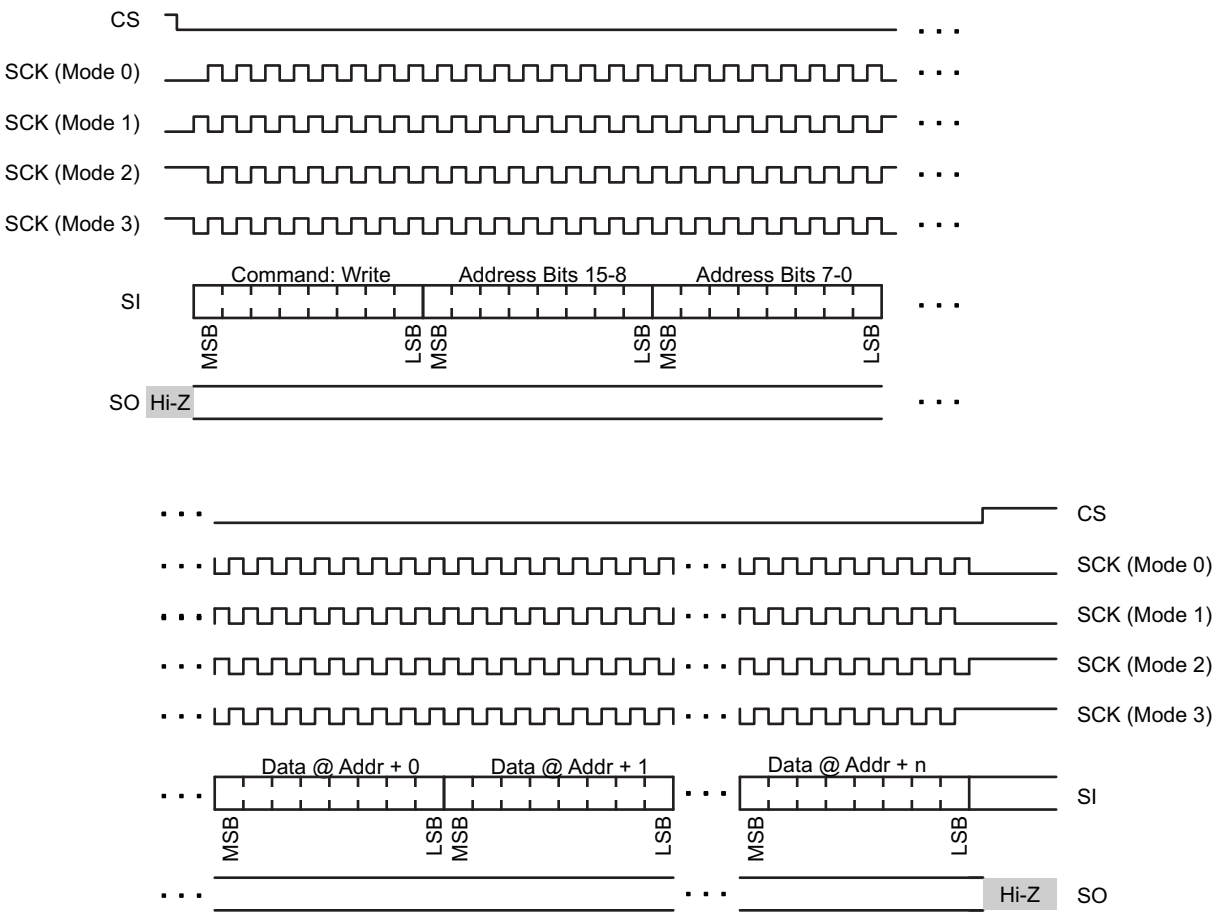


图 5-6. SPI Write Access

To read data from the device, pulling the $\overline{CS}$ pin low is followed by the master sending a read command (0x03 or 0x0B) followed by the upper 8 bits of the first address to be read, the lower 8 bits of that address, and a dummy byte. The device responds with the data that is read starting at the specified address until the $\overline{CS}$ pin is pulled high.

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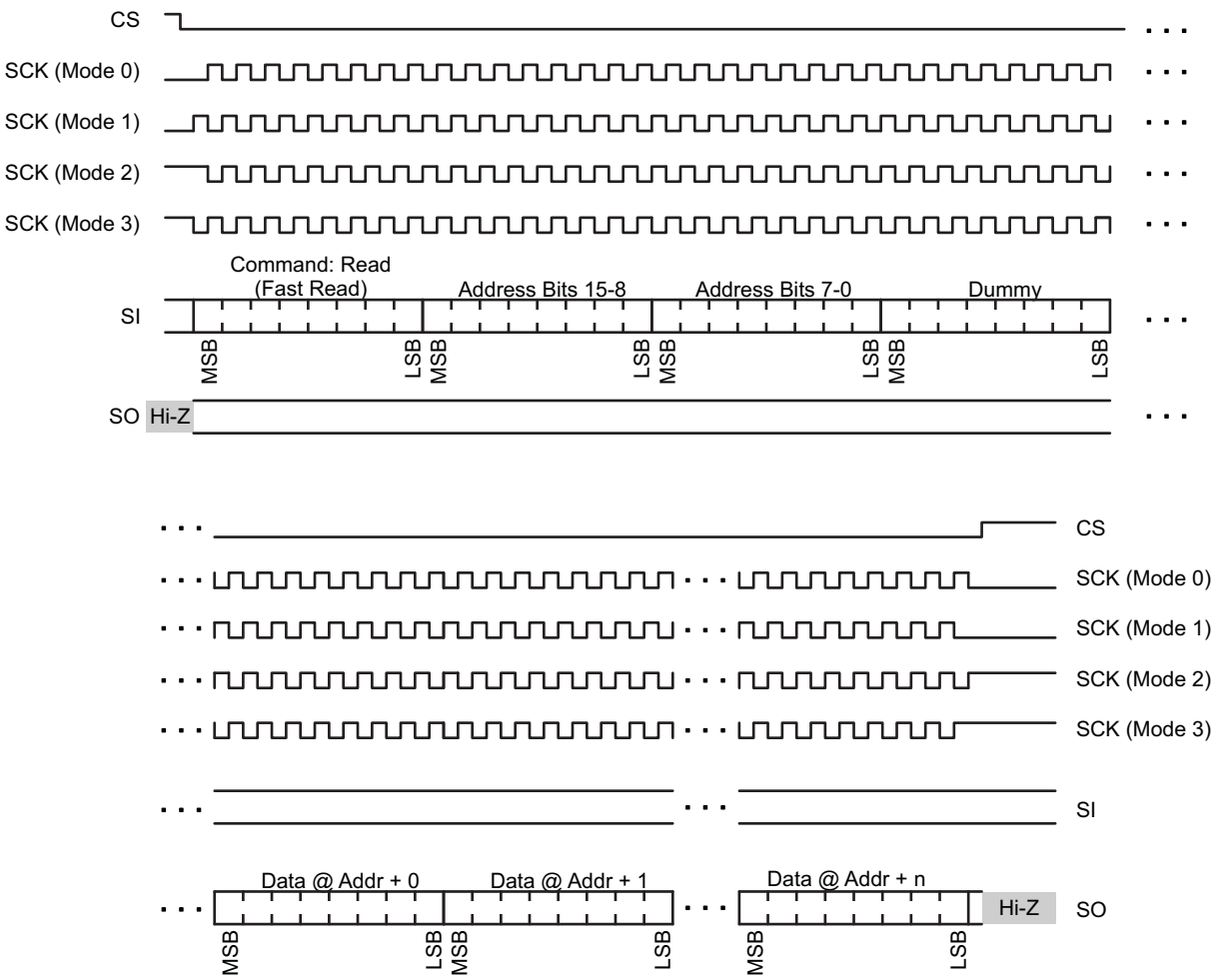


图 5-7. SPI Read Access (Command: 0x03 or 0x0B)

Commands other than write (0x02) and read (0x03 or 0x0B) are ignored. There is no difference in using the read command 0x03 or 0x0B.

图 5-8 and 图 5-9 show examples of SPI accesses to the Control register at address 0xFFFE.



图 5-8. SPI Access Example: Write of the Control Register at Address 0xFFFE With 0x00, 0x02 (RF Enable = 1)

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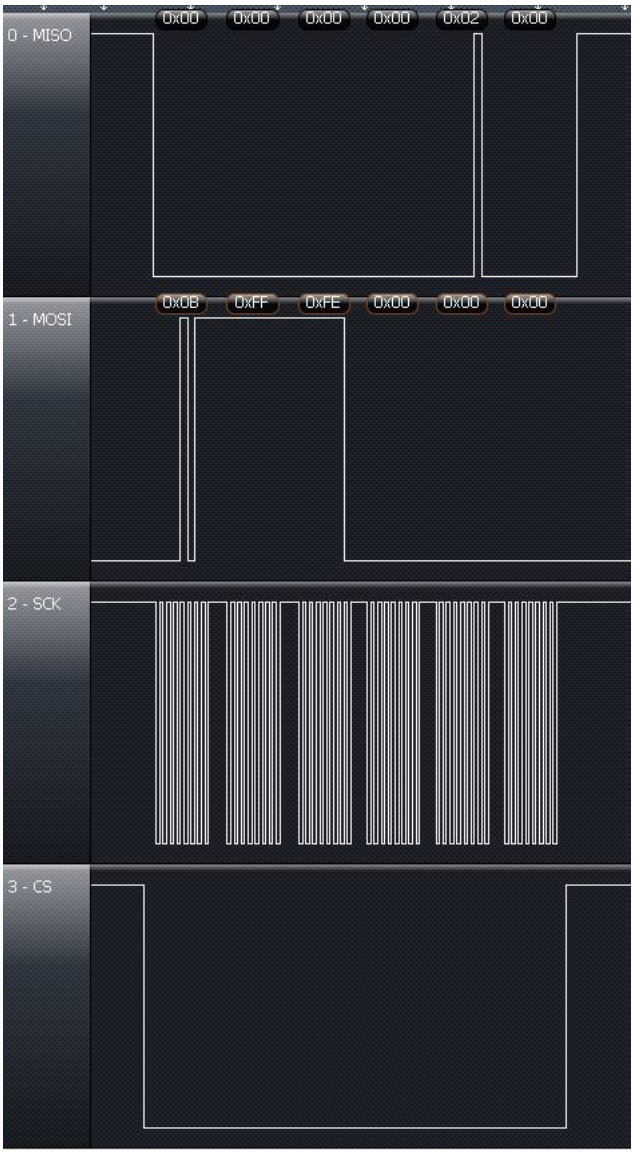


图 5-9. SPI Access Example: Read of the Control Register at Address 0xFFFE, Responds With 0x00, 0x02 (RF Enable = 1)

5.6.1 BIP-8 Communication Mode With SPI

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

表 5-7. Write Access

SI	Command: Write	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
SO	n/a	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the write-command byte.)

表 5-8. Read Access

SI	Command: Read	Address Bits 15 to 8	Address Bits 7 to 0	Dummy Byte	n/a	n/a	n/a
SO	n/a	n/a	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address, the received dummy byte and the 2 transmitted data bytes and transmitted back to the master. It does not include the read-command byte.

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5.7 Registers

注

Endianness

All 16-bit registers are little-endian: the least significant byte with bits 7-0 is at the lowest address (and this address is always even). The most significant byte with bits 15-8 is at the highest address (always odd).

5.7.1 General Control Register

表 5-9. General Control Register

Addr:	15	14	13	12	11	10	9	8
0xFFFF	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFFE	Reserved	Standby Enable	BIP-8	INTO Drive	INTO High	Enable INT	Enable RF	SW-Reset

表 5-10. General Control Register Description

Bit	Field	Type	Reset	Description
0	SW-Reset	W	0	0b = Always reads 0. 1b = Resets the device to default settings and clears memory. The serial communication is restored after t_{Ready}, and the register settings and NDEF memory must be restored afterward.
1	Enable RF	R/W	0	Global enable of RF interface. The RF interface should be disabled when writing to the NDEF memory. Enabling the RF interface triggers a basic check of the NDEF structure. If this check fails, the RF interface remains disabled and the NDEF Error interrupt flag is set. When the RF interface is enabled, writes using the serial interface (except to disable the RF interface) are discouraged to avoid any interference with RF communication. 0b = RF interface disabled 1b = RF interface enabled
2	Enable INT	R/W	0	Global Interrupt Output Enable 0b = Interrupt output disabled. The INTO pin is Hi-Z. 1b = Interrupt output enabled. The INTO pin signals any enabled interrupt according to the INTO High and INTO Drive bits.
3	INTO High	R/W	0	Interrupt Output pin INTO Configuration 0b = Interrupts are signaled with an active low 1b = Interrupts are signaled with an active high
4	INTO Drive	R/W	0	Interrupt Output pin INTO Configuration 0b = Pin is Hi-Z if there is no pending interrupt. Application provides an external pullup resistor if bit 3 (INTO Active High) = 0. Application provides an external pulldown resistor if bit 3 (INTO Active High) = 1. 1b = Pin is actively driven high or low if there is no pending interrupt. It is driven high if bit 3 (INTO Active High) = 0. It is driven low if bit 3 (INTO Active High) = 1.

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表 5-10. General Control Register Description (continued)

Bit	Field	Type	Reset	Description
5	BIP-8	R/W	0	Enables BIP-8 communication mode (bit interleaved parity). If BIP-8 is enabled, a separate running tally is kept of the parity (that is, the number of ones that occur) for every bit position in the bytes included in the BIP-8 calculation. The corresponding bit position of the BIP-8 byte is set to 1 if the parity is currently odd and is set to 0 if the parity is even – resulting in an overall even parity for each bit position including the BIP-8 byte. All communication when this bit is set must follow the conventions defined in the BIP-8 communication mode sections for I2C and SPI. 0b = BIP-8 communication mode disabled 1b = BIP-8 communication mode enabled
6	Standby Enable	R/W	0	Enables a low-power standby mode. The standby mode is entered if the RF interface is disabled, the communication watchdog is disabled, and no serial communication is ongoing. 0b = Standby mode disabled 1b = Standby mode enabled
7	Reserved	R/W	0	
8-15	Reserved	R	0	

5.7.2 Status Register

表 5-11. Status Register

Addr:	15	14	13	12	11	10	9	8
0xFFFD	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFFC	Reserved					RF Busy	CRC Active	NDEF Ready

表 5-12. Status Register Description

Bit	Field	Type	Reset	Description
0	Ready	R	0	0b = Device not ready to receive updates to the NDEF memory from the serial interface. 1b = Device ready. NDEF memory can be written by the serial interface.
1	CRC Active	R	0	0b = No CRC calculation ongoing 1b = CRC calculation ongoing
2	RF Busy	R	0	0b = No RF communication ongoing 1b = RF communication ongoing
3-15	Reserved	R	0	

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5.7.3 Interrupt Registers

The interrupt enable register (see 表 5-13 and 表 5-14) determines which interrupt events are signaled on the external output pin INTO. Setting any bit high in this register allows the corresponding event to trigger the interrupt signal. See 表 5-17 for a description of each interrupt.

All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO.

表 5-13. Interrupt Enable Register

Addr:	15	14	13	12	11	10	9	8
0xFFFB	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFFA	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

表 5-14. Interrupt Enable Register Description

Bit	Field	Type	Reset	Description
0-15	Interrupt Enables	R/W	0	Enable for the corresponding IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled

The interrupt flag register (see 表 5-15 and 表 5-16) is used to report the status of any interrupts that are pending. Setting any bit high in this register acknowledges and clears the interrupt associated with the respective bit. See 表 5-17 for a description of each interrupt.

表 5-15. Interrupt Flag Register

Addr:	15	14	13	12	11	10	9	8
0xFFF9	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFF8	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

表 5-16. Interrupt Flag Register Description

Bit	Field	Type	Reset	Description
0-15	Interrupt Flags	R/W	0	Flag pending IRQ. Read Access: 0b = No pending IRQ. 1b = Pending IRQ. Write Access: 0b = No change. 1b = Clear pending IRQ flag.

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表 5-17. Interrupts

Bit	Field	Description
0	Reserved	
1	End of Read	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a read of the NDEF message.
2	End of Write	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a write into the NDEF message.
3	CRC Calculation Completed	This IRQ occurs when a CRC calculation that is triggered by writing into the CRC registers is completed and the result can be read from the CRC result register (see 节 5.7.4).
4	BIP-8 Error Detected	This IRQ occurs when a BIP-8 error is detected (only if the BIP-8 communication mode is enabled).
5	NDEF Error	This IRQ occurs if an error is detected in the NDEF structure after an attempt to enable the RF interface.
6	Reserved	
7	Generic Error	This IRQ occurs for any error that makes the device unreliable or non-operational.
8-15	Reserved	

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5.7.4 CRC Registers

Writing the CRC address and the CRC length registers initiates a 16-bit CRC calculation of the specified address range. The length is always assumed to be even (16-bit aligned). Writing the length register starts the CRC calculation.

During the CRC calculation, the CRC active bit is set (=1). When the calculation is complete, the "CRC completion" interrupt flag is set and the result of the CRC calculation can be read from the CRC result register. It is recommended to perform a CRC calculation only when the RF interface is disabled (RF Enable = 0).

表 5-18. CRC Result Register

Addr:	15	14	13	12	11	10	9	8
0xFFF7	CRC CCITT Result (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF6	CRC CCITT Result (low byte)							

表 5-19. CRC Result Register Description

Bit	Field	Type	Reset	Description
0-15	CRC-CCITT Result	R	0	CRC-CCITT Result

表 5-20. CRC Length Register

Addr:	15	14	13	12	11	10	9	8
0xFFF5	CRC Length (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF4	CRC Length (low byte)							

表 5-21. CRC Length Register Description

Bit	Field	Type	Reset	Description
0-15	CRC Length	RW	0	CRC Length - always assumed to be even (Bit 0 = 0). Writing into high byte starts CRC calculation.

表 5-22. CRC Start Address Register

Addr:	15	14	13	12	11	10	9	8
0xFFF3	CRC Start Address (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF2	CRC Start Address (low byte)							

表 5-23. CRC Start Address Register Description

Bit	Field	Type	Reset	Description
0-15	CRC Start Address	RW	0	CRC Start Address. Defines start address within NDEF memory. This address is always assumed to be even (bit 0 = 0).

The CRC is calculated based on the CCITT polynomial initialized with 0xFFFF.

CCITT polynomial: $x^{16} + x^{12} + x^5 + 1$

5.7.5 Communication Watchdog Register

When the communication watchdog is enabled, it expects a write or read access within a specified period; otherwise, the watchdog resets the device. If the BIP-8 communication mode is enabled, the transfer must be valid to be accepted as a watchdog reset.

表 5-24. Communication Watchdog Register

Addr:	15	14	13	12	11	10	9	8
0xFFF1	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFF0	Reserved				Timeout Period Selection			Enable

表 5-25. Communication Watchdog Register Description

Bit	Field	Type	Reset	Description
0	Enable	R/W	0	0b = Communication Watchdog disabled 1b = Communication Watchdog enabled
1	Timeout Period Selection	R/W	0	000b = 2 s ± 30%(1) 001b = 32 s ± 30%(1) 010b = 8.5 min ± 30%(1) 011b to 111b = Reserved
4-15	Reserved	R	0	

(1) This value is based on use of the integrated low-frequency oscillator with a frequency of 256 kHz ± 30%.

5.7.6 Version Registers

Provides version information about the implemented ROM code.

表 5-26. Version Register

Addr:	15	14	13	12	11	10	9	8
0xFFEF	Software Version							
Addr:	7	6	5	4	3	2	1	0
0xFFEE	Software Identification							

表 5-27. Version Register Description

Bit	Field	Type	Reset	Description
0-7	Software Identification	R		0x01: RF430CL330H Firmware
8-15	Software Version	R		Software version

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5.8 NFC Type-4 Tag Functionality

This device is an ISO14443B-compliant transponder that operates according to the NFC Forum Tag Type-4 specification and supports the NFC Forum NDEF (NFC Data Exchange Format) requirements. Through the RF interface, the user can read and update the contents in the NDEF memory. The contents in the NDEF memory (stored in SRAM) are stored as long as power is maintained.

注

This device does not have nonvolatile memory; therefore, the information stored in the NDEF memory is lost when power is removed.

This device does not support the peer-to-peer or reader/writer modes in the ISO18092/NFC Forum specification. All RF communication between an NFC forum device and this device is in the passive tag mode. The device responds by load modulation and is not considered an intentional radiator.

This device is intended to be used in applications where the primary reader/writer is for example an NFC-enabled cell phone. The device enables data transfer to and from an NFC phone by RF to the host application that is enabled with the dual interface device. In this case, the host application can be considered the destination device, and the cell phone or other type of mobile device is treated as the end-point device.

This device supports ISO14443-3, ISO14443-4, and NFC Forum commands as described in the following sections. A high-level overview of the ISO14443B and NFC commands and responses are shown in 图 5-10.

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported.

The device always answers ATTRIB commands from the PCD that request higher data rates. Note, this is not NFC-compliant, because for NFC-B the maximum data rate specified is 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates thus no interoperability issues are expected.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD. To change this behavior, use the sequence described in 节 5.8.3.

The ISO14443B command and response structure is detailed in ISO14443-3, ISO14443-4, and NFC Forum-TS-Digital Protocol. The applicable ISO7816-4 commands are detailed in NFC Forum-TS-Type-4-Tag_2.0.

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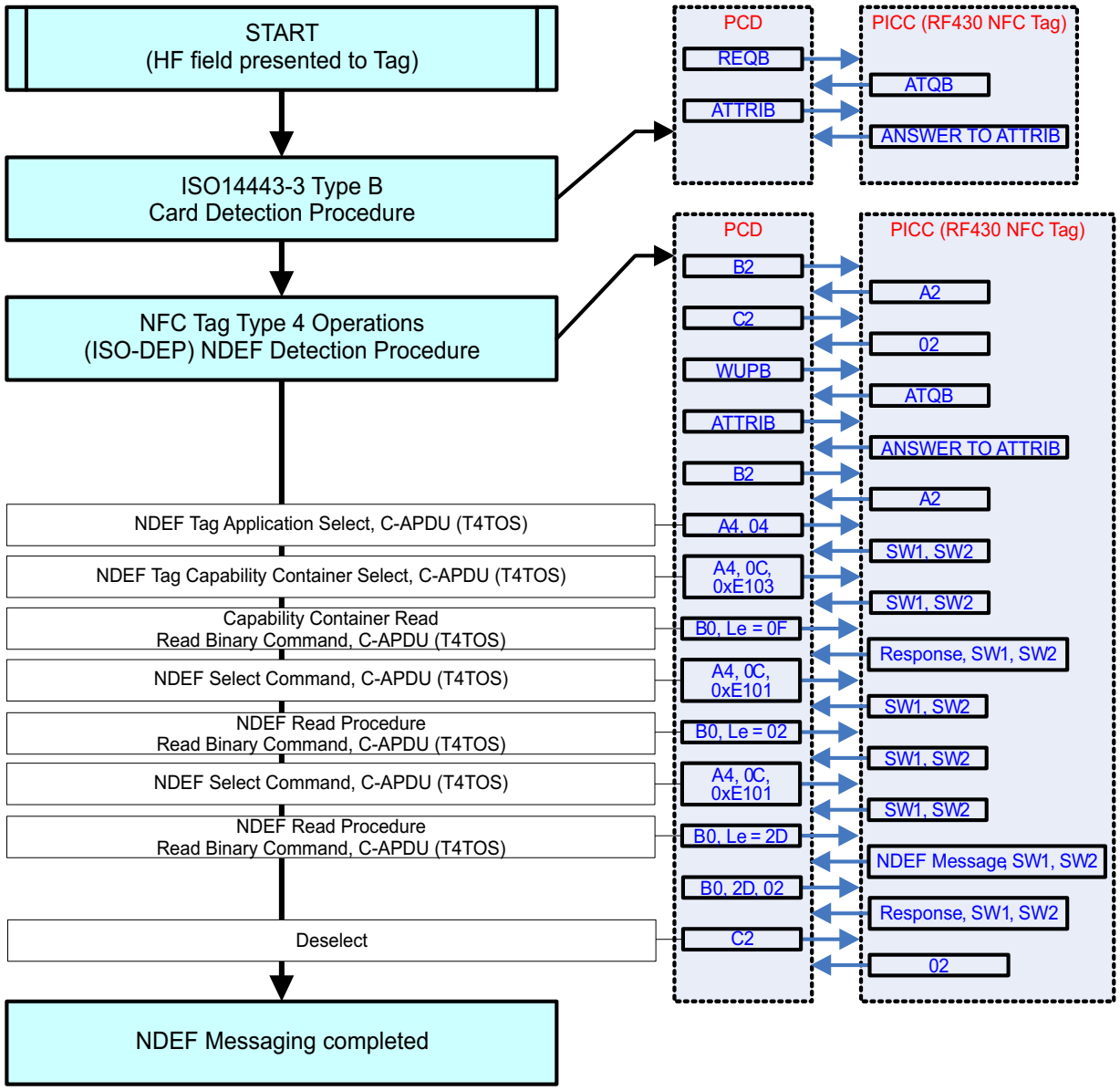


图 5-10. Command and Response Exchange Flow

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5.8.1 ISO14443-3 Commands

These commands use the character, frame format, and timing that are described in ISO14443-3, clause 7.1. The following commands are used to manage communication:

REQB and WUPB

The REQB and WUPB Commands sent by the PCD are used to probe the field for PICCs of Type B. In addition, WUPB is used to wake up PICCs that are in the HALT state. The number of slots N is included in the command as a parameter to optimize the anticollision algorithm for a given application.

Slot-MARKER

After a REQB or WUPB Command, the PCD may send up to (N-1) Slot-MARKER Commands to define the start of each timeslot. Slot-MARKER Commands can be sent after the end of an ATQB message received by the PCD to mark the start of the next slot or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

ATTRIB

The ATTRIB Command sent by the PCD includes information required to select a single PICC. A PICC receiving an ATTRIB Command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only responds to commands defined in ISO/IEC 14443-4 that include its unique CID.

HLTB

The HLTB Command is used to set a PICC in HALT state and stop responding to a REQB.

After answering to this command, the PICC ignores any commands except the WUPB.

5.8.2 NFC Tag Type 4 Commands

Select

Selection of applications or files

ReadBinary

Read data from file

UpdateBinary

Update (erase and write) data to file

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5.8.3 Data Rate Settings

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported by the device.

The device always answers ATTRIB commands from the PCD that request higher data rates. Note, this is not NFC-compliant, because for NFC-B the maximum data rate specified is 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates thus no interoperability issues are expected.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD.

To change this behavior, follow these steps using the selected serial interface (I^2C or SPI):

1. Read the version register.
2. Use the version register content to select one of the following sequences:
   – If "Software Identification" = 01h and "Software Version" = 01h, follow the sequence in 表 5-28.
   – If "Software Identification" = 01h and "Software Version" = 02h , follow the sequence in 表 5-29.
3. If you do not want to support all data rates up to 847 kbps, then change the Data Rate Capability byte (Data 0 of Step 3. Write Access) according to 表 5-30.
4. Perform the steps in the following tables.

表 5-28. Data Rate Setting Sequence (Version = 0101h)

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0xA4	0xC4 (1)	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to 表 5-30. 0xC4: all data rates up to 847 kbps are supported.

表 5-29. Data Rate Setting Sequence (Version = 0201h)

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0x7C	0xC4 (1)	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to 表 5-30. 0xC4: all data rates up to 847 kbps are supported.

表 5-30. Data Rate Capability

Data Rata Capability Byte								Description
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	PICC supports only 106-kbps in both directions (default).
1	x	x	x	0	x	x	x	Same data rate from PCD to PICC and from PICC to PCD compulsory
x	x	x	1	0	x	x	x	PICC to PCD, data rate supported is 212 kbps
x	x	1	x	0	x	x	x	PICC to PCD, data rate supported is 424 kbps
x	1	x	x	0	x	x	x	PICC to PCD, data rate supported is 847 kbps
x	x	x	x	0	x	x	1	PCD to PICC, data rate supported is 212 kbps
x	x	x	x	0	x	1	x	PCD to PICC, data rate supported is 424 kbps
x	x	x	x	0	1	x	x	PCD to PICC, data rate supported is 847 kbps

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5.9 NDEF Memory

This device implements 3KB of SRAM memory that must be written with the NDEF Application data.

表 5-31 shows the mandatory structure. The data can be accessed through the RF interface only after the NDEF memory is correctly initialized through the serial interface (I^2C or SPI).

While writing into the NDEF memory, the RF interface must be disabled by clearing the Enable RF bit in the General Control register. After the NDEF memory is properly initialized, the RF interface can be enabled be setting the Enable RF bit in the General Control register to 1. When the RF interface is enabled, the basic NDEF structure is checked for correctness. If an error in the structure is detected, the NDEF Error IRQ is triggered, and the RF interface remains disabled (the Enable RF bit in the General Control register is cleared to 0).

If the NDEF application data must be modified through the serial interface after the RF interface is enabled, it is recommended to read the RF Busy bit in the Status register. If the RF interface is busy, defer disabling the RF interface until the RF transaction is completed (indicated by RF Busy bit = 0).

图 5-11 shows the recommended flow how to control the access to the NDEF memory.

The address range for the NDEF memory is 0x0000 to 0x0BFF.

表 5-31. NDEF Application Data (Mandatory)

<table>
<tr><td rowspan="11">NDEF Application
Selectable by Name = D2_7600_0085_0101h</td><td rowspan="8">Capability Container
Selectable by File ID = E103h</td><td colspan="3">2B - CCLen</td><td rowspan="4"></td></tr>
<tr><td colspan="3">1B - Mapping version</td></tr>
<tr><td colspan="3">2B - MLe = 000F9h</td></tr>
<tr><td colspan="3">2B - MLc = 000F6h</td></tr>
<tr><td rowspan="5">NDEF File Ctrl TLV</td><td colspan="2">1B - Tag = 04h</td><td rowspan="5">The NDEF file control TLV is mandatory</td></tr>
<tr><td colspan="2">1B - Len = 06h</td></tr>
<tr><td rowspan="4">6B - Val</td><td>2B - File Identifier</td></tr>
<tr><td>2B - Max file size</td></tr>
<tr><td>1B - Read access</td></tr>
<tr><td>1B - Write access</td></tr>
<tr><td rowspan="3">NDEF File
Selectable by File ID = xxyyh</td><td colspan="3">2B - Len</td><td rowspan="3">Mandatory NDEF file</td></tr>
<tr><td colspan="3">xB - Binary NDEF file content</td></tr>
<tr><td colspan="3">yB - Unused if Len < Max file size in File Ctrl TLV</td></tr>
</table>

表 5-32. NDEF Application Data (Includes Proprietary Sections)

NDEF Application Selectable by Name = D2_7600_0085_0101h	Capability Container Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version			
		2B - MLe = 000F9h			
		2B - MLc = 000F6h			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
		Proprietary File Ctrl TLV (1)	1B - Tag = 05h		Zero or more proprietary file control TLVs
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
		⋮			
		Proprietary File Ctrl TLV (N)	1B - Tag = 05h		
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
	NDEF File Selectable by File ID = xxyyh	2B - Len			Mandatory NDEF file
		xB - Binary NDEF file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			
	Proprietary File (1) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			
	⋮				
	Proprietary File (N) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			

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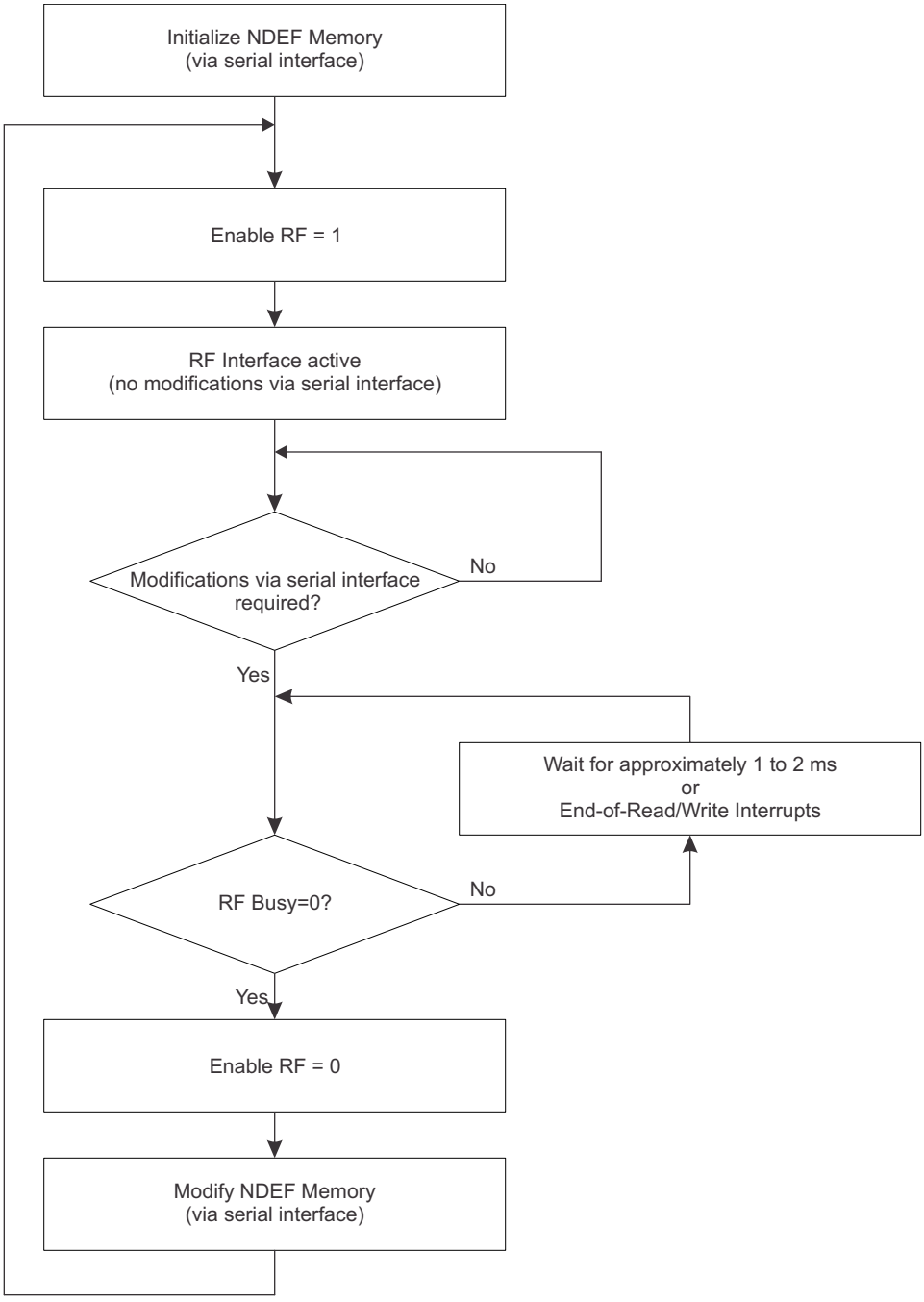


图 5-11. Recommended NDEF Memory Flow

5.9.1 NDEF Error Check

With the RF interface is enabled, the basic NDEF structure is automatically checked for correctness. If any of the following conditions are true, the error check fails, an NDEF error IRQ is triggered, and the RF interface remains disabled.

- CCLEN less than 0x000F or greater than 0xFFFE.
- MLe value is less than 0xF. Note, for best performance the MLe value should be programmed to 0x00F9.
- MLc is equal to zero. Note, for best performance the MLc value should be programmed to 0x00F6.
- TLV tag does not equal 0x4.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

Also the proprietary TLVs are checked. The check fails if any of the following conditions are true.

- TLV tag does not equal 0x05.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

5.10 Typical Usage Scenario

A typical usage scenario is as follows:

1. Write capability container and messages into the NDEF memory (starting from address 0) using the serial interface.
2. Enable interrupts (especially End of Read and End of Write).
3. Configure the interrupt pin INTO as needed and enable the RF interface.
4. Wait for interrupt signaled by INTO.
5. Disable RF interface (but keep INTO settings unchanged).
6. Read interrupt flag register to determine interrupt sources.
7. Clear interrupt flags. INTO returns to inactive state.
8. Read and modify NDEF memory as needed.
9. Enable RF interface again (keeping INTO settings unchanged) and continue with .

5.11 References

ISO/IEC 14443-2: 2001, Part 2: Radio frequency interface power and signal interface

ISO/IEC 14443-3: 2001, Part 3: Initialization and anticollision

ISO/IEC 14443-4: 2001, Part 4: Transmission protocols

ISO/IEC 18092, NFC Communication Interface and Protocol-1 (NFCIP-1)

ISO/IEC 21481, NFC Communication Interface Protocol-2 (NFCIP-2)

NDEF NFC Forum Spec, NFC Data Exchange Format Specification

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6 器件和文档支持

6.1 器件支持

6.1.1 开发支持

6.1.1.1 入门和下一步

如需获得有助于您开发的 RF430 系列器件、工具及软件的更多信息，请访问 NFC/RFID 工具和软件页面。

动态近场通信 (NFC) 类型 4B 标志设计 (TIDM-DYNAMICNFCTAG) 列出了所需组件和布局考量因素，并提供了相关固件示例，用于指导在各项应用（例如*蓝牙*/Wi-Fi 配对，设备配置和诊断）中实现 NFC 或将 NFC 用作通用 NFC 接口。 设计人员可利用提供的文档、硬件和示例代码，选择 MSP430™ MCU 或其它可选 MCU 快速实现 NFC功能。

6.1.2 器件和开发工具命名规则

为了指明产品开发周期所处的阶段，TI 为所有 RF430 MCU 器件和支持工具的产品型号分配了前缀。 每个商业系列产品都具有以下三个前缀中的一个：RF、P 或 X（例如，RF430CL330H）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：RF 和 X。这些前缀代表了产品开发的发展阶段：即从工程原型设计（器件和工具中包含 X）直到完全合格的生产器件和工具（器件和工具中包含 RF）。

器件开发进化流程：

X - 试验器件不一定代表最终器件的电气技术规格

P - 最终的芯片模型符合器件的电气技术规格，但是未经完整的质量和可靠性验证

RF - 完全合格的生产器件

支持工具开发发展流程：

X - 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

RF – 完全合格的开发支持产品

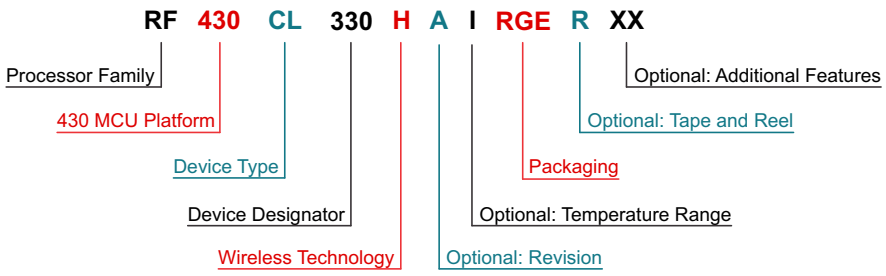
X 和 P 器件和 X 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

RF 器件和 RF 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（X 和 P）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀包括封装类型（例如，RGE）和温度范围（例如，T）。图 6-1 提供了读取任一系列产品成员完整器件名称的图例。



Processor Family	RF = Embedded RF Radio X = Experimental Silicon P = Prototype Device
430 MCU Platform	TI's Low Power Microcontroller Platform
Device Type	C = Fixed Function L = Low Power
Device Designator	Various Levels of Integration Within a Series
Wireless Technology	H = High Frequency
Optional: Revision	A = Device Revision
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C
Packaging	www.ti.com/packaging
Optional: Tape and Reel	T = Small Reel (7 inch) R = Large Reel (11 inch) No Markings = Tube or Tray
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C)

图 **6-1.** 器件命名规则

6.2 文档支持

以下文档对 RF430CL330H 器件进行了介绍。 www.ti.com.cn 网站上提供了这些文档的副本。

SLAZ540 ***RF430CL330H 器件勘误表***。说明了 RF430CL330H 器件功能技术规格的已知例外情况。

SLOA187 *通过近场通信 (NFC) 实现自动蓝牙 (R) 配对*。这份合作完成的文档是 NFC 论坛之前发布的名为《*NFC 论坛连接切换技术规范*》的后续文档，之前发布的技术规范开始定义交互的结构和顺序，此交互使两个启用 NFC 的器件能够使用其他无线通信技术建立一个连接。 这份应用报告解释了如何在一个嵌入式应用中使用 RF430CL330H 动态 NFC 应答机执行 NFC 论坛 / Bluetooth SIG 技术规范。

6.3 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商"按照原样"提供。 这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》。

TI E2E™ 社区

TI 工程师间 (E2E) 社区。此社区的创建目的是为了促进工程师之间协作。 在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

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6.4 商标

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.
Wi-Fi is a registered trademark of Wi-Fi Alliance.
All other trademarks are the property of their respective owners.

6.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。



ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

7.1 封装信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RF430CL330HCPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H
RF430CL330HCPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H
RF430CL330HIRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H
RF430CL330HIRGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

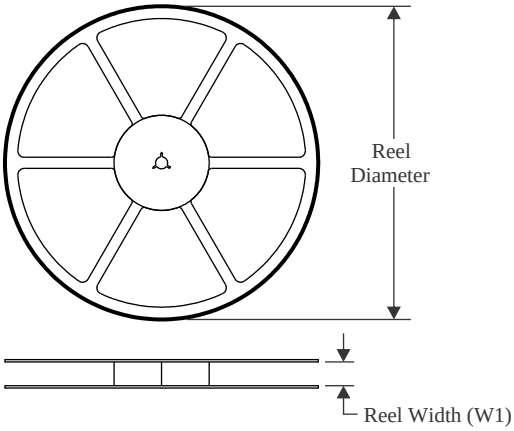
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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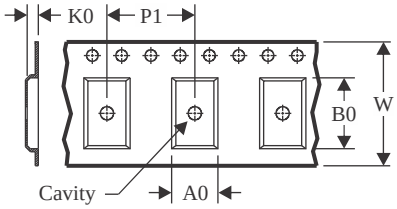
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

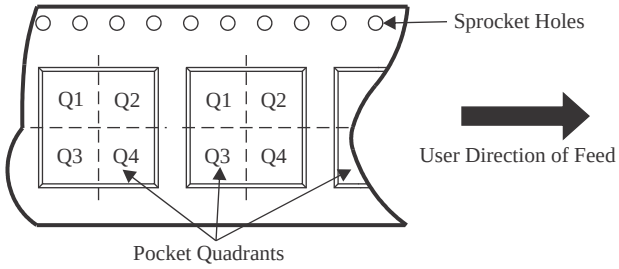


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

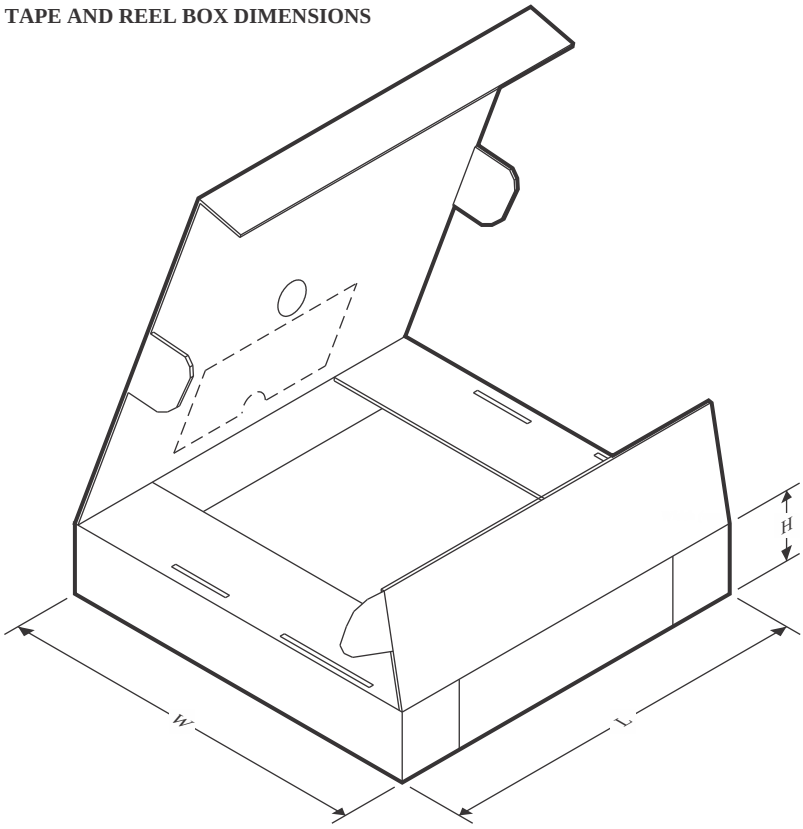
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RF430CL330HIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

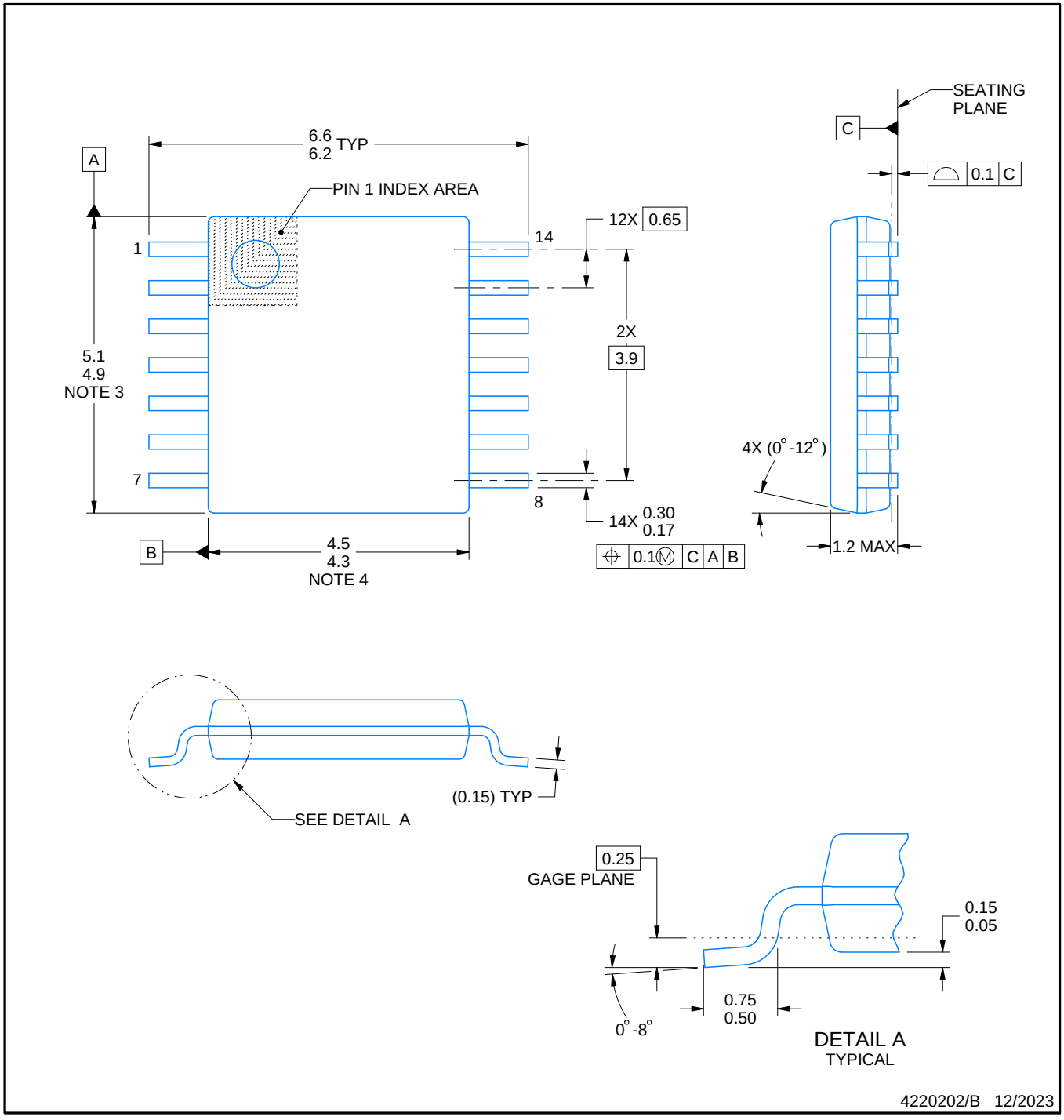
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RF430CL330HIRGTR	VQFN	RGT	16	3000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0014A

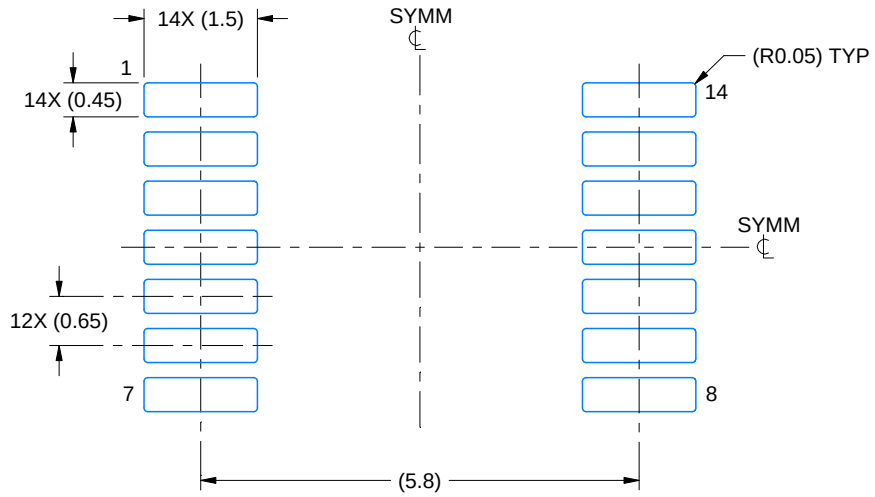
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

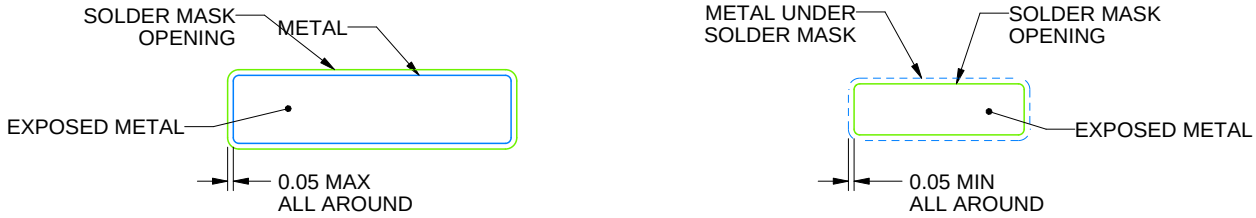


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

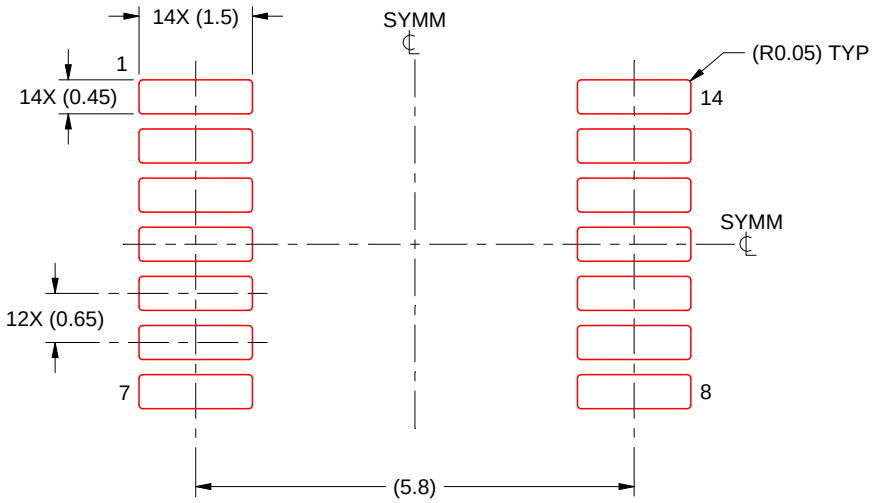


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

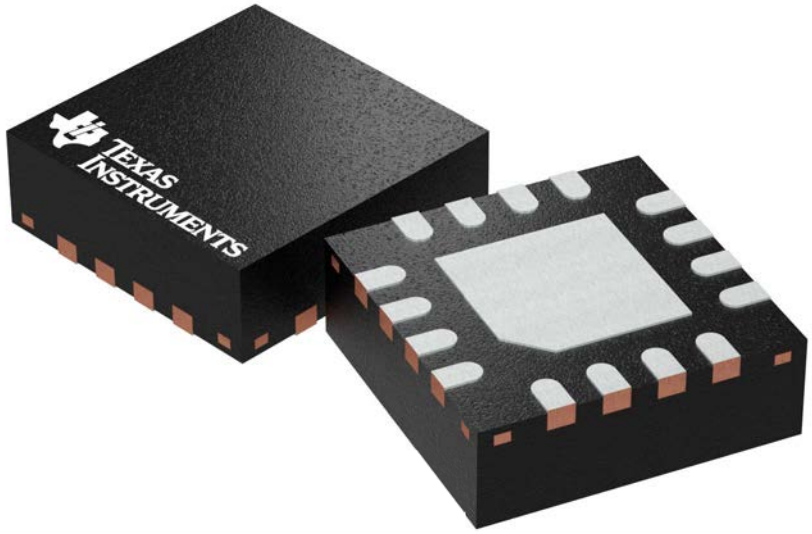
4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



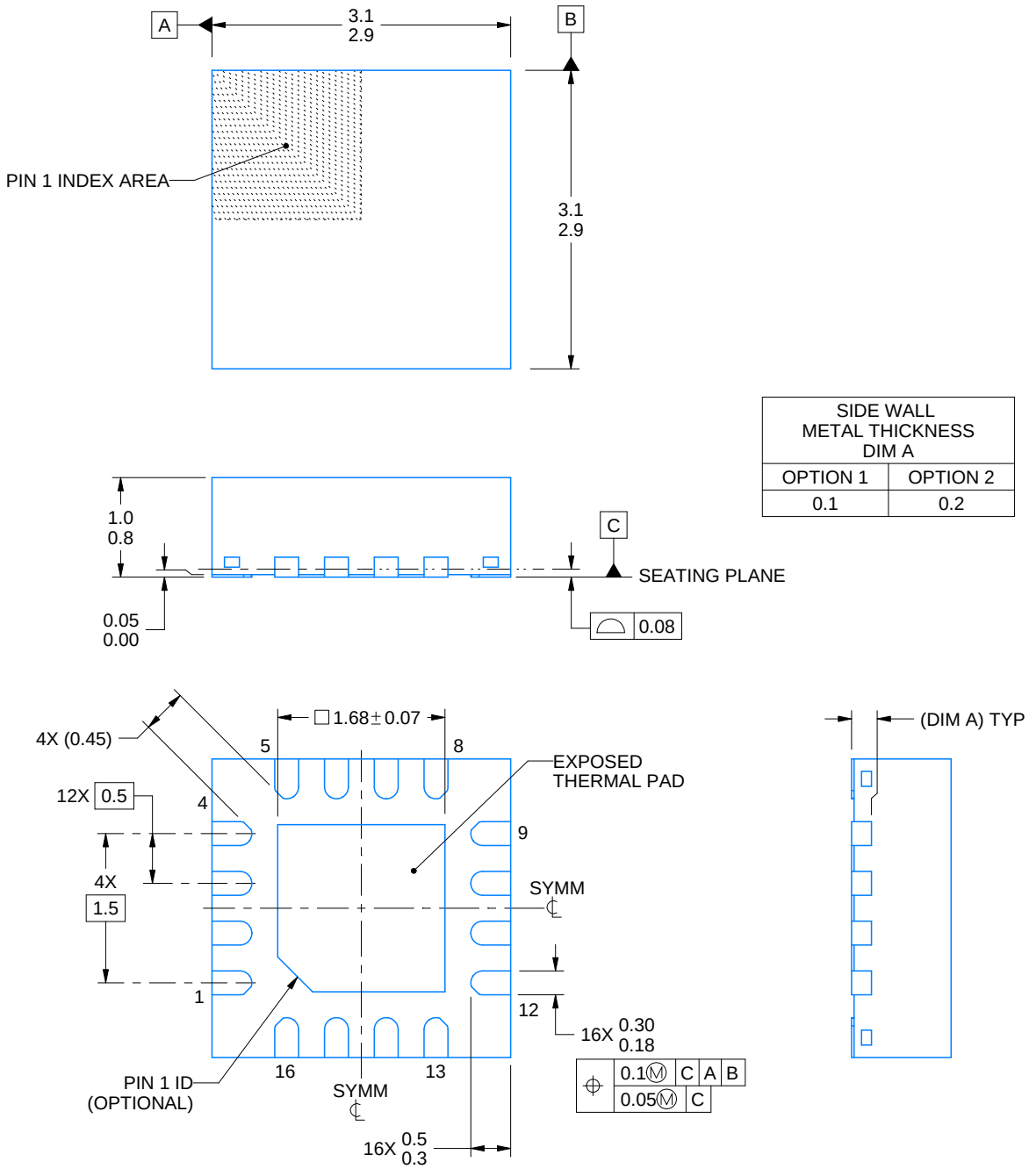
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

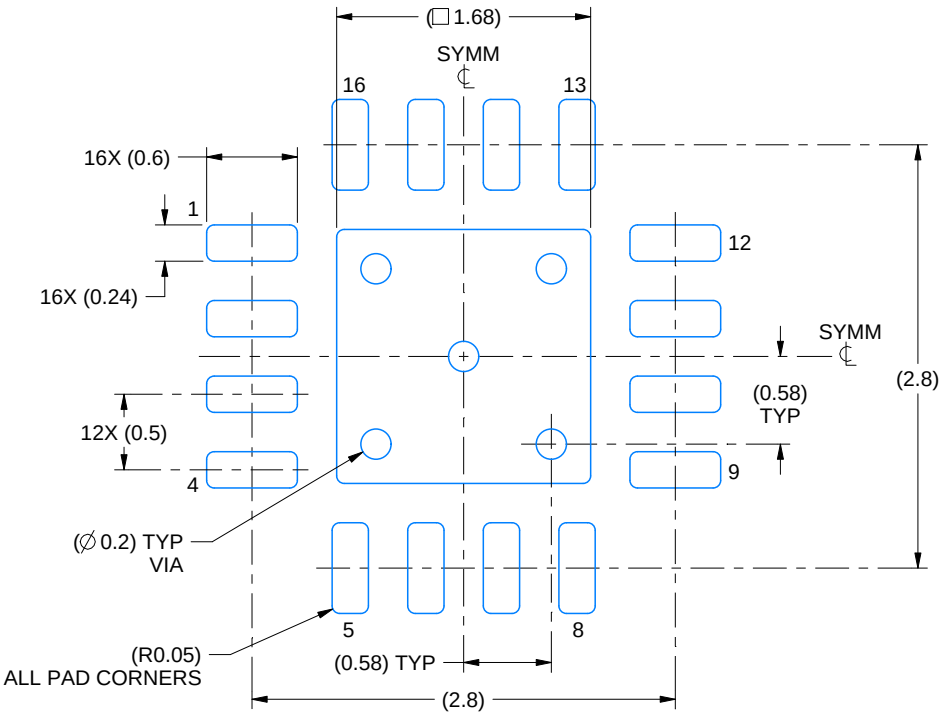
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

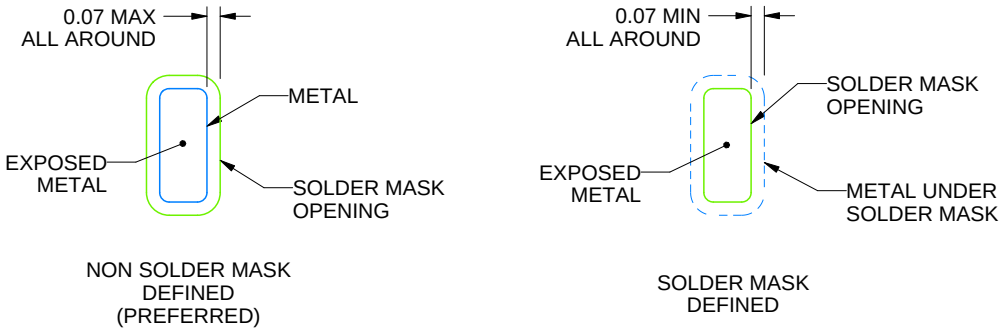


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

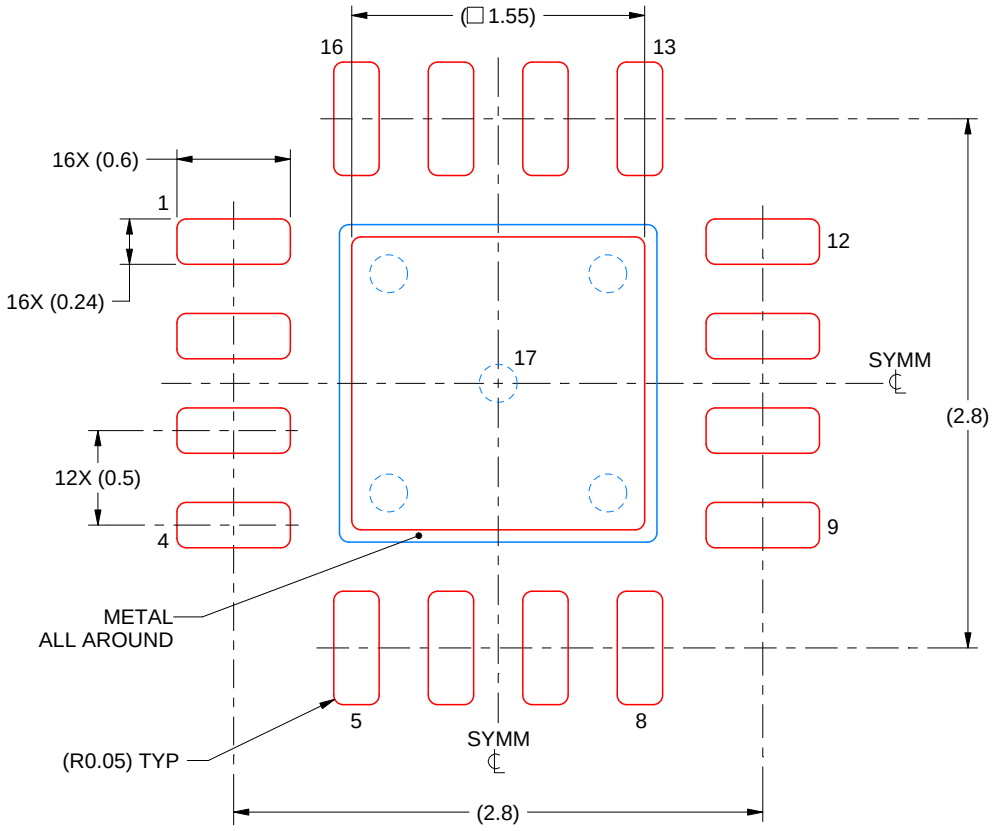


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月