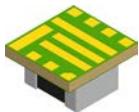


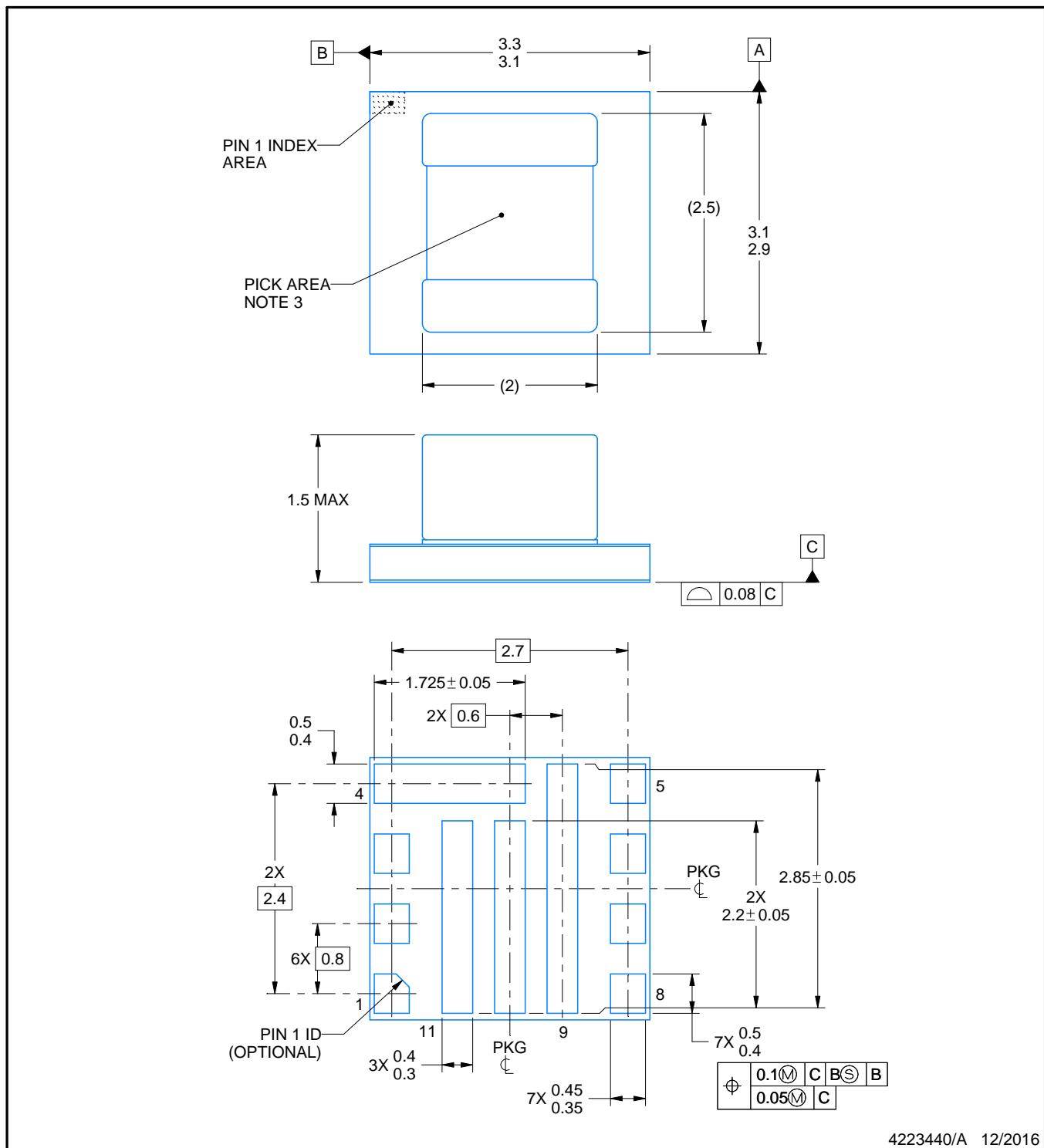
PACKAGE OUTLINE

SIL0011A



uSIP™ - 1.5 mm max height

MICRO SYSTEM IN PACKAGE



4223440/A 12/2016

NOTES:

MicroSiP is a trademark of Texas Instruments

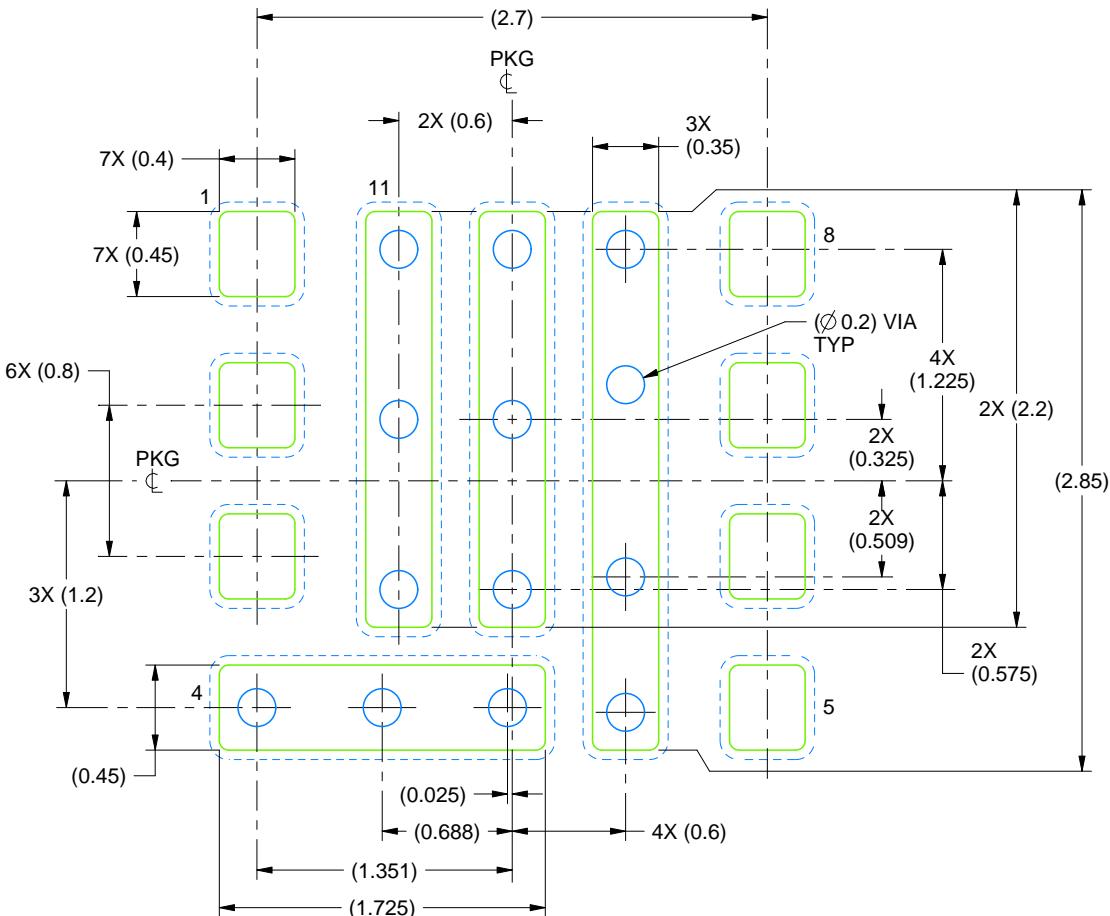
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Pick and place nozzle ϕ 1.3 mm or smaller recommended.
 4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

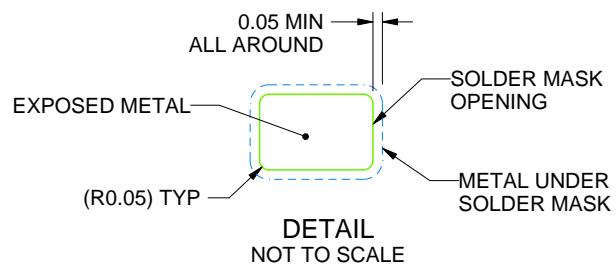
SIL0011A

uSIP™ - 1.5 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:25X



DETAIL
NOT TO SCALE

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NOTES: (continued)

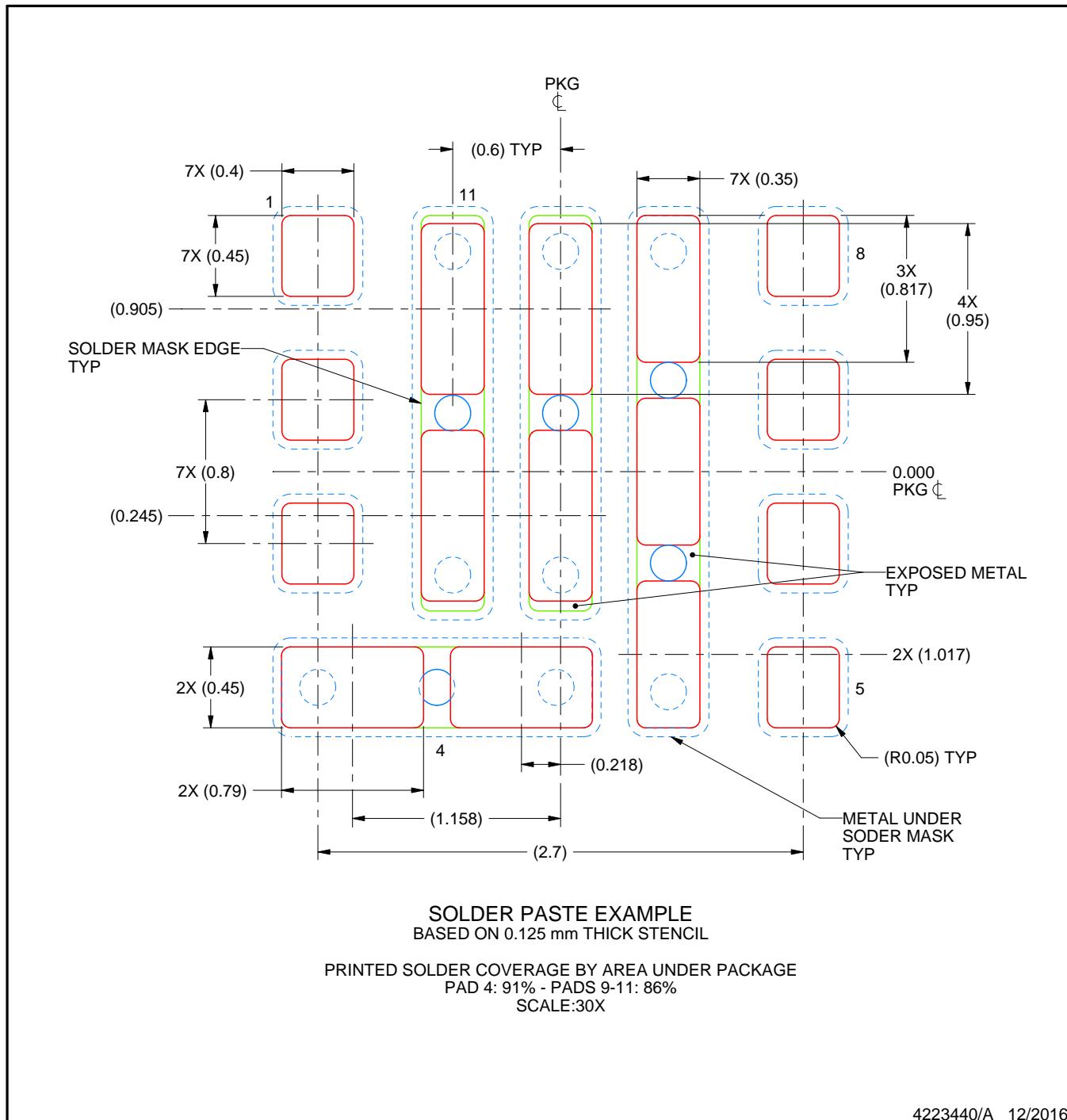
5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

SIL0011A

uSIP™ - 1.5 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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