

ARM Simulator Datasheet (v4.6)

FEATURES

- **Integrated With Code Composer Studio™ With Unified Loader Support for Both Microsoft Windows® and Linux Platforms**
- **Pin Connect for Injecting Interrupts to the Core**
- **Advanced Profiling**
- **Watchpoints**
- **Ease of Configuring the Simulator Through Enhanced Code Composer Studio Setup**
- **Full Instruction Set Simulators for ARM11™, ARM9e™, Cortex-M3™, and Cortex-R4™**
- **Endianness (Little, Big, BE-8: byte invariant; and BE-32: word invariant)**
- **Cycle Count Accurate ARM968 Simulator**
- **Cycle Count Accurate Cortex-M3 Simulator (alpha)**
- **Protocol Memory Compliant Interfaces in Cortex-M3 and ARM968™ Simulators**

DESCRIPTION

- Simulators are available with the Code Composer Studio for ARM-based devices.
- The complete instruction set is modeled for ARM11, ARM9e, Cortex-M3, and Cortex-R4 simulators.
- ARM simulators support device-level features such as, profiling, cycle accuracy, pin or port connect and watchpoints.
- The ARM968 simulator has been validated for cycle accuracy using internal design cases.
- Cycle accurate version of M3 Simulator (alpha release) is available.
- Functional device simulators (ARM 11, Cortex-M3, and Cortex-R4) for ARM-based devices model the functionality of the device without accounting for cycle effects. They are fast and can be used for application validation.

PRODUCT PREVIEW



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Summary of Architectural Features

Table 1. Architecture Features

FEATURE	ARM 11	ARM 968	CORTEX-R4	CORTEX-M3
Cycle count accurate	No	Yes	No	Yes
Protocol compliant memory interface	No	Yes	No	Yes
Exception Model	Yes	Yes	Yes	Yes
Memory Protection Unit	NA	NA	No	Yes

Summary of Simulator Configurations

Table 2. Simulator Configuration⁽¹⁾

DEVICE SIMULATED	CCS CONFIGURATION	CYCLE ACCURACY	SPEED IN MIPS	SPEED IN MCPS
ARM11	Little Endian	No	2.56	NA
	Big Endian	No	2.55	NA
	Big Endian [BE-8]	No	2.55	NA
ARM968	Little Endian	Yes	NA	2.90
	Big Endian	Yes	NA	2.89
Cortex-M3	Little Endian	Yes	0.84	1.23
	Big Endian	Yes	0.81	1.15
	Big Endian [BE-8]	Yes	0.81	1.15
Cortex-R4	Little Endian	No	2.58	NA
	Big Endian	No	2.57	NA
	Big Endian [BE-8]	No	2.57	NA

(1) Refer to table 7 for details

Summary of Capabilities

Table 3. Capabilities of Simulator Configuration

CCS CONFIGURATION	CYCLE ACCURACY	PROFILER	PIN CONNECT	PORT CONNECT	WATCH-POINT	
ARM11	Little Endian	No	Yes	Yes	No	Yes
	Big Endian	No	Yes	Yes	No	Yes
	Big Endian [BE-8]	No	Yes	Yes	No	Yes
ARM968	Little Endian	Yes	Yes	Yes	No	Yes
	Big Endian	Yes	Yes	Yes	No	Yes
Cortex-M3	Little Endian	Yes	Yes	Yes	No	Yes
	Big Endian	Yes	Yes	Yes	No	Yes
	Big Endian [BE-8]	Yes	Yes	Yes	No	Yes
Cortex-R4	Little Endian	No	Yes	Yes	No	Yes
	Big Endian	No	Yes	Yes	No	Yes
	Big Endian [BE-8]	No	Yes	Yes	No	Yes

Summary of Events

Table 4. Summary of Events

EVENTS SUPPORTED	DESCRIPTION	ARM 11			ARM 968		CORTEX-M3			CORTEX-R4		
		LE ⁽¹⁾	BE ⁽²⁾	[BE-8] ⁽³⁾	LE	BE	LE	BE	[BE-8]	LE	BE	[BE-8]
cycle.Total	This event count includes instruction execution cycle count, all stalls (including pipeline stalls cycles).	No	No	No	Yes	Yes	Yes	Yes	Yes	No	No	No
cycle.CPU	This event counts the cycles consumed by the CPU (including instruction execution, pipeline stall cycles).	No	No	No	Yes	Yes	Yes	Yes	Yes	No	No	No
CPU.instruction.decoded	This event is the number of instructions that are decoded. For a packet having two instructions in parallel, the counter will be incremented by two. For soft-dual instructions also, the counter will be incremented by two. In all cases, it will be the address of the first instruction that events is binned against.	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CPU.instruction.condition_failure	This event is the number of instructions that have been killed because of the execution condition. Instructions killed as a result of pipeline flush (such as in reset) are excluded from the list.	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

- (1) LE - Little Endian
- (2) BE - Big Endian
- (3) [BE-8] - Big Endian [BE-8]

Peripherals Supported

Table 5. Peripherals Supported

MODULE	ARM 11	ARM 968	CORTEX-R4	CORTEX-M3
AHBLite slave memory model	No	Yes	No	Yes
Memory Protection Unit	No	NA	No	Yes

Pins Supported on Pin Connect

Table 6. Pins Supported

PIN NAME	ARM 11	ARM 968	CORTEX-R4	CORTEX-M3
IRQ	Yes	Yes	Yes	No
FIQ	Yes	Yes	Yes	No
NMI	NA	NA	NA	Yes
ISR_0	NA	NA	NA	Yes
ISR_1	NA	NA	NA	Yes
ISR_2	NA	NA	NA	Yes
ISR_3	NA	NA	NA	Yes
ISR_4	NA	NA	NA	Yes
ISR_5	NA	NA	NA	Yes

PRODUCT PREVIEW

Table 6. Pins Supported (continued)

PIN NAME	ARM 11	ARM 968	CORTEX-R4	CORTEX-M3
ISR_6	NA	NA	NA	Yes
ISR_7	NA	NA	NA	Yes

Performance Numbers**Table 7. Performance Numbers ⁽¹⁾**

SIMULATOR CONFIGURATION	TEST CASE	MIPS	MCPS
ARM11	g723_arm9	3.17	NA
	g729_arm9	2.63	NA
	gsm51_arm9	3.18	NA
	gsmAMR_arm9	2.44	NA
	gsmefr_arm9	3.19	NA
	mpeg4_arm9	2.50	NA
	wbamr_arm9	3.17	NA
ARM968 (Flat Memory)	g723_arm9	2.58	3.91
	g729_arm9	1.66	2.47
	gsm51_arm9	2.63	3.88
	gsmARM_arm9	2.45	3.61
	Gsmefr_arm	2.27	3.40
	mpeg4_arm9	2.07	2.94
	wbamr_arm9	2.55	3.89
ARM968 (AHBLite compliant memory interface)	g723_arm9	1.65	2.50
	g729_arm9	1.35	2.00
	gsm51_arm9	2.30	3.40
	gsmARM_arm9	1.67	2.46
	gsmefr_arm9	1.15	1.73
	mpeg4_arm9	1.04	1.47
	wbamr_arm9	1.81	1.19
Cortex-M3	g723_arm9	0.83	1.43
	g729_arm9-m3	0.98	1.43
	gsm51_arm9-m3	0.98	1.37
	gsmARM_arm9	0.93	1.45
	gsmefr_arm-m3	0.99	1.07
	mpeg4_arm-m3	0.82	1.45
	wbamr_arm9	0.99	1.17
Cortex-R4	g723_thumb	2.68	NA
	g729_thumb	2.66	NA
	gsm51_thumb	2.70	NA
	gsmARM_thumb	2.68	NA
	gsmefr_thumb	2.69	NA
	mpeg4_thumb	2.47	NA
	wbamr_thumb	2.65	NA

(1) All benchmarks were run on a Microsoft Windows machine with a P4 Processor and 1GB RAM.

Cycle Accuracy

- Cycle accuracy validation for ARM968 and Cortex-M3 were performed with internal design test cases.

References

You can refer to the following manuals on www.arm.com:

- ARM968 Technical reference manual
- ARM11 Technical reference manual
- Cortex-M3 Technical reference manual
- Cortex-R4 Technical specification manual

Glossary

Term	Description
Cycle Accuracy	Correlation between cycles reported by simulator versus the real hardware

Acronyms

Acronym	Description
MIPS	Million Instructions Per Second
MCPS	Million Cycles Per Second
MPU	Memory Protection Unit

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