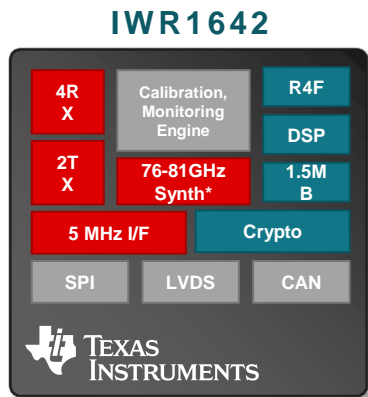


Device Overview – IWR6843

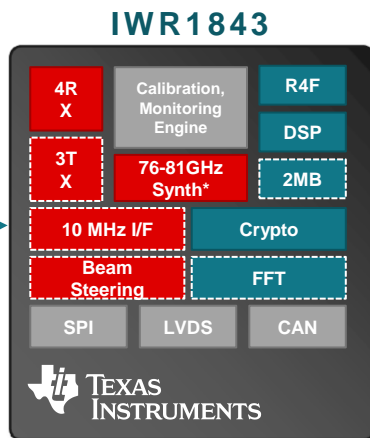
Path to 60GHz: Changes from 77GHz to 60GHz

77GHz Today



* 2x VCO: 76-77GHz & 77-81GHz

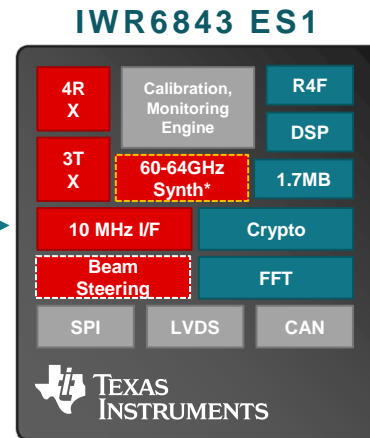
77GHz Next



Delta from IWR1642

* 2x VCO: 76-77GHz & 77-81GHz

60GHz



Delta from IWR1843

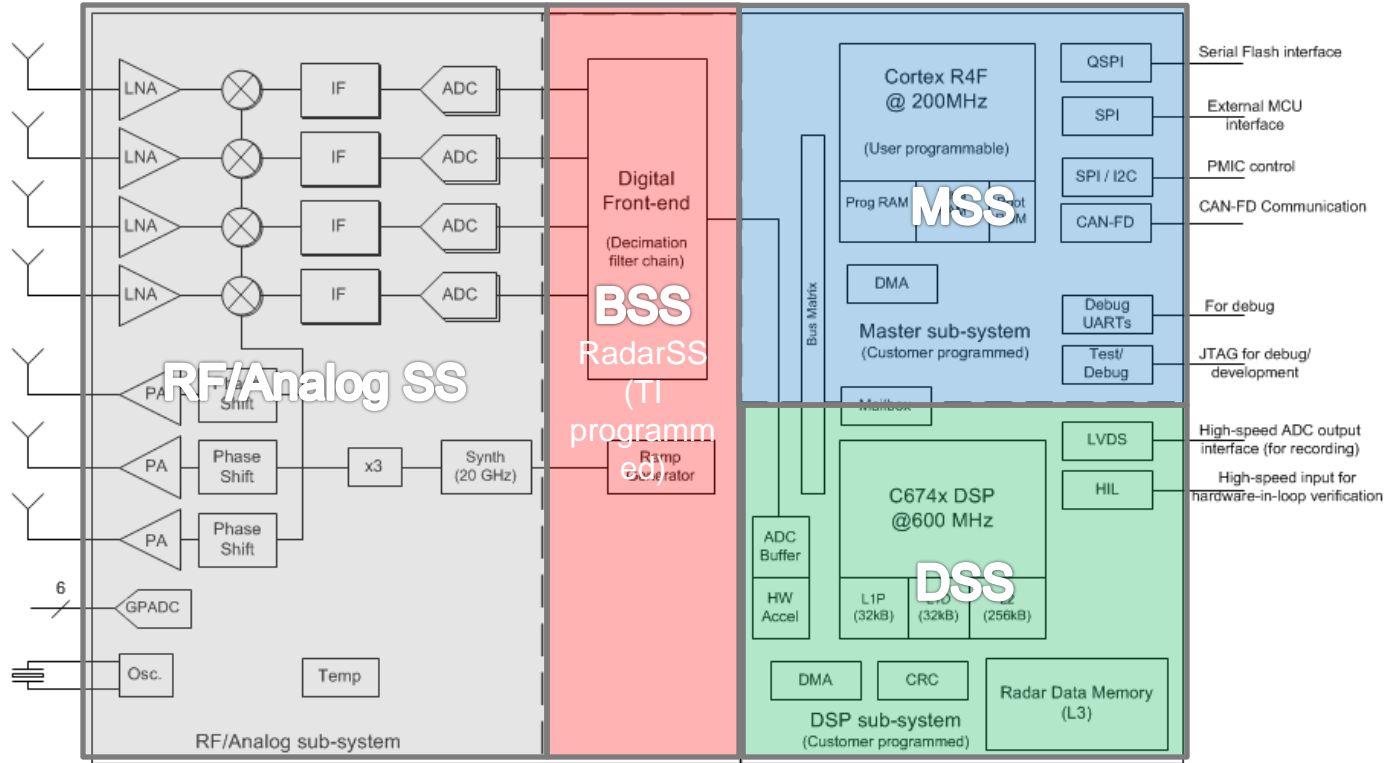
Package Change

Same Package & Pinout

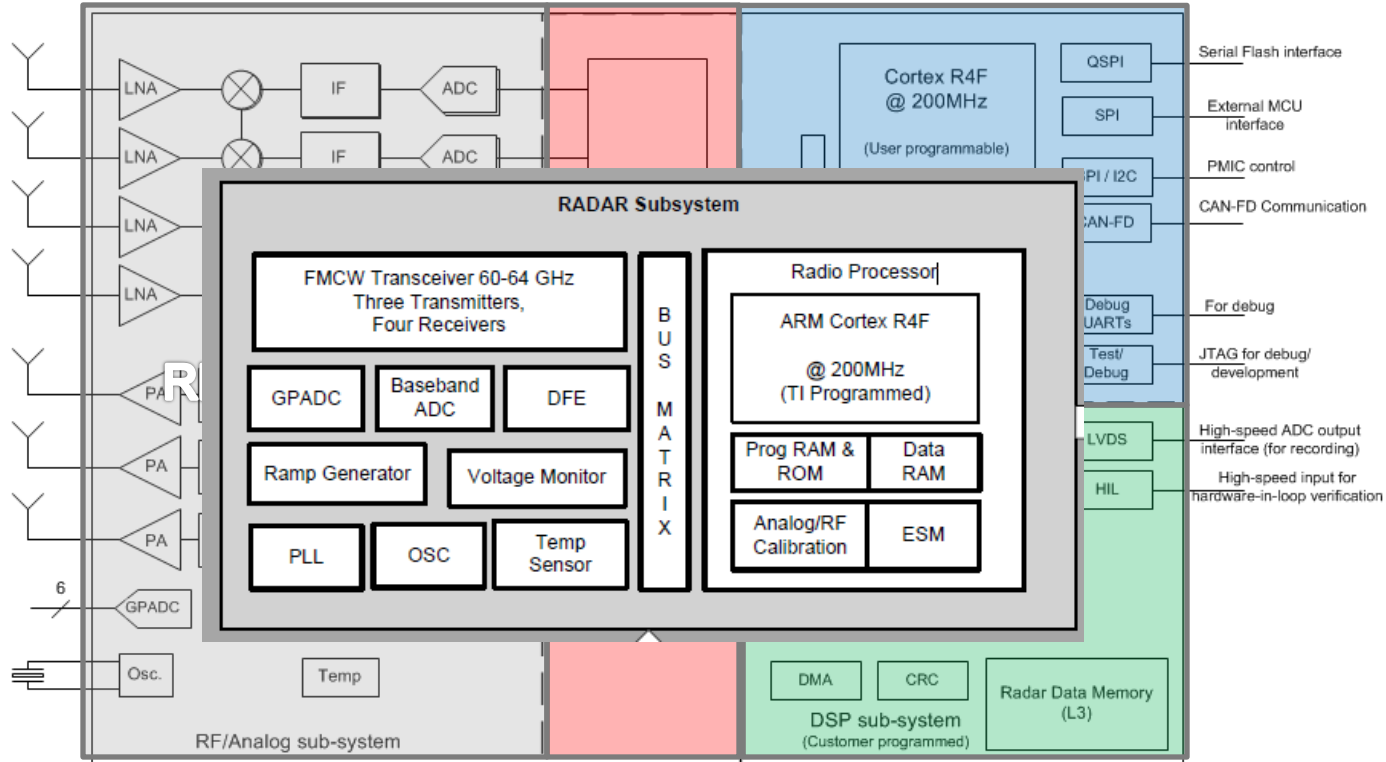
Device feature comparison

FUNCTION		IWR6843	IWR1642	IWR1443
Number of receivers		4	4	4
Number of transmitters		3	2	3
RF frequency range		60 to 64 GHz	76 to 81 GHz	76 to 81 GHz
On-chip memory		1.75MB	1.5MB	576KB
Max I/F (Intermediate Frequency) (MHz)		10	5	15
Max real sampling rate (MSPs)		25	12.5	37.5
Max complex sampling rate (MSPs)		12.5	6.25	18.75
Processor				
MCU (R4F)		Yes	Yes	Yes
DSP (C674x)		Yes	Yes	—
Peripherals				
Serial Peripheral Interface (SPI) ports		2	2	1
Quad Serial Peripheral Interface (QSPI)		Yes	Yes	Yes
Inter-Integrated Circuit (I ² C) interface		1	1	1
Controller Area Network (DCAN) interface		—	Yes	Yes
Controller Area Network (CAN-FD) interface		Yes	—	—
Trace		Yes	Yes	—
PWM		Yes	Yes	—
Hardware In Loop (HIL/DMM)		Yes	Yes	—
GPADC		Yes	Yes	Yes
LVDS/Debug		Yes	Yes	Yes
CSI2		—	—	Yes
Hardware accelerator		Yes	—	Yes
1-V bypass mode		Yes	Yes	Yes
JTAG		Yes	Yes	Yes
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	AI ⁽¹⁾	PD ⁽²⁾	PD ⁽²⁾

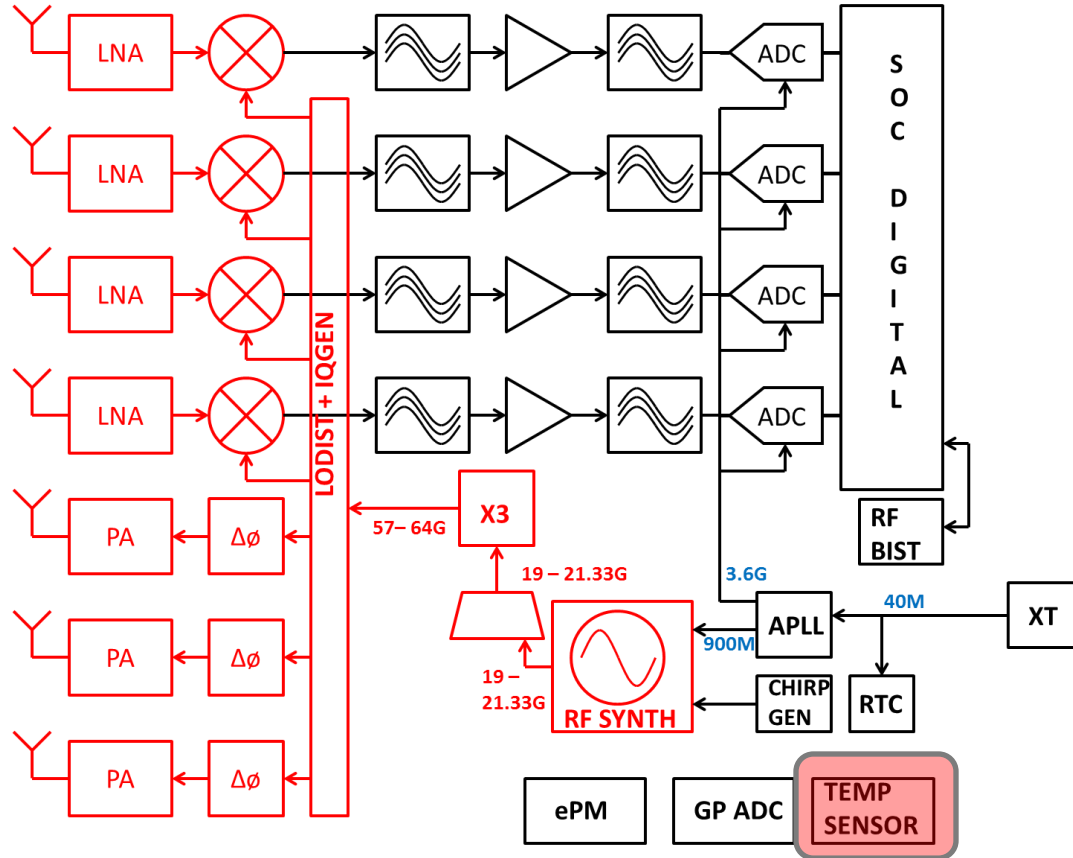
IWR6843 device block diagram



IWR6843 device block diagram



IWR6843 RF Block diagram

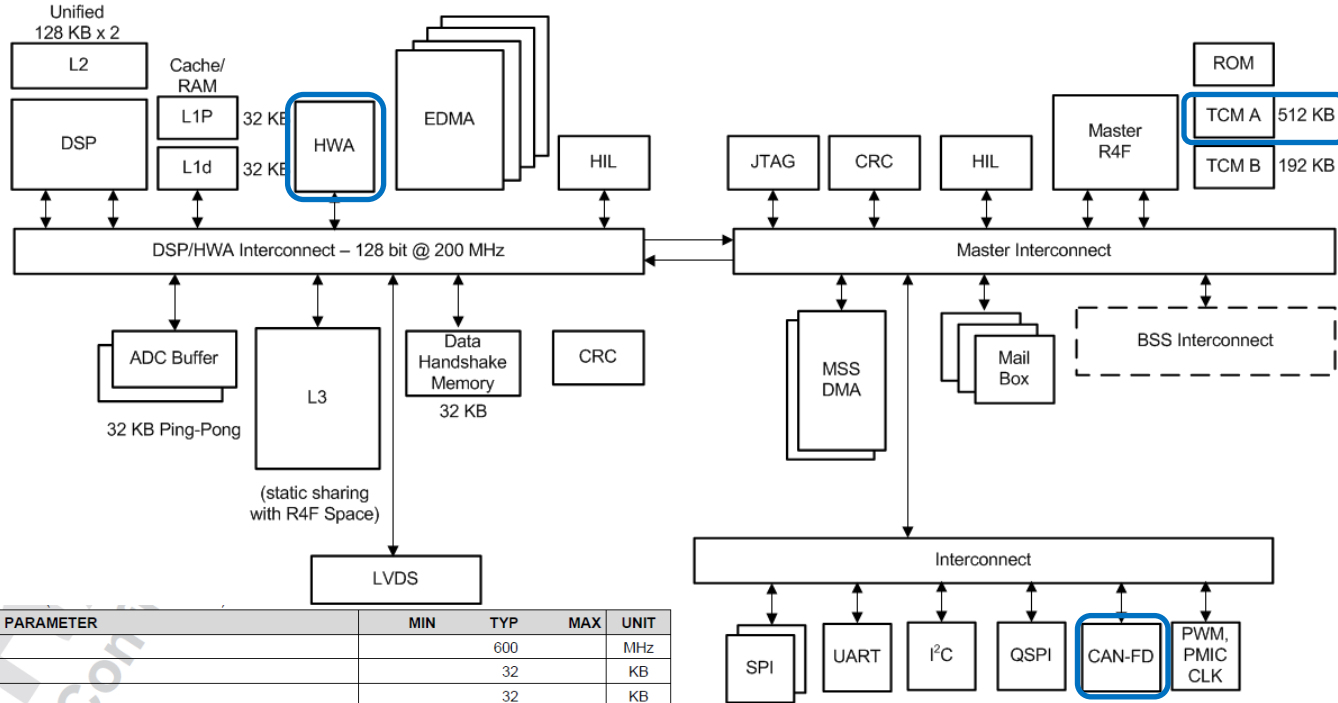


RF specification

PARAMETER		MIN	TYP	MAX	UNIT
Receiver	Noise figure	60 to 64 GHz	14		dB
	IF bandwidth ⁽¹⁾			10	MHz
	A2D sampling rate (real)			25	Msp/s
	A2D sampling rate (complex 1x)			12.5	Msp/s
	A2D resolution		12		Bits
	Idle Channel Spurs		-90		dBFS
Transmitter	Output power		10		dBm
Clock subsystem	Frequency range	60		64	GHz
	Ramp rate			266	MHz/ μ s
	Phase noise at 1-MHz offset	60 to 64 GHz	-92		dBc/Hz

Processor Subsystem

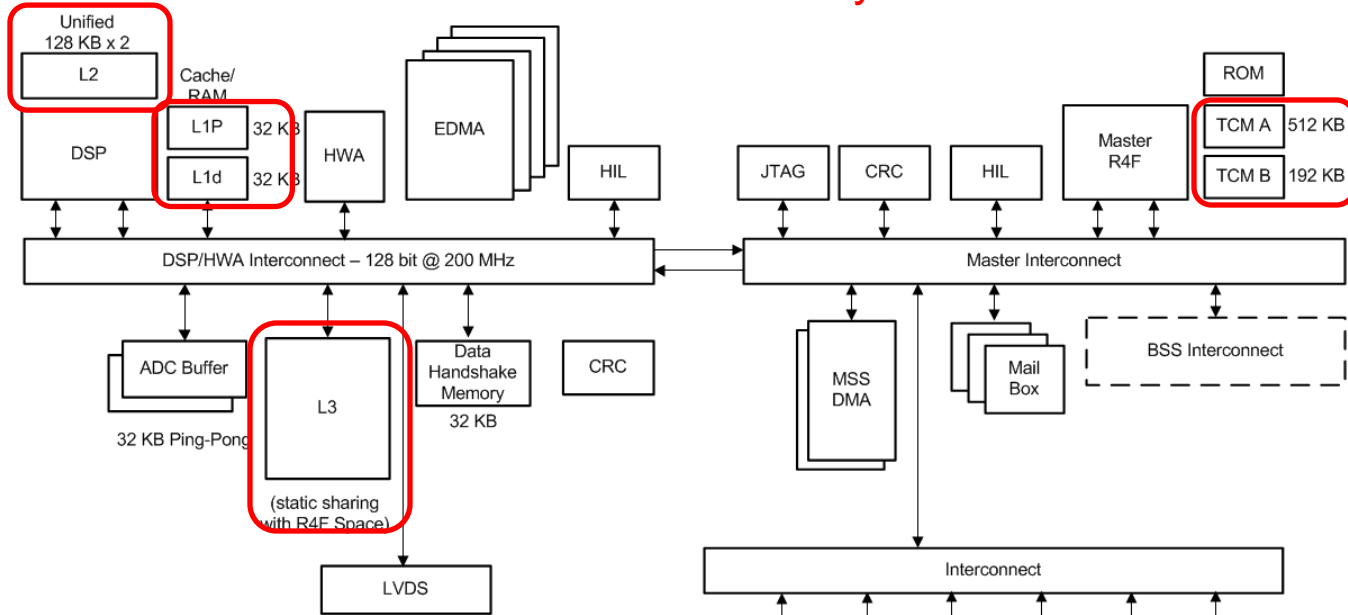
 New added in IWR6843



PARAMETER		MIN	TYP	MAX	UNIT
DSP Subsystem (C674 Family)	Clock Speed		600		MHz
	L1 Code Memory		32		KB
	L1 Data Memory		32		KB
	L2 Memory		256		KB
Master Controller Subsystem (R4F Family)	Clock Speed		200		MHz
	Tightly Coupled Memory - A (Program)		512		KB
	Tightly Coupled Memory - B (Data)		192		KB
Shared Memory	Shared L3 Memory		768		KB

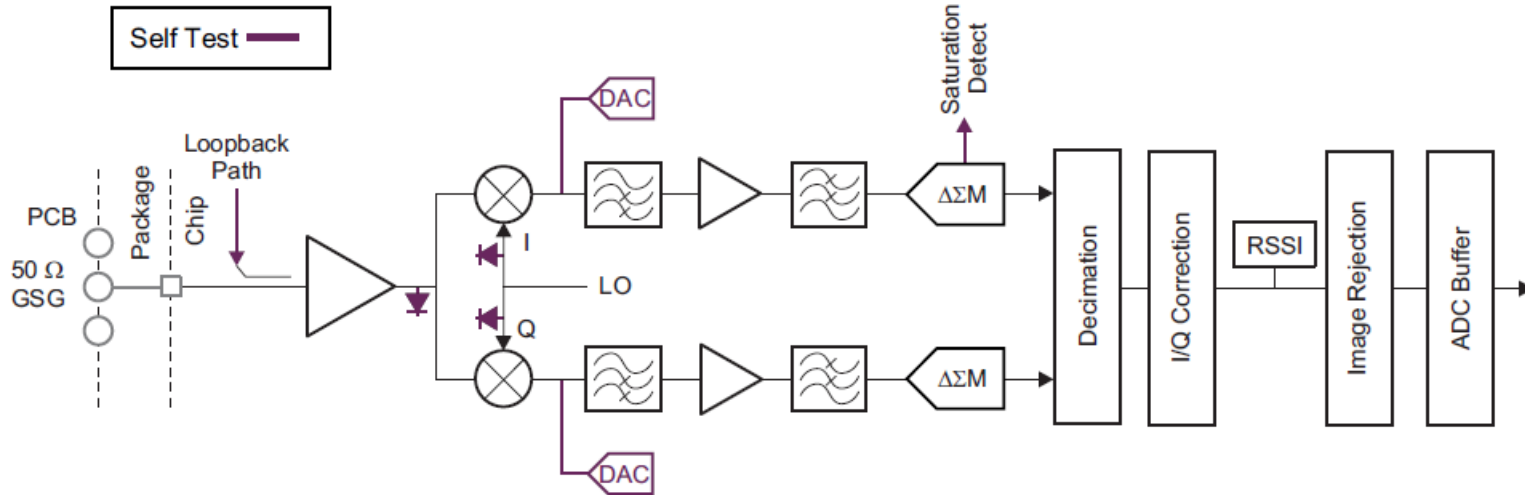
Processor Subsystem

Total Memory $32+32+256+512+192+768=1792$



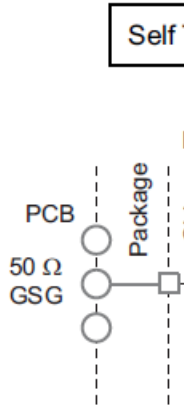
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	Tightly Coupled Memory - A (Program)		512		KB
	Tightly Coupled Memory - B (Data)		192		KB
Shared Memory	Shared L3 Memory		768		KB

RX Subsystem



- The IWR6843 receive subsystem consists of four parallel channels
- Unlike conventional real-only receivers, the IWR6843 device supports a complex baseband architecture (see the [white paper](#))
- Device is targeted for fast chirp systems

RX Subsystem



- The IWR
- Unlike co
- baseban
- Device i

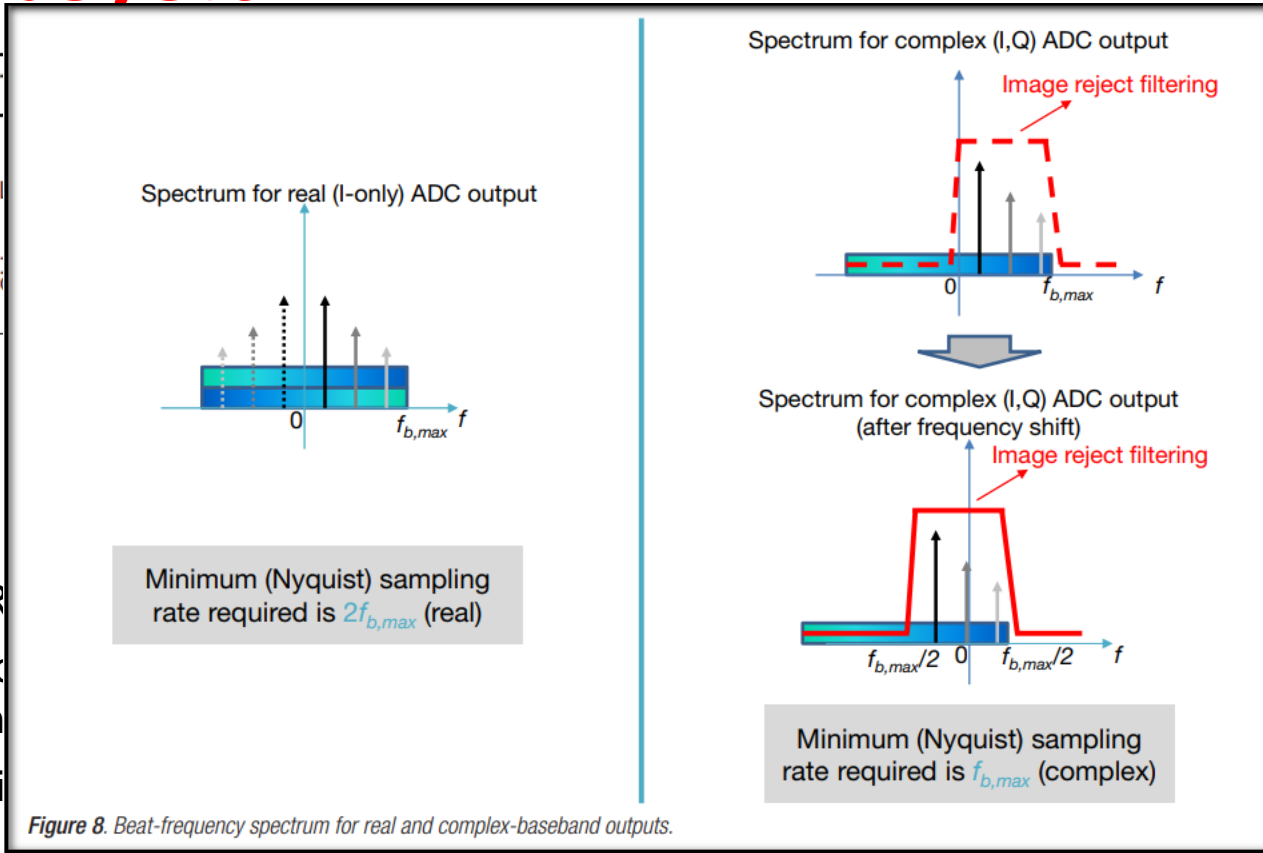



Figure 8. Beat-frequency spectrum for real and complex-baseband outputs.

RX Subsystem

Self Test 

DAC

Saturation Detect

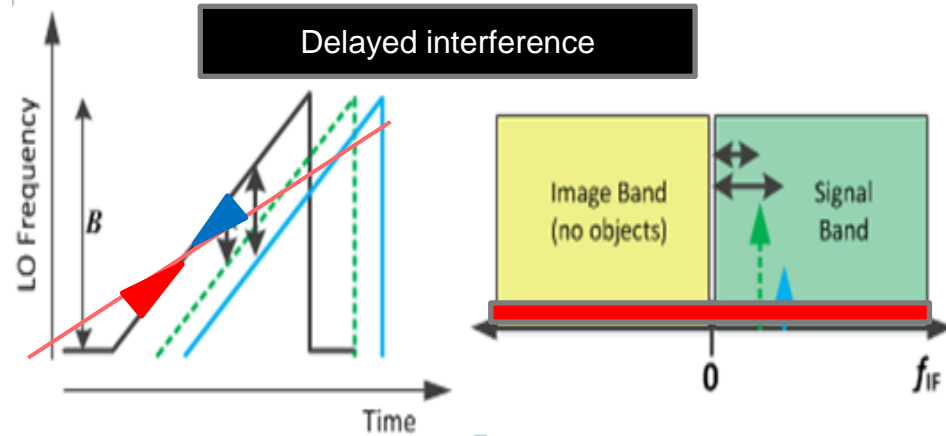
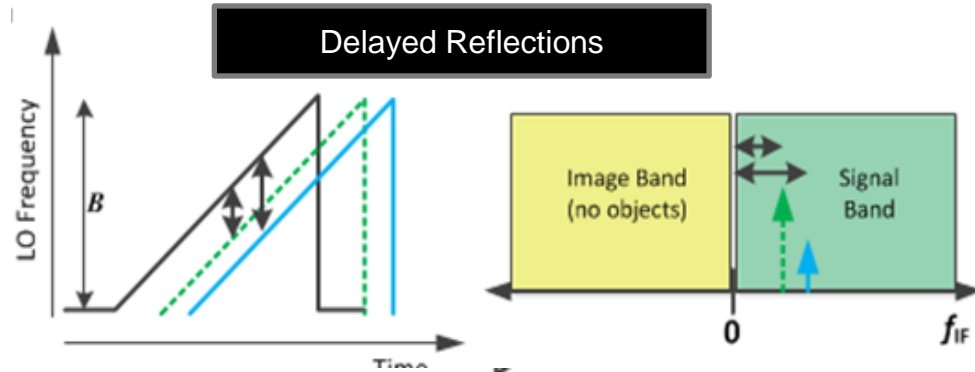
Loopback

PCB	Comparison item	Complex-baseband option	Real-only option	Comments
50 Ω	ADC output data rate	Complex (I,Q) samples at $f_{b,max}$	Real (I-only) samples at $2f_{b,max}$	Both options are similar
GSG	FFT complexity ($N = T_c f_{b,max}$)	N-point FFT with complex input	2N-point FFT with real input	Both options are similar, with complex baseband having a slight advantage (2N-point FFT of real samples is possible using N-point complex FFT, plus a few additional operations)
	Memory requirement (for M chirps/frame, for 1 RX)	NM complex samples to be stored	NM complex samples to be stored (negative frequency components discarded after 2N-point FFT of real input)	Both options are similar
	Noise figure	Better than baseline by up to 3dB	Baseline	Advantage with complex baseband

- The
- Unlike conventional real-only receivers, the IWR6843 device supports a complex baseband architecture (see the [white paper](#))
- Device is targeted for fast chirp systems

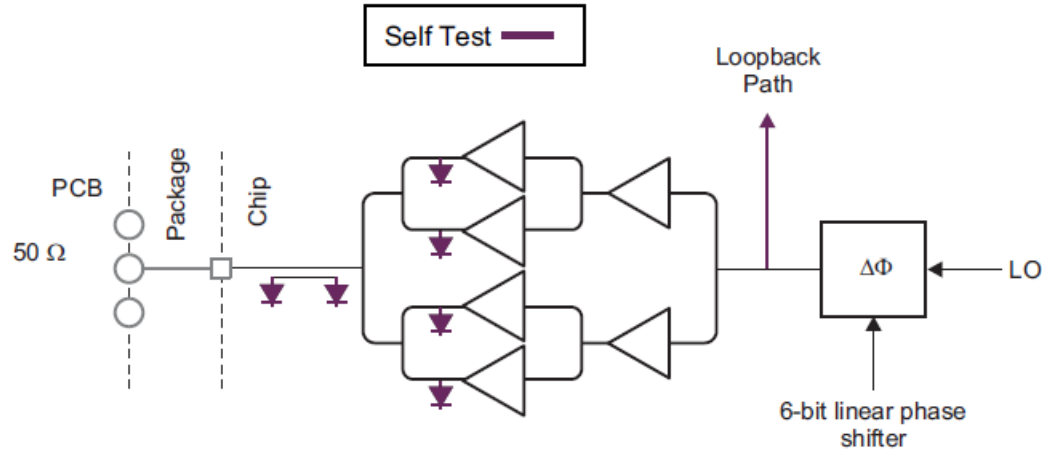
Crossing interferer: Frequency Domain

- All the target reflection are in signal band, the image band only has thermal noise, the power is very low.
- When the FMCW interferer and FMCW victim chirp cross in time.
 - In frequency domain, there will be an increase of noise floor.



TX Subsystem

- IWR6843 transmit subsystem consists of three parallel transmit chains
 - Each with independent phase and amplitude control
 - 2 TX simultaneously
- The device supports binary phase modulation for MIMO radar and interference mitigation.



Reference

- Using a complex-baseband architecture in FMCW radar systems
<http://www.ti.com/lit/wp/spyy007/spyy007.pdf>
- mmWave Training Series
<https://training.ti.com/mmwave-training-series>

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