

EMI Suppression of FPD-Link Device In Automotive Application (I)

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ABSTRACT

Electronics content in vehicles is increasing rapidly in recent years and becoming more advanced. These installations are creating a hostile electromagnetic environment, which affects the critical operations of the system by creating interference to other parts of the system and making automotive electromagnetic compatibility (EMC) more difficult. As safety measures have become higher priorities, dealing with electromagnetic interference (EMI), especially reducing radiated emission (RE), has become a huge challenge to automotive electronics designers.

This series of application notes, which contains two reports, covers how to reduce FPD-Link system EMI in different aspects, including component and system level. This report focuses on spread spectrum clock generation (SSCG) on chip clock dithering, which is one of the most important component-level EMI reduction technologies in FPD-Link products. Also, the principle of triangular modulation is discussed in detail and formulae have been derived to make useful estimates of improvement in EMI suppression through SSCG.

The documentation was validated, by product-level testing of DS90UH926Q, and expected reduction in EMI was observed through SSCG.

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1 Introduction

EMI has become an increasingly critical issue for modern electronic control system design, especially for the rapidly evolving automotive industry. In this industry, installation of electronic subassembly (ESA) refers to almost any electrical or electronic device fitted to a vehicle during the past 10 years to enhance safety, controllability, and comfort. As safety has become an important consideration, extremely high reliability is a necessity for designing an automotive electronics system. A single failure over millions of vehicles cannot be tolerated.

Among traditional electronics installations, such as engine management unit (EMU), electronic control unit (ECU), heating, ventilation and air-conditioning systems (HVAC), the entertainment terminals (DVD, MP3, navigation, Bluetooth[®], phone) have become popular and essential vehicle accessories. These terminal installations radiate RF emission, which is fatal to other critical systems, related to the safety of people. On the other hand, these terminal installations are also easily disturbed by the external source.

Because the automotive environment is so severe, many strict standards have been built to ensure the reliability. Besides the International Special Committee on Radio Interference (CISPR) and ISO that mainly develop the automotive EMI standards, nearly all manufacturers around the world have developed their own EMI standards (based on CISPR-25 and ISO11452) that must be passed by ESA suppliers.

1.1 Radiated Emissions Standard

Generally, EMI can be divided into two groups,

- **Electromagnetic Emission:** This refers to automotive electronics acting as a source of EMI. Emissions can be subdivided into Radiated Emissions and Conducted Emissions.
- **Electromagnetic Immunity:** This refers to the ability to reject external EMI/RF noise. Immunity can also be classified as Radiated Immunity and Conducted Immunity, correspondingly.

For a vehicle entertainment terminal, because high-speed components (such as LVDS Serializer/Deserializer) or RF devices (GPS, WIFI) are used, RE is dominant compared to conducted type. Currently, RE tests of almost all automotive OEMs are derived from RE standards of CISPR-25, such as GS95002 of BMW and GMW3097 of General Motors.

CISPR-25 covers a wider frequency range from 76 to 1000 MHz. Emission from the components must be measured in an absorber lined screened enclosure (ALSE). Figure 1 shows the test setup. Table 1 lists the radiated measurement of narrowband limit levels.

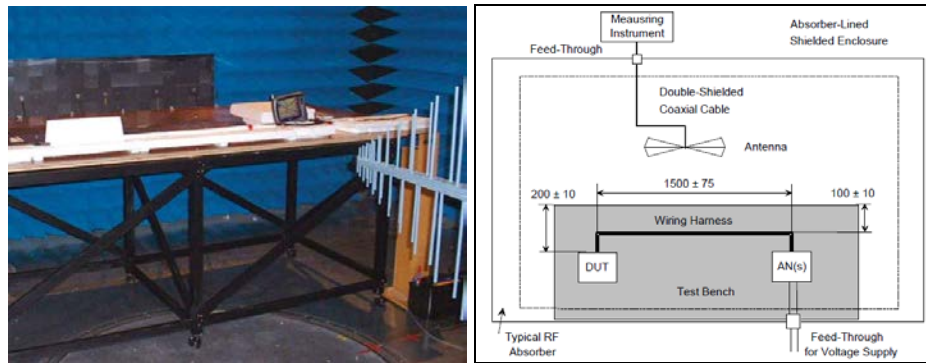


Figure 1. Radiated Emissions Measurements for an Automotive ESA

Table 1. CISPR-25 Radiated Measurement of Narrowband Limit Levels for Specified Frequency Bands (Global Requirements)

Test No.	Usage	Frequency Range (MHz)	Measuring Instrument Bandwidth (kHz)	Limit Value (dBuV/m)
G6	VHF	76–108	100/120	12
G7	Communications	140–180	9/10	12
G8	TETRA/Trunking	380–430	9/10	12
G9	Remote Keyless Entry	430–433	9/10	8
		433–435		6
		435–438		8
G10	Communications	420–520	9/10	18
G11	Cell Phone	869–894	9/10	18
G12	GSM 30m	925–960	9/10	18

1.2 FPD-Link for Automotive Application

TI has been dedicated to automotive industry for many years as one of the major IC suppliers. TI released the FPD-Link series of devices to help customers successfully achieve excellent system design. DS90UR905/906Q, FPD-Link II devices are widely used in vehicle LCD panel displays. The High-Bandwidth Digital Content Protection (HDCP) feature was added to new generation of the devices called FPD-Link III (for example, DS90UH925/6Q). These devices let automotive OEMs design systems that support content protection of video signals from sources such as Blu-Ray discs, iTunes purchases, and other media formats.

These products provide an automotive qualified solution to transport high-definition video and audio between automotive subsystems. The solution is designed to operate with minimal software support. More importantly, it is designed to implement a very low EMI profile with several enhanced functions, which helps ESA suppliers quickly pass EMI tests, and hence shorten the design cycle.

2 RE Suppression in Component Level

EMI is a system-level issue to which designers must pay full attention. During the component selection stage, the device with a built-in RE suppression function is of prime importance to designers. Devices in the FPD-Link family have a built-in spread spectrum clock generator (SSCG) feature to reduce RE. The following sections discuss the effectiveness of the SSCG feature.

2.1 SSCG in FPD-Link

The deserializer from FPD-Link II/III provides an internal SSCG to modulate output over the parallel bus by modulating the output at a frequency, f_{mod} , and with a maximum frequency deviation of $F_{dev}/2$. Both clock and data outputs are modulated to reduce RE to the maximum extent.

In DS90UH926Q, internal SSCG generates a triangular modulation with maximum frequency deviation, f_{dev} , of $\pm 2.5\%$ (total 5% of main clock [PCLK]) and with modulation frequency up to 100 kHz. Figure 2 shows the modulation expectation. f_{dev} is frequency deviation from PCLK, and f_{mod} is modulation frequency (see Figure 2).

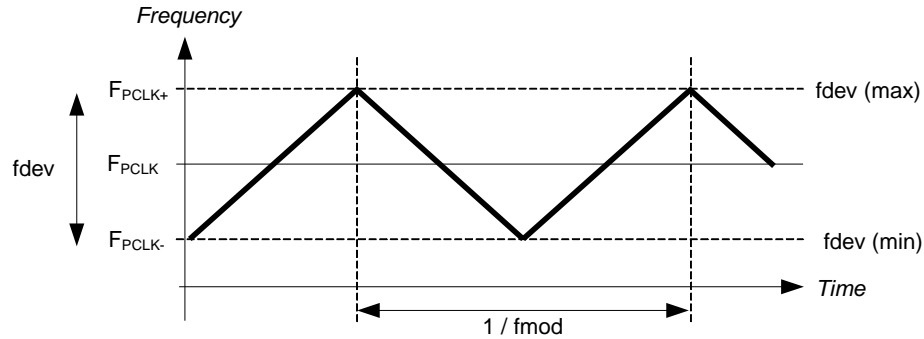


Figure 2. SSCG Waveform

In typical PLL design, VCO output is modulated by an output of a charge pump. Let $x(t)$ represent VCO control signal, then VCO output, $f = f_c + x(t)$, where, f_c is VCO center oscillation frequency. Theoretically, $x(t)$ could be any waveform. However, in practice, sinusoidal, triangular, and exponential are the most common forms used to implement SSCG. In TI's FPD-Link, the triangular SSCG (using symmetrical waveform to remove accumulated DC component in PLL) is used for optimization to obtain flat attenuation of the modulating bandwidth (BW).

PCLK of these devices outputs a square wave (an unmodulated signal when SSCG is off). The square wave contains harmonics. For example, consider a pure sinusoidal carrier with frequency f_c (fundamental component of square) and modulated by one sinusoid with frequency f_m . The resultant modulated signal can be mathematically represented as follows:

$$V(t) = A \cos(2\pi f_c t + \int x(t) dt),$$

Where, $x(t) = 2\pi \cdot \Delta f \cdot \cos(2\pi f_m t)$,

Use a complex number concept and Bessel Function,

$$V(t) = A \sum_{n=-\infty}^{\infty} J_n(\Delta f / f_m) \cos(2\pi f_c t + n \cdot 2\pi f_m t)$$

Where, $J_n(\Delta f / f_m)$ is Bessel Function of The First Kind. It presents frequency spectrum which consists of fundamental component of f_c and SB (side-band) components of nf_m . The amplitudes A_n of frequency $f_c \pm nf_m$ meet power conservation constraint $A^2 = A_c^2 + 2(A_1^2 + A_2^2 + A_3^2 \dots)$. According to Parseval and Carson's rule, the total power of an FM signal is contained within a bandwidth of amplitude $B_p = 2(m+1)f_m$, where $m = \Delta f / f_m$ is the frequency modulation index. Therefore, the power of the unmodulated signal gets spread over the bandwidth $[f_c - B_{p/2}, f_c + B_{p/2}]$ after modulation, thus reducing the highest energy at unmodulated frequency f_c .

Every harmonic of a square wave is a sinusoidal wave. Hence, due to SSCG (that is, triangular frequency modulation) every harmonic spreads over a BW with the fundamental harmonic. Accordingly, the BW occupied by each modulated harmonic can be written using Carson's rule as, $B_p^n = 2(nm+1)f_m \approx nB_p$ (for $m \gg 1$), where n represents the n^{th} harmonic of square wave clock.

Based on the preceding analysis, a triangular modulated square wave is not a simple close form. The expression is highly complicated and not suitable for EMI suppression prediction. To avoid complications and make a feasible estimate, use the average power density spectrum concept to calculate the power spreading into B_p^n .

According to Fourier series, a square wave can be expressed by the following equation:

$$V(t) = \frac{4A}{\pi} \sum_{n=1}^{\infty} \left[\frac{1}{2n-1} \sin(2n-1)2\pi f_c \right],$$

$$n^{th} \text{ harmonic of square wave is } V_n(t) = \frac{4A}{\pi} \left[\frac{1}{2n-1} \sin(2n-1)2\pi f_c \right],$$

So, average PDS after modulated by triangular wave of $V_n(t)$ is $B \times \frac{1}{2} \left[\frac{4A}{\pi} \left(\frac{1}{2n-1} \right) \right]^2 / nB_p$,

where B is resolution BW of the spectrum analyzer. nB_p is BW of n^{th} harmonic after modulation.

So the power of n^{th} harmonic of square wave compared to the corresponding average power of n^{th} modulated harmonic is:

$$\begin{aligned} S_{nn} &= 10 \log \left\{ \frac{1}{2} \left(\frac{4A}{\pi} \frac{1}{2n-1} \right)^2 / \left[B \times \frac{1}{2} \left(\frac{4A}{\pi} \frac{1}{2n-1} \right)^2 / nB_p \right] \right\} \\ &= 10 \log \frac{nB_p}{B} \end{aligned}$$

And the power of fundamental component of square wave compare to the average power of n^{th} modulated harmonic is:

$$S_{1n} = 10 \log \left\{ \frac{1}{2} \left(\frac{4A}{\pi} \right)^2 / \left[B \times \frac{1}{2} \left(\frac{4A}{\pi} \frac{1}{2n-1} \right)^2 / nB_p \right] \right\}$$

$$= 10 \log \frac{nB_p (2n-1)^2}{B}$$

Formula of S_{nn} and S_{1n} derived above can be applied to estimate RE improvement of SSCG while not only limited to FPD-Link device. For example, S_{33} represents the attenuation of the 3rd harmonic of square wave or RE improvement after SSCG turns on.

2.2 RE Improvement From SSCG

FPD-Link II/III modulates parallel output bus by modulating the output at a frequency, f_{mod} , and with a maximum frequency deviation of $F_{\text{dev}}/2$. For DS90UR906Q, output SSCG frequency deviates by $\pm 2.0\%$ of PCLK and up to 35 kHz modulation frequency, as compare to deviation up to $\pm 2.5\%$ at 100 kHz(max) for DS90UH926Q.

The remaining part of this section summarizes estimated RE improvement through SSCG function for DS90UH926Q, based on the results derived in the preceding section. Because the device has two modes—LFMODE = L(15–85 MHz) and LFMODE = H(5–<15 MHz)—calculations are made by setting LFMODE = L at 33 MHz clock and LFMODE = H at 10 MHz clock. See the detailed calculations in Table 2 and Table 3.

Table 2. DS90UH926Q SSCG Performance of LFMODE = L

SSCG Configuration when LFMODE = L (15–85 MHz), PCLK = 33 MHz									
SSC[2:0]			Results						
SSC[2]	SSC[1]	SSC[0]	Fmod(kHz)	Fdev(%)	$m = \Delta f/f_m$	Bp(kHz)	dB		
							S ₁₁	S ₂₂	S ₃₃
L	L	L	CLK/2168 =33 MHz/2168 =15.2 kHz	+/- 0.9=297 kHz	39	1216	10.8	13.8	15.6
L	L	H		+/- 1.2=396 kHz	52.2	1617	12.1	15.1	16.9
L	H	L		+/- 1.9=627 kHz	82.6	2541	14.1	17.1	18.8
L	H	H		+/- 2.5=825 kHz	108.6	3332	15.2	18.2	20
H	L	L	CLK/1300 =33 MHz/1300 =25.4 kHz	+/- 0.7=231 kHz	18.2	975	9.9	12.9	14.7
H	L	H		+/- 1.3=429 kHz	33.8	1767	12.4	15.5	17.2
H	H	L		+/- 2.0=660 kHz	52	2692	14.3	17.3	19.1
H	H	H		+/- 2.5=825 kHz	65	3353	15.2	18.3	20

Table 3. DS90UH926Q SSCG Performance of LFMODE = H

SSCG Configuration when LFMODE = H, CLK (5-<15 MHz) ,PCLK = 10 MHz									
SSC[2:0]			Results						
SSC[2]	SSC[1]	SSC[0]	fmod (kHz)	Fdev(%)	m = Δf/f _m	B _p (kHz)	dB		
							S ₁₁	S ₂₂	S ₃₃
L	L	L	CLK/628 =10 MHz/628 =15.9 kHz	+/- 0.5=50 kHz	6.3	232	3.7	6.7	8.4
L	L	H		+/- 1.3=130 kHz	16.4	553	7.4	10.4	12.2
L	H	L		+/- 1.8=180 kHz	22.6	750	8.8	11.7	13.5
L	H	H		+/- 2.5=250 kHz	31.4	1030	10.1	13.1	14.8
H	L	L	CLK/388 =10 MHz/388 =25.8 kHz	+/- 0.7=70 kHz	5.4	330	5.2	8.1	9.9
H	L	H		+/- 1.2=120 kHz	9.3	531	7.2	10.3	12
H	H	L		+/- 2.0=200 kHz	15.5	851	9.2	12.3	14.1
H	H	H		+/- 2.5=250 kHz	19.4	1052	10.2	13.2	15

To keep similar value for fmod, different scale factors are used in different modes. In LFMODE = L (**high-frequency clock**), the scale factor is 1/2168 and 1/1300, while in LFMODE=H (**low-frequency clock**), the scale factor is 1/628 and 1/388. Although scale factor is different for the two mode, fmod is comparable for the two modes; Fdev(%) is also of similar range, varying from 0.5% to 2.5%.

A larger Fdev(%) results in a larger modulation index, $m = \Delta f / f_m$ and wider B_p (because $B_p = 2(m+1)f_m$). Hence, the total peak power occurring at a single frequency in unmodulated signals spreads over a band of frequency, B_p . This eventually results in reduced RE.

In Table 2, when fmod = CLK/2168, Fdev varies from 0.9% to 2.5%, S_{11} improves from 10.8 to 15.2 dB. Because every harmonic of a 33-MHz square wave is modulated by a triangular wave, n^{th} harmonic (S_{22}, S_{33}) has the same effect as the fundamental wave (S_{11}).

Comparing Table 2 and Table 3 by using similar Fdev level (using the same SSC[2:0] setting), the result is different due to the different clock used. For example, when SSC[2:0] = LHH, with LFMODE = L (see Table 2), m is 108.6, B_p is 3332 kHz, and S_{11} is 15.2 dB; with LFMODE = H (see Table 3), m is 31.4, B_p is 1030 kHz, and S_{11} is 10.1 dB.

The designer can use the preceding tables to evaluate the contribution of SSCG toward RE improvement, which the data sheet does not include. The same calculation is also applied to FPD-Link II (DS90UR906Q). One thing that designers must know when using SSCG is that more reduction in RE can be achieved with wider B_p . However, it also means more power leaks to wider frequency bands. This situation limits the desirable frequency bands from which to choose. The designer must make the tradeoff according to these requirements.

2.3 Other RE Suppression Solution in FPD-Link

Besides SSCG lowering EMI by spreading the peak power at harmonic frequencies over a certain band of frequencies, there are several other effective methods to suppress RE in the FPD-Link device.

- Lowering the PCLK power supply is more direct way to suppress RE in the FPD-Link device. The deserializer parallel bus of DS90UH926Q and DS90UR906Q can operate with 1.8 V. Compared to 3.3 V, 1.8 V VDDIO for PCLK can be 5.3 dB lower at the fundamental wave.
- Enhanced Progressive Turn-On (EPTO). The deserializer LVCMOS parallel outputs timing are delayed. Groups of 8-bit R, G, and B outputs switch in a different time, thus minimizing the number of outputs switching simultaneously and helping to reduce supply noise.
- Serialized data is randomized and scrambled, thus reducing harmonics that may be associated with repetitive data patterns.

3 RE Experimentation

Table 4 summarizes RE test results based on an OEM RE standard. The system under test used DS90UH926Q to deserialize LVDS signal and sent RGB signals to a LCD panel, using 25MHz PCLK.

Initial Test Results with SSCG OFF:

As listed in Table 4, many harmonics from a 25-MHz clock exceed the limitation of the 75-MHz standard, which is the 3rd harmonic, and is 10.7 dB over the 12dBuV/m limitation, 7 dB for 100 MHz (4th), 32 dB for 175 MHz (7th), and 31 dB for 225 MHz (9th). Among the harmonics, the 7th harmonic is the most severe RE source.

EMI and signal integrity violations in both the high-speed signal path (LVDS) and low-speed signal path (LVCMOS) are the most probable reasons for such EMI failure. To way to achieve the expected results without making much change to the whole design is to use SSCG followed by scaling Fdev to optimize the performance.

Test Results with SSCG ON:

Table 4 and Figure 3 show the result with SSCG ON. After optimizing Fdev% (27.4 MHz clock used as per OEM requirement), a huge improvement can be observed as compared to when SSCG was OFF.

Table 4. RE Test With SSCG OFF and ON

Band	Freq Band (Hz)	RBW (Hz)	Step (Hz)	Dwell Time (ms/Pts)	Maximum Emission			Limit (dBuV/m)	Result With SSCG OFF	Results With SSCG ON
					Freq (MHz)	Level (dBuV/m)	Margin (dB)			
1	45.2-47.8M	9k	4.5k	10	45.5	-2.9	-14.9	12	Pass	Pass
2	65.2-88.1M	9k	4.5k	10	75	22.73	10.73	12	Fail	Pass
3	75.2-90.9M	9k	4.5k	10	85	3.21	-8.79	12	Pass	Pass
4	86.5-109.1M	9k	4.5k	10	100	19	7	12	Fail	Pass
5	140.6-176.3M	9k	4.5k	10	174.998	43.16	31.16	12	Fail	Pass
6	172.4-200M	9k	4.5k	10	175	44.17	32.17	12	Fail	Fail
7	200-242.4M	9k	4.5k	10	225	43.15	31.15	12	Fail	Pass
8	310-320M	9k	4.5k	10	319.975	24.06	4.06	12	Fail	Pass
9	429-439M	9k	4.5k	10	433.077	6.83	-18.17	25	Pass	Pass

NOTE:

From Figure 3, the 7th harmonic is 20.8dBuV/m, which still exceeds the 12dBuV/m limitation. Techniques to mitigate these system-level EMI issues are discussed in *EMI Suppression of FPD-Link Device In Automotive Application (II)*.

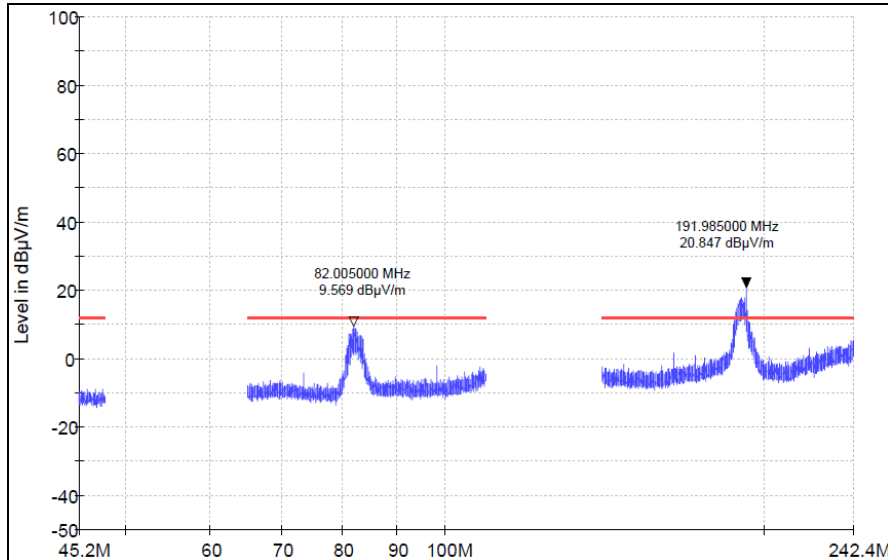


Figure 3. RE Test With SSCG ON

Although different clock is used in SSCG OFF and ON (respectively, 25 MHz and 27.4 MHz with same power), it can still be used to verify the SSCG theory. For example, there is about 14 dB improvement for the 3rd harmonic, 22 dB for the 4th, 34 dB for the 7th, and 31 dB for the 9th.

Looking at Table 2, recalculate SSCG performance for CLK = 25 MHz, achieves $S_{33} = 18.7dB$, $S_{44} = 20dB$, $S_{77} = 23dB$, $S_{99} = 24dB$ (almost the same S_{mn} for 27.4 MHz as measured in this experiment, due to lesser difference between clocks; that is, 25 and 27.4 MHz). The test result shows the improvement is close to the theoretical calculation. Despite the improved variation with different harmonic order, it follows the similar trend as calculated theoretically.

4 Conclusion

This application note addressed the challenge of EMI in automotive domain and mainly focused on component-level EMI suppression. It also discussed SSCG as one of the important solutions and derived useful formulae as a rule of thumb based on the FPD-Link spread spectrum principle. It documents a case study on RE Experiment, which validates the EMI improvement through SSCG. Because the EMI issue is not always a component-level issue, the system-level consideration is equally important. The second application report will continue to discuss how to reduce EMI issues from a system-level point of view.

5 References

1. DS90UH926Q data sheet <http://www.ti.com/product/ds90uh926q-q1>
2. DS90UR906Q data sheet <http://www.ti.com/product/ds90ur906q-q1>
3. CISPR-25 standard <http://de.wikipedia.org/wiki/CISPR>

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