







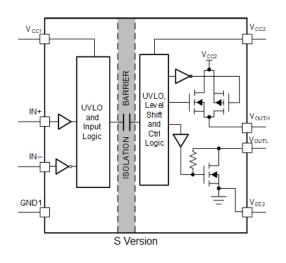
UCC5350-Q1

ZHCSP86E - MAY 2020 - REVISED FEBRUARY 2024

# UCC5350-Q1 适用于 SiC/IGBT 器件和汽车应用的 单通道隔离式栅极驱动器

## 1 特性

- 5kV<sub>RMS</sub>和 3kV<sub>RMS</sub> 单通道隔离式栅极驱动器
- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1
  - HBM ESD 分类等级 H2
  - CDM ESD 分类等级 C6
- 特性选项
  - 分离输出, 8V UVLO (UCC5350SB-Q1)
  - 米勒钳位, 12V UVLO (UCC5350MC-Q1)
- ±5A 最小峰值电流驱动强度
- 3V 至 15V 输入电源电压
- 驱动器电源电压高达 33V
  - 8V 和 12V UVLO 选项
- 100V/ns 最小 CMTI
- 输入引脚具有负 5V 电压处理能力
- 100ns (最大)传播延迟和 <25ns 器件间偏移
- 8 引脚 DWV (8.5mm 爬电) 和 D (4mm 爬电) 封装
- 隔离栅寿命 > 40 年
- 安全相关认证:
  - 符合 UL 1577 标准且长达 1 分钟的 5000V<sub>RMS</sub> DWV 和 3000V<sub>RMS</sub> D 隔离等级
- CMOS 输入
- 工作结温:-40°C 至+150°C



## 2 应用

- 车载充电器
- 适用于 EV 的牵引逆变器
- 直流充电站
- **HVAC**
- 加热器

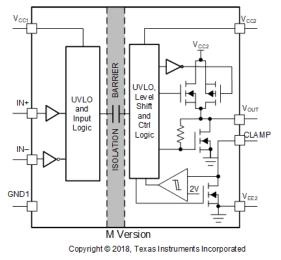
## 3 说明

UCC5350-Q1 是一款单通道隔离式栅极驱动器,具有 5A 最小峰值拉电流和 5A 最小峰值灌电流,专为驱动 MOSFET、IGBT 和 SiC MOSFET 而设计。 UCC5350-Q1 具有米勒钳位或分离输出选项。CLAMP 引脚除了可将晶体管栅极连接到输出端之外,还用于将 栅极连接到内部 FET,以防止米勒电流造成假接通。 借助分离输出选项,可以使用 OUTH 和 OUTL 引脚单 独控制栅极电压的上升和下降时间。

哭仳信自

器件版本	特性	封装 <sup>(1)</sup>	封装尺寸 (标称 值)
UCC5350MC-Q1	米勒钳位 <b>,12</b> V	DWV SOIC-8	7.5mm × 5.85mm
000000000-01	UVLO	D SOIC-8	3.91mm x 4.9mm
UCC5350SB-Q1	分离输出,8V UVLO	D SOIC-8	3.91mm x 4.9mm

(1) 有关所有可选封装,请参阅节14。



功能框图(S和M版本)





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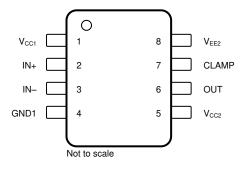
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## 4 说明(续)

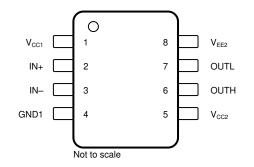
UCC5350-Q1 采用 4mm SOIC-8 (D) 或 8.5mm 宽体 SOIC-8 (DWV) 封装,可分别支持高达 3kV<sub>RMS</sub>和 5kV<sub>RMS</sub>的隔离电压。输入侧通过 SiO2 电容隔离技术与输出侧相隔离,隔离栅使用寿命超过 40 年。UCC5350-Q1 非常适用于在高压牵引逆变器和车载充电器等应用中驱动 IGBT 或 MOSFET。

与光耦隔离器相比,UCC5350-Q1器件的器件间偏移更低,传播延迟更小,工作温度更高,并且CMTI更高。

## **5** Pin Configuration and Function



## 图 5-1. UCC5350MC-Q1 8-Pin SOIC Top View



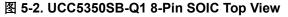


	表	5-1.	Pin	Functions	
_					

	PIN				
	NO.	NO.	TYPE <sup>(1)</sup>	DESCRIPTION	
NAME	UCC5350MC-Q1	UCC5350SB-Q1			
CLAMP	7	_	I	Active Miller-clamp input used to prevent false turn-on of the power switches found on the 'M' version.	
GND1	4	4	G	Input ground. All signals on the input side are referenced to this ground.	
IN+	2	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMO input threshold. This pin is pulled low internally if left open. Use 表 8-4 to understand the input and output logic of these devices.	
IN -	3	3	I	Inverting gate-drive voltage control input. The IN - pin has a CMOS input threshold. This pin is pulled high internally if left open. Use 表 8 to understand the input and output logic of these devices.	
OUT	6	_	0	Gate-drive output found on the 'M' version	
OUTH	_	6	0	Gate-drive pullup output found on the 'S' version	
OUTL	_	7	0	Gate-drive pulldown output found on the 'S' version	
V <sub>CC1</sub>	1	1	Р	Input supply voltage. Connect a locally decoupled capacitor to GND1. Use a low-ESR or ESL capacitor located as close to the device as possible.	
V <sub>CC2</sub>	5	5	Р	Positive output supply rail. Connect a locally decoupled capacitor to $V_{\text{EE2}}.$ Use a low-ESR or ESL capacitor located as close to the device as possible.	
V <sub>EE2</sub>	8	8	G	Ground pin. Connect to MOSFET source or IGBT emitter. Connect a locally decoupled capacitor from $V_{CC2}$ to $V_{EE2}$ . Use a low-ESR or ESL capacitor located as close to the device as possible.	

(1) P = Power, G = Ground, I = Input, O = Output



## **6** Specifications

## 6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input bias pin supply voltage	V <sub>CC1</sub> - GND1	GND1 - 0.3	18	V
Driver bias supply	V <sub>CC2</sub> - V <sub>EE2</sub>	- 0.3	35	V
Output signal voltage	Vouth - Vee2, Voutl - Vee2, Vout - Vee2, Vclamp - Vee2	$V_{EE2} - 0.3$	V <sub>CC2</sub> + 0.3	V
Input signal voltage	V <sub>IN+</sub> - GND1, V <sub>IN-</sub> - GND1	GND1 - 5	V <sub>CC1</sub> + 0.3	V
Junction temperature, T <sub>J</sub> <sup>(2)</sup>	·	- 40	150	°C
Storage temperature, T <sub>stg</sub>		- 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) To maintain the recommended operating conditions for T<sub>J</sub>, see the Thermal Information table.

## 6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per AEC Q100-011	±1500	v

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V <sub>CC1</sub>	Supply voltage, input side	3	15	V
V <sub>CC2</sub>	Positive supply voltage output side (V <sub>CC2</sub> $-$ V <sub>EE2</sub> ), UCC5350MC	13.2	33	V
V <sub>CC2</sub>	Positive supply voltage output side (V <sub>CC2</sub> $-$ V <sub>EE2</sub> ), UCC5350SB	9.5	33	V
TJ	Junction Temperature	-40	150	°C

### 6.4 Thermal Information

		UCC53	50-Q1	
	THERMAL METRIC <sup>(1)</sup>	D	DWV	UNIT
		8 PINS	8 PINS	
R <sub>θ JA</sub>	Junction - to-ambient thermal resistance	109.5	119.8	°C/W
R <sub>0</sub> JC(top)	Junction - to-case (top) thermal resistance	43.1	64.1	°C/W
R <sub>0 JB</sub>	Junction - to-board thermal resistance	51.2	65.4	°C/W
ΨJT	Junction - to-top characterization parameter	18.3	37.6	°C/W
ΨJB	Junction - to-board characterization parameter	50.7	63.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics Application Report.



## 6.5 Power Ratings

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
D Pack	(age (UCC5350MC-Q1)	· · · · ·				
PD	Maximum power dissipation on input and output	V <sub>CC1</sub> = 15 V, V <sub>CC2</sub> = 15 V, f = 2.1-MHz,			1.14	W
P <sub>D1</sub>	Maximum input power dissipation	50% duty cycle, square wave, 2.2-nF load		·	0.05	W
$P_{D2}$	Maximum output power dissipation				1.09	W
D Pack	(age (UCC5350SB-Q1)					
PD	Maximum power dissipation on input and output	V <sub>CC1</sub> = 15 V, V <sub>CC2</sub> = 15 V, f = 1.8-MHz,			0.99	W
P <sub>D1</sub>	Maximum input power dissipation	50% duty cycle, square wave, 2.2-nF load			0.05	W
P <sub>D2</sub>	Maximum output power dissipation				0.94	W
DWV F	Package (UCC5350MC-Q1)	· · · · · ·				
P <sub>D</sub>	Maximum power dissipation on input and output	V <sub>CC1</sub> = 15 V, V <sub>CC2</sub> = 15 V, f = 1.9-MHz,			1.04	W
P <sub>D1</sub>	Maximum input power dissipation	50% duty cycle, square wave, 2.2-nF load			0.05	W
P <sub>D2</sub>	Maximum output power dissipation				0.99	W

## 6.6 Insulation Specifications for D Package

PARAMETER		TEST CONDITIONS	VALUE	
	FARAMETER		D	
CLR	External Clearance <sup>(1)</sup>	Shortest pin - to-pin distance through air	≥ 4	mm
CPG	External Creepage <sup>(1)</sup>	Shortest pin - to-pin distance across the package surface	≥ 4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	μm
СТІ	Comparative tracking index	DIN EN 60112 (VDE 0303 - 11); IEC 60112	> 400	V
	Material Group	According to IEC 60664 - 1	II	
Ou com colt		Rated mains voltage $\leq 150_{VRMS}$	I-IV	
Overvoit	age category per IEC 60664-1	Rated mains voltage $\leq 300_{VRMS}$	1-111	
DIN V VI	DE 0884 - 11: 2017 - 01 <sup>(2)</sup>			
VIORM	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990 <sup>(6)</sup>	V <sub>PK</sub>
VIOWM	Maximum isolation working	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	700 <sup>(6)</sup>	V <sub>RMS</sub>
_	voltage	DC Voltage	990 <sup>(6)</sup>	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}, t = 60 \text{ s (qualification);}$ $V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}, t = 1 \text{ s (100\% production)}$	4242	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50- $\mu$ s waveform, V <sub>TEST</sub> = 1.3 × V <sub>IOSM</sub> (qualification)	4242	V <sub>PK</sub>
		Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10$ s	≤ 5	
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>		≤ 5	рС
		$ \begin{array}{l} \mbox{Method b1: At routine test (100\% production) and} \\ \mbox{preconditioning (type test),} \\ \mbox{V}_{ini} = 1.2 \ x \ \mbox{V}_{IOTM}, t_{ini} = 1 \ s; \\ \mbox{V}_{pd(m)} = 1.5 \ \times \ \mbox{V}_{IORM}, t_m = 1 \ s \end{array} $	≤ 5	

## 6.6 Insulation Specifications for D Package (续)

	PARAMETER	TEST CONDITIONS	VALUE			
	PARAMETER	TEST CONDITIONS	0	)		
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2 π ft), f = 1 MHz	1.	2	pF	
		V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 1	0 <sup>12</sup>		
R <sub>IO</sub>	R <sub>IO</sub> Isolation resistance, input to output <sup>(5)</sup>	$V_{IO}$ = 500 V, 100°C $\leqslant$ T <sub>A</sub> $\leqslant$ 125°C	> 1	0 <sup>11</sup>	Ω	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 1	0 <sup>9</sup>		
	Pollution degree		2	)		
	Climatic category		40/12	25/21		
UL 1577						
V <sub>ISO</sub>	Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}}, t = 60 \text{ s} \text{ (qualification); } V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}, (100\% \text{ production})$	t = 1 s	3000	V <sub>RMS</sub>	

<sup>(1)</sup> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

- (5) All pins on each side of the barrier tied together creating a two-pin device.
- (6) System isolation working voltages need to be verified according to application parameters.



## 6.7 Insulation Specifications for DWV Package

PARAMETER			VALUE	UNIT	
		TEST CONDITIONS	DWV		
CLR	External Clearance <sup>(1)</sup>	Shortest pin - to-pin distance through air	≥ 8.5	mm	
CPG	External Creepage <sup>(1)</sup>	Shortest pin - to-pin distance across the package surface	≥ 8.5	mm	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	μm	
СТІ	Comparative tracking index	DIN EN 60112 (VDE 0303 - 11); IEC 60112	> 600	V	
	Material Group	According to IEC 60664 - 1	I		
Material Group Overvoltage category per IEC 60664-1		Rated mains voltage $\leq 600_{VRMS}$	1-111		
		Rated mains voltage $\leq 1000_{VRMS}$	I-II		
	E 0884 - 11: 2017 - 01 <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>	
V <sub>IOWM</sub>	Maximum isolation working	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1500	V <sub>RMS</sub>	
100010	voltage	DC Voltage	2121	V <sub>DC</sub>	
V <sub>IOTM</sub>	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}$ , t = 60 s (qualification) ; $V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , t = 1 s (100% production)	7000	V <sub>PK</sub>	
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50- $\mu$ s waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> (qualification)	8000	V <sub>PK</sub>	
	Apparent charge <sup>(4)</sup>		≤ 5		
q <sub>pd</sub>		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}, t_{ini} = 60 \text{ s};$ $V_{pd(m)} = 1.6 \times V_{IORM}, t_m = 10 \text{ s}$	≤ 5	рС	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1 \text{ s}$ ; $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1 \text{ s}$	≤ 5		
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2 π ft), f = 1 MHz	1.2	pF	
		V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>		
R <sub>IO</sub>	Isolation resistance, input to output <sup>(5)</sup>	$V_{IO}$ = 500 V, 100°C $\leqslant$ T <sub>A</sub> $\leqslant$ 125°C	> 10 <sup>11</sup>	Ω	
	<b>h</b>	V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>		
	Pollution degree		2		
	Climatic category		40/125/21		
UL 1577					
V <sub>ISO</sub>	Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}}$ , t = 60 s (qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , t = 1 s (100% production)	5000	V <sub>RMS</sub>	

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.



## 6.8 Safety-Related Certifications For D Package

UL		
Recognized under UL 1577 Component Recognition Program		
Single protection, 3000 V <sub>RMS</sub>		
File Number: E181974		

## 6.9 Safety-Related Certifications For DWV Package

UL		
Recognized under UL 1577 Component Recognition Program		
Single protection, 5000 V <sub>RMS</sub>		
File Number: E181974		

### 6.10 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
D PAC	CKAGE (UCC5350MC-Q1)						
I <sub>S</sub> Safety output supply current		R <sub>θ JA</sub> = 109.5°C/W, V <sub>CC2</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see $\boxed{8}$ 6-2	Output side			73	mA
IS		$R_{\theta JA} = 109.5^{\circ}C/W, V_{CC2} = 30 V, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C, see  \boxed{\$} 6-2$	Output side			36	IIIA
			Input side			0.05	
Ps	Safety output supply power	$R_{,0,JA} = 109.5^{\circ}C/W, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C,$ see § 6-4	Output side			1.09	W
			Total			1.14	
Ts	Maximum safety temperature <sup>(1)</sup>					150	°C
D PAC	CKAGE (UCC5350SB-Q1)						
	150°C, 1 <sub>A</sub> = 25°C, see 🚳 6-2		Output side		63		
I <sub>S</sub> S	Safety output supply current	$R_{\theta JA} = 109.5^{\circ}C/W, V_{CC2} = 30 V, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C, see [\frac{1}{3}] 6-2$	Output side			31	mA
		Safety output supply power $R_{0 JA} = 109.5^{\circ}C/W, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C,$ see $\boxed{8}$ 6-4	Input side			0.05	w
Ps	Safety output supply power		Output side			0.94	
			Total			0.99	
Ts	Maximum safety temperature <sup>(1)</sup>					150	°C
DWV	PACKAGE (UCC5350MC-Q1)						
	Safety input, output, or supply	$R_{\theta JA} = 119.8^{\circ}C/W, V_{I} = 15 V, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C, \text{ see } \mathbb{8} \text{ 6-1}$	Output side			66	
I <sub>S</sub>	current	$R_{0 JA} = 119.8^{\circ}C/W, V_{I} = 30 V, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C, \text{ see } \mathbb{8} \text{ 6-1}$	Output side			33	mA
			Input side			0.05	
Ps	Safety input, output, or total power		Output side			0.99	w
	power		Total			1.04	
Ts	Maximum safety temperature <sup>(1)</sup>					150	°C

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R  $_{\theta JA}$ , in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

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 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum allowed junction temperature.

 $P_S = I_S \times V_I$ , where  $V_I$  is the maximum input voltage.

### **6.11 Electrical Characteristics**

 $V_{CC1}$  = 3.3 V or 5 V, 0.1-µF capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1-µF capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_L$  = 100-pF,  $T_J$  = -40°C to +125°C (UCC5350MC-Q1),  $T_J$  = -40°C to +150°C (UCC5350SB-Q1), (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CU	RRENTS	· · · · · · · · · · · · · · · · · · ·				
I <sub>VCC1</sub>	Input supply quiescent current			1.67	2.4	mA
I <sub>VCC2</sub>	Output supply quiescent current			1.1	1.8	mA
SUPPLY VOI	LTAGE UNDERVOLTAGE THRES	SHOLDS				
V <sub>IT+(UVLO1)</sub>	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
V <sub>IT - (UVLO1)</sub>	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
V <sub>hys(UVLO1)</sub>	VCC1 UVLO threshold hysteresis			0.1		V
OUTPUT SU	PPLY VOLTAGE UNDERVOLTAG	GE THRESHOLDS (UCC5350MC-Q1)				
V <sub>IT+(UVLO2)</sub>	VCC2 Positive-going UVLO threshold voltage			12	13	V
V <sub>IT - (UVLO2)</sub>	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
V <sub>hys(UVLO2)</sub>	VCC2 UVLO threshold voltage hysteresis			1		V
OUTPUT SU	PPLY VOLTAGE UNDERVOLTAG	E THRESHOLDS (UCC5350SB-Q1)			I	
V <sub>IT+(UVLO2)</sub>	VCC2 Positive-going UVLO threshold voltage			8.7	9.4	V
V <sub>IT - (UVLO2)</sub>	VCC2 Negative-going UVLO threshold voltage		7.3	8.0		V
V <sub>hys(UVLO2)</sub>	VCC2 UVLO threshold voltage hysteresis			0.7		V
LOGIC I/O						
V <sub>IT+(IN)</sub>	Positive-going input threshold voltage (IN+, IN - )			0.55 × V <sub>CC1</sub>	0.7 × V <sub>CC1</sub>	V
V <sub>IT - (IN)</sub>	Negative-going input threshold voltage (IN+, IN - )		0.3 × V <sub>CC1</sub>	0.45 × V <sub>CC1</sub>		V
V <sub>hys(IN)</sub>	Input hysteresis voltage (IN+, IN - )			0.1 × V <sub>CC1</sub>		V
I <sub>IH</sub>	High-level input leakage at IN+	IN+ = V <sub>CC1</sub>		40	240	μA
		IN - = GND1	- 240	- 40		
IIL	Low-level input leakage at IN -	IN - = GND1 - 5 V	- 310	- 80		μA
GATE DRIVE	R STAGE	· I				
V <sub>OH</sub>	High-level output voltage (VCC2 - OUT) and (VCC2 - OUTH)	I <sub>OUT</sub> = - 20 mA	100	240		mV
V <sub>OL</sub>	Low level output voltage (OUT and OUTL)	IN+ = low, IN - = high; I <sub>OUT</sub> = 20 mA	5	7		mV
	Daals aanmaa an muut	UCC5350MC, IN+ = high, IN - = low	5	10		А
I <sub>OH</sub>	Peak source current	UCC5350SB, IN+ = high, IN - = low	5	8.5		А
I <sub>OL</sub>	Peak sink current	IN+ = low, IN - = high	5	10		А

## 6.11 Electrical Characteristics (续)

 $V_{CC1}$  = 3.3 V or 5 V, 0.1-µF capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1-µF capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_L$  = 100-pF,  $T_J$  = -40°C to +125°C (UCC5350MC-Q1),  $T_J$  = -40°C to +150°C (UCC5350SB-Q1), (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Active Mille	r Clamp (UCC5350MC-Q1 only)	· · · · · · · · · · · · · · · · · · ·				
V <sub>CLAMP</sub>	Low-level clamp voltage	I <sub>CLAMP</sub> = 20 mA		7	10	mV
I <sub>CLAMP</sub>	Clamp low-level current	V <sub>CLAMP</sub> = V <sub>EE2</sub> + 15 V	5	10		А
I <sub>CLAMP(L)</sub>	Clamp low-level current for low output voltage	V <sub>CLAMP</sub> = V <sub>EE2</sub> + 2 V	5	10		А
V <sub>CLAMP-TH</sub>	Clamp threshold voltage			2.1	2.3	V
SHORT CIR	CUIT CLAMPING	L L			I	
V <sub>CLP-OUT</sub>	Clamping voltage (V <sub>OUT</sub> - V <sub>CC2</sub> )	IN+ = high, IN - = low, $t_{CLAMP}$ = 10 µs, $I_{OUT}$ = 500 mA		1	1.3	V
V	Clamping voltage	IN+ = low, IN - = high, $t_{CLAMP}$ = 10 µs, I <sub>OUT</sub> = - 500 mA		1.5		V
V <sub>CLP-OUT</sub> (V <sub>EE2</sub> - V <sub>OUT</sub> )		IN+ = low, IN - = high, I <sub>OUT</sub> = - 20 mA		0.9	1	v
ACTIVE PU	LLDOWN					
V <sub>OUTSD</sub>	Active pulldown voltage on OUT	$I_{OUT} = 0.1 \times I_{OUT(typ)}, V_{CC2} = open$		1.8	2.5	V

## 6.12 Switching Characteristics

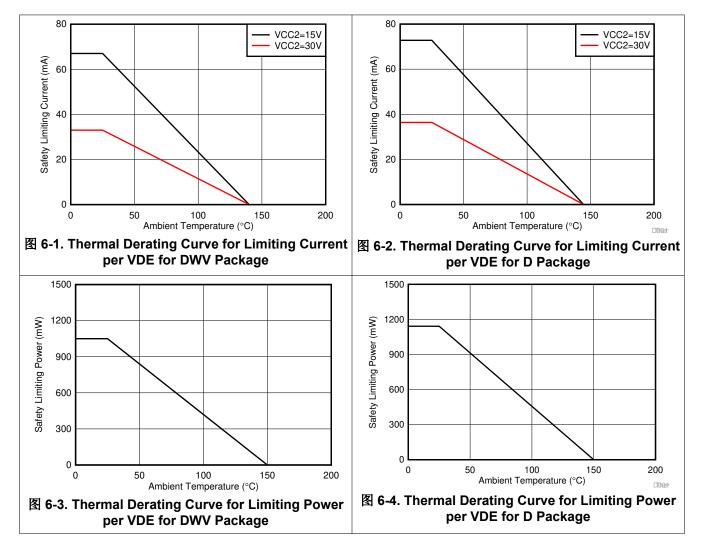
 $V_{CC1}$  = 3.3 V or 5 V, 0.1-µF capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1-µF capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $T_J$  = -40°C to +125°C, (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Output-signal rise time	C <sub>LOAD</sub> = 1 nF		10	26	ns
t <sub>f</sub>	Output-signal fall time	C <sub>LOAD</sub> = 1 nF		10	22	ns
t <sub>PLH</sub>	Propagation delay, high	C <sub>LOAD</sub> = 100 pF		65	100	ns
t <sub>PHL</sub>	Propagation delay, low	C <sub>LOAD</sub> = 100 pF		65	100	ns
t <sub>UVLO1_rec</sub>	UVLO recovery delay of $V_{CC1}$	See 图 8-7.		30		μs
t <sub>UVLO2_rec</sub>	UVLO recovery delay of $V_{\text{CC2}}$	See 图 8-7.		50		μs
t <sub>PWD</sub>	Pulse width distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	C <sub>LOAD</sub> = 100 pF		1	20	ns
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(1)</sup>	C <sub>LOAD</sub> = 100 pF		1	25	ns
t <sub>PWmin1</sub>	No response at OUT where OUT <10% × $V_{CC2}$	C <sub>LOAD</sub> = 100 pF	8			ns
t <sub>PWmin2</sub>	No response at OUT where OUT $\geqslant\!90\%$ × $V_{CC2}$	C <sub>LOAD</sub> = 100 pF			38	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or $V_{CC1}$ , $V_{CM}$ = 1200 V	100	120		kV/µs

(1) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.



#### 6.13 Insulation Characteristics Curves

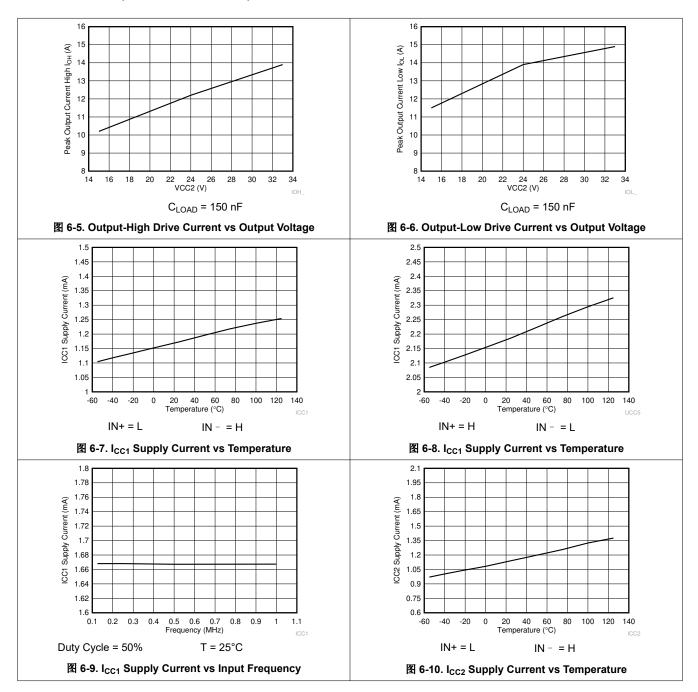






## **6.14 Typical Characteristics**

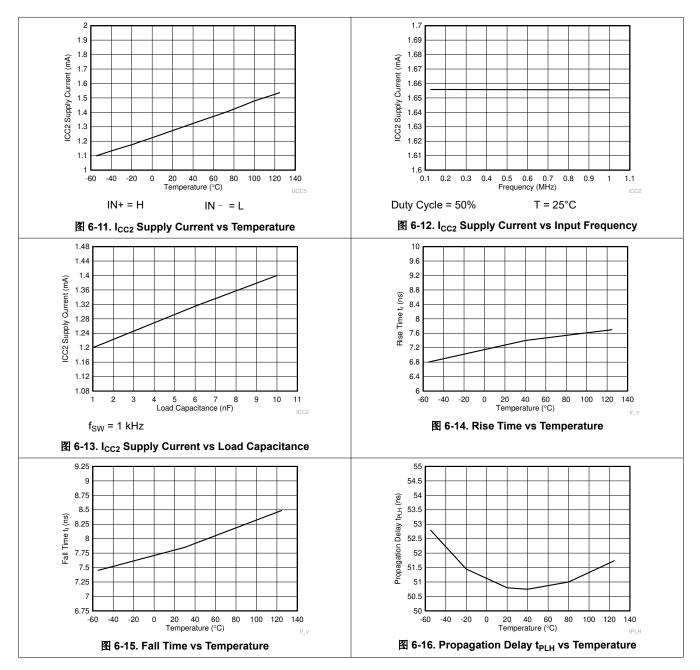
 $V_{CC1}$  = 3.3 V or 5 V, 0.1-µF capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1-µF capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD}$  = 1 nF,  $T_{J}$  = -40°C to +125°C, (unless otherwise noted)





## 6.14 Typical Characteristics (continued)

 $V_{CC1}$  = 3.3 V or 5 V, 0.1-µF capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1-µF capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD}$  = 1 nF,  $T_{J}$  = -40°C to +125°C, (unless otherwise noted)

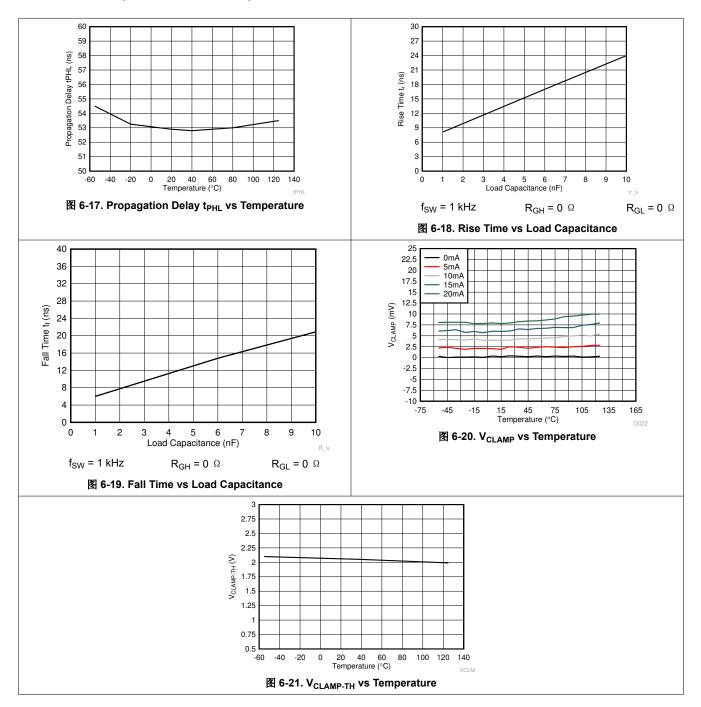






## 6.14 Typical Characteristics (continued)

 $V_{CC1}$  = 3.3 V or 5 V, 0.1- $\mu$ F capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$ = 15 V, 1- $\mu$ F capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD}$  = 1 nF,  $T_{J}$  = -40°C to +125°C, (unless otherwise noted)





## 7 Parameter Measurement Information

## 7.1 Propagation Delay, Inverting, and Noninverting Configuration

 $\mathbb{X}$  7-1 shows the propagation delay for noninverting configurations.  $\mathbb{X}$  7-2 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t<sub>r</sub>) and fall (t<sub>f</sub>) times.

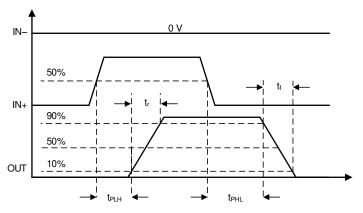


图 7-1. Propagation Delay, Noninverting Configuration

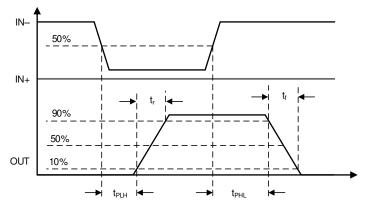


图 7-2. Propagation Delay, Inverting Configuration



## 7.1.1 CMTI Testing

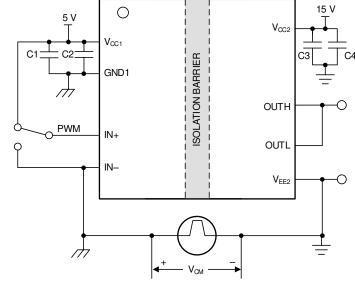
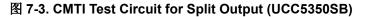
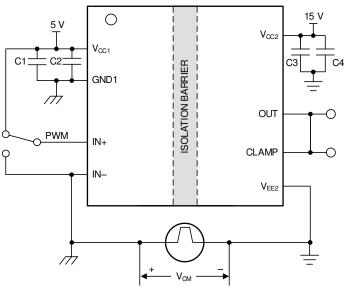


图 7-3 and 图 7-4 are simplified diagrams of the CMTI testing configuration.

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图 7-4. CMTI Test Circuit for Miller Clamp (UCC5350MC)



## 8 Detailed Description

## 8.1 Overview

The UCC5350-Q1 family of isolated gate drivers has two variations: split output, and Miller clamp. The isolation inside the UCC5350-Q1 is implemented with high-voltage SiO<sub>2</sub>-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see 8 8-2). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5350-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 8 8-1, shows a functional block diagram of a typical channel. 8 8-2 shows a conceptual detail of how the OOK scheme works.

8-1 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

## 8.2 Functional Block Diagram

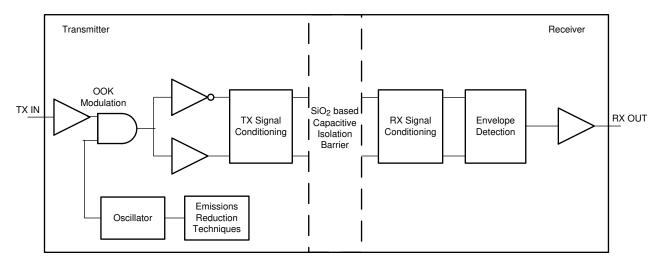


图 8-1. Conceptual Block Diagram of a Capacitive Data Channel

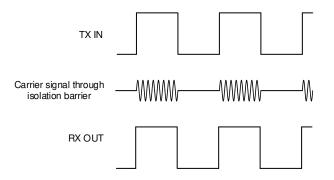
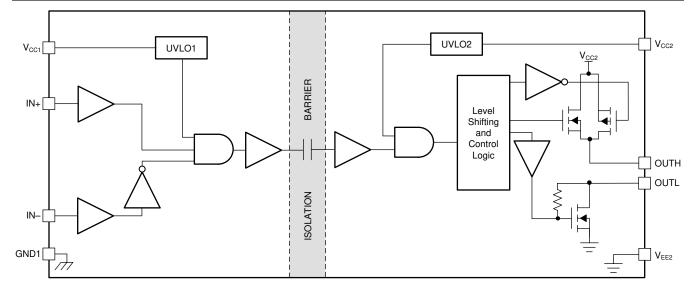
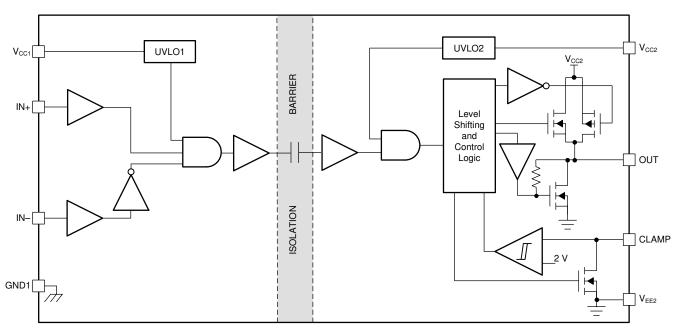


图 8-2. On-Off Keying (OOK) Based Modulation Scheme











## 8.3 Feature Description

## 8.3.1 Power Supply

The V<sub>CC1</sub> input power supply supports a wide voltage range from 3 V to 15 V and the V<sub>CC2</sub> output supply supports a voltage range from 13.2 V to 33 V (UCC5350MC) or 9.5 V to 33 V (UCC5350SB).

For operation with unipolar supply, the V<sub>CC2</sub> supply is connected to 15 V with respect to VEE2 for IGBTs, and 20 V for SiC MOSFETs. The V<sub>EE2</sub> supply is connected to 0 V. In this use case, the Miller clamp helps to prevent a false turn-on of the power switch without a negative voltage rail. The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the V<sub>EE2</sub> supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate.

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### 8.3.2 Input Stage

The input pins (IN+ and IN – ) of the UCC5350-Q1 are based on CMOS-compatible input-threshold logic that is completely isolated from the V<sub>CC2</sub> supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC5350-Q1 has a typical high threshold (V<sub>IT+(IN)</sub>) of  $0.55 \times V_{CC1}$  and a typical low threshold of  $0.45 \times V_{CC1}$ . A wide hysteresis (V<sub>hys(IN)</sub>) of  $0.1 \times V_{CC1}$  makes for good noise immunity and stable operation. If either of the inputs are left open, 128 k $\Omega$  of internal pull-down resistance forces the IN+ pin low and 128 k $\Omega$  of internal resistance pulls IN – high. However, TI still recommends grounding an input or tying to VCC1 if it is not being used for improved noise immunity.

Because the input side of the UCC5350-Q1 is isolated from the output driver, the input signal amplitude can be larger or smaller than  $V_{CC2}$  provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient  $V_{CC2}$  for any gate. However, the amplitude of any signal applied to IN+ or IN - must never be at a voltage higher than  $V_{CC1}$ .

### 8.3.3 Output Stage

The output stage of the UCC5350-Q1 features a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.  $\frac{1}{5}$  8-1 lists the typical internal resistance values of the pull-up and pull-down structure.

DEVICE OPTION	R <sub>NMOS</sub>	R <sub>OH</sub>	R <sub>OL</sub>	R <sub>CLAMP</sub>	UNIT
UCC5350MC-Q1	1.54	12	0.26	0.26	Ω
UCC5350SB-Q1	1.54	12	0.26	Not applicable	Ω

#### 表 8-1. UCC5350-Q1 On-Resistance

The R<sub>OH</sub> parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pull-up N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC5350-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the R<sub>OH</sub> parameter, which yields a faster turn-on. The turn-on-phase output resistance is the parallel combination  $R_{OH} \parallel R_{NMOS}$ .

The pull-down structure in the UCC5350-Q1 is simply composed of an N-channel MOSFET. The output of the UCC5350-Q1 is capable of delivering, or sinking, 5-A peak current pulses. The output voltage swing between  $V_{CC2}$  and  $V_{EE2}$  provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

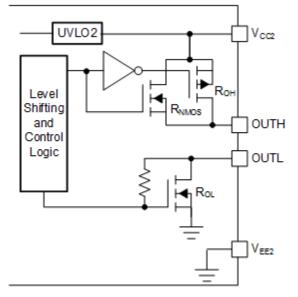


图 8-5. Output Stage—S Version

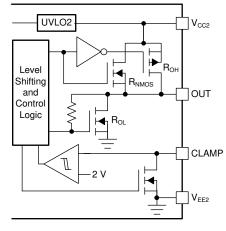


图 8-6. Output Stage—M Version

## 8.3.4 Protection Features

## 8.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V<sub>CC1</sub> and V<sub>CC2</sub> supplies between the V<sub>CC1</sub> and GND1, and V<sub>CC2</sub> and V<sub>EE2</sub> pins to prevent an underdriven condition on IGBTs and MOSFETs. When V<sub>CC</sub> is lower than V<sub>IT+ (UVLO)</sub> at device start-up or lower than V<sub>IT- (UVLO)</sub> after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN - ) as shown in  $\frac{1}{8}$  8-2. The V<sub>CC</sub> UVLO protection has a hysteresis feature (V<sub>hys(UVLO)</sub>). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. 8 8-7 shows the UVLO functions.



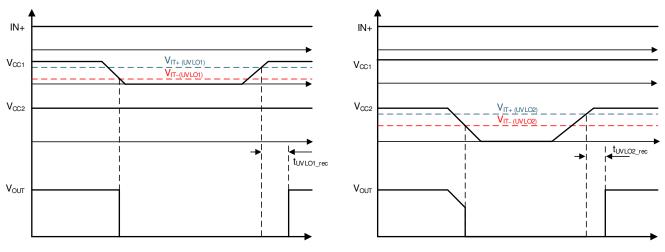
CONDITION	INP	INPUTS	
CONDITION	IN+	IN -	OUT
	Н	L	L
V <sub>CC1</sub> - GND1 < V <sub>IT+(UVLO1)</sub> during device start-up	L	н	L
	Н	н	L
	L	L	L
	Н	L	L
$V_{\rm eff} = CND1 < V_{\rm eff}$ ofter device start up	L	н	L
$V_{CC1}$ - GND1 < $V_{IT - (UVLO1)}$ after device start-up	Н	н	L
	L	L	L

## 表 8-2. UCC5350-Q1 V<sub>CC1</sub> UVLO Logic

CONDITION	INF	INPUTS		
CONDITION	IN+	IN -	OUT	
	н	L	L	
	L	Н	L	
$V_{CC2}$ - $V_{EE2} < V_{IT+(UVLO2)}$ during device start-up	Н	н	L	
	L	L	L	
	н	L	L	
	L	н	L	
$V_{CC2} - V_{EE2} < V_{IT - (UVLO2)}$ after device start-up	Н	Н	L	
	L	L	L	

## 表 8-3. UCC5350-Q1 V<sub>CC2</sub> UVLO Logic

When  $V_{CC1}$  or  $V_{CC2}$  drops below the UVLO1 or UVLO2 threshold, a delay,  $t_{UVLO1\_rec}$  or  $t_{UVLO2\_rec}$ , occurs on the output when the supply voltage rises above  $V_{IT+(UVLO)}$  or  $V_{IT+(UVLO2)}$  again.  $\boxtimes$  8-7 shows this delay.



### 图 8-7. UVLO Functions

## 8.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the  $V_{CC2}$  supply. This feature prevents false IGBT and MOSFET turn-on on the OUT and CLAMP pins by clamping the output to approximately 2 V.



When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pull-up resistor while the lower NMOS gate is tied to the driver output through a 500-k $\Omega$  resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

#### 8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the  $V_{CC2}$  voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the  $V_{CC2}$  pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

#### 8.3.4.4 Active Miller Clamp

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground ( $V_{EE2}$ ) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state.  $\boxed{8}$  9-2 shows a typical application circuit of this function.

#### 8.4 Device Functional Modes

 $\frac{1}{8}$  8-5 lists the functional modes for the UCC5350-Q1 assuming V<sub>CC1</sub> and V<sub>CC2</sub> are in the recommended range.

IN+	IN -	OUTH	OUTL		
Low	Х	Hi-Z	Low		
Х	High	Hi-Z	Low		
High	Low	High	High-Z		

#### 表 8-4. Function Table for UCC5350SB-Q1

表 8-5. Function Table for UCC5350MC-Q1					
IN+	IN -	OUT			
Low	Х	Low			
Х	High	Low			
High	Low	High			

#### 8.4.1 ESD Structure

8-9 shows the multiple diodes involved in the ESD protection components of the UCC5350-Q1 device. This provides pictorial representation of the absolute maximum rating for the device.



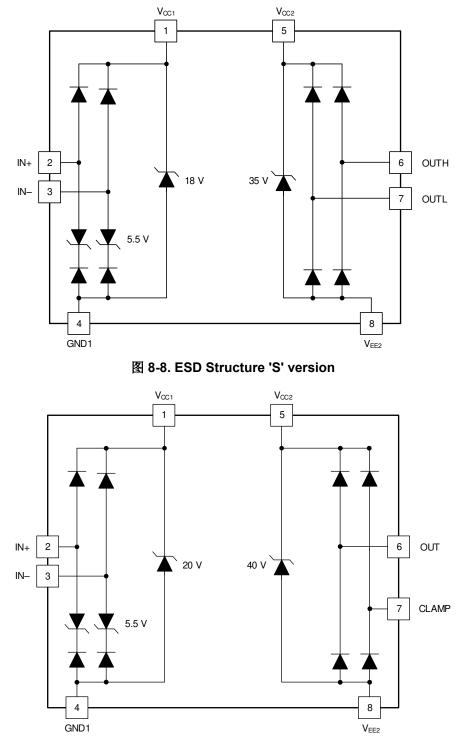


图 8-9. ESD Structure ' M' Version



## 9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围, TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计,以确保系统功能。

## **9.1 Application Information**

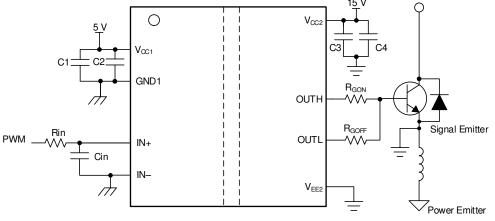
The UCC5350-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

The UCC5350-Q1 has two pinout configurations, featuring split outputs and Miller clamp. The split outputs, OUTH and OUTL, are used to separately decouple the power transistor turn on and turn off commutations.

The M version features active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The device comes in an 8-pin D and 8-pin DWV package and has creepage, or clearance, of 4 mm and 8.5 mm, respectively, which is suitable for applications where basic or reinforced isolation is required. The UCC5350-Q1 offers a 5-A minimum drive current.

### 9.2 Typical Application

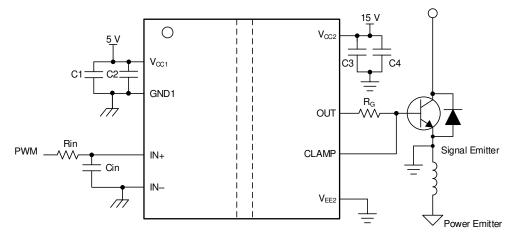
The circuits in [8] 9-1 and [8] 9-2 show a typical application for driving IGBTs.



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#### 图 9-1. Typical Application Circuit for UCC5350SB-Q1 to Drive IGBT





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### 图 9-2. Typical Application Circuit for UCC5350MC-Q1 to Drive IGBT

#### 9.2.1 Design Requirements

PARAMETER	VALUE	UNIT
V <sub>CC1</sub>	3.3	V
V <sub>CC2</sub> - V <sub>EE2</sub>	18	V
IN+	3.3	V
IN -	GND1	-
Switching frequency	150	kHz
Gate Charge of Power Device	126	nC

表 9-1. UCC5350-Q1 Design Requirements

#### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Designing IN+ and IN – Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter,  $R_{IN}$ - $C_{IN}$ , can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R<sub>IN</sub> resistor with a value from 0  $\Omega$  to 100  $\Omega$  and a C<sub>IN</sub> capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for R<sub>IN</sub> is 51  $\Omega$  and C<sub>IN</sub> is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

#### 9.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors,  $R_{G(ON)}$  and  $R_{G(OFF)}$  are used to:

- 1. Limit ringing caused by parasitic inductances and capacitances
- 2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
- 3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
- 4. Reduce electromagnetic interference (EMI)

The output stage has a pull-up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined typical peak source current is 10 A for UCC5350-Q1. Use 5 Rt 1 to estimate the peak source current.



(1)

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} | R_{OH} + R_{GON} + R_{GFET\_Int}}$$

where

- $R_{ON}$  is the external turn-on resistance, which is 2.2  $\Omega$  in this example.
- R<sub>GFET\_Int</sub> is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 1.8 Ω for our example.
- I<sub>OH</sub> is the typical peak source current which is the minimum value between 10 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak source current is approximately 3.36 A as calculated in 方程式 2.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} ||R_{OH} + R_{GON} + R_{GFET\_Int}} = \frac{18 V}{1.54\Omega ||12\Omega + 2.2\Omega + 1.8\Omega} \approx 3.36A$$
(2)

Similarly, use 方程式 3 to calculate the peak sink current.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}}$$
(3)

where

- $R_{OFF}$  is the external turn-off resistance, which is 2.2  $\Omega$  in this example.
- I<sub>OL</sub> is the typical peak sink current which is the minimum value between 10 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum value between 方程式 4 and 10 A.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} = \frac{18V}{0.26\Omega + 2.2\Omega + 1.8\Omega} \approx 4.23A$$
(4)

备注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

#### 9.2.2.3 Estimate Gate-Driver Power Loss

The total loss,  $P_{G}$ , in the gate-driver subsystem includes the power losses ( $P_{GD}$ ) of the UCC5350-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The  $P_{GD}$  value is the key power loss which determines the thermal safety-related limits of the UCC5350-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P<sub>GDQ</sub>, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The P<sub>GDQ</sub> parameter is measured on the bench with no load connected to the OUT pins at a given V<sub>CC1</sub>, V<sub>CC2</sub>, switching frequency, and ambient temperature. In this example, V<sub>CC1</sub> is 3.3V and V<sub>CC2</sub> is 18 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 150 kHz, is measured to be I<sub>CC1</sub> = 1.67 mA and I<sub>CC2</sub> = 1.11 mA . Therefore, use 方程式 5 to calculate P<sub>GDQ</sub>.

$$P_{GDQ} = V_{CC1} \times I_{VCC1} + (V_{CC2} - V_{FE2}) \times I_{CC2} \approx 23.31 \text{mW}$$

(5)



(6)

The second component is the switching operation loss,  $P_{GDO}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 5  $\pm$  6 to calculate the total dynamic loss from load switching,  $P_{GSW}$ .

$$P_{GSW} = (V_{CC2} - V_{EE2}) \times Q_G \times f_{SW}$$

where

Q<sub>G</sub> is the gate charge of the power transistor at V<sub>CC2</sub>.

So, for this example application the total dynamic loss from load switching is approximately 340 mW as calculated in 5程式 7.

$$P_{GSW} = 18 \text{ V} \times 126 \text{ nC} \times 150 \text{ kHz} = 340 \text{ mW}$$
 (7)

 $Q_G$  represents the total gate charge of the power transistor and is subject to change with different testing conditions. The UCC5350-Q1 gate-driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  is equal to  $P_{GSW}$  if the external gate-driver resistance and power-transistor internal resistance are 0  $\Omega$ , and all the gate driver-loss will be dissipated inside the UCC5350-Q1. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 10 A, however, it will be non-linear if the source/sink current is saturated. The gate driver loss will be estimated in the case in which it is not saturated as given in  $au \neq 1$ .

$$P_{GDO} = \frac{P_{GSW}}{2} \left( \frac{R_{OH} || R_{NMOS}}{R_{OH} || R_{NMOS} + R_{GON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} \right)$$
(8)

In this design example, all the predicted source and sink currents are less than 10 A, therefore, use 方程式 9 to estimate the gate-driver loss.

$$P_{\text{GDO}} = \frac{340 \text{ mW}}{2} \left( \frac{12 \Omega \| 1.54 \Omega}{12 \Omega \| 1.54 \Omega + 2.2 \Omega + 1.8 \Omega} + \frac{0.26 \Omega}{0.26 \Omega + 2.2 \Omega + 1.8 \Omega} \right) \approx 53.66 \text{ mW}$$
(9)

where

V<sub>OUTH/L(t)</sub> is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (10 A at turnon and turnoff) charging or discharging a load capacitor. Then, the V<sub>OUTH/L(t)</sub> waveform will be linear and the T<sub>R\_Sys</sub> and T<sub>F Sys</sub> can be easily predicted.

Use 方程式 10 to calculate the total gate-driver loss dissipated in the UCC5350-Q1 gate driver, PGD.

$$P_{GD} = P_{GDQ} + P_{GDO} = 25.31 \text{mW} + 53.66 \text{mW} = 78.97 \text{mW}$$
(10)

### 9.2.2.4 Estimating Junction Temperature

Use the equation below to estimate the junction temperature  $(T_J)$  of the UCC5350-Q1 family.

$$T_{J} = T_{C} + \Psi_{JT} \times P_{GD}$$
<sup>(11)</sup>

where

- T<sub>C</sub> is the UCC5350-Q1 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$  is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance (R<sub>θ JC</sub>) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The R<sub>θ JC</sub> resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of R<sub>θ JC</sub> will inaccurately estimate the true junction temperature. The  $\Psi_{JT}$  parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

## 9.2.3 Selecting $V_{CC1}$ and $V_{CC2}$ Capacitors

Bypass capacitors for the  $V_{CC1}$  and  $V_{CC2}$  supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

#### 备注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-  $\mu$  F X7R capacitor is measured to be only 500 nF when a DC bias of 15-V<sub>DC</sub> is applied.

### 9.2.3.1 Selecting a V<sub>CC1</sub> Capacitor

A bypass capacitor connected to the V<sub>CC1</sub> pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V<sub>CC1</sub> pin, a tantalum or electrolytic capacitor with a value greater than 1  $\mu$  F should be placed in parallel with the MLCC.

### 9.2.3.2 Selecting a V<sub>CC2</sub> Capacitor

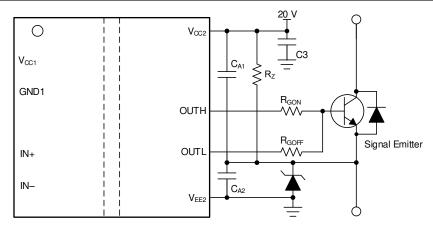
A 50-V, 10-  $\mu$  F MLCC and a 50-V, 0.22-  $\mu$  F MLCC are selected for the C<sub>VCC2</sub> capacitor. If the bias power supply output is located a relatively long distance from the V<sub>CC2</sub> pin, a tantalum or electrolytic capacitor with a value greater than 10  $\mu$  F should be used in parallel with C<sub>VCC2</sub>.

#### 9.2.3.3 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turn-on and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

[ 9-3 shows the first example with negative bias turn-off on the output using a Zener diode on the isolated power-supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply is equal to 20 V, the turn-off voltage is − 5.1 V and the turn-on voltage is 20 V − 5.1 V ≈ 15 V.





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#### 图 9-3. Negative Bias With Zener Diode on Iso-Bias Power-Supply Output

Solution requires more flexibility when setting the positive and negative rail voltages.

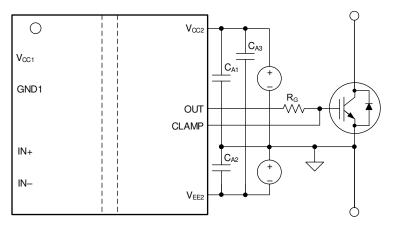


图 9-4. Negative Bias With Two Iso-Bias Power Supplies



### 9.2.4 Application Curve

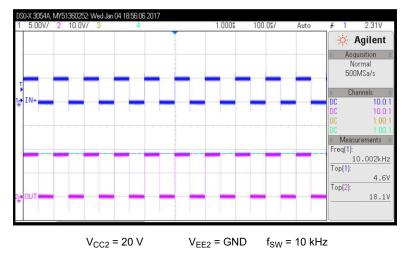


图 9-5. PWM Input and Gate Voltage Waveform

## **10 Power Supply Recommendations**

The recommended input supply voltage (V<sub>CC1</sub>) for the UCC5350-Q1 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage (V<sub>CC2</sub>) is determined by the internal UVLO protection feature of the device. The V<sub>CC1</sub> and V<sub>CC2</sub> voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50  $\mu$ s by the UVLO protection feature. For more information on UVLO, see  $\ddagger$  8.3.4.1. The higher limit of the V<sub>CC2</sub> range depends on the maximum gate voltage of the power device that is driven by the UCC5350-Q1 device, and should not exceed the recommended maximum V<sub>CC2</sub> of 33 V. A local bypass capacitor should be placed between the V<sub>CC2</sub> and V<sub>EE2</sub> pins, with a value of 220-nF to 10-  $\mu$  F for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the V<sub>CC1</sub> and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC5350-Q1 device, this bypass capacitor has a minimum recommended value of 100 nF.

## 11 Layout

## **11.1 Layout Guidelines**

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC5350-Q1. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the V<sub>CC1</sub> and GND1
    pins and between the V<sub>CC2</sub> and V<sub>EE2</sub> pins to bypass noise and to support high peak currents when turning
    on the external power transistor.
  - To avoid large negative transients on the V<sub>EE2</sub> pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:

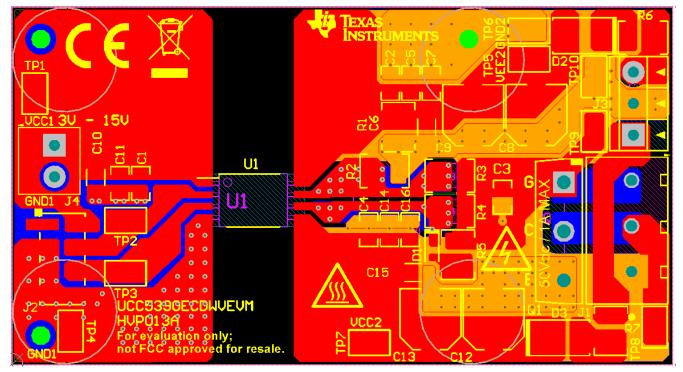


- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:

  - Increasing the PCB copper connecting to the V<sub>CC2</sub> and V<sub>EE2</sub> pins is recommended, with priority on
    maximizing the connection to V<sub>EE2</sub>. However, the previously mentioned high-voltage PCB considerations
    must be maintained.
  - If the system has multiple layers, TI also recommends connecting the V<sub>CC2</sub> and V<sub>EE2</sub> pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

### 11.2 Layout Example

I1-1 shows a PCB layout example with the signals and key components labeled. The UCC5390ECDWV evaluation module (EVM) is given as an example, available in the same DWV package as the UCC5350-Q1. The UCC5390EC has a split emitter versus Miller clamp so although the layout is not exactly the same, general guidelines and practices still apply. The evaluation board can be configured for the Miller clamp version, as well, as described in the UCC5390ECDWV Isolated Gate Driver Evaluation Module User's Guide.



A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

### 图 11-1. Layout Example

图 11-2 and 图 11-3 show the top and bottom layer traces and copper.



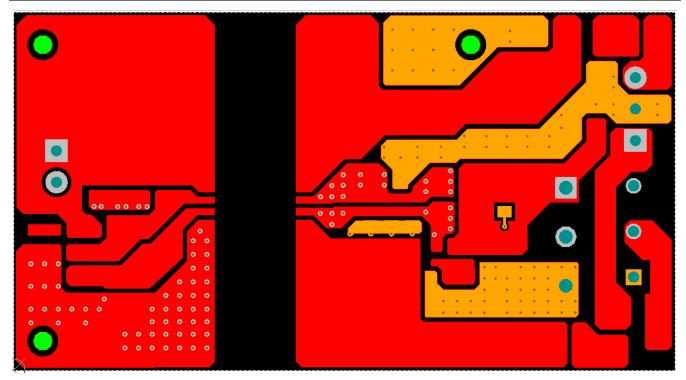


图 11-2. Top-Layer Traces and Copper

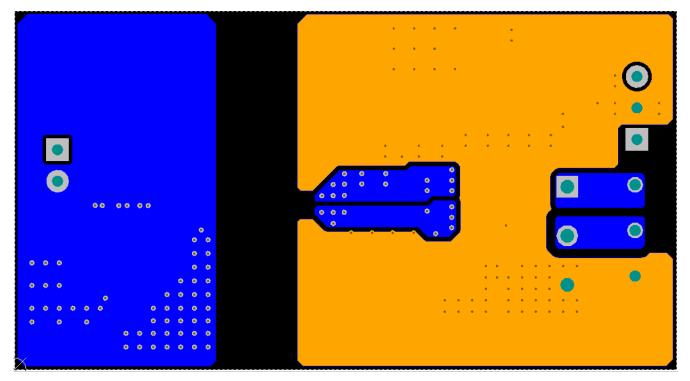
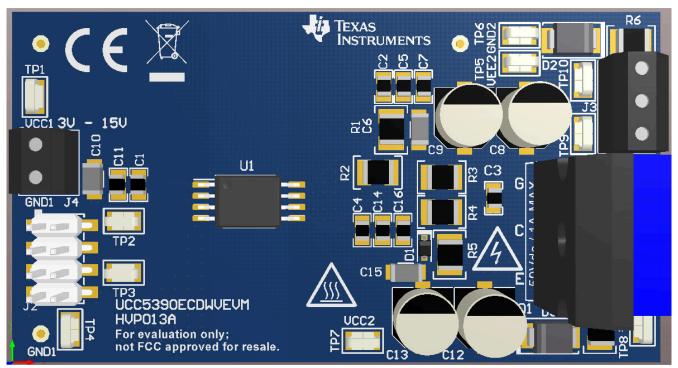


图 11-3. Bottom-Layer Traces and Copper (Flipped)

图 11-4 shows the 3D layout of the top view of the PCB.

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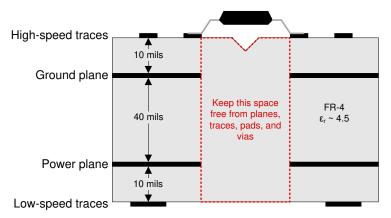


## 图 11-4. 3-D PCB View

## 11.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

图 11-5 shows the recommended layer stack.



## 图 11-5. Recommended Layer Stack



## 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 第三方产品免责声明

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### **12.2 Documentation Support**

#### 12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Digital Isolator Design Guide
- Texas Instruments, Isolation Glossary
- Texas Instruments, SN6501 Transformer Driver for Isolated Power Supplies data sheet
- Texas Instruments, SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet
- Texas Instruments, UCC5390ECDWV Isolated Gate Driver Evaluation Module user's guide
- Texas Instruments, UCC53x0xD Evaluation Module user's guide

#### 12.3 Certifications

UL Online Certifications Directory, "FPPT2.E181974 Nonoptical Isolating Devices - Component" Certificate Number: 20170718-E181974,

#### 12.4 接收文档更新通知

要接收文档更新通知,请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

### 12.5 支持资源

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### 12.6 Trademarks

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### 12.7 静电放电警告



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ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.8 术语表

TI术语表 本术语表列出并解释了术语、首字母缩略词和定义。



## **13 Revision History**

注:以前版本的页码可能与当前版本的页码不同

Changes from Revision D (August 2022) to Revision E (February 2024)		Page
•	Changed CTI and Material Group values in insulation specifications and added table note	6

Changes from Revision C (June 2022) to Revision D (August 2022)		
•	将 UCC5350SB-Q1 从 "预告信息" 更改为 "量产数据"	1

Changes from Revision B (June 2020) to Revision C (June 2022)		Page
•	添加了 UCC5350SBQDRQ1 器件的预告信息	1
•	已添加 节 4	3
	Added the UCC5350SB device to $rac{17}{5}$	
	Added SB-Q1 D package power ratings	
	Added SB-Q1 insulation specs	
	Added the UL certificate number for the D package	
•	Added the UL certificate number for the DWV package	9
•	Added SB-Q1 D package safety limiting values	9
•	Added SB-Q1 parameters	
	Added minimum pulse width specs	
	Added 表 8-4	
•	Added SB-Q1 ESD figure	23
	Added typical application circuit for SB-Q1	

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead finish/	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	Ball material	(3)		(4/5)	
PUCC5350MCQDWVQ1	OBSOLETE	SOIC	DWV	8		TBD	(6) Call TI	Call TI			
UCC5350MCQDQ1	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350Q	
UCC5350MCQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350Q	Complex.
											Samples
UCC5350MCQDWVQ1	LIFEBUY	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ	
UCC5350MCQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ	Samples
UCC5350SBQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI   NIPDAU	Level-3-260C-168 HR	-40 to 125	5350Q	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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### PACKAGE OPTION ADDENDUM

12-Apr-2024

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF UCC5350-Q1 :

• Catalog : UCC5350

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product



Texas

\*All dimensions are nominal

STRUMENTS

#### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5350MCQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5350MCQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5350MCQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5350SBQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



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## PACKAGE MATERIALS INFORMATION

1-Mar-2024



\*All dimensions are nominal

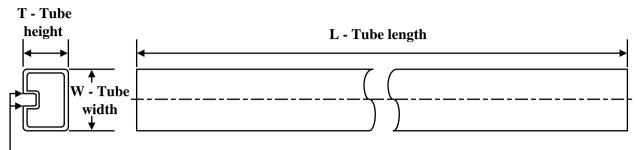
Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5350MCQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
UCC5350MCQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
UCC5350MCQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5350SBQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

### TEXAS INSTRUMENTS

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### TUBE



### - B - Alignment groove width

#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
UCC5350MCQDQ1	D	SOIC	8	75	505.46	6.76	3810	4
UCC5350MCQDQ1	D	SOIC	8	75	506.6	8	3940	4.32
UCC5350MCQDWVQ1	DWV	SOIC	8	64	505.46	13.94	4826	6.6

# DWV0008A



### SOIC - 2.8 mm max height

SOIC



- NOTES:
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- Per ASME Y14.5M.
   This drawing is subject to change without notice.
   This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

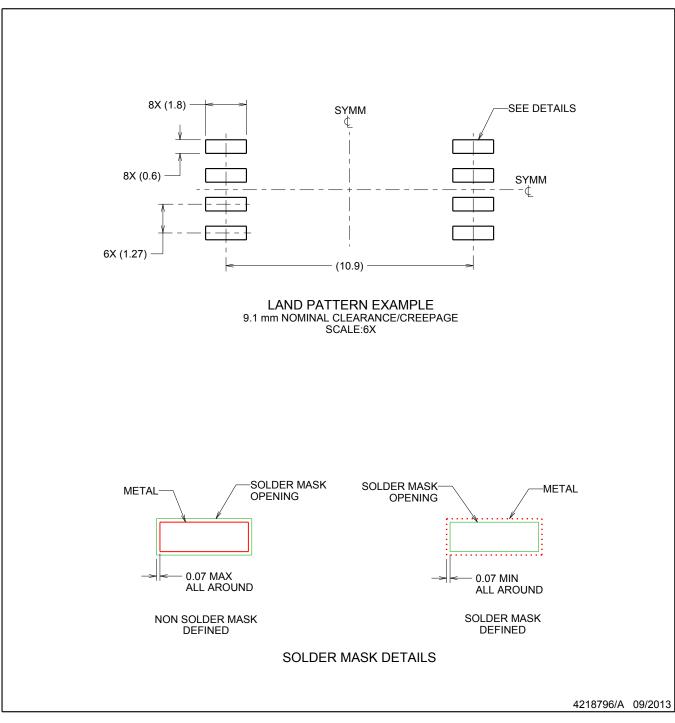


## DWV0008A

# EXAMPLE BOARD LAYOUT

### SOIC - 2.8 mm max height

SOIC



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

# DWV0008A

### SOIC - 2.8 mm max height

SOIC



NOTES: (continued)



<sup>7.</sup> Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

<sup>8.</sup> Board assembly site may have different recommendations for stencil design.

# D0008A



## **PACKAGE OUTLINE**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



# D0008A

# **EXAMPLE BOARD LAYOUT**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## D0008A

# **EXAMPLE STENCIL DESIGN**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



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