UCC28063A 具有改进的可闻噪声和输入浪涌噪声抑制性能的 Natural Interleaving™ 转换模式 PFC 控制器

1 特性

- 输入滤波器和输出电容纹波电流消除
  - 减少了电流纹波，可提高系统可靠性并降低电容容量需求
  - 减小了电磁干扰 (EMI) 滤波器的尺寸
- 相位管理能力
- 双路故障安全过压保护 (OVP)，可防止出现电压感测故障所导致的输出过压情况
- 采用无传感器电流整形技术，可简化电路板布局并提高效率
- 高级可闻噪声性能
- 非线性误差放大器增益
- 过压软恢复
- 集成欠压和压降处理
- 降低了偏置电流
- 相比传统的单相连续导通模式 (CCM)，提升了效率和设计灵活性
- 浪涌安全电流限制：
  - 在浪涌期间防止金属氧化物半导体场效应晶体管 (MOSFET) 导通
  - 消除输出整流器中的反向恢复事件
- 无需大量的缓冲器电路，使用低成本二极管即可
- 提高了轻负载时的效率
- 快速且平滑的瞬态响应
- 扩展了系统级保护功能
- 1A 拉电流/1.8A 灌电流栅极驱动器
- 工作温度范围为 -40°C 至 125°C，采用 16 引脚小外形尺寸集成电路 (SOIC) 封装

2 应用

- 100W 至 800W 电源
- 游戏机
- 数模转换机顶盒
- 适配器
- 液晶电视、等离子电视以及 DLP™ 电视
- 家用音频系统

3 说明

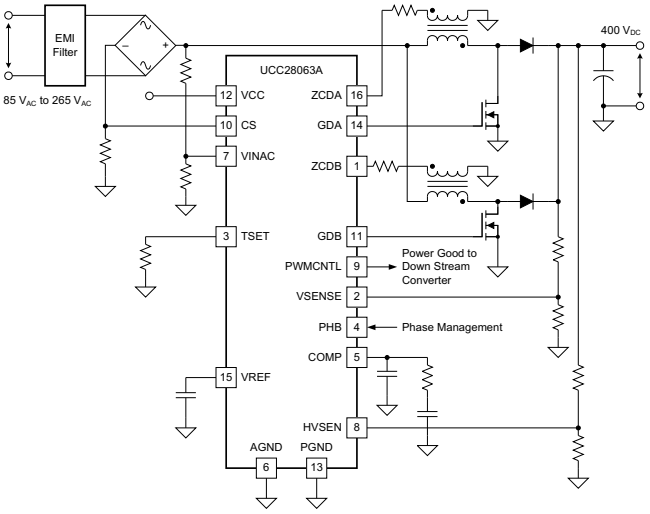
该器件的特性与 UCC28063 几乎相同，只不过删除了 TSET 引脚开路/短路故障检测和 CS 引脚开路故障检测特性。 在某些应用中，当交流电源上出现快速瞬变、浪涌或脉冲噪声时，会有大量电压噪声耦合到 TSET 或 CS 引脚上。而删除上述两个故障检测特性可提升噪声抑制性能，从而为这类应用提供更强的“承受能力”。

器件信息(1)

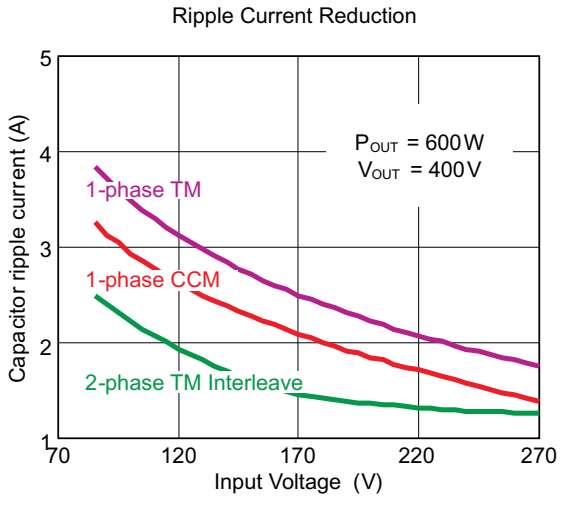
器件型号	封装	封装尺寸（标称值）
UCC28063A	SOIC (16)	9.90mm x 3.91mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



通过 **Natural Interleaving** 技术降低输入纹波电流



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4 修订历史记录

Changes from Revision A (February 2015) to Revision B **Page**

- 已从产品预览更改为量产数据 ... 1

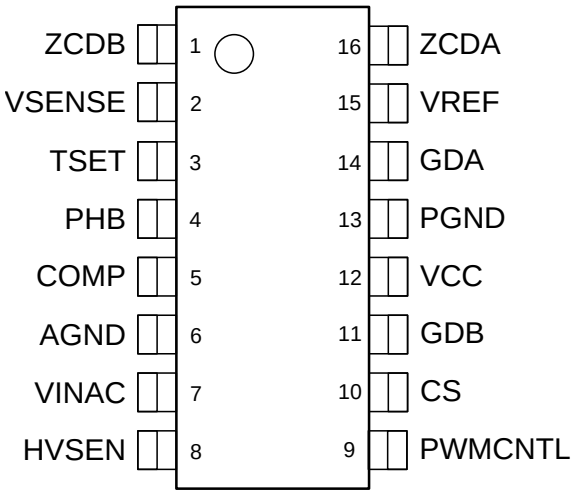
5 说明（继续）

这套解决方案针对消费类应用在可闻噪声抑制方面的需求进行了优化，不仅保留了转换模式的高效率与低元件成本两大优势，还提高了额定功率。 利用 Natural Interleaving ™ 技术，可使两个通道均作为主通道运行（即，没有从通道），而且这两个通道同步至同一频率。 此方案本身可提供高匹配度的快速响应、并确保每个通道都运行在转换模式下。

该器件具有扩展系统级保护，其中包括输入欠压和压降恢复、输出过压、开环、过载、软启动、相位故障检测以及热关断保护。 附加故障安全过压保护 (OVP) 特性可防止发生中间电压短路，如果未成功检测到此类短路，则可能会导致灾难性的器件故障。 该器件具有高级非线性增益，可针对线路和负载瞬态事件提供快速而更为平滑的响应。并且偏置电流较小，提高了待机功率效率。 该器件还具备特殊的线路压降处理特性，可防止出现明显的电流中断并以最大限度抑制可闻噪声的产生。

6 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	-	Analog Ground
COMP	5	O	Error Amplifier Output
CS	10	I	Current Sense Input
GDA	14	O	Channel A and Channel B Gate Drive Output
GDB	11	O	
HVSEN	8	I	High Voltage Output Sense
PHB	4	I	Phase-B Enable/Disable
PWMCNTL	9	O	PWM-Control Output
TSET	3	I	Timing Set
VCC	12	-	Bias Supply Input
VINAC	7	I	Input AC Voltage Sense
VREF	15	O	Voltage Reference Output
VSENSE	2	I	Output DC Voltage Sense
ZCDA	16	I	Zero Current Detection Inputs
ZCDB	1	I	

7 Specifications

7.1 Absolute Maximum Ratings(1)

All voltages are with respect to GND, −40 °C < T_J = T_A < 125 °C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

			MIN	MAX	UNIT
	Continuous input voltage range	VCC(2)	−0.5	21	V
		PWMCNTL	−0.5	20	
		COMP(3), PHB, HVSEN(4), VINAC(4), VSENSE(4)	–0.5	7	
		ZCDA, ZCDB	–0.5	4	
		CS(5)	–0.5	3	
	Continuous input current	VCC		20	mA
		PWMCNTL		10	
		ZCDA, ZCDB		±5	
	Peak input current	CS		–30	
	Output current	VREF		–10	
	Continuous gate current	GDA, GDB(6)		±25	
T_J	Junction Temperature	Operating	–40	125	°C
		Storage	–65	150	
T_{SOL}	Lead Temperature	Soldering, 10s		260	
T_{stg}	Storage temperature		–40	125	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.
(2) Voltage on VCC is internally clamped. VCC may exceed the continuous absolute maximum input voltage rating if the source is current limited below the absolute maximum continuous VCC input current level.
(3) In normal use, COMP is connected to capacitors and resistors and is internally limited in voltage swing.
(4) In normal use, VINAC, VSENSE, and HVSEN are connected to high-value resistors and are internally limited in negative-voltage swing. Although not recommended for extended use, VINAC, VSENSE, and HVSEN can survive input currents as high as -10mA from negative voltage sources, and input currents as high as +0.5mA from positive voltage sources.
(5) In normal use, CS is connected to a series resistor to limit peak input current during brief system line-inrush conditions. In these situations, negative voltage on CS may exceed the continuous absolute maximum rating.
(6) No GDA or GDB current limiting is required when driving a power MOSFET gate. However, a small series resistor may be required to damp resonant ringing due to stray inductance.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

All voltages are with respect to GND, −40 °C < $T_J = T_A$ < 125 °C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	14	21	V
VCC input current from a high-impedance source	8	18	mA
VREF load current	0	–2	
VINAC input voltage	0	6	V
ZCDA, ZCDB series resistor	20	80	kΩ
TSET resistor to program PWM on-time	66.5	400	
HVSEN input voltage	0.8	4.5	V

7.4 Thermal Information

THERMAL METRIC(1)		UCC28063A SOIC (D) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	91.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	52.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	48.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	48.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < $T_J = T_A$ < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
VCC_{SHUNT}	VCC shunt voltage(1)	I_{VCC} = 10 mA	22	24	26	V
$I_{VCC(ULVO)}$	VCC current, UVLO	VCC = 11.4 V prior to turn-on		95	200	µA
$I_{VCC(stby)}$	VCC current, disabled	VSENSE = 0 V		100	200	
$I_{VCC(on)}$	VCC current, enabled	VSENSE = 2 V		5	8	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC turn-on threshold	VCC rising	11.5	12.6	13.5	V
VCC_{OFF}	VCC turn-off threshold	VCC falling	9.5	10.35	11.5	
	UVLO Hysteresis		1.85	2.15	2.45	
REFERENCE						
V_{REF}	VREF output voltage, no load	I_{VREF} = 0 mA	5.82	6.00	6.18	V
	VREF change with load	0 mA ≤ I_{VREF} ≤ −2 mA		−1	−6	mV
	VREF change with VCC	12 V ≤ VCC ≤ 20 V		2	10	

(1) Excessive VCC input voltage and current will damage the device. This clamp will not protect the device from an unregulated bias supply. If an unregulated bias supply is used, a series-connected Fixed Positive-Voltage Regulator such as the UA78L15A is recommended. See the Absolute Maximum Ratings table for the limits on VCC voltage, current, and junction temperature.

Electrical Characteristics (接下页)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
VSENSEreg25	VSENSE input regulation voltage	T_A = 25 °C	5.85	6	6.15	V
VSENSEreg	VSENSE input regulation voltage		5.82	6	6.18	
I_{VSENSE}	VSENSE input bias current	In regulation	50	100	150	nA
V_{ENAB}	VSENSE enable threshold, rising		1.15	1.25	1.35	V
	VSENSE enable hysteresis		0.02	0.07	0.15	
$V_{COMPCLMP}$	COMP high voltage, clamped	VSENSE = VSENSEreg – 0.3 V	4.70	4.95	5.10	
	COMP low voltage, saturated	VSENSE = VSENSEreg + 0.3 V		0.03	0.125	
g_M	VSENSE to COMP transconductance, small signal	0.99(VSENSEreg) < VSENSE < 1.01(VSENSEreg), COMP = 3 V	40	55	70	µS
	VSENSE high-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	3.25%	5%	6.75%	
	VSENSE low-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	−3.25%	−5%	−6.75%	
	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg – 0.4 V , COMP = 3 V	210	290	370	µS
	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg + 0.4 V, COMP = 3 V	210	290	370	
	COMP maximum source current	VSENSE = 5 V, COMP = 3 V	−80	−125	−170	µA
$R_{COMPDCHG}$	COMP discharge resistance	HVSEN = 5.2 V, COMP = 3 V	1.6	2	2.4	kΩ
I_{DODCHG}	COMP discharge current during Dropout	VSENSE = 5 V, VINAC = 0.3 V	3.2	4	4.8	µA
V_{LOW_OV}	VSENSE over-voltage threshold, rising	Relative to VSENSEreg	7%	8%	10%	
	VSENSE over-voltage hysteresis	Relative to V_{LOW_OV}	−1.5%	−2%	−3%	
V_{HIGH_OV}	VSENSE 2nd over-voltage threshold, rising	Relative to VSENSEreg	10.5%	11.3%	14%	
SOFT START						
V_{SSTHR}	COMP Soft-Start threshold, falling	VSENSE = 1.5 V	15	23	30	mV
$I_{SS,FAST}$	COMP Soft-Start current, fast	SS-state, V_{ENAB} < VSENSE < VREF/2	−80	−125	−170	µA
$I_{SS,SLOW}$	COMP Soft-Start current, slow	SS-state, VREF/2 < VSENSE < 0.88VREF	−11.5	−16	−20	
K_{EOSS}	VSENSE End-of-Soft-Start threshold factor	Percent of VSENSEreg	96.5%	98.3%	99.8%	
OUTPUT MONITORING						
$V_{PWMCNTL}$	HVSEN threshold to PWMCNTL	HVSEN rising	2.35	2.50	2.65	V
I_{HVSEN}	HVSEN input bias current, high	HVSEN = 3 V		±0.03	±0.5	µA
I_{HV_HYS}	HVSEN hysteresis bias current, low	HVSEN = 2 V	9.2	11.4	14	

Electrical Characteristics (接下页)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HV\_OV\_FLT}$	HVSEN threshold to over-voltage fault	HVSEN rising	4.64	4.87	5.1	V
$V_{HV\_OV\_CLR}$	HVSEN threshold to over-voltage clear	HVSEN falling	4.45	4.67	4.8	
V_{COMP_PHFOFF}	Phase Fail monitoring-disable threshold	COMP falling	0.21	0.225	0.25	
V_{COMP_PHFHYS}	Phase Fail monitoring hysteresis	COMP rising		0.051		
	PWMCNTL output voltage low	HVSEN = 3 V, $I_{PWMCNTL}$ = 5 mA, COMP = 0 V		0.2	0.5	
t_{PHFDLY}	Phase Fail filter time to PWMCNTL high	PHB = 5 V, ZCDA switching, ZCDB = 0.5 V, COMP = 3 V	7.9	12	17	ms
$I_{PWMCNTL\_LEAK}$	PWMCNTL leakage current, high	HVSEN = 2 V, PWMCNTL = 15 V		±0.03	±0.5	µA
GATE DRIVE(2)						
	GDA, GDB output voltage, high	I_{GDA}, I_{GDB} = −100 mA	11.5	12.4	15	V
	GDA, GDB on-resistance, high	I_{GDA}, I_{GDB} = −100 mA		8.8	14	Ω
	GDA, GDB output voltage, low	I_{GDA}, I_{GDB} = 100 mA		0.18	0.32	V
	GDA, GDB on-resistance, low	I_{GDA}, I_{GDB} = 100 mA		2	3.2	Ω
	GDA, GDB output voltage high, clamped	VCC = 20 V, I_{GDA}, I_{GDB} = −5 mA	12	13.5	15	V
	GDA, GDB output voltage high, low VCC	VCC = 12 V, I_{GDA}, I_{GDB} = −5 mA	10	10.5	11.5	
	Rise time	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
	Fall time	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GDA, GDB output voltage, UVLO	VCC = 3.0 V, I_{GDA}, I_{GDB} = 2.5 mA		100	200	mV
ZERO CURRENT DETECTOR						
	ZCDA, ZCDB voltage threshold, falling		0.8	1	1.2	V
	ZCDA, ZCDB voltage threshold, rising		1.5	1.7	1.9	
	ZCDA, ZCDB clamp, high	I_{ZCDA} = +2 mA, I_{ZCDB} = +2 mA	2.6	3	3.4	
	ZCDA, ZCDB clamp, low	I_{ZCDA} = −2 mA, I_{ZCDB} = −2 mA	0	−0.2	−0.4	
	ZCDA, ZCDB input bias current	ZCDA = 1.4 V, ZCDB = 1.4 V		±0.03	±0.5	µA
	ZCDA, ZCDB delay to GDA, GDB outputs(2)	From ZCDx input falling to 1 V to respective gate drive output rising 10%		50	100	ns
	ZCDA blanking time(3)	From GDA rising and GDA falling		100		
	ZCDB blanking time(3)	From GDB rising and GDB falling		100		
CURRENT SENSE						
	CS input bias current, dual-phase	At rising threshold	−120	−166	−200	µA
	CS current-limit rising threshold, dual-phase	PHB = 5 V	−0.18	−0.2	−0.22	V
	CS current-limit rising threshold, single-phase	PHB = 0 V	−0.149	−0.166	−0.183	
	CS current-limit reset falling threshold		−0.003	–0.015	−0.025	

(2) Refer to 图 13, 图 14, 图 15, and 图 16 of the Typical Characteristics for typical gate drive waveforms.
(3) ZCD blanking times are ensured by design.

Electrical Characteristics (接下页)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CS current-limit response time(2)	From CS exceeding threshold−0.05 V to GDx dropping 10%		60	100	ns
	CS blanking time	From GDx rising and falling edges		100		
VINAC INPUT						
I_{VINAC}	VINAC input bias current, above brownout	VINAC = 2 V		±0.03	±0.5	µA
V_{BODET}	VINAC brownout detection threshold	VINAC falling	1.33	1.39	1.44	V
t_{BODLY}	VINAC brownout filter time	VINAC below the brownout detection threshold for the brownout filter time	340	440	540	ms
V_{BOHYS}	VINAC brownout threshold hysteresis	VINAC rising	30	62	75	mV
I_{BOHYS}	VINAC brownout hysteresis current	VINAC = 1 V for > t_{BODLY}	1.6	2	2.5	µA
V_{DODET}	VINAC dropout detection threshold	VINAC falling	0.315	0.35	0.38	V
t_{DODLY}	VINAC dropout filter time	VINAC below the dropout detection threshold for the dropout filter time	3.5	5	7	ms
V_{DOCLR}	VINAC dropout clear threshold	VINAC rising	0.67	0.71	0.75	V
PULSE-WIDTH MODULATOR						
K_T	On-time factor, phases A and B	VSENSE = 5.8 V(4)	3.6	4.0	4.4	µs/V
K_{TS}	On-time factor, single-phase, A	VSENSE = 5.8 V, PHB = 0 V(4)	7.2	8.0	8.9	
	Phase B to phase A on-time matching error	VSENSE = 5.8 V		±2%	±6%	
	Zero-crossing distortion correction additional on time	COMP = 0.25 V, VINAC = 1 V	1.2	2	2.8	µs
		COMP = 0.25 V, VINAC = 0.1 V	12.6	20	29	
V_{PHBF}	PHB threshold falling, to single-phase operation	To GDB output shutdown, VINAC = 1.5 V	0.7	0.8	0.9	V
V_{PHBR}	PHB threshold rising, to two-phase operation	To GDB output running, VINAC = 1.5 V	0.9	1	1.1	
T_{MIN}	Minimum switching period	R_{TSET} = 133 kΩ(4)	1.7	2.2	3	µs
T_{START}	PWM restart time	ZCDA = ZCDB = 2 V(5)	165	210	265	
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature	Temperature rising(6)		160		°C
T_J	Thermal restart temperature	Temperature falling(6)		140		

(4) Gate drive on-time is proportional to (V_{COMP} – 0.125 V). The on-time proportionality factor, K_T, scales linearly with the value of R_{TSET} and is different in two-phase and single-phase modes. The minimum switching period is proportional to R_{TSET}.
(5) An output on-time is generated at both GDA and GDB if both ZCDA and ZCDB negative-going edges are not detected for the restart time. In single-phase mode, the restart time applies for the ZCDA input and the GDA output.
(6) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance above the normal operating temperature is not specified or assured.

7.6 Typical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

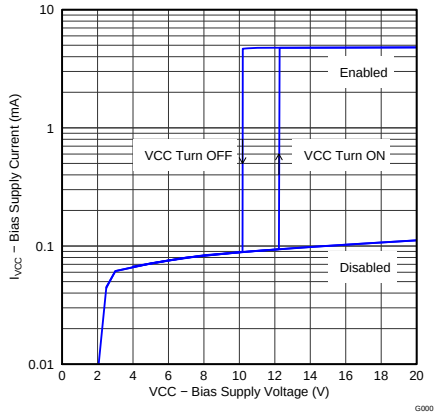


图 1. Bias Supply Current vs Bias Supply Voltage

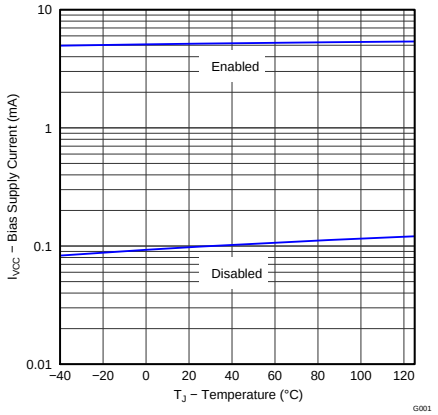
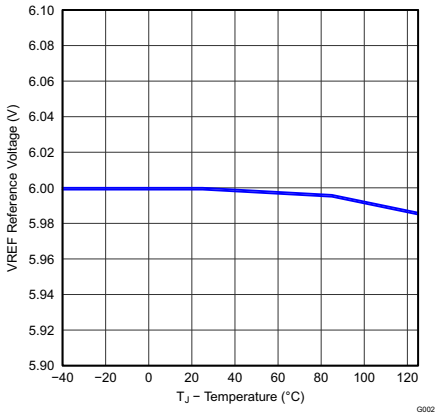


图 2. Bias Supply Current vs Temperature



I_{VREF} = 0 to –2 mA

图 3. Reference Voltage vs Temperature

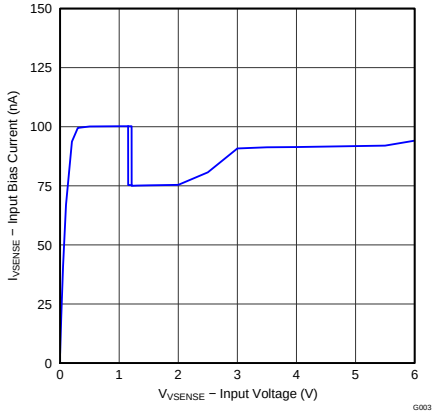
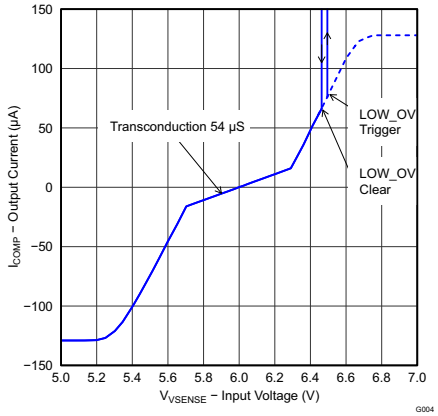


图 4. VSENSE Input Bias Current vs Input Voltage



Soft-Start Completed

图 5. Error Amplifier Output Current vs Input Voltage

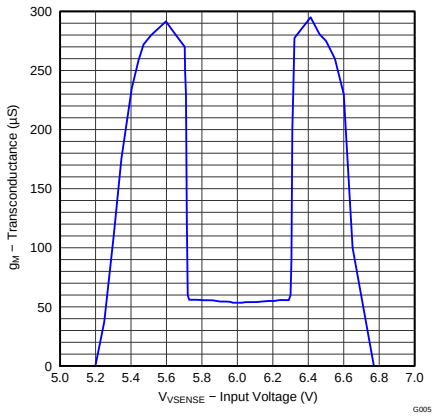
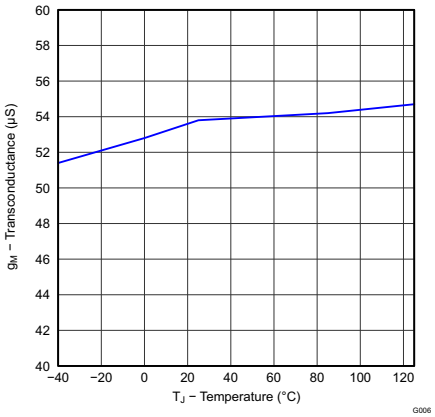


图 6. Error Amplifier Transconductance vs VSENSE

Typical Characteristics (接下页)



5.9 V < V_{VSENSE} < 6.1 V

图 7. Error Amplifier Transconductance vs Temperature

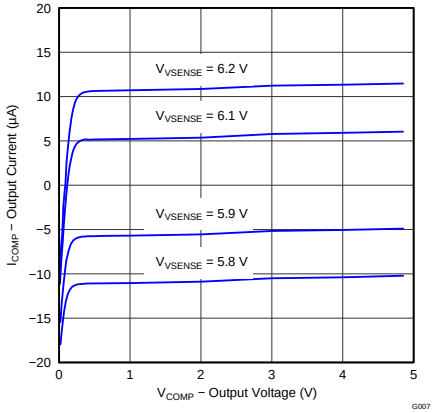


图 8. Error Amplifier Output Current vs Output Voltage

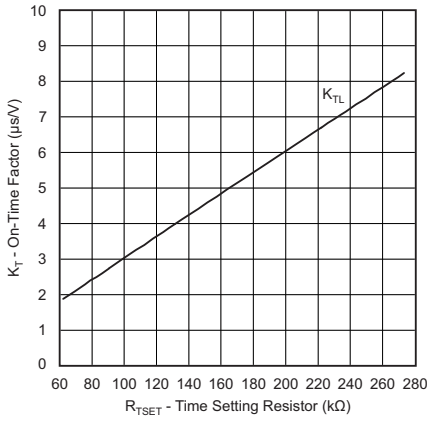


图 9. On-Time Factor vs Time Setting Resistor

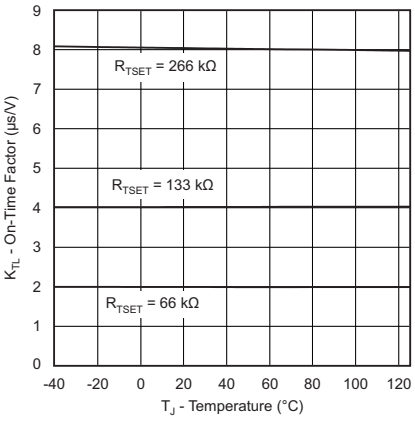
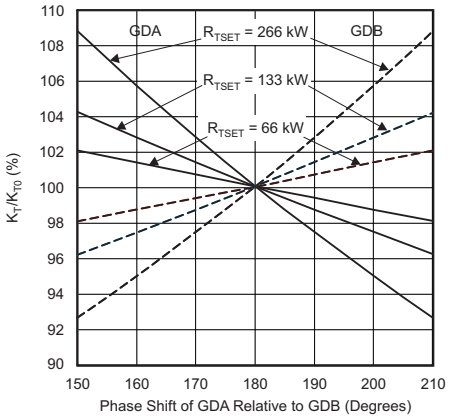


图 10. On-Time Factor Phase A and B vs Temperature



$K_{TO} = 2(K_{TA} \times K_{TB}) / K_{TA} + K_{TB}$

图 11. On-Time Factor vs Phase Error

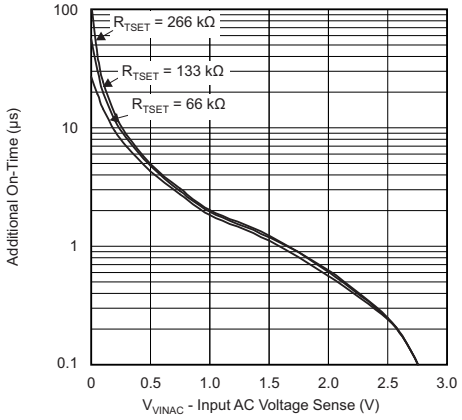
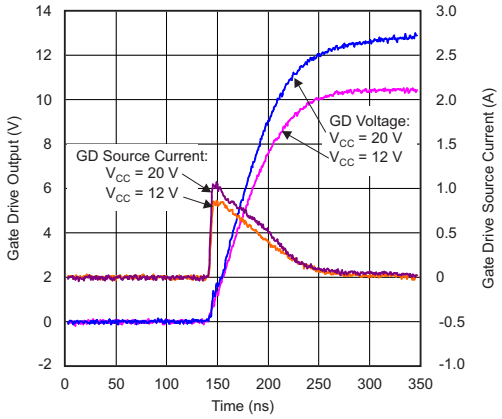


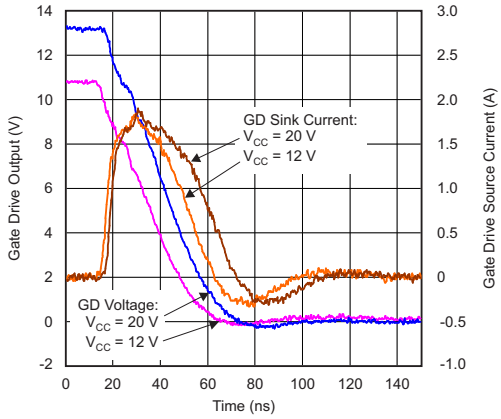
图 12. Additional On Time vs VINAC

Typical Characteristics (接下页)



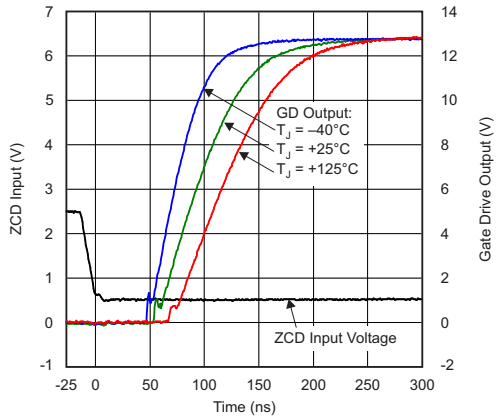
C_{LOAD} = 4.7 nF

图 13. Gate Drive Rising vs Time



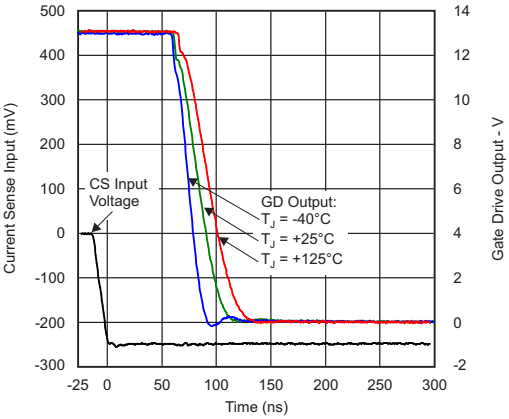
C_{LOAD} = 4.7 nF

图 14. Gate Drive Falling vs Time



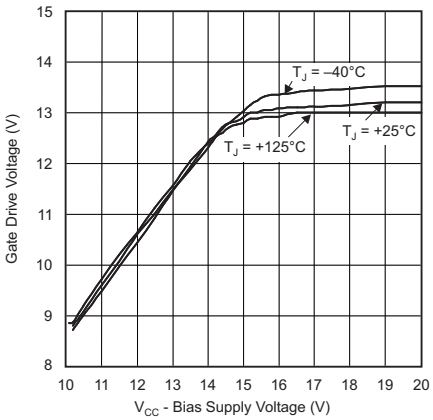
C_{LOAD} = 4.7 nF

图 15. Gate Drive Rising and Delay From ZCD Input vs Time



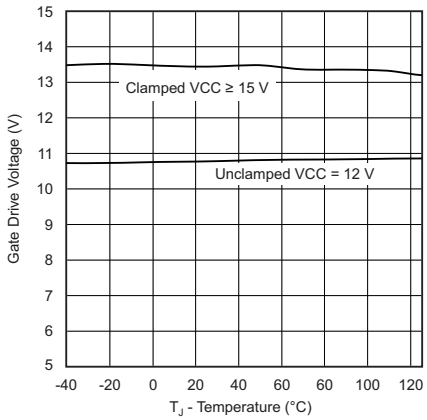
C_{LOAD} = 4.7 nF

图 16. Gate Drive Falling and Delay From CS Input vs Time



R_{LOAD} = 2.7 kΩ

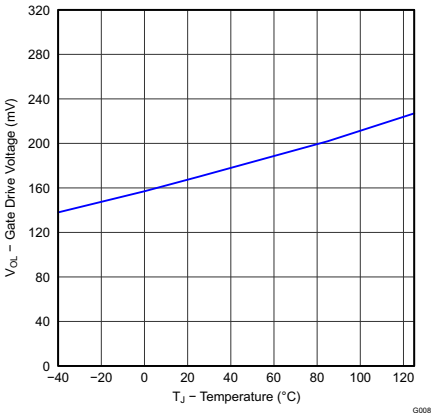
图 17. Gate Drive Output High vs VCC



R_{LOAD} = 2.7 kΩ

图 18. Gate Drive High Voltage vs Temperature

Typical Characteristics (接下页)



Load = 100 mA

图 19. Gate Drive Low Voltage vs Temperature

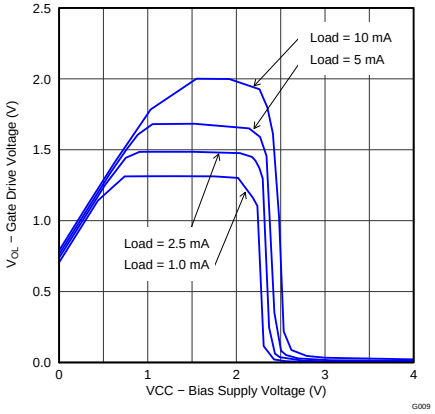


图 20. Gate Drive Low Voltage in UVLO vs Bias Supply Voltage

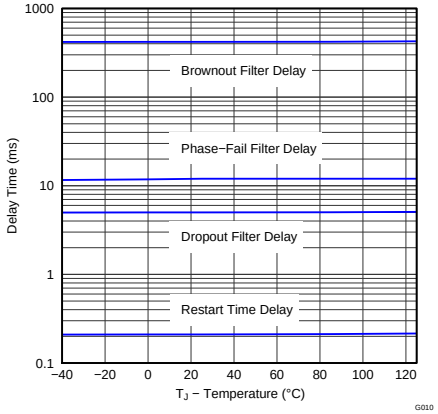


图 21. Various Delay Times vs Temperature

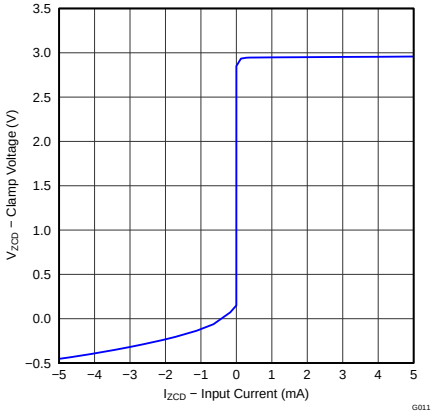
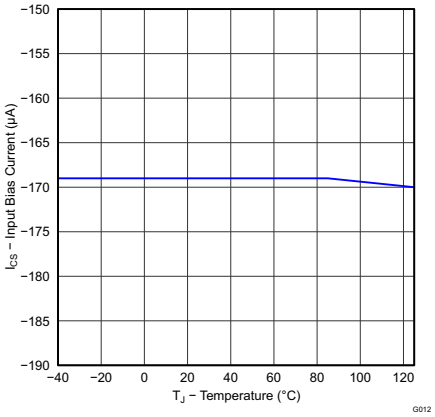


图 22. Zero Current Detect Clamp Voltage vs Input Current



V_{CS} = –195 mV

图 23. Current Sense Input Bias Current vs Temperature

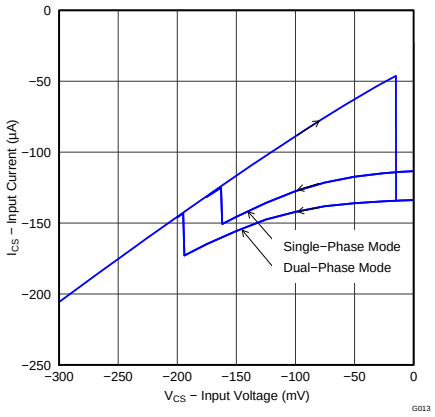


图 24. Current Sense Input Bias Current vs Input Voltage

8 Detailed Description

8.1 Overview

This part is identical to UCC28063 with the exception that the TSET pin Open/ Short Fault Detect and the CS pin Open Fault Detect features are removed. Removal of these fault detect mechanisms provides a higher degree of noise immunity for applications where significant voltage noise could be coupled onto the TSET or CS pins during conditions of extreme fast transient, surge or impulse noise events. The Soft Re-Start fault protection which would be triggered on the UCC28063 will not occur with the UCC28063A. The system will continue to provide power delivery through such events, albeit with the possibility of some dynamic regulation irregularity.

Transition Mode Control is the most popular choice for the Boost Power Factor Correction topology at lower power levels because of its lower complexity in achieving high power factor while at the same time not placing demanding requirements on the power component specifications. A lower cost boost diode with higher reverse recovery current specification may be used, for instance, in the Transition Mode Boost. Interleaved Transition Mode Control retains this benefit and generally extends the applicability up to much higher power levels while simultaneously conferring the interleaving benefits of reduced input and output ripple, phase management for light load efficiency enhancement, redundancy, system thermal optimization and low profile or planar solutions.

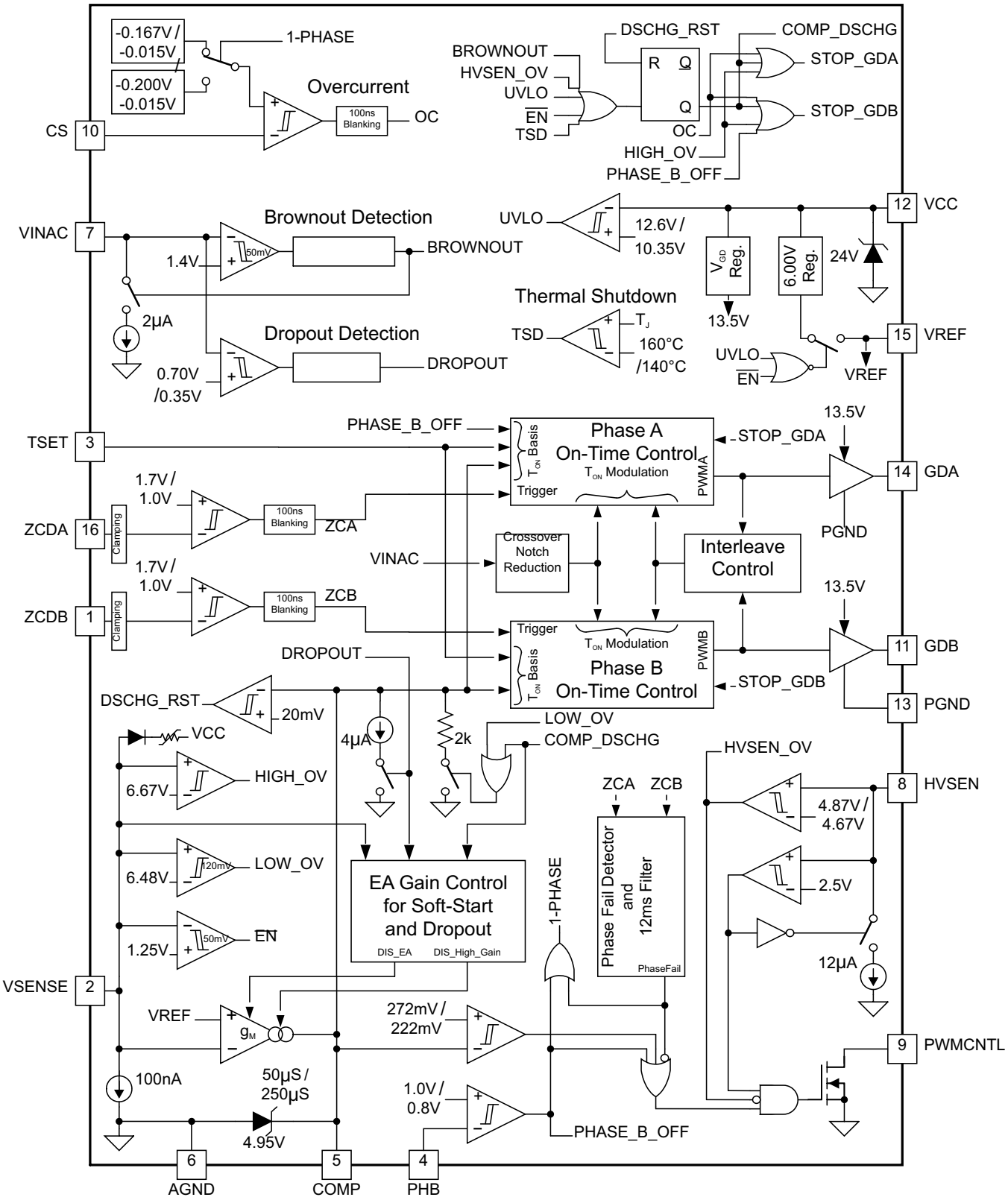
The UCC28063A enables a very cost effective solution with a particular focus on ruggedness, fault management, fault recovery, efficiency and higher end performance in areas such as acoustic management and fast transient response. It may be regarded as an enhanced and new generation UCC28061.

Interleaving control and phase management facilitates 80+ and Energy Star designs with reduced input and output ripple. The Natural Interleaving method allows TM operation and achieves 180 degrees between the phases by On-time management and does not rely on tight tolerance requirements on the inductors. The Crossover Notch Reduction block implements a non-linear current shaping characteristic on the instantaneous voltage sense (VINAC) in order to reduce distortion and increase Power Factor. Negative current sensing is implemented on the total input current instead of just the MOSFET current which prevents MOSFET switching during inrush surges or in any mode where the inductor current may become substantially continuous (CCM). This prevents reverse recovery conduction events between the MOSFET and output rectifier. Downstream power stage management is facilitated by the PWMCNTL signal. This open drain signal provides an enable with hysteresis for a downstream converter when the PFC stage voltage is above an operating threshold, FailSafe OV protection is not in operation and there is no PhaseFail fault.

Independent output voltage sense chains with their separate fault management behaviors provide a high degree of redundancy against PFC stage overvoltage. Brown-Out, HVSENSE OV, UVLO, and IC Overtemperature will all cause a complete Soft-Start cycle. Other faults such as short duration AC Drop-Out, minor overvoltage or cycle-by-cycle overcurrent cause a live recovery process to initiate by pulling down on the COMP pin or by terminating the pulses early.

In general IC operation is designed to ensure smooth and acoustic noise free start-up, good transient response behavior and well behaved recovery from faults. The Error amplifier transconductance is designed to allow smaller compensation components and optimum transient response for larger deviations. The Soft-Start process is carefully optimized. A complete Soft Start is implemented on recovery from every fault, for consistency. The Soft Start speed is dependent on the output voltage sense to speed up start-up from low AC line and to minimize the effect of excessive "COMP" during start-up into no-load. This complete discharge of COMP aids with preventing excessive currents on recovery from an AC Brown-Out event.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Principles of Operation

The UCC28063A contains the control circuits for two parallel-connected boost pulse-width modulated (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output. Each power converter then turns off the power MOSFET until current in the boost inductor decays to zero, as sensed on the zero current detection inputs (ZCDA and ZCDB). Once the inductor is demagnetized, the power converter starts another cycle. This on/off cycling produces a triangle wave of current, with peak current set by the on-time and instantaneous power mains input voltage, $V_{IN}(t)$, as shown in 公式 1.

$$I_{PEAK}(t) = \frac{V_{IN}(t) \times T_{ON}}{L} \tag{1}$$

The average line current is exactly equal to half of the peak line current, as shown in 公式 2.

$$I_{AVG}(t) = \frac{V_{IN}(t) \times T_{ON}}{2 \times L} \tag{2}$$

With T_{ON} and L being essentially constant during an AC-line period, the resulting triangular current waveform during each switching cycle will have an average value proportional to the instantaneous value of the rectified AC-line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

8.3.2 Natural Interleaving

Under normal operating conditions, the UCC28063A regulates the relative phasing of the channel A and channel B inductor currents to be very close to 180°. This greatly reduces the switching-frequency ripple currents seen at the line-filter and output capacitors, compared to the ripple current of each individual converter. This design allows a reduction in the size and cost of input and output filtering. The phase-control function differentially modulates the on-times of the A and B channels based on their phase and frequency relationship. The Natural Interleaving method allows the converter to achieve 180° phase-shift and transition-mode operation for both phases without tight requirements on boost inductor tolerance.

Ideally, the best current-sharing is achieved when both inductors are exactly the same value. Typically the inductances are not the same, so the current-sharing of the A and B channels is proportional to the inductor tolerance. Also, switching delays and resonances of each channel typically differ slightly, and the controller allows some necessary phase-error deviation from 180° to maintain equal switching frequencies. Optimal phase balance occurs if the individual power stages and the on-times are well matched. Mismatches in inductor values do not affect the phase relationship.

8.3.3 On-Time Control, Maximum Frequency Limiting, and Restart Timer

Gate-drive on-time varies proportionately with the error-amplifier output voltage by a factor called K_T (in units of µs/V), as shown in 公式 3.

$$T_{ON} = K_T \left(V_{COMP} - 125\,mV\right) \tag{3}$$

Where:

- V_{COMP} is the output voltage of the error amplifier and 125 mV is a modulator offset voltage.

The maximum output of the error amplifier is limited to 4.95 V. This value, minus the 125-mV modulator offset, limits maximum on-time as determined by 公式 4.

$$T_{ON(max)} = K_T \times 4.825\,V \tag{4}$$

This on-time limit sets the maximum power that can be delivered by the converter at a given input voltage.

At lower power, one boost channel (phase) may be turned off to achieve efficiency benefits (see Phase Management section, below). To provide a smooth transition between two-phase and single-phase operation, K_T increases by a factor of two in single-phase mode:

$$K_{TS} = 2 \times K_T;\ \text{active during single-phase operation} \tag{5}$$

Feature Description (接下页)

The maximum switching frequency of each phase is limited by minimum-period timers. If inductor current decays to zero before the minimum-period timer elapses, the next turn-on will be delayed, resulting in discontinuous phase current.

A restart timer ensures starting under all circumstances by restarting both phases if the ZCD input of either phase has not transitioned from high-to-low within approximately 200 µs. To prevent the circuit from operating in continuous conduction mode (CCM), the restart timer does not trigger turn-on until both phase-currents return to zero.

The on-time factors (K_T, K_{TS}) and the minimum switching period, $T_{(MIN)}$, are proportional to the time-setting resistor R_{TSET} (the resistor from the TSET pin to ground), and these factors can be calculated by 公式 5, 公式 6 and 公式 7:

$$K_T = \frac{R_{TSET}}{133\,k\Omega} \times 4.0 \frac{\mu s}{volt} \quad (6)$$

$$T_{(MIN)} = \frac{R_{TSET}}{133\,k\Omega} \times 2.2\,\mu s \text{ ; Minimum Switching Period} \quad (7)$$

The proper value of R_{TSET} will result in the clamped maximum on-time, $T_{ON(max)}$, required by the converter operating at the minimum input line voltage and maximum load.

8.3.4 Distortion Reduction

Due to the parasitic resonance between the drain-source capacitance of the switching MOSFET and the boost inductor, conventional transition-mode PFC circuits may not be able to absorb power from the input line when the input voltage is near zero. This limitation increases total harmonic distortion as a result of ac-line current waveform distortion in the form of flat spots. To help reduce line-current distortion, the UCC28063A increases switching MOSFET on-time when the input voltage is near 0 V to improve the power absorption capability and compensate for this effect.

图 12 in the Typical Characteristics section shows the increase in on-time with respect to VINAC voltage. Excessive filtering of the VINAC signal will nullify this function.

8.3.5 Zero-Current Detection and Valley Switching

In transition-mode PFC circuits, the MOSFET turns on when the boost inductor current reaches zero. Because of the resonance between the boost inductor and the parasitic capacitance at the MOSFET drain node, part of the energy stored in the MOSFET junction capacitor can be recovered, reducing switching losses. Furthermore, when the rectified input voltage is less than half of the output voltage, all the energy stored in the MOSFET junction capacitor can be recovered and zero-voltage switching (ZVS) can be realized. By adding an appropriate delay, the MOSFET can be turned on at the valley of its resonating drain voltage (valley-switching). In this way, the energy recovery can be maximized and switching loss is minimized.

The optimal time delay is generally derived empirically, but a good starting point is a value equal to 25% of the resonant period of the drain circuit. The delay can be realized by a simple RC filter, as shown in 图 25, but the delay time increases slightly as the input voltage nears the output voltage. Because the ZCD pin is internally clamped, a more accurate delay can also be realized by using the circuit shown in 图 26.

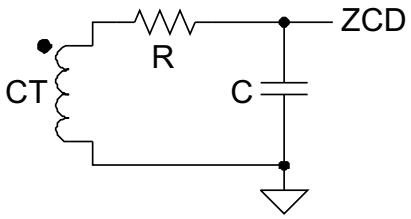


图 25. Simple RC Delay Circuit

Feature Description (接下页)

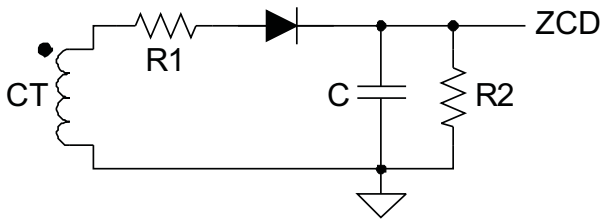


图 26. More Accurate Time Delay Circuit

8.3.6 Phase Management and Light-Load Operation

Under light-load conditions, switching losses may dominate over conduction losses and efficiency may be improved if one phase (channel) is turned off. At a certain power level, the reduction of switching losses is greater than the increase in conduction losses. Turning off one phase at light load is especially valuable for meeting light-load efficiency standards. This is one of the major benefits of interleaved PFC and it is especially valuable for meeting 80+ design requirements.

The PHB input can be used to force the UCC28063A to operate in single-phase mode. When PHB is driven below 0.8 V, channel B will stop switching and channel A on-time will automatically double to compensate. The device will resume dual-phase mode when PHB is raised above 1.0 V. For customized phase management, an external circuit can detect the conditions for switching to single-phase operation and drive PHB accordingly. To operate continuously in two-phase mode (normal mode) when phase management is not desired, simply connect PHB to VREF.

As load current decreases, the error amplifier commands less ac-line input current by lowering COMP voltage. In applications where the ac-line is limited to the low-voltage range only, it may be advantageous to connect PHB directly to COMP to allow automatic selection of single-phase operation without additional external circuitry.

8.3.7 External Disable

The UCC28063A can be externally disabled by purposefully grounding the VSENSE pin with an open-drain or open-collector driver. When disabled, the device supply current drops significantly and COMP is actively pulled low. This disable method forces the device into standby mode and minimizes its power consumption. This is particularly useful when standby power is a key design aspect. When VSENSE is released, the device enters soft-start mode.

8.3.8 Improved Error Amplifier

The voltage-error amplifier is a transconductance amplifier. Voltage-loop compensation is connected from the error amplifier output, COMP, to analog ground, AGND. The recommended Type-II compensation network is shown in 图 27. For loop-stability purposes, the compensation network values are calculated based on small-signal perturbations of the output voltage using the nominal transconductance (gain) of 55 µS.

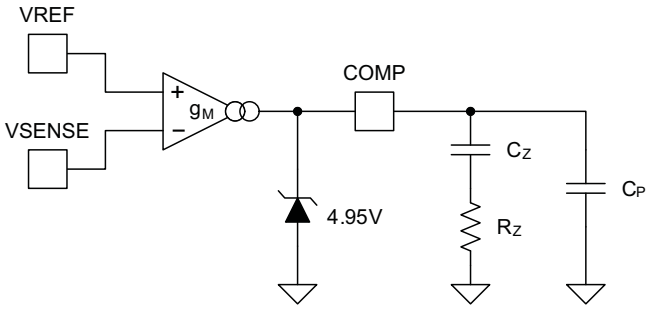
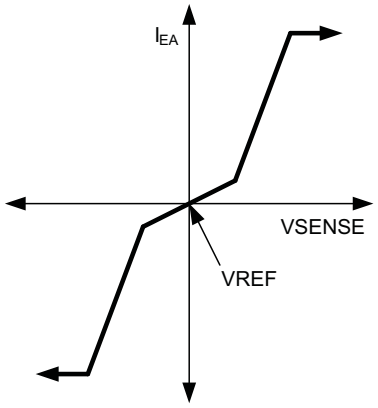


图 27. Transconductance Error Amplifier With Typical Compensation Network

Feature Description (接下页)

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of ~5X when the error amp input deviates more than ±5% from the nominal regulation voltage, VSENSEreg. This increase allows faster charging and discharging of the compensation components following sudden load-current increases or decreases (also refer to 图 5 in the *Typical Characteristics*).



Basic voltage-error amplifier transconductance curve showing small-signal and large-signal gain sections, with maximum current limitations.

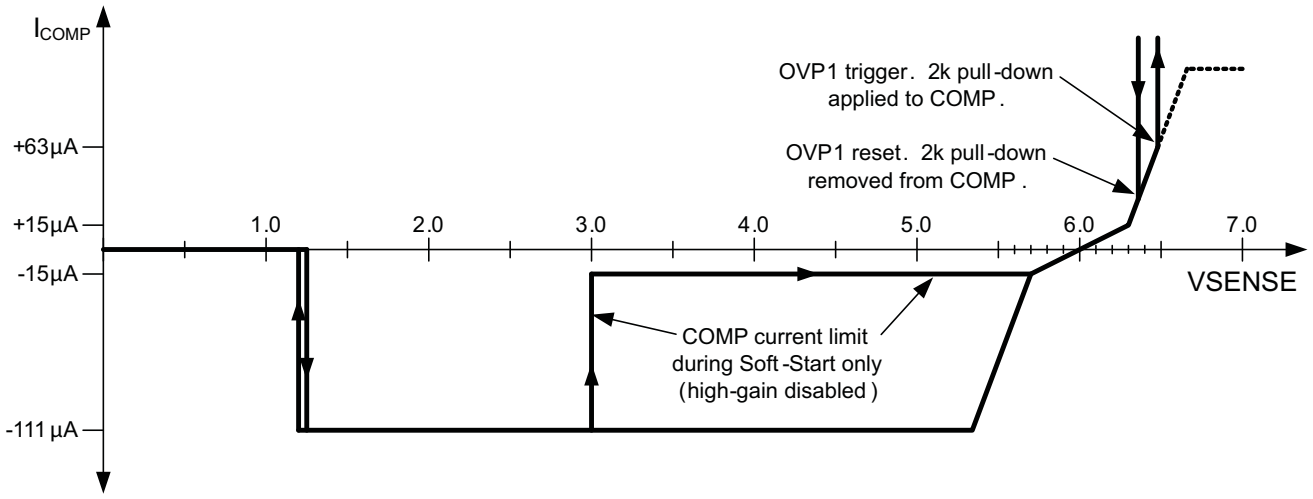
图 28. Basic Voltage-Error Amplifier Transconductance Curve

8.3.9 Soft Start

Soft-start is a process for boosting the output voltage of the PFC converter from the peak of the ac-line input voltage to the desired regulation voltage under controlled conditions. Instead of a dedicated soft-start pin, the UCC28063A uses the voltage error amplifier as a controlled current source to increase the PWM duty-cycle by way of increasing the COMP voltage. To avoid excessive start-up time-delay when the ac-line voltage is low, a higher current is applied until VSENSE exceeds 3 V at which point the current is reduced to minimize the tendency for excess COMP voltage at no-load start-up.

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from zero to near its final value. This process implements a soft-start, with timing set by the output current of the error amplifier and the value of the compensation capacitors. In the event of a HVSEN FailSafe OVP, brownout, external-disable, UVLO fault, or other protection faults, COMP is actively discharged and the UCC28063A will soft-start after the triggering event is cleared. Even if a fault event happens very briefly, the fault is latched into the soft-start state and soft-start is delayed until COMP is fully discharged to 20 mV and the fault is cleared. See 图 29 for details on the COMP current. See 图 30 which illustrates an example of typical system behavior during soft-start.

Feature Description (接下页)



Expanded COMP output current curve including voltage-error amplifier transconductance and modifications applicable to soft-start and overvoltage conditions.

图 29. Expanded Comp Output Current Curve

Feature Description (接下页)

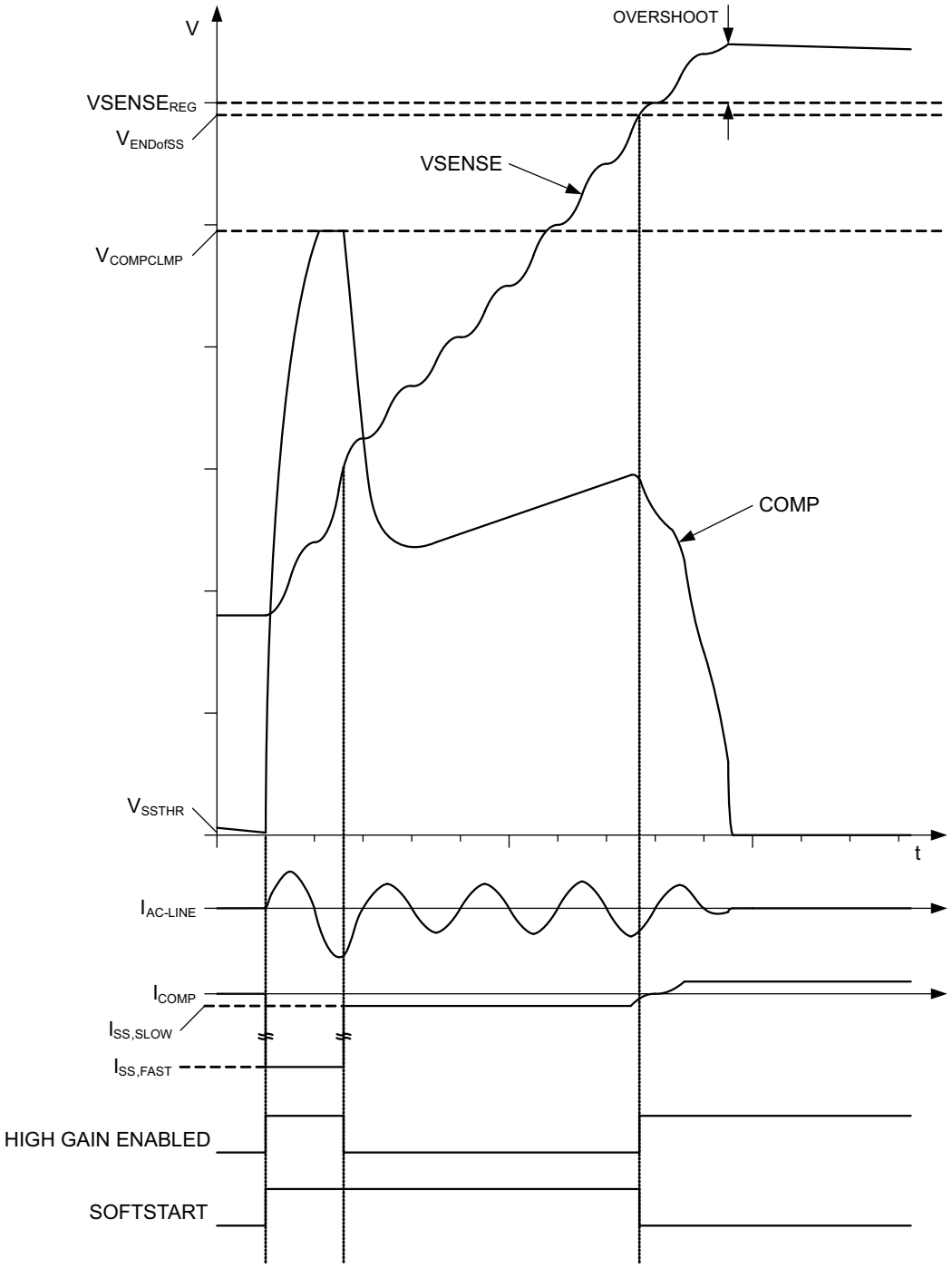


图 30. Soft-Start Timing With Illustrative System Behavior

Feature Description (接下页)

8.3.10 Brownout Protection

As the power line RMS voltage decreases, RMS input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level. Power-line voltage is sensed at VINAC. When the VINAC fails to exceed the brownout threshold for the brownout filter time, a brownout condition is detected and both gate drive outputs are turned off. During brownout, COMP is actively pulled low and a soft-start condition is initiated. Hysteresis is built into the brownout detection circuit to avoid chatter around the threshold. When VINAC rises above the brownout threshold, the power stage soft-starts as COMP rises with controlled current.

The brownout detection threshold and its hysteresis are set by the voltage-divider ratio and resistor values. Brownout protection is based on VINAC peak voltage; the threshold and hysteresis are also based on the line peak voltage. Major hysteresis is provided by a 2-µA current-sink (I_{BOHYS}) enabled whenever VINAC falls below the brownout detection threshold. Minor hysteresis is also present in the form of a 50-mV offset (V_{BOHYS}) between the VINAC detection and clear thresholds. The peak VINAC voltage can be easily translated into an RMS value. Example resistor values for the voltage divider are 8.61 MΩ ±1% from the rectified input voltage to VINAC and 133 kΩ ±1% from VINAC to ground. These resistors set the typical thresholds for RMS line voltages, as shown in 表 1.

表 1. Brownout Thresholds (For Conditions Stated in the Text)

THRESHOLD	AC-LINE VOLTAGE (RMS)
Falling	66 V
Rising	78 V

公式 8 and 公式 9 can be used to calculate the VINAC divider-resistor values based on desired brownout detection and brownout clear voltage levels. V_{AC_OK} is the desired RMS turn-on voltage, V_{AC_BO} is the desired RMS turn-off brownout voltage, and V_{LOSS} is total series voltage drop due to wiring, EMI-filter, and bridge-rectifier impedances at V_{AC_BO}. V_{BODET}, V_{BOHYS} and I_{BOHYS} are found in the data-tables of this datasheet.

$$R_A = \left(\frac{\sqrt{2}(V_{AC\_OK} - V_{AC\_BO}) - V_{BOHYS}}{I_{BOHYS}} \right) \left(1 + \frac{V_{BOHYS}}{V_{BODET}} \right) \tag{8}$$

$$R_B = \frac{R_A}{\left(\frac{\sqrt{2} V_{AC\_BO} - V_{LOSS}}{V_{BODET}} - 1 \right)} \tag{9}$$

Once standard values for the VINAC divider-resistors R_A and R_B are selected, the actual turn-on and brownout threshold RMS voltages for the ac-line can be back-calculated with 公式 10 and 公式 11:

$$V_{AC\_BO} = \left(1 + \frac{R_A}{R_B} \right) \frac{V_{BODET}}{\sqrt{2}} + \frac{V_{LOSS}}{\sqrt{2}} \tag{10}$$

$$V_{AC\_OK} = V_{AC\_BO} + \frac{R_A I_{BOHYS}}{\sqrt{2}\left(1 + \frac{V_{BOHYS}}{V_{BODET}} \right)} + \frac{V_{BOHYS}}{\sqrt{2}} \tag{11}$$

An example of the timing for the brownout function is illustrated in 图 31.

For a quick estimation of the turn-on and brownout voltages, simplify the foregoing equations by setting the V_{LOSS} and V_{BOHYS} terms to zero.

8.3.11 Dropout Detection

It is often the case that the ac-line voltage momentarily drops to zero or nearly zero, due to transient abnormal events affecting the local ac power distribution network. Referred to as ac-line dropouts (or sometimes as line-dips) the duration of such events usually extends to only 1 or 2 line cycles. During a dropout, the down-stream power conversion stages depend on sufficient energy storage in the PFC output capacitance, which is sized to provide the ride-through energy for a specified hold-up time. Typically while the PFC output voltage is falling, the voltage-loop error amplifier output rises in an attempt to maintain regulation. As a consequence, excess duty-cycle is commanded when the ac-line voltage returns and high peak current surges may saturate the boost inductors with possible overstress and audible noise.

The UCC28063A incorporates a dropout detection feature which suspends the action of the error amplifier for the duration of the dropout. If the VINAC voltage falls below 0.35 V for longer than 5 ms, a dropout condition is detected and the error amplifier output is turned off. In addition, a 4-µA pull-down current is applied to COMP to gently discharge the compensation network capacitors. In this way, when the ac-line voltage returns, the COMP voltage (and corresponding duty-cycle setting) remains very near or even slightly below the level it was before the dropout occurred. Current surges due to excess duty-cycle, and their undesired attendant effects, are avoided. The dropout condition is cancelled and the error amplifier resumes normal operation when VINAC rises above 0.71 V.

Based on the VINAC divider-resistor values calculated for brownout in the previous section, the input RMS voltage thresholds for dropout detection V_{AC_DO} and dropout clearing V_{DO_CLR} can be determined using 公式 12 and 公式 13, below.

$$V_{AC\_DO} = \frac{V_{DODET}\left(\frac{R_A}{R_B}+1\right)+V_{LOSS}}{\sqrt{2}} \quad (12)$$

$$V_{DO\_CLR} = \frac{V_{DOCLR}\left(\frac{R_A}{R_B}+1\right)+V_{LOSS}}{\sqrt{2}} \quad (13)$$

Avoid excessive filtering of the VINAC signal, or dropout detection may be delayed or defeated. An RC time-constant of ≤ 100-µs should provide good performance. An example of the timing for the dropout function is illustrated in 图 32.

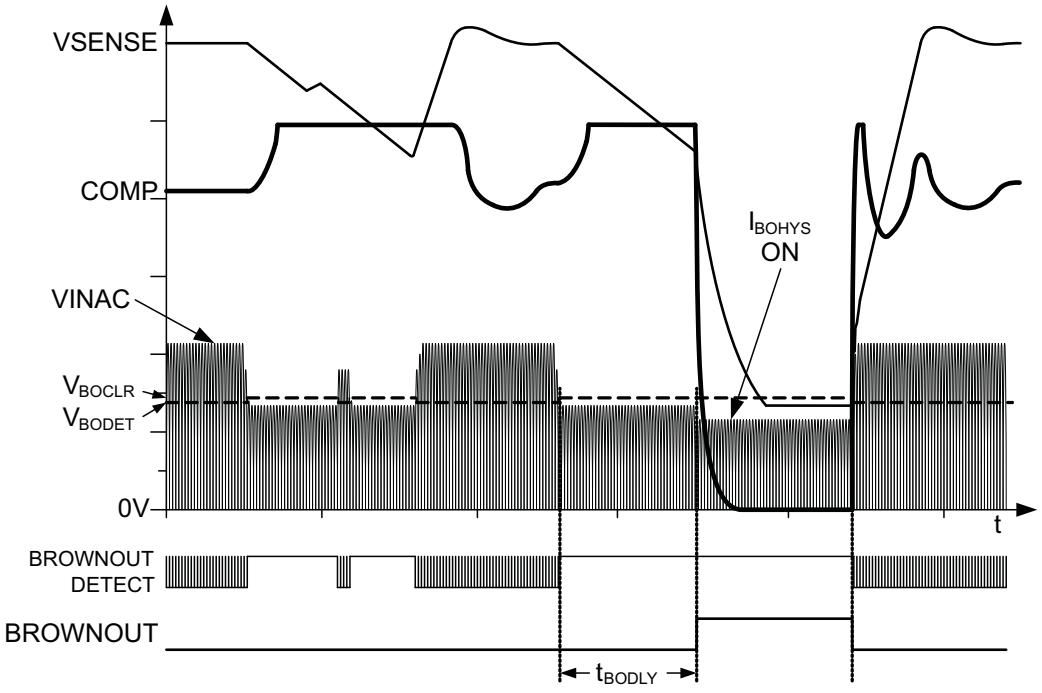


图 31. AC-Line Brownout Timing With Illustrative System Behavior

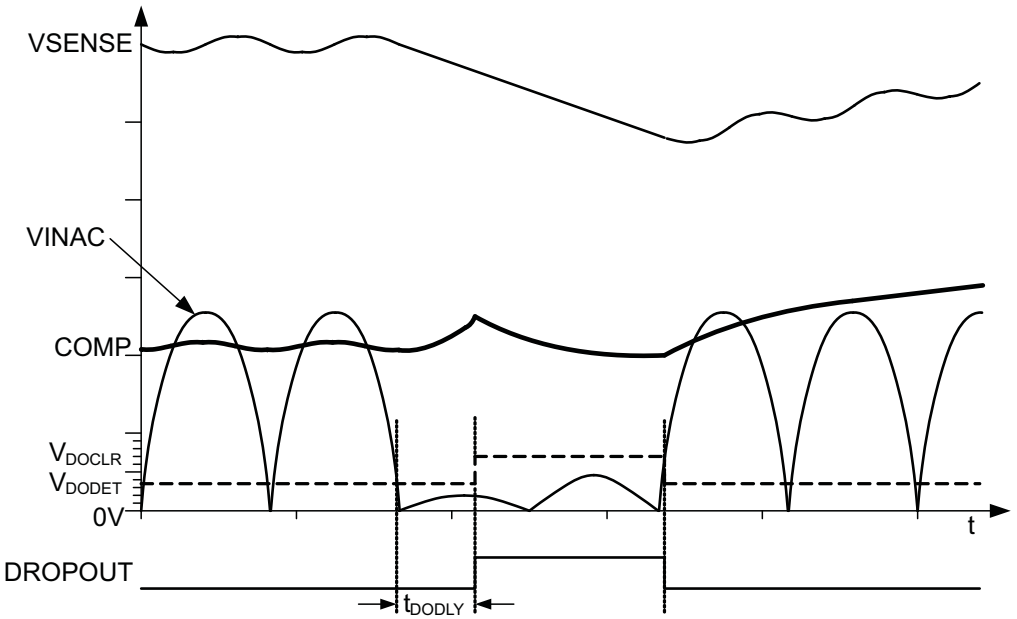


图 32. AC-Line Dropout Timing With Illustrative System Behavior

8.3.12 VREF

VREF is an output which supplies a well-regulated reference voltage to circuits within the device as well as serving as a limited source for external circuits. This output must be bypassed to GND with a low-impedance 0.1-µF or larger capacitor placed as close to the VREF and GND pins as possible. Current draw by external circuits should not exceed a few milli-amperes and should not be pulsing.

The VREF output is disabled under the following conditions: when VCC is in UVLO, or when VSENSE is below the Enable threshold. This output can only source current and is unable to accept current into the pin.

8.3.13 VCC

VCC is usually connected to a bias supply of between 13 V and 21 V. To minimize switching ripple voltage on VCC, it should be by-passed with a low-impedance capacitor as close to the VCC and GND pins as possible. The capacitance should be sized to adequately decouple the peak currents due to gate-drive switching at the highest operating frequency. When powered from a poorly-regulated low-impedance supply, an external zener diode is recommended to prevent excessive current into VCC.

The undervoltage-lockout (UVLO) condition is when VCC voltage has not yet reached the turn-on threshold or has fallen below the turn-off threshold, having already been turned on. While in UVLO, the VREF output and most circuits within the device are disabled and VCC current falls significantly below the normal operating level. The same situation applies when VSENSE is below its Enable threshold. This helps minimize power loss during pre-powerup and standby conditions.

8.3.14 Control of Downstream Converter

In the UCC28063A, the PWMCNTL pin can be used to coordinate the PFC stage with a downstream converter. Through the HVSEN pin, the PFC output voltage is monitored. A 12-µA current source (I_{HV_HYS}) is enabled as long as the output voltage remains below a programmed threshold. When the output voltage exceeds that threshold, PWMCNTL pin is pulled to ground internally and can be used to enable a downstream converter. At the same time the current source is disabled, providing hysteresis for a lower threshold at which the downstream converter should be turned off. The enable/disable hysteresis is adjusted through the HVSEN voltage-divider ratio and resistor values. The HVSEN pin is also used for the FailSafe over-voltage protection (OVP). When designing the voltage divider, make sure this FailSafe OVP level is set above normal VSENSE OVP levels.

Because there are two thresholds associated with the HVSEN input detected through a single resistor divider, the PWMCNTL turn-off voltage, $V_{PWM-OFF}$, is linked to the FailSafe OVP voltage, V_{FLSF_OV}, as shown by 公式 14:

$$\frac{V_{PWM-OFF}}{2.5\,V} = \frac{V_{FLSF\_OV}}{4.87\,V} \quad (14)$$

Choosing either one first arbitrarily determines the other, so a trade-off may be necessary. The PWMCNTL turn-on voltage, V_{PWM-ON}, is programmed by choosing the upper divider resistor value in consideration with the HVSEN hysteresis current, as shown in 公式 15 and 公式 16. The lower divider resistor is then calculated as shown in 公式 17.

$$V_{PWM-ON} = V_{PWM-OFF} + I_{HV\_HYS} R_{HV\_UPPER} \quad (15)$$

$$R_{HV\_UPPER} = \frac{V_{PWM-ON} - V_{PWM-OFF}}{I_{HV\_HYS}} \quad (16)$$

$$R_{HV\_LOWER} = \frac{R_{HV\_UPPER}}{\left(\frac{V_{PWM-OFF}}{2.5\,V} - 1\right)} \quad (17)$$

8.3.15 System Level Protections

8.3.15.1 Failsafe OVP - Output Overvoltage Protection

FailSafe OVP prevents any single failure from allowing the output to boost above safe levels. Redundant paths for output voltage sensing provide additional protection against output over-voltage. Over-voltage protection is implemented through two independent paths: VSENSE and HVSEN. The converter shuts down if either input senses a severe over-voltage condition. The output voltage can still remain below a safe limit if either sense path fails. The device is re-enabled when both sense inputs fall back into their normal ranges. At that time, the gate drive outputs will resume switching under PWM control. A low-level over-voltage on VSENSE does not trigger soft-start, but the COMP pin is discharged by an internal 2-kΩ resistance until the output voltage falls below the 2% hysteresis OV-clear threshold. A higher-level over-voltage on VSENSE additionally shuts off the gate-drive outputs until the OV clears, but still does not trigger a soft-start. However, an overvoltage detected on HVSEN does trigger a full soft-start and the COMP pin is fully discharged to 20 mV before the soft-start can begin.

8.3.15.2 Overcurrent Protection

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

The conventional current-sensing method uses a shunt resistor in series with each MOSFET source leg to sense the converter currents, resulting in multiple ground points and high power dissipation. Furthermore, since no current information is available when the MOSFETs are off, the source-resistor current-sensing method results in repeated turn-on of the MOSFETs during overcurrent (OC) conditions. Consequently, the converter may temporarily operate in continuous conduction mode (CCM) and may experience failures induced by excessive reverse-recovery currents in the boost diodes or other abnormal stresses.

The UCC28063A uses a single resistor to continuously sense the combined total inductor (input) current. This way, turn-on of the MOSFETs is completely avoided when the inductor currents are excessive. The gate drive to the MOSFETs is inhibited until total inductor current drops to near zero, precluding reverse-recovery-induced failures (these failures are most likely to occur when the ac-line recovers from a brownout condition).

The nominal OC threshold voltage during two-phase operation is -200 mV, which helps minimize losses. This threshold is automatically reduced to -166 mV during single-phase operation, either by detection of a phase failure or because PHB is driven below 0.8 V. Note that the single-phase threshold is not simply 1/2 of the dual-phase threshold, because the ratio of the single-phase peak current to the interleaved peak current is higher than 1/2.

An OC condition immediately turns off both gate-drive outputs, but does not trigger a soft-start and does not modify the error amplifier operation. The over-current condition is cleared when the total inductor current-sense voltage falls below the OC-clear threshold (-15 mV).

Following an over-current condition, both MOSFETs are turned on simultaneously once the input current drops to near zero. Because the two phase currents are temporarily operating in-phase, the current-sense resistance should be chosen so that OC protection is not triggered with twice the maximum current peak value of either phase in order to allow quick return to normal operation after an over-current event. Automatic phase-shift control will re-establish interleaving within a few switching cycles.

8.3.15.3 Open-Loop Protection

If the feedback loop is disconnected from the device, a 100-nA current source internal to the UCC28063A pulls the VSENSE pin voltage towards ground. When VSENSE falls below 1.20 V, the device becomes disabled. When disabled, the bias supply current decreases, both gate-drive outputs and COMP are actively pulled low, and a soft-start condition is initiated. The device is re-enabled when VSENSE rises above 1.25 V. At that time, the gate drive outputs will begin switching under soft-start PWM control.

If the feedback loop is disconnected from ground, the VSENSE voltage will be pulled high. When VSENSE rises above the 2nd-level over-voltage protection threshold, both gate drive outputs are shut off and COMP is actively pulled low. The device is re-enabled when VSENSE falls below the OV-clear threshold. The VSENSE input can tolerate a limited amount of current into the device under abnormally high input voltage conditions. Refer to the Absolute Maximum Ratings table near the beginning of this datasheet for details.

8.3.15.4 VCC Undervoltage Lock-Out (UVLO) Protection

VCC must rise above the turn-on threshold for the PWM to begin functioning. If VCC drops below the UVLO threshold during operation, both gate-drive outputs are actively pulled low, COMP is actively pulled low, and a soft-start condition is triggered. VCC must again rise above the turn-on threshold for the PWM function to restart in soft-start mode.

8.3.15.5 Phase-Fail Protection

The UCC28063A detects failure of either of the phases by monitoring the sequence of ZCD pulses. During normal two-phase operation, if one ZCD input remains idle for longer than approximately 12 ms while the other ZCD input switches normally, the over-current threshold is reduced and PWMCNTL goes to a high-impedance state, indicating that the PFC power stage is not operating correctly. During normal single-phase operation (PHB < 0.8 V), phase failure is not monitored. Also on the UCC28063A, phase failure is not monitored when COMP is below approximately 222 mV.

8.3.15.6 Thermal Shutdown Protection

Overloading of the gate-drive outputs, VREF, or both can dissipate excess power within the device which may raise the internal temperature of the circuits beyond a safe level. Even normal power dissipation can generate excess heat if the thermal impedance is too high or the ambient temperature is too high. When the UCC28063A detects an internal over-temperature condition it will shutdown the outputs and trigger a full soft-start condition. When the internal device junction temperature has cooled below the thermal hysteresis temperature, operation will resume under soft-start control.

8.3.15.7 AC-Line Brownout and Dropout Protections

See specific discussions for each topic in previous sections of this data sheet.

8.3.15.8 Fault Logic Diagram

图 33 depicts the fault-handling logic involving VSENSE, COMP, and several internal states.

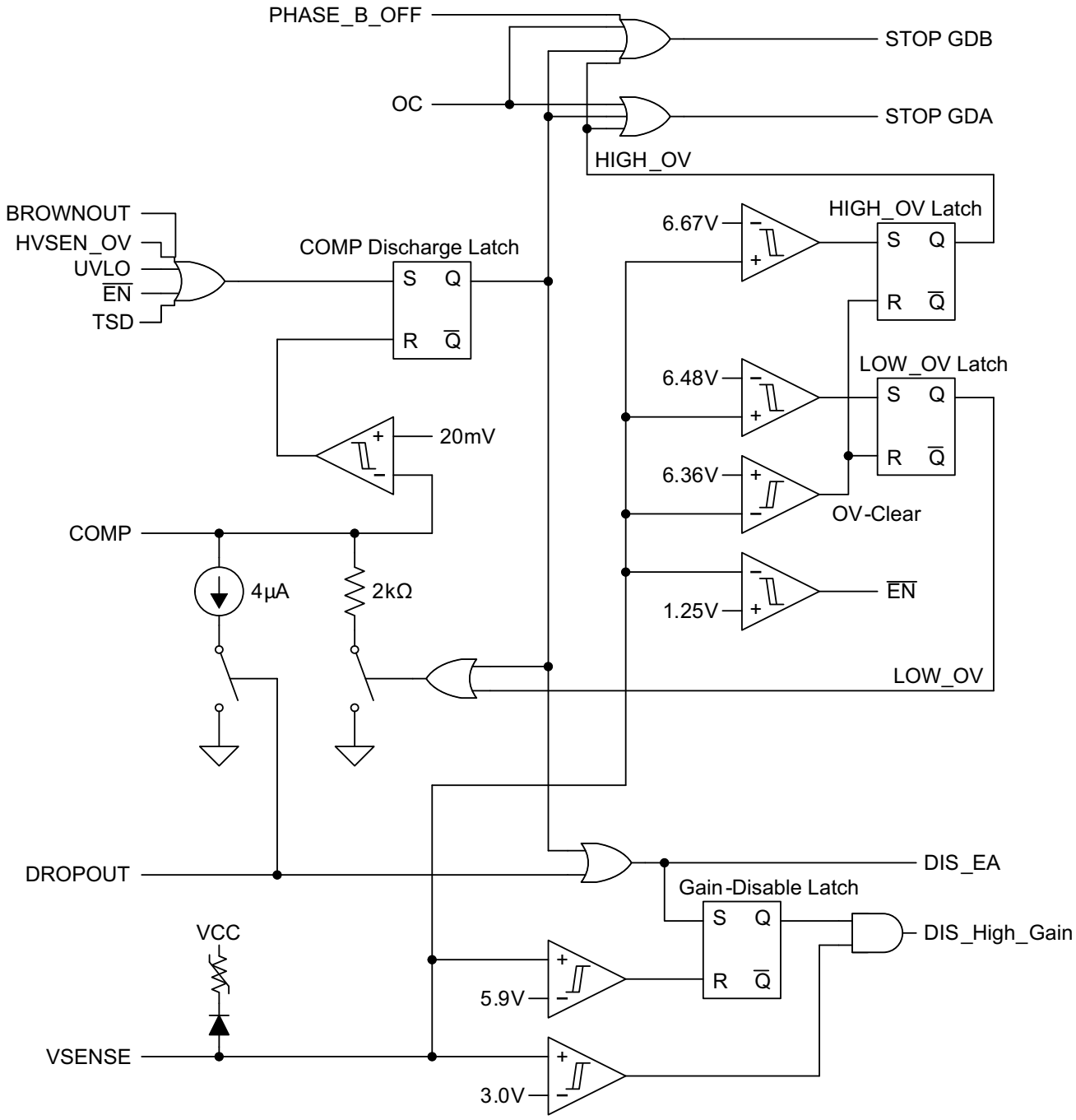


图 33. Fault Logic With VSENSE Detections and Error Amplifier Control

8.4 Device Functional Modes

The controller is primarily intended for set up as a dual phase interleaved PFC which utilizes inductor demagnetization information based on inductor sense winding voltages which are routed to ZCDA and ZCDB to trigger the start of a switching cycle.

The functionality may be extended in a couple of ways:

- **Phase-B Enable and Disable:** Phase-B may be *shed* by explicit user control or it may be set up as an automatic light load efficiency management feature. When the voltage applied to the PHB pin is below VPHBF threshold, Phase B and the Phase Fail Detector will be disabled. The commanded On-time for Phase-A will be doubled to minimize the output voltage transient which would otherwise occur. When the voltage on the PHB pin is greater than the VPHBR threshold, two phase mode is continuously enabled. Tie PHB to VREF pin for this mode. Alternatively PHB may be tied to the COMP pin for *automatic* phase shedding at light load.
- **PFC Stage Enable and Disable Control:** Controller operation is enabled when VSENSE voltage exceeds the 1.25-V enable threshold. The primary disable method should be by pulling VSENSE low by an open drain or open collector logic output. This will disable the outputs and significantly reduce VCC current. Releasing VSENSE will initiate a Soft-Start. Avoid any PCB traces which would couple any noise into this node.

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This control IC is generally applicable to the control of AC-DC power supplies which require Active Power Factor Correction off Universal AC line. Applications using this IC will generally meet the Class D equipment input current harmonics standards per EN61000-3-2. This standard applies to equipment with rated Powers higher than 75W. The IC brings two phase interleaved control capability to the Transition Mode Boost and hence will be generally a very good choice for cost optimized applications in the 150W to 800W space, or to even lower powers that wish to exploit the interleaving benefits of reduced filtering component size, lower profile solutions and distributed thermal management.

The *UCC28063EVM-723 300-W Interleaved PFC Pre-Regulator User's Guide* (SLUU512) describes an EVM design for a 300W Application.

This EVM has an associated Excel file to help automate calculations for its component choices available at SLUC292.

9.2 Typical Application

An example of the UCC28063A PFC controller in a two-phase interleaved, transition-mode PFC pre-regulator is shown in .

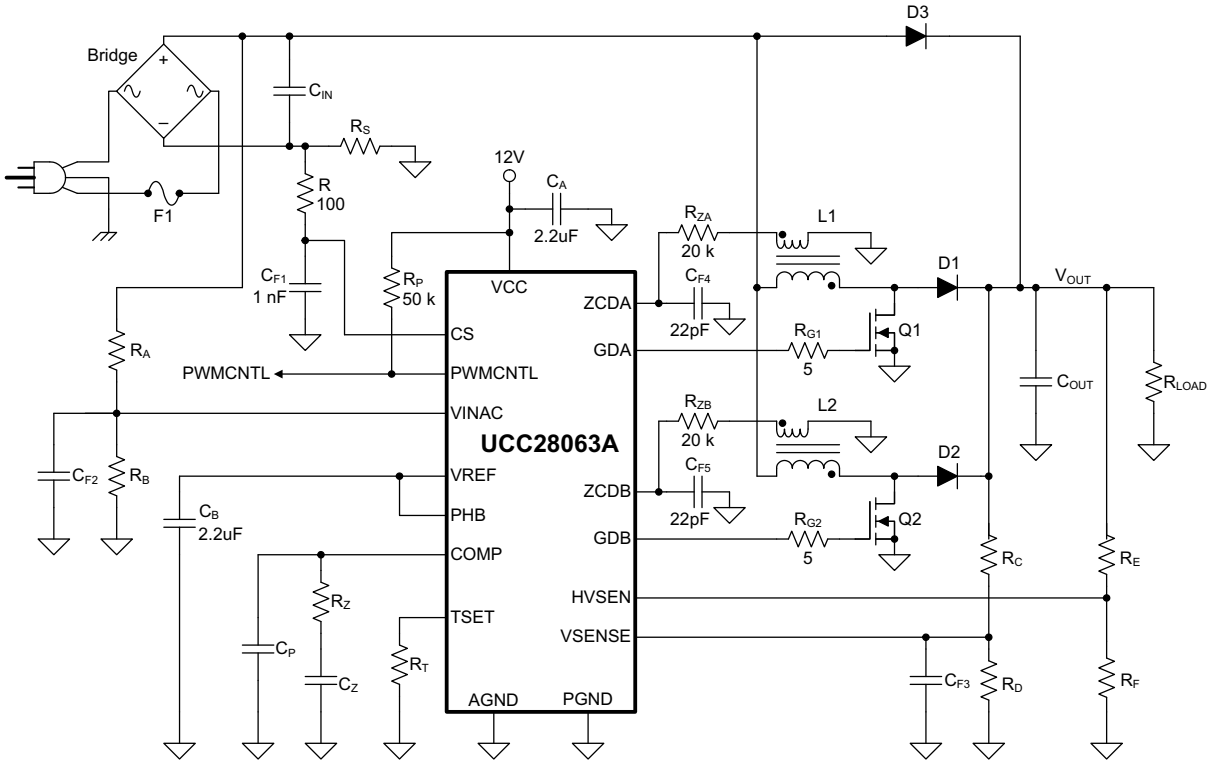


图 34. Typical Interleaved Transition-Mode PFC Pre-Regulator

Typical Application (接下页)

9.2.1 Design Requirements

The specifications for this design were chosen based on the power requirements of a typical 300-W LCD TV. These specifications are shown in 表 2.

表 2. Design Specifications

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	85 (VIN_MIN)		265 (VIN_MAX)	VRMS
V_{OUT}	Output voltage		390		V
f_{LINE}	AC-line frequency	47		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}				300	W
η	Full-load efficiency	92%			
f_{MIN}	Minimum switching frequency	45			kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The boost inductor is selected based on the inductor ripple current requirements at the peak of low line. Selecting the inductor requires calculating the boost converter duty cycle at the peak of low line ($D_{PEAK\_LOW\_LINE}$), as shown in 公式 18.

$$D_{PEAK\_LOW\_LINE} = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390\,V - 85\,V\sqrt{2}}{390\,V} \approx 0.69 \quad (18)$$

The minimum switching frequency of the converter (f_{MIN}) under low line conditions occurs at the peak of low line and is set between 25 kHz and 50 kHz to avoid audible noise. For this design example, f_{MIN} is set to 45 kHz. For a 2-phase interleaved design, L1 and L2 are determined as shown in 公式 19.

$$L1 = L2 = \frac{\eta \times V_{IN\_MIN}^{2} \times D_{PEAK\_LOW\_LINE}}{P_{OUT} \times f_{MIN}} = \frac{0.92(85\,V)^{2}0.69}{300\,W \times 45\,kHz} \approx 340\,\mu H \quad (19)$$

The inductor for this design would have a peak current (I_{LPEAK}) of 5.4 A, as shown in 公式 20, and an RMS current (I_{LRMS}) of 2.2 A, as shown in 公式 21.

$$I_{LPEAK} = \frac{P_{OUT}\sqrt{2}}{V_{IN\_MIN} \times \eta} = \frac{300\,W\sqrt{2}}{85\,V \times 0.92} \approx 5.4\,Apk \quad (20)$$

$$I_{LRMS} = \frac{I_{LPEAK}}{\sqrt{6}} = \frac{5.4\,A}{\sqrt{6}} \approx 2.2\,Arms \quad (21)$$

This converter uses constant on time (T_{ON}) and zero-current detection (ZCD) to set up the converter timing. Auxiliary windings on L1 and L2 detect when the inductor currents are zero. Selecting the turns ratio using 公式 22 ensures that there will be at least 2 V at the peak of high line to reset the ZCD comparator after every switching cycle.

The turns-ratio of each auxiliary winding is:

$$\frac{N_P}{N_s} = \frac{V_{OUT} - V_{IN\_MAX}\sqrt{2}}{2\,V} = \frac{390\,V - 265\,V\sqrt{2}}{2\,V} \approx 8 \quad (22)$$

9.2.2.2 ZCD Resistor Selection (R_{ZA}, R_{ZB})

The minimum value of the ZCD resistors is selected based on the internal clamps maximum current ratings of 3 mA, as shown in 公式 23.

$$R_{ZA} = R_{ZB} \geq \frac{V_{OUT} N_S}{N_P \times 3\,mA} = \frac{390\,V}{8 \times 3\,mA} \approx 16.3\,k\Omega \tag{23}$$

In this design the ZCD resistors are set to 20 kΩ, as shown in 公式 24.

$$R_{ZA} = R_{ZB} = 20\,k\Omega \tag{24}$$

9.2.2.3 HVSEN

The HVSEN pin programs the PWMCNTL output of the UCC28063A. The PWMCNTL open-drain output can be used to disable a downstream converter while the PFC output capacitor is charging. PWMCNTL starts high impedance and pulls to ground when HVSEN increases above 2.5 V. Setting the point where PWMCNTL becomes active requires a voltage divider from the boost voltage to the HVSEN pin to ground. 公式 25 to 公式 30 show how to set the PWMCNTL pin to activate when the output voltage is within 90% of its nominal value.

$$V_{OUT\_OK} = V_{OUT} \times 0.90 \approx 351\,V \tag{25}$$

Resistor R_E sets up the high side of the voltage divider and programs the hysteresis of the PWMCNTL signal. For this example, R_E was selected to provide 99 V of hysteresis, as shown in 公式 26. Three resistors in series were used to meet voltage requirements.

$$R_E = \frac{Hysteresis}{12\,\mu A} = \frac{99\,V}{12\,\mu A} = 8.25\,M\Omega \approx 3 \times 2.74\,M\Omega \tag{26}$$

Resistor R_F is used to program the PWMCNTL active threshold, as shown in 公式 27.

$$R_F = \frac{2.5\,V}{\frac{V_{OUT\_OK} - 2.5\,V}{R_E} - 12\,\mu A} = \frac{2.5\,V}{\frac{351\,V - 2.5\,V}{8.22\,M\Omega} - 12\,\mu A} = 82.25\,k\Omega \tag{27}$$

Select a standard resistor value for R_F.

$$R_F = 82.5\,k\Omega \tag{28}$$

This PWMCNTL output will remain active until a minimum output voltage (V_{OUT_MIN}) is reached, as shown in 公式 29.

$$V_{OUT\_MIN} = \frac{2.5\,V\left(R_E + R_F\right)}{R_F} = \frac{2.5\,V\left(8.22\,M\Omega + 82.5\,k\Omega\right)}{82.5\,k\Omega} \approx 252\,V \tag{29}$$

According to these resistor values, the FailSafe OVP threshold will be set according to 公式 30

$$V_{OV\_FAILSAFE} = \frac{4.87\,V\left(R_E + R_F\right)}{R_F} = \frac{4.87\,V\left(8.22\,M\Omega + 82.5\,k\Omega\right)}{82.5\,k\Omega} \approx 490\,V \tag{30}$$

9.2.2.4 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements, as shown in 公式 31.

$$C_{OUT} \geq \frac{2\frac{P_{OUT}}{\eta}\frac{1}{f_{LINE}}}{V_{OUT}^{\,2} - (V_{OUT\_MIN})^2} = \frac{2\frac{300\,W}{0.92}\frac{1}{47\,Hz}}{390\,V^2 - (252\,V)^2} \approx 156\,\mu F \tag{31}$$

Two 100-µF capacitors were used in parallel for the output capacitor.

$$C_{OUT} = 200\,\mu F \tag{32}$$

For this size capacitor, the low-frequency peak-to-peak output voltage ripple (V_{RIPPLE}) is approximately 14 V, as shown in 公式 33:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta} \frac{1}{V_{OUT} \times 4\pi \times f_{LINE} \times C_{OUT}} = \frac{2 \times 300\,W}{0.92 \times 390\,V \times 4\pi \times 47\,Hz \times 200\,\mu F} \approx 14\,Vppk \tag{33}$$

In addition to holdup requirements, a capacitor must be selected so that it can withstand the low-frequency RMS current (I_{COUT_100Hz}) and the high-frequency RMS current (I_{COUT_HF}); see 公式 34 to 公式 36. High-voltage electrolytic capacitors generally have both a low- and a high-frequency RMS current ratings on the product data sheets.

$$I_{COUT\_100Hz} = \frac{P_{OUT}}{V_{OUT} \times \eta \times \sqrt{2}} = \frac{300\,W}{390\,V \times 0.92 \times \sqrt{2}} = 0.591\,Arms \tag{34}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{P_{OUT}\,2\sqrt{2}}{2 \times \eta \times V_{IN\_MIN}} \sqrt{\frac{4\sqrt{2}V_{IN\_MIN}}{9\pi V_{OUT}}}\right)^2 - \left(I_{COUT\_100Hz}\right)^2} \tag{35}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{300\,W \times 2\sqrt{2}}{2 \times 0.92 \times 85\,V} \sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}}\right)^2 - \left(0.591A\right)^2} \approx 0.966\,Arms \tag{36}$$

9.2.2.5 Selecting (R_S) For Peak Current Limiting

The UCC28063A peak limit comparator senses the total input current and is used to protect the MOSFETs during inrush and over-load conditions. For reliability, the peak current limit (I_{PEAK}) threshold in this design is set for 120% of the nominal maximum current that will be observed during power up, as shown in 公式 37.

$$I_{PEAK} = \frac{2P_{OUT}\sqrt{2}(1.2)}{\eta \times V_{IN\_MIN}} = \frac{2 \times 300\,W\sqrt{2} \times 1.2}{0.92 \times 85\,V} \approx 13\,A \tag{37}$$

A standard 15-mΩ metal-film current-sense resistor will be used for current sensing, as shown in 公式 38. The estimated power loss of the current-sense resistor (P_{RS}) is less than 0.25 W during normal operation, as shown in 公式 39.

$$R_S = \frac{200\,mV}{I_{PEAK}} = \frac{200\,mV}{13\,A} \approx 15\,m\Omega \tag{38}$$

$$P_{RS} = \left(\frac{P_{OUT}}{V_{IN\_MIN} \times \eta}\right)^2 R_S = \left(\frac{300\,W}{85\,V \times 0.92}\right)^2 \times 15\,m\Omega \approx 0.22\ W \tag{39}$$

The most critical parameter in selecting a current-sense resistor is the surge rating. The resistor needs to withstand a short-circuit current larger than the current required to open the fuse (F1). I^2t (ampere-squared-seconds) is a measure of thermal energy resulting from current flow required to melt the fuse, where I^2t is equal to RMS current squared times the duration of the current flow in seconds. A 4-A fuse with an I^2t of 14 A^2s was chosen to protect the design from a short-circuit condition. To ensure the current-sense resistor has high-enough surge protection, a 15-mΩ, 500-mW, metal-strip resistor was chosen for the design. The resistor has a 2.5-W surge rating for 5 seconds. This result translates into 833 A^2s and has a high-enough I^2t rating to survive a short-circuit before the fuse opens, as described in 公式 40.

$$I^2t = \frac{2.5\,W}{0.015\,\Omega} \times 5s = 833\,A^2s \tag{40}$$

9.2.2.6 Power Semiconductor Selection (Q1, Q2, D1, D2)

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. Application Note SLUU138, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*, explains how to select power semiconductor components for transition-mode PFC pre-regulators.

The MOSFET (Q1, Q2) pulsed-drain maximum current is shown in 公式 41:

$$I_{DM} \geq I_{PEAK} = 13\,A \tag{41}$$

The MOSFET (Q1, Q2) RMS current calculation is shown in 公式 42:

$$I_{DS} = \frac{I_{PEAK}}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 2.3\,A \tag{42}$$

To meet the power requirements of the design, IRFB11N50A 500-V MOSFETs were chosen for Q1 and Q2.

The boost diode (D1, D2) RMS current is shown in 公式 43:

$$I_D = \frac{I_{PEAK}}{2}\sqrt{\frac{4\sqrt{2} \times V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 1.4\,A \tag{43}$$

To meet the power requirements of the design, MURS360T3, 600-V diodes were chosen for D1 and D2.

9.2.2.7 Brownout Protection

Resistor R_A and R_B are selected to activate brownout protection at ~75% of the specified minimum-operating input voltage. Resistor R_A programs the brownout hysteresis comparator, which is selected to provide 17 V (~12 V_{RMS}) of hysteresis. Calculations for R_A and R_B are shown in 公式 44 through 公式 47.

$$R_A = \frac{\text{Hysteresis}}{2\,\mu A} = \frac{17\,V}{2\,\mu A} = 8.5\,M\Omega \tag{44}$$

To meet voltage requirements, three 2.87-MΩ resistors were used in series for R_A.

$$R_A = 3 \times 2.87\,M\Omega = 8.61\,M\Omega \tag{45}$$

$$R_B = \frac{1.4\,V \times R_A}{V_{IN\_MIN} \times 0.75\sqrt{2} - 1.4\,V} = \frac{1.4\,V \times 8.61\,M\Omega}{85\,V \times 0.75\sqrt{2} - 1.4\,V} = 135.8\,k\Omega \tag{46}$$

Select a standard value for R_B.

$$R_B = 133\,k\Omega \tag{47}$$

In this design example, brownout becomes active (shuts down PFC) when the input drops below 66 V_{RMS} for longer than 440 ms and deactivates (restarts with a full soft start) when the input reaches 78 V_{RMS}.

9.2.2.8 Converter Timing

The maximum on-time T_{ON} depends on f_{MIN} as determined by 公式 48. To ensure proper operation, the timing must be set based on the highest boost inductance ($L1_{MAX}$) and output power (P_{OUT}). In this design example, the boost inductor could be as high as 390 µH. Calculate the timing resistor R_T as shown in 公式 49.

$$f_{MIN} = \frac{\eta \times \left(V_{IN\_MIN}\right)^2 \left(1 - \frac{V_{IN\_MIN} \times \sqrt{2}}{V_{OUT}}\right)}{P_{OUT} \times L1_{MAX}} = \frac{0.92 \times (85\,V)^2 \left(1 - \frac{85\,V \times \sqrt{2}}{390\,V}\right)}{300\,W \times 390\,\mu H} = 39.2\,kHz \tag{48}$$

$$R_T = \frac{133\,k\Omega\left(1 - \frac{V_{IN\_MIN} \times \sqrt{2}}{Vout}\right)}{4.85\,V \times \frac{4\,\mu s}{V} \times f_{MIN}} = \frac{133\,k\Omega\left(1 - \frac{85\,V \times \sqrt{2}}{390\,V}\right)}{4.85\,V \times \frac{4\,\mu s}{V} \times 39.2\,kHz} \approx 121\,k\Omega \tag{49}$$

This result sets the maximum frequency clamp (f_{MAX}), as shown in 公式 50, which improves efficiency at light load.

$$f_{MAX} = \frac{133\,k\Omega}{2\,\mu s \times R_T} = \frac{133\,k\Omega}{2\,\mu s \times 121\,k\Omega} \approx 550\,kHz \tag{50}$$

9.2.2.9 Programming V_{OUT}

Resistor R_C is selected to minimize loading on the power line when the PFC is disabled. Construct resistor R_C from two or more resistors in series to meet high-voltage requirements. Resistor R_D is then calculated based on R_C, the reference voltage, V_{REF}, and the required output voltage, V_{OUT}. Based on the values shown in 公式 51 to 公式 54, the primary output over-voltage protection threshold should be as shown in 公式 55:

$$R_C = 2.74\,M\Omega + 2.74\,M\Omega + 3.01\,M\Omega = 8.49\,M\Omega \quad (51)$$

$$V_{REF} = 6\ V \quad (52)$$

$$R_D = \frac{V_{REF} \times R_C}{V_{OUT} - V_{REF}} = \frac{6\,V \times 8.49\,M\Omega}{390\,V - 6\,V} = 132.7\,k\Omega \quad (53)$$

Select a standard value for R_D.

$$R_D = 133\,k\Omega \quad (54)$$

$$V_{OVP} = 6.48\,V \frac{R_C + R_D}{R_D} = 6.48\,V \frac{8.49\,M\Omega + 133\,k\Omega}{133\,k\Omega} = 420.1V \quad (55)$$

9.2.2.10 Voltage Loop Compensation

Resistor R_Z is sized to attenuate low-frequency ripple to less than 2% of the voltage amplifier output range. This value ensures good power factor and low harmonic distortion on the input current.

The transconductance amplifier small-signal gain is shown in 公式 56:

$$g_m = 50\,\mu S \quad (56)$$

The voltage-divider feedback gain is shown in 公式 57:

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6\,V}{390\,V} \approx 0.015 \quad (57)$$

The value of R_Z is calculated as shown in 公式 58:

$$R_Z = \frac{100\,mV}{V_{RIPPLE} \times H \times g_m} = \frac{100\,mV}{14\,V \times 0.015 \times 50\,\mu S} = 9.52\ k\Omega \quad (58)$$

C_Z is then set to add 45° phase margin at 1/5th of the line frequency, as shown in 公式 59:

$$C_Z = \frac{1}{2\pi \times \frac{f_{LINE}}{5} \times R_Z} = \frac{1}{2\pi \times \frac{47\,Hz}{5} \times 9.52\,k\Omega} = 1.78\,\mu F \quad (59)$$

C_P is sized to attenuate high-frequency switching noise, as shown in 公式 60:

$$C_p = \frac{1}{2\pi \times \frac{f_{MIN}}{2} \times R_Z} = \frac{1}{2\pi \times \frac{45\,kHz}{2} \times 9.52\,k\Omega} = 770\,pF \quad (60)$$

Standard values should be chosen for R_Z, C_Z and C_P, as shown in 公式 61 to 公式 63.

$$R_Z = 9.53\,k\Omega \quad (61)$$

$$C_Z = 2.2\,\mu F \quad (62)$$

$$C_P = 820\,pF \quad (63)$$

9.2.3 Application Curves

Refer to *UCC28063EVM-723 300-W Interleaved PFC Pre-Regulator EVM User's Guide*, SLUU512, for more implementation details and application curves.

9.2.3.1 Input Ripple Current Cancellation with Natural Interleaving

图 35 through 图 37 show the input current (M1= IL1 + IL2), Inductor Ripple Currents (IL1, IL2) versus rectified line voltage. From these graphs, it can be observed that natural interleaving reduces the overall magnitude of input (and output) ripple current caused by the individual inductor current ripples.

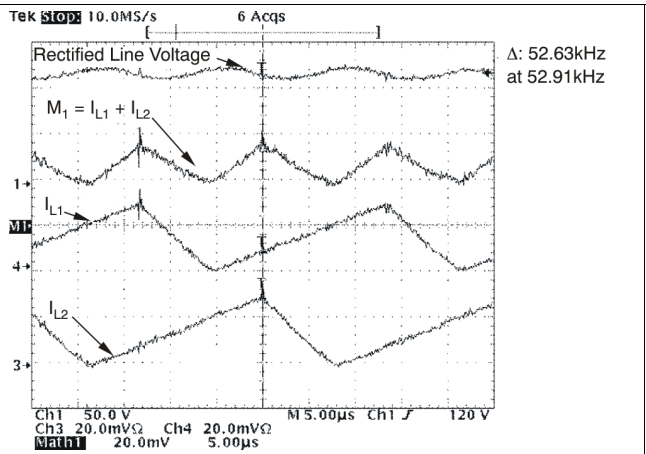


图 35. Inductor and Input Ripple Current at 85 V_{RMS} at Peak of Line Voltage

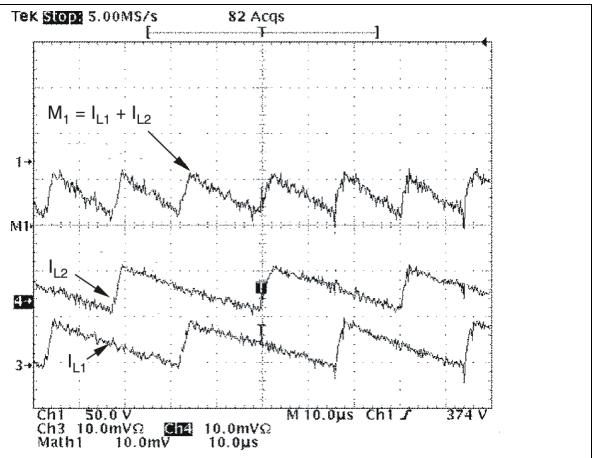


图 36. Inductor and Input Ripple Current at 265 V_{RMS} Input at Peak Line Voltage

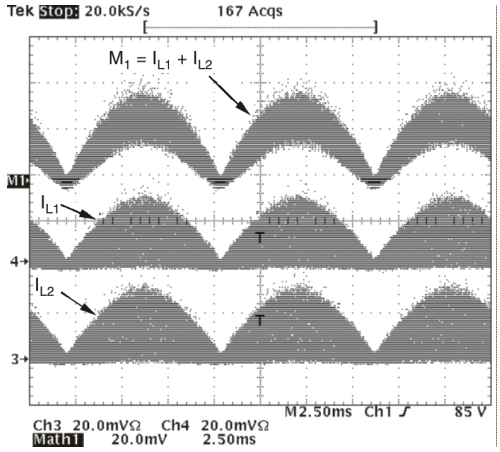


图 37. Inductor and Input Ripple Current at V_{IN} = 85 V_{RMS}, P_{OUT} = 300 W

9.2.3.2 Brownout Protection

The UCC28063A has a brownout protection that shuts down both gate drives (GDA and GDB) when the VINAC pin detects that the RMS input voltage is too low. This EVM was designed to go into a brownout state when the line drops below 64 VRMS. Once the UCC28063A control device has determined that the input is in a brownout condition, a 400-ms timer starts to allow the line to recover before shutting down the gate drivers. After 400 ms of brownout, both gate drivers turn off, as shown in 图 38.

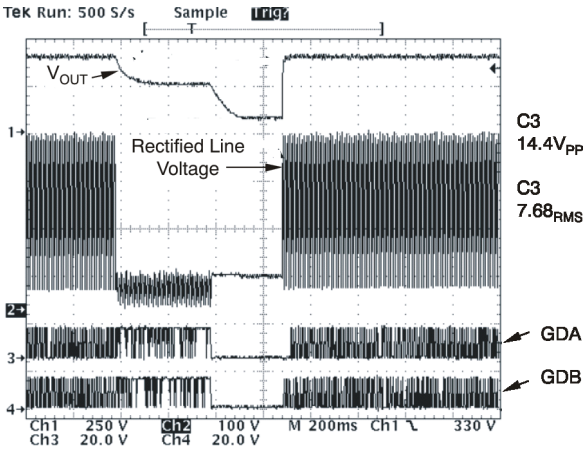


图 38. UCC28063A Response to a Line Brownout Event at 265 V_{RMS}

10 Power Supply Recommendations

The IC receives all of its power through the VCC pin. This voltage should be as well regulated as possible through all of the operating conditions of the PFC stage. Consider creating the steady state bias for this stage from a downstream DC:DC stage which will in general be able to provide a bias winding with very well regulated voltage. This strategy will enhance the overall efficiency of the bias generation. A lower efficiency alternative will be to consider a series connected Fixed Positive Voltage Regulator such as the UA78L15A.

For all normal and abnormal operating conditions it is critically important that VCC remains within its Recommended Operating Range for both Voltage and Input Current. VCC overvoltage may cause excessive power dissipation in the internal voltage clamp and undervoltage may cause inadequate drive levels for power MOSFETs, UVLO events (causing interrupted PFC operation) or inadequate headroom for the various on-chip linear regulators and references.

Note also that the high RMS and peak currents required for the MOSFET gate drives are provided through the IC 13.5-V linear regulator, which does not have provision for the addition of external decoupling capacitance. For higher Powers, very high Q_G power MOSFETs or high switching frequencies, consider using external driver transistors, local to the power MOSFETs. These will reduce the IC operating temperature and ensure that the VCC maximum input current rating is not exceeded.

Use decoupling capacitances between VREF and AGND and between VCC and PGND which are as local as possible to the IC. These should have some ceramic capacitance which will provide very low ESR. PGND and AGND should ideally be star connected at the control IC so that there is negligible DC or high frequency AC voltage difference between PGND and AGND. Use values for decoupling capacitors similar to or a little larger than those used in the EVM.

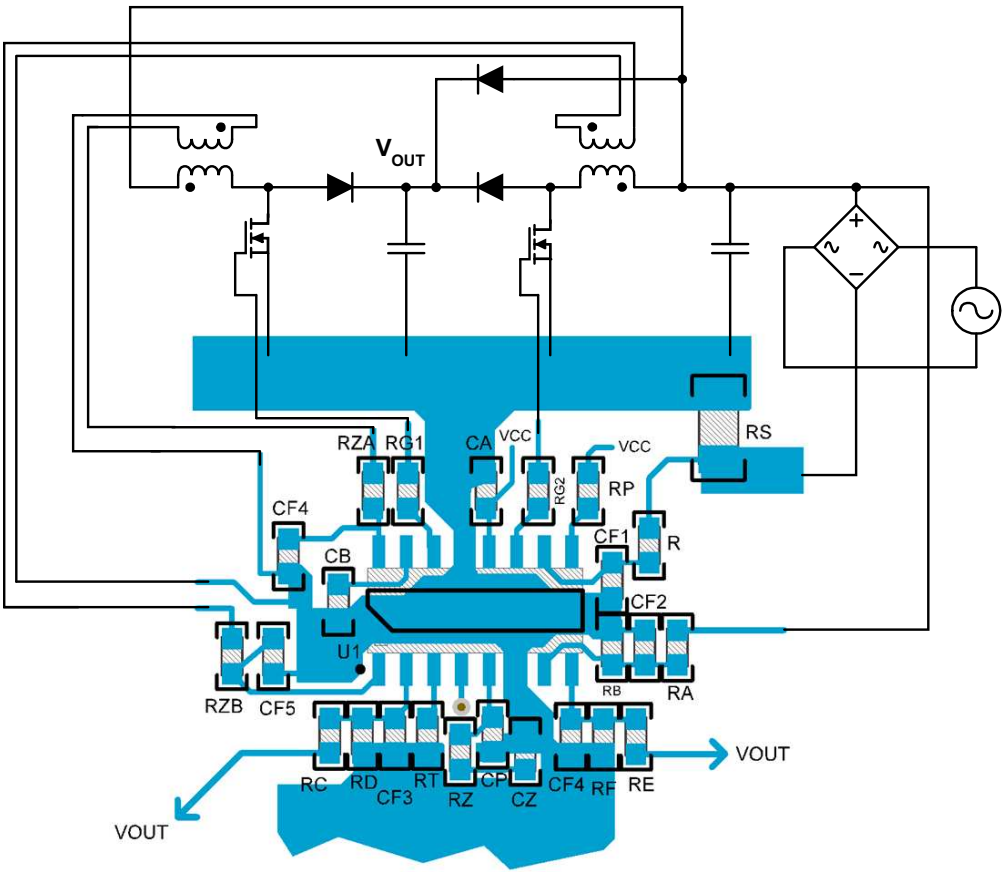
Pay close attention to start-up and shutdown VCC bias bootstrap arrangements so that these provide adequate regulated bias power as early as possible during power application and as late as possible during power removal. Ensure that these start-up bias bootstrap circuits do not cause unnecessary steady-state power drain.

11 Layout

11.1 Layout Guidelines

Interleaved transition-mode PFC system architecture dramatically reduces input and output ripple current, allowing the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the input and output filter capacitors should be located after the two phase currents are combined together. Similar to other power management devices, when laying out the printed circuit board (PCB) it is important to use star grounding techniques and keep filter capacitors as close to device ground as possible. To minimize the interference caused by capacitive coupling from the boost inductor, the device should be located at least 1 in (25.4 mm) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. Because of the precise timing requirement, timing-setting resistor R_T should be placed as close as possible to the TSET pin and returned to the analog ground pin with the shortest possible path. See 图 39 for a recommended component placement and layout.

11.2 Layout Example



PHB and VREF pins are connected by a jumper on the back of the board.

图 39. Recommended PCB Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 相关器件

表 3 列出了几个与 UCC28063A 特性相似的 TI 器件。

表 3. TI 相关器件

器件	说明
UCC28050/51	面向中低功率应用的转换模式 PFC 控制器
UCC28019	8 引脚连续导通模式 (CCM) PFC 控制器（具有转换率校正电流）
UCC28019A	8 引脚连续导通模式 (CCM) PFC 控制器（具有两级电压误差增益）
UCC28060	两相交错式转换模式 PFC 控制器（输入电压范围增益可变）
UCC28061	两相交错式转换模式 pfc 控制器（输入电压范围增益不变）
UCC28070	两相交错式 CCM（平均电流模式）PFC 控制器
UCC28063	两相交错式转换模式 PFC 控制器（具有改进的可闻噪声性能）

12.1.2 器件命名规则

12.1.2.1 详细引脚说明

模拟接地：将模拟信号旁路电容、补偿元件以及模拟信号回路连接至该引脚。 将模拟接地和电源接地连接在一起，以防止功率元件的高电流噪声信号干扰到低电流模拟电路。

误差放大器输出：误差放大器是一种跨导放大器，因此该输出是高阻抗电流源。 在该引脚与 AGND 之间连接稳压环路补偿元件。 栅极驱动输出的导通时间与该引脚电压和 125mV 左右偏移量的差值成正比。 正常工作期间，当 VSENSE 上的信号干扰较小时，误差放大器可保持 55μS 的跨导；而当 VSENSE 偏离 VSENSEreg 超过 ±5% 时，跨导将转变为 290μS 左右。 在交流线路压降情况期间，将禁用误差放大器，并且在此期间内部 4μA 源将使 COMP 放电。 在基于 VSENSE 的 OV 事件期间，COMP 与 GND 之间应连接一个 2kΩ 的内部电阻，直到 OV 条件清除。 在软启动触发事件（UVLO、禁用、欠压、HVSEN 过压、或热关断）期间，将禁用误差放大器输出，并通过一个 2kΩ 的内部电阻将 COMP 拉为低电平。 软启动状态在触发事件清除并且 COMP 已放电至 20mV 以下后才开始，这样可确保电路以较低的 COMP 电压与较短的导通时间重新启动。 （不要将 COMP 连接至低阻抗源，否则会导致 COMP 无法降至 20mV 以下。）在软启动期间，只要 VSENSE < VREF/2，便会启用误差放大器高跨导，并且 COMP 电流为 -125μA。当 VSENSE 超过 VREF/2 时，将禁用高增益，而只提供小信号增益能力，最大 COMP 电流约为 –16μA。 当 VSENSE > 0.983VREF（约 5.9V）之后，器件将恢复正常工作。

电流感测输入：将电流感测电阻和二极管桥的负引脚连接至该引脚。 将电流感测电阻回路通过一条独立走线连接至 AGND 引脚。 随着输入电流的增大，CS 上的负电压会越来越高。 当 CS 上的负电压超过 CS 上升阈值（两相操作中约为 -200mV，单相和相位故障情况下约为 -167mV）时，这种逐周期过流保护会将两个栅极驱动器输出 (GDx) 关断，从而限制输入电流。 栅极驱动输出将保持低电平，直到 CS 降至 CS 下降阈值（约 -15mV）。在任一 GDx 输出的上升沿和下降沿之后约 100ns 的时间内，电流感测是无效的。 这样可以滤掉来自栅极驱动电流的噪声，或者在电感电流从功率 FET 切换至升压二极管时产生的噪声。 在大多数情况下，无需进行额外的电流感测滤波。 如果必须进行外部滤波，或者为防止因交流浪涌情况导致 CS 引脚上的负电压过大，建议在电流感测电阻与 CS 引脚之间串联一个电阻。 由于存在 CS 偏置电流，该外部电阻应小于 100Ω 以保持精度。

通道 A 和通道 B 栅极驱动输出：将这些引脚通过可行的最短连接与每相的功率 FET 的栅极相连。 如果连接时需要使用超过 0.5 英寸 (12.6mm) 的走线，则可能会因为走线串联电感的原因而产生振铃。 这种振铃可通过为 GDA 和 GDB 串联一个低值电阻进行阻尼。

高电压输出感测：UCC28063A 具备故障安全 OVP，因此任何一种故障都不会导致输出电压超过安全电平上限。输出过压由 VSENSE 和 HVSEN 共同监视，不过当这两个引脚的电压超过各自的过压阈值时，二者的动作有所不同。 使用两个引脚来监视过压情况，可提供冗余保护和容错功能。 当 HVSEN 超过其过压阈值时，会触发一次控制器完全软启动。 当 HVSEN 引脚的电压在其工作区域内时，HVSEN 还可用于使能下游功率转换器。 当 HVSEN 大于 2.5V 时，PWMCNTL 输出可驱动为低电平（假设不存在其他故障）。 当 HVSEN 降至 2.5V 以下时，PWMCNTL 输出呈高阻态。 针对所需过压阈值和电源正常阈值选择 HVSEN 分压比。 根据滞后电流为所需的电源正常滞后选择 HVSEN 分压阻抗。 正常工作期间，HVSEN 不得低于 0.8V。当 HVSEN 低于 0.8V 时，UCC28063A 将进入一种特殊的测试模式（仅供出厂测试使用）。 建议在 HVSEN 与 AGND 之间连接一个旁路电容，以便滤除噪声并避免出现错误的过压关断。

相位 B 启用/禁用：当施加到该引脚上的电压低于相位 B 启用阈值时，将禁用升压转换器的相位 B 和相位故障检测器。 当禁用相位 B 时，定义的相位 A 导通时间会立即翻一倍，这有助于在相位管理瞬变期间保持 COMP 电压恒定。 利用 PHB 引脚，用户可以根据需要添加外部相位管理控制电路。 如需禁用相位管理，将 PHB 引脚连接至 VREF 引脚即可。

PWM 控制输出：此开漏输出在 HVSEN 处于 HVSEN 正常区域内 (HVSEN > 2.5V) 时为低电平，不存在故障安全 OV，并且在两相模式下工作时不存在相位故障条件（请参见 PHB 引脚）。 否则，PWMCNTL 呈高阻态。

定时设置：PWM 导通时间编程输入。 TSET 与 AGND 之间连接有一个电阻，用于设置导通时间与 COMP 电压以及栅极驱动输出的最短开关周期。

偏置电源输入：将该引脚连接到介于 14V 和 21V 之间的受控偏置电源。并在该引脚与 PGND 之间通过可能的最短电路板走线连接一个 0.1μF 或更大的陶瓷旁路电容。 该偏置电源为器件内的所有电路供电，并且必须能够提供稳态直流电流与瞬时功率 MOSFET 栅极充电电流。 欠压闭锁 (UVLO) 或待机状态 (VSENSE < 1.25V) 下的输入偏置电流非常低。

输入交流电压感测：正常工作期间，该引脚连接至跨接于经整流输入市电电源两端的分压器。 当 VINAC 上的电压低于欠压阈值的时间超过欠压滤波时间时，器件将进入欠压模式，同时将禁用两个输出驱动器并触发完全软启动。针对所需欠压阈值选择输入电压分压比。 根据滞后电流为所需欠压滞后选择分压阻抗。 当 VINAC 低于压降阈值的时间超过压降滤波时间时，将触发压降条件。 在压降状态期间，误差放大器将被禁用，同时 4μA 内部电流源将使 COMP 放电。 当 VINAC 超过压降清除阈值时，压降状态会立即清除，同时器件恢复正常工作。

电压参考输出：在该引脚与 AGND 之间连接一个 0.1μF 或更大的陶瓷旁路电容。 在 UVLO 和 VSENSE 禁用期间，VREF 将关断以节省偏置电流并提高待机效率。 该参考输出可用于偏置其他所需非脉冲总电源电流不到几毫安的电路。

输出直流电压感测：将该引脚连接至跨接于电源转换器输出两端的分压器。 在闭环系统中，VSENSE 上的电压被稳压在误差放大器参考电压上。 针对所需输出电压选择输出电压分压比。 将该分压器的接地端通过一条独立的短走线连接至模拟接地 (AGND)，以便获得最佳输出调节精度和噪声抑制性能。 当 VSENSE 电压超过 1.25V 使能阈值时，可以使能控制器操作。 VSENSE 可通过开漏逻辑输出，或者与低泄漏二极管串联的 > 6V 的逻辑输出拉为低电平，以禁用输出并降低 VCC 电流。 此输入可检测到两个级别的输出过压。 当 VSENSE 超过第一级过压保护阈值 V_{LOW_OV} 时，会对 COMP 应用一个 2kΩ 内部电阻，以便快速缩短栅极驱动导通时间。 当 VSENSE 继续升高并超过第二级阈值 V_{HIGH_OV} 时，将立即锁闭 GDA 和 GDB。 当 VSENSE 低于 OV 清除阈值时，将清除该锁闭操作。 当 VSENSE 断开时，开环保护会提供一个内部电流源以将 VSENSE 拉为低电平，从而禁用控制器并触发软启动条件。

零电流检测输入：这些输入用于在各相位的升压电感电流变为零时检测负向边沿。 这些输入被钳位在 0V 和 3V 之间。每个引脚均通过一个限流电阻连接至对应升压电感的过零检测 (ZCD) 绕组。 所选电阻值应将钳位电流限制在 ±3mA 以内。 必须对电感绕组的极性加以适当排布，以便当电感电流衰减到零时，ZCD 电压能够下降。 当电感电流降为零时，ZCD 输入必须降至下降阈值（约 1V）以下，以使栅极驱动输出上升。 随后，当功率 MOSFET 关断时，ZCD 输入必须升至上升阈值（约 1.7V）以上，以定义另一个 ZCD 下降沿的逻辑。

12.2 文档支持

12.2.1 相关文档

这些参考资料、设计工具以及附加参考资料的链接（包括设计软件）均可在 www.power.ti.com 网站上找到。

- 评估模块《*UCC28063EVM 300W 交错式 PFC 前置稳压器*》（文献编号：SLUU512）
- 应用手册 《*UCC38050 100W 临界导通功率因数校正 (PFC) 前置稳压器*》（文献编号：SLUU138）

12.3 商标

DLP, Natural Interleaving are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28063AD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A
UCC28063AD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A
UCC28063AD.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A
UCC28063ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A
UCC28063ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A
UCC28063ADR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

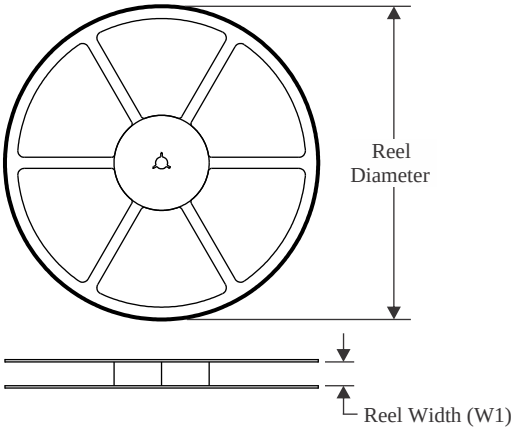
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

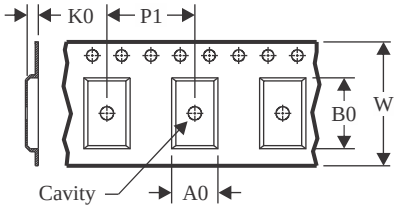
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

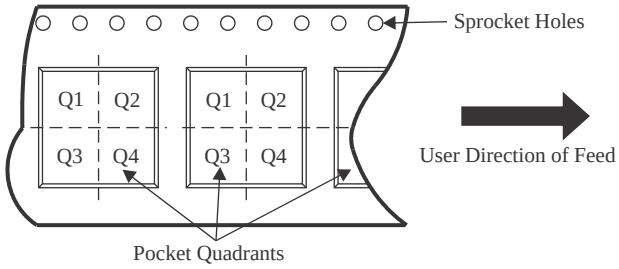


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

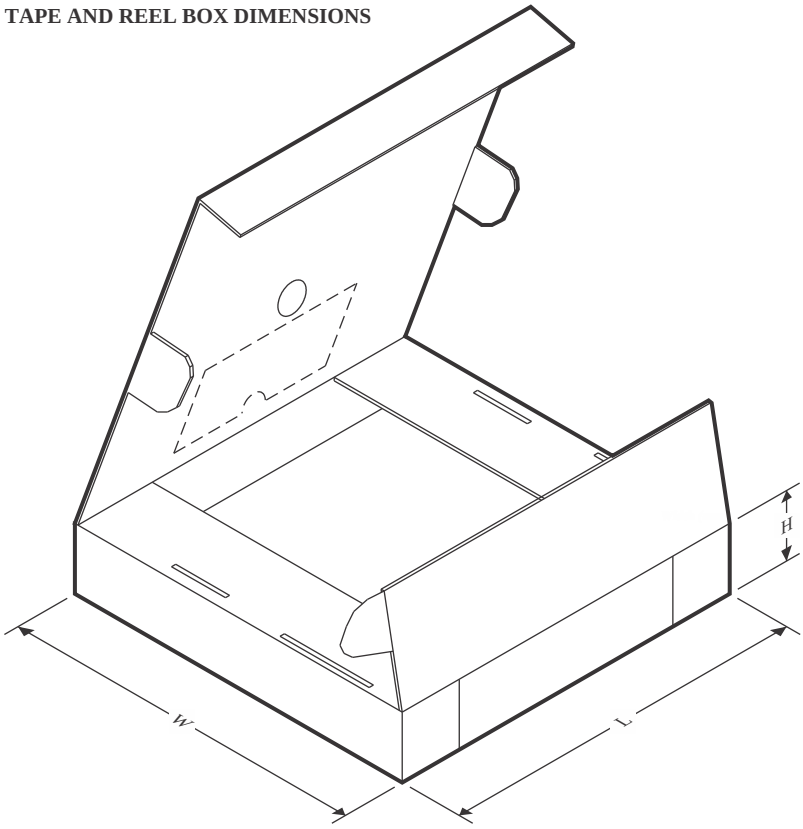
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28063ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

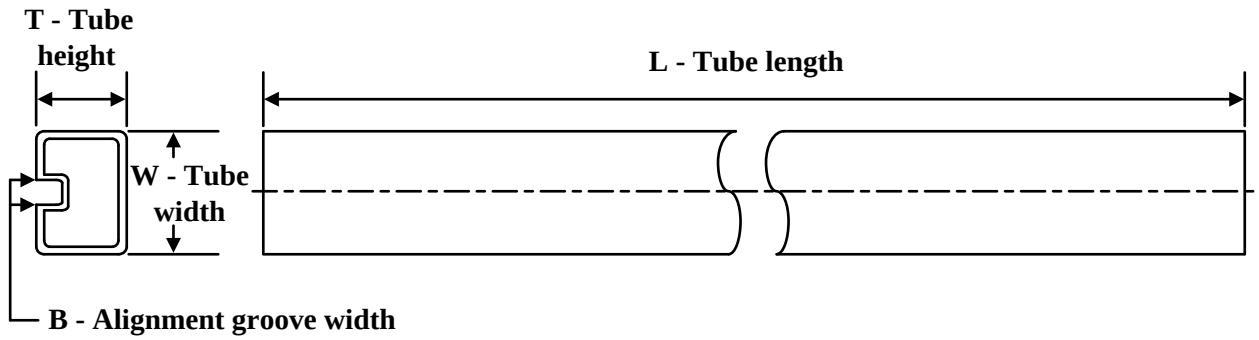
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28063ADR	SOIC	D	16	2500	353.0	353.0	32.0

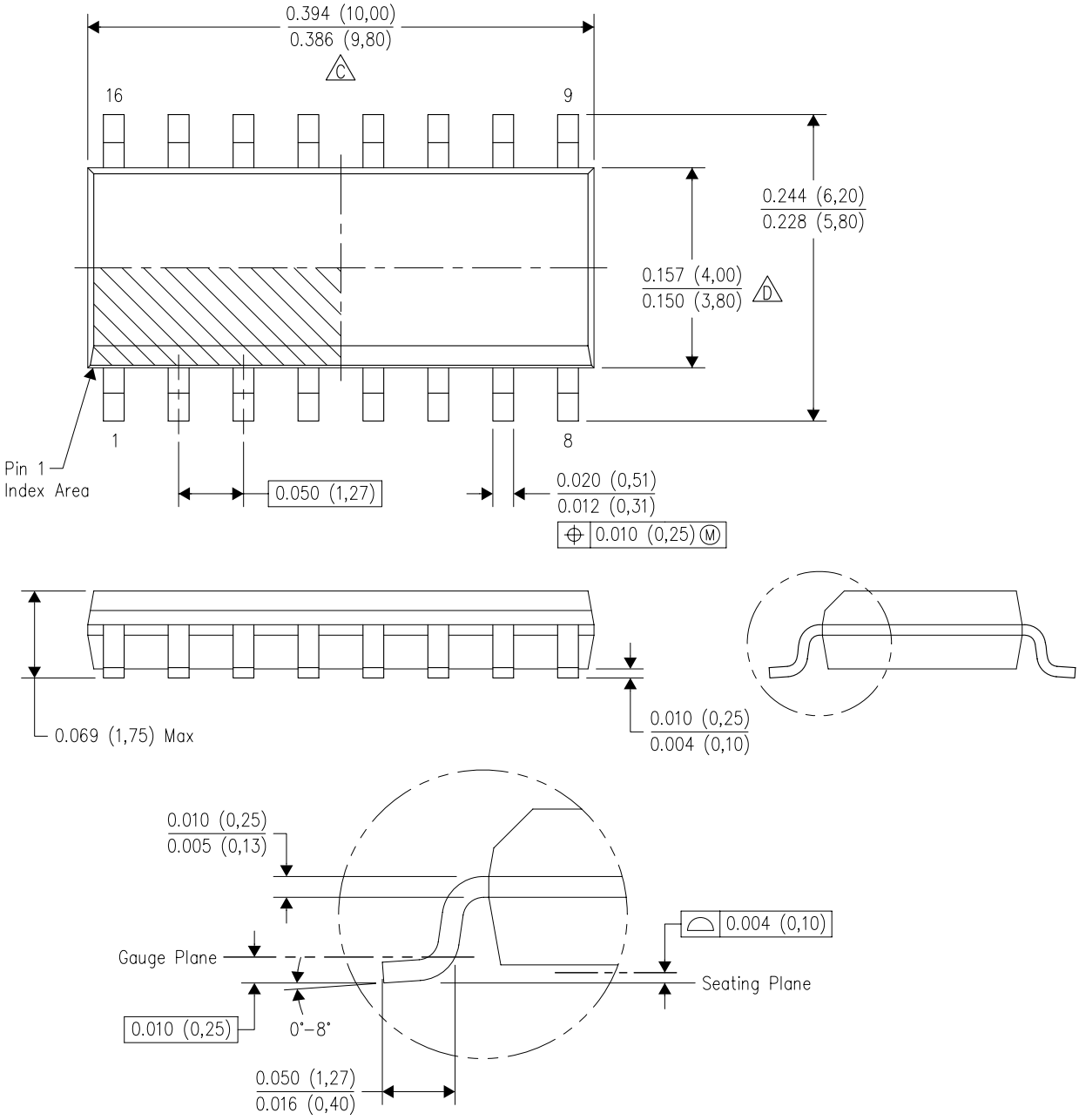
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28063AD	D	SOIC	16	40	507	8	3940	4.32
UCC28063AD.A	D	SOIC	16	40	507	8	3940	4.32
UCC28063AD.B	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

重要通知和免责声明

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