

# UCC23511-Q1 1.5A 拉电流、2A 灌电流、5.7kV<sub>RMS</sub> 光兼容 单通道隔离式栅极驱动器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
- 具有光兼容输入的 5.7kV<sub>RMS</sub> 单通道隔离式栅极驱动器
- 适用于光隔离式栅极驱动器的引脚对引脚普适版升级
- 1.5A 拉电流/2A 灌电流，峰值输出电流
- 最高 33V 输出驱动器电源电压
- 12V VCC UVLO
- 轨到轨输出
- 105ns (最大值) 传播延迟
- 25ns (最大值) 器件对器件延迟匹配
- 35ns (最大值) 脉宽失真度
- 150kV/μs (最小值) 共模瞬态抗扰度 (CMTI)
- 隔离栅寿命大于 50 年
- 输入级具有 13V 反极性电压处理能力，支持互锁
- 扩展型 SO-6 封装，爬电距离和间隙大于 8.5mm
- 运行结温  $T_J$ ：-40°C 至 +150°C
- 提供功能安全**
  - 可帮助进行功能安全系统设计的文档
- 安全相关认证：
  - 符合 UL 1577 标准且长达 1 分钟的 5.7kV<sub>RMS</sub> 隔离
  - 符合 DIN V VDE V0884-11:2017-01 标准的 8000V<sub>PK</sub> 增强型隔离 (进展中)

## 2 应用

- 适用于电动汽车的牵引逆变器
- 车载充电器和直流充电站
- HVAC
- 加热器
- 工业电机控制驱动

## 3 说明

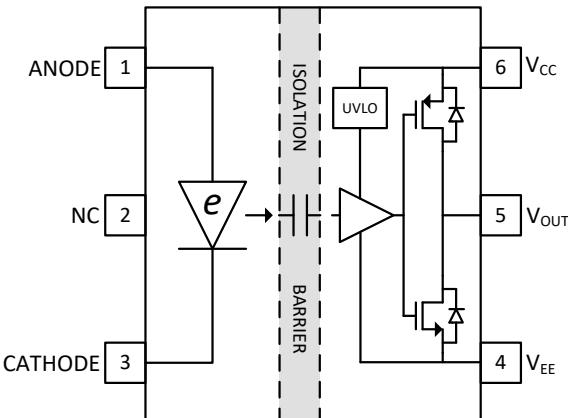
UCC23511-Q1 是一款适用于 IGBT、MOSFET 和 SiC MOSFET 的光兼容单通道隔离式栅极驱动器，具有 1.5A 峰值拉电流和 2A 峰值灌电流以及 5.7kV<sub>RMS</sub> 增强型隔离额定值。33V 的高电源电压范围允许使用双极电源来有效驱动 IGBT 和 SiC 功率 FET。UCC23511-Q1 可以驱动低侧和高侧功率 FET。与基于光耦合器的标准栅极驱动器相比，此器件的主要特性和特征可显著提高性能和可靠性，同时在原理图和布局设计中保持引脚对引脚兼容性。性能亮点包括高共模瞬态抗扰度 (CMTI)、低传播延迟和小脉宽失真。严格的过程控制可实现较小的器件对器件偏移。输入级是仿真二极管 (ediode)，这意味着与光耦合器栅极驱动器中传统的 LED 相比，可靠性和老化特性更为出色。该器件采用

扩展型 SO6 封装，爬电距离和间隙大于 8.5mm，塑封材料 (材料组 I) 的相对漏电起痕指数 (CTI) 大于 600V。UCC23511-Q1 具有高性能和高可靠性，因此非常适合用于汽车电机驱动器，例如牵引逆变器、车载充电器、直流充电站以及汽车暖通空调和加热系统。更高的工作温度为传统光耦合器以前无法支持的应用开辟了机会。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
UCC23511-Q1	扩展型 SO-6	7.5mm x 4.68mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



UCC23511-Q1 (SO6) 的功能方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 [www.ti.com](http://www.ti.com)，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

English Data Sheet: [SLUSE93](#)

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision * (August 2020) to Revision A (March 2021)</b>	<b>Page</b>
• 将销售状态从“预告信息”更改为“量产数据” .....	<b>1</b>

## 5 Pin Configuration and Function

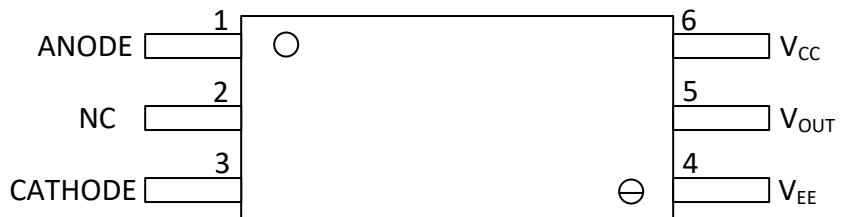


图 5-1. UCC23511-Q1 Package SO-6 Top View

## Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
ANODE	1	I	Anode
CATHODE	3	I	Cathode
NC	2	-	No Connection
V <sub>CC</sub>	6	P	Positive output supply rail
V <sub>EE</sub>	4	P	Negative output supply rail
V <sub>OUT</sub>	5	O	Gate-drive output

(1) P = Power, G = Ground, I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Average Input Current	$I_F(\text{AVG})$	-	25	mA
Peak Transient Input Current	$I_F(\text{TRAN})$ <1us pulse, 300pps		1	A
Reverse Input Voltage	$V_R(\text{MAX})$		14	V
Output supply voltage	$V_{CC} - V_{EE}$	-0.3	35	V
Output signal voltage	$V_{OUT} - V_{CC}$		0.3	V
Output signal voltage	$V_{OUT} - V_{EE}$	-0.3		V
Junction temperature	$T_J$ <sup>(2)</sup>	-40	150	°C
Storage temperature	$T_{\text{stg}}$	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) To maintain the recommended operating conditions for  $T_J$ , see the [# 6.4](#) section.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(\text{ESD})}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Output Supply Voltage( $V_{CC} - V_{EE}$ )	14	33		V
$I_F$ (ON)	Input Diode Forward Current (Diode "ON")	7	16		mA
$V_F$ (OFF)	Anode voltage - Cathode voltage (Diode "OFF")	-13	0.9		V
$T_J$	Junction temperature	-40	150		°C
$T_A$	Ambient temperature	-40	125		°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC23511-Q1	UNIT
		SO6	
		6 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	66.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	29.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	60.8	°C/W

(1) For more information about traditional and new thermal metrics, see the <http://www.ti.com/lit/SPRA953> application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$	Maximum power dissipation on input and output <sup>(1)</sup>	$V_{CC} = 20$ V, $I_F = 10$ mA, 10-kHz, 50% duty cycle, square wave, 180-nF load, $T_A = 25^\circ\text{C}$			750	mW
$P_{D1}$	Maximum input power dissipation <sup>(2)</sup>				10	mW
$P_{D2}$	Maximum output power dissipation				740	mW

(1) Derate at 6 mW/ $^\circ\text{C}$  above 25 $^\circ\text{C}$  ambient temperature

(2) Recommended maximum  $P_{D1} = 40$  mW. Absolute maximum  $P_{D1} = 55$  mW

## 6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFIC ATION	UNIT
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	>8.5	mm
CPG	External Creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	>8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 600 \text{ V}_{\text{RMS}}$	I-IV	
		Rated mains voltage $\leq 1000 \text{ V}_{\text{RMS}}$	I-III	
<b>DIN V VDE 0884-11 (VDE V 0884-11)<sup>(2)</sup></b>				
$V_{\text{IORM}}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	$\text{V}_{\text{PK}}$
$V_{\text{IOWM}}$	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1	1500	$\text{V}_{\text{RMS}}$
		DC voltage	2121	$\text{V}_{\text{DC}}$
$V_{\text{IOTM}}$	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60 \text{ sec}$ (qualification) $V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1 \text{ s}$ (100% production)	8000	$\text{V}_{\text{PK}}$
$V_{\text{IOSM}}$	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368, 1.2/50 ms waveform, $V_{\text{TEST}} = 1.6 \times V_{\text{IOSM}} = 12800 \text{ V}_{\text{PK}}$ (qualification)	8000	$\text{V}_{\text{PK}}$
$q_{\text{pd}}$	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60 \text{ s}$ ; $V_{\text{pd(m)}} = 1.2 \times V_{\text{IORM}} = 1800 \text{ V}_{\text{PK}}$ , $t_{\text{m}} = 10 \text{ s}$	$\leq 5$	pC
		Method a: After environmental tests subgroup 1, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60 \text{ s}$ ; $V_{\text{pd(m)}} = 1.6 \times V_{\text{IORM}} = 2400 \text{ V}_{\text{PK}}$ , $t_{\text{m}} = 10 \text{ s}$	$\leq 5$	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 1 \text{ s}$ ; $V_{\text{pd(m)}} = 1.875 \times V_{\text{IORM}} = 2813 \text{ V}_{\text{PK}}$ , $t_{\text{m}} = 1 \text{ s}$	$\leq 5$	
$C_{\text{IO}}$	Barrier capacitance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 0.4 \times \sin(2\pi \text{ ft})$ , $f = 1 \text{ MHz}$	0.5	pF
$R_{\text{IO}}$	Insulation resistance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 500 \text{ V}$ , $T_A = 25^\circ\text{C}$	$>10^{12}$	$\Omega$
		$V_{\text{IO}} = 500 \text{ V}$ , $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$>10^{11}$	
		$V_{\text{IO}} = 500 \text{ V}$ at $T_S = 150^\circ\text{C}$	$>10^9$	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
$V_{\text{ISO}}$	Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}} = 5700 \text{ V}_{\text{RMS}}$ , $t = 60 \text{ s}$ (qualification), $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}} = 6840 \text{ V}_{\text{RMS}}$ , $t = 1 \text{ s}$ (100% production)	5700	$\text{V}_{\text{RMS}}$

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN V VDE V 0884-11: 2017-01	Plan to certify according to UL 1577 Component Recognition Program
Reinforced insulation Maximum transient isolation voltage, 8000 V <sub>PK</sub> ; Maximum repetitive peak isolation voltage, 2121 V <sub>PK</sub> ; Maximum surge isolation voltage, 8000 V <sub>PK</sub>	Single protection, 5700 V <sub>RMS</sub>
Certificate in progress	File number: E181974

## 6.8 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>qJA</sub> = 126°C/W, V <sub>I</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			50	mA
		R <sub>qJA</sub> = 126°C/W, V <sub>I</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			25	
P <sub>S</sub>	Safety input, output, or total power		R <sub>qJA</sub> = 126°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		750	mW
T <sub>S</sub>	Maximum safety temperature <sup>(1)</sup>				150	°C

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>. The junction-to-air thermal resistance, R<sub>qJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: T<sub>J</sub> = T<sub>A</sub> + R<sub>qJA</sub> ' P, where P is the power dissipated in the device. T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>qJA</sub> ' P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature. P<sub>S</sub> = I<sub>S</sub> ' V<sub>I</sub>, where V<sub>I</sub> is the maximum supply voltage.

## 6.9 Electrical Characteristics

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 15\text{V}$ ,  $V_{EE} = \text{GND}$ . All min and max specifications are at recommended operating conditions ( $T_J = -40\text{C}$  to  $150^\circ\text{C}$ ,  $I_{F(on)} = 7\text{ mA}$  to  $16\text{ mA}$ ,  $V_{EE} = \text{GND}$ ,  $V_{CC} = 15\text{ V}$  to  $30\text{ V}$ ,  $V_{F(off)} = -5\text{V}$  to  $0.8\text{V}$ )

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$I_{FLH}$	Input Forward Threshold Current Low to High	$V_{OUT} > 5\text{ V}$ , $C_g = 1\text{ nF}$	1.5	2.8	4	mA
$V_F$	Input Forward Voltage	$I_F = 10\text{ mA}$	1.8	2.1	2.4	V
$V_{F\_HL}$	Threshold Input Voltage High to Low	$V < 5\text{ V}$ , $C_g = 1\text{ nF}$	0.9			V
$\Delta V_F / \Delta T$	Temp Coefficient of Input Forward Voltage	$I_F = 10\text{ mA}$		1	1.35	mV/°C
$V_R$	Input Reverse Breakdown Voltage	$I_R = 10\text{ uA}$	15			V
$C_{IN}$	Input Capacitance	$F = 0.5\text{ MHz}$		15		pF
<b>OUTPUT</b>						
$I_{OH}$	High Level Peak Output Current	$I_F = 10\text{ mA}$ , $V_{CC} = 15\text{V}$ , $C_{LOAD} = 0.18\text{uF}$ , $R_{G\_total} = 6\Omega$ <sup>(1)</sup> , $C_{VDD} = 10\text{uF}$ , Pulse width <10us	1	1.5		A
$I_{OL}$	Low Level Peak Output Current	$V_F = 0\text{ V}$ , $V_{CC} = 15\text{V}$ , $C_{LOAD} = 0.18\text{uF}$ , $R_{G\_total} = 6\Omega$ <sup>(1)</sup> , $C_{VDD} = 10\text{uF}$ , Pulse width <10us	1	2.0		A
$V_{OH}$	High Level Output Voltage	$I_F = 10\text{ mA}$ , $I_O = -20\text{mA}$ (with respect to VCC)	0.07	0.18	0.36	V
$V_{OL}$	Low Level Output Voltage	$I_F = 10\text{ mA}$ , $I_O = 0\text{ mA}$		VCC		V
$I_{CC\_H}$	Output Supply Current (Diode On)	$I_F = 10\text{ mA}$ , $I_O = 0\text{ mA}$			2.2	mA
$I_{CC\_L}$	Output Supply Current (Diode Off)	$V_F = 0\text{ V}$ , $I_O = 0\text{ mA}$			2	mA
<b>UNDER VOLTAGE LOCKOUT</b>						
$UVLO_R$	Under Voltage Lockout VCC rising	$V_{CC\_Rising}$ , $I_F = 10\text{ mA}$	11	12.5	13.5	V
$UVLO_F$	Under Voltage Lockout VCC falling	$V_{CC\_Falling}$ , $I_F = 10\text{ mA}$	10	11.5	12.5	V
$UVLO_{HYS}$	UVLO Hysteresis				1.0	V

(1)  $R_{G\_total}$  is the total gate resistance. It includes the external gate resistor on the PCB + the internal gate resistance of the power switch. Min  $R_{G\_total}$  of  $4\Omega$  is recommended (for  $V_{CC} - V_{EE} = 15\text{V}$ ). For more details, refer to section 9 (Application and Implementation) of this datasheet.

## 6.10 Switching Characteristics

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 30\text{ V}$ ,  $V_{EE} = \text{GND}$ . All min and max specifications are at recommended operating conditions ( $T_J = -40$  to  $150^\circ\text{C}$ ,  $I_{F(on)} = 7\text{ mA}$  to  $16\text{ mA}$ ,  $V_{EE} = \text{GND}$ ,  $V_{CC} = 15\text{ V}$  to  $30\text{ V}$ ,  $V_{F(off)} = -5\text{V}$  to  $0.8\text{V}$ )

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output-signal Rise Time	$C_g = 1\text{nF}$ $F_{sw} = 20\text{ kHz}$ , (50% Duty Cycle) $V_{CC} = 15\text{V}$			28	ns
$t_f$	Output-signal Fall Time				25	ns
$t_{PLH}$	Propagation Delay, Low to High			70	105	ns
$t_{PHL}$	Propagation Delay, High to Low			70	105	ns
$t_{PWD}$	Pulse Width Distortion $ t_{PHL} - t_{PLH} $				35	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay Between any Two Parts <sup>(1)</sup>				25	ns
$t_{UVLO\_rec}$	UVLO Recovery Delay	$V_{CC}$ Rising from $0\text{V}$ to $15\text{V}$		20	30	μs

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC}-V_{EE} = 30\text{ V}$ ,  $V_{EE} = \text{GND}$ . All min and max specifications are at recommended operating conditions ( $T_J = -40$  to  $150^\circ\text{C}$ ,  $I_{F(ON)} = 7\text{ mA}$  to  $16\text{ mA}$ ,  $V_{EE} = \text{GND}$ ,  $V_{CC} = 15\text{ V}$  to  $30\text{ V}$ ,  $V_{F(OFF)} = -5\text{ V}$  to  $0.8\text{ V}$ )

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMTI <sub>H</sub>	Common-mode Transient Immunity (Output High) $I_F = 10\text{ mA}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$ , $T_A = 25^\circ\text{C}$	150			kV/μs
CMTI <sub>L</sub>	Common-mode Transient Immunity (Output Low) $V_F = 0\text{ V}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$ , $T_A = 25^\circ\text{C}$	150			kV/μs

(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads ensured by characterization.

## 6.11 Insulation Characteristics Curves

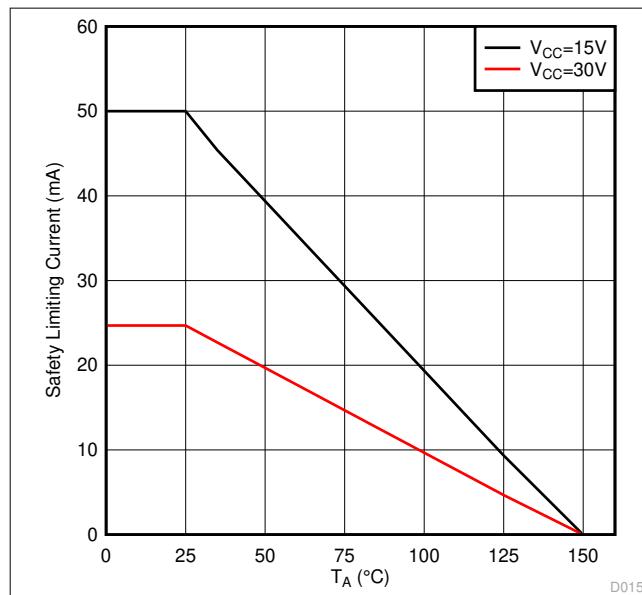


图 6-1. Thermal Derating Curve for Limiting Current per VDE

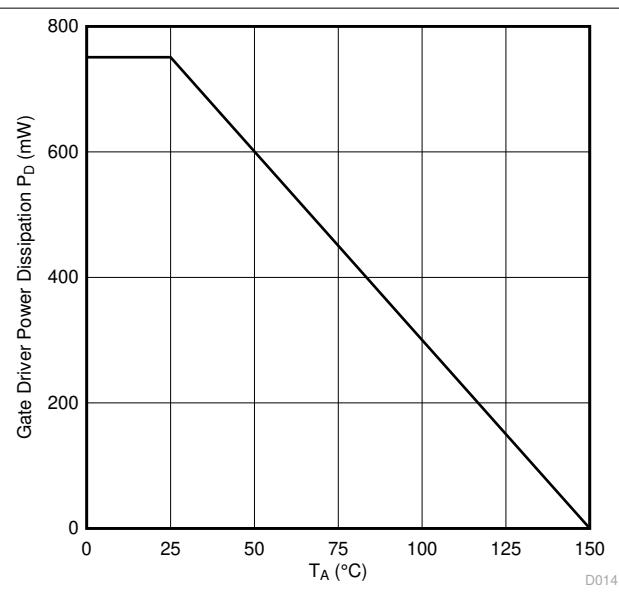


图 6-2. Thermal Derating Curve for Limiting Power per VDE

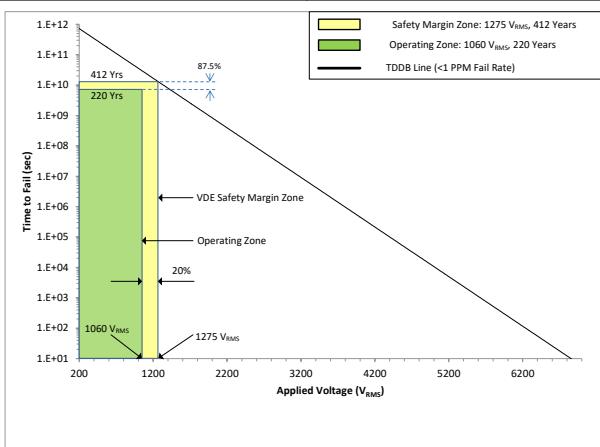


图 6-3. Reinforced Isolation Capacitor Life Time Projection

## 6.12 Typical Characteristics

$V_{CC} = 15$  V, 1- $\mu$ F capacitor from  $V_{CC}$  to  $V_{EE}$ ,  $C_{LOAD} = 1$  nF for timing tests and 180nF for  $I_{OH}$  and  $I_{OL}$  tests,  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , (unless otherwise noted)

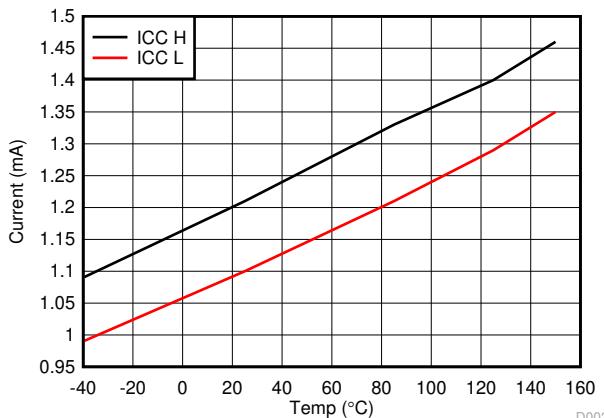


图 6-4. Supply currents versus Temperature

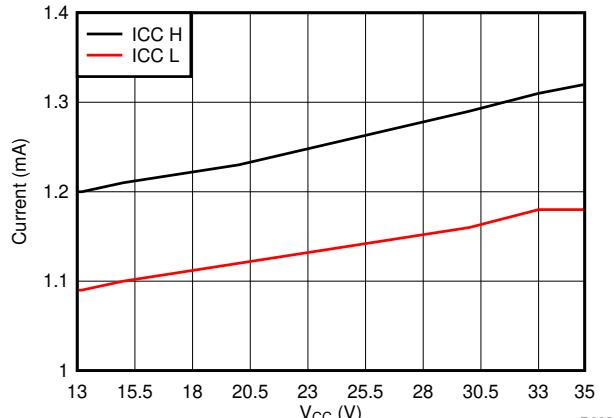


图 6-5. Supply current versus Supply Voltage

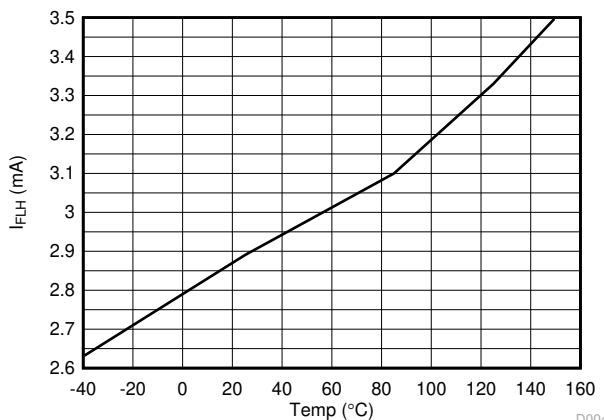


图 6-6. Forward threshold current versus Temperature

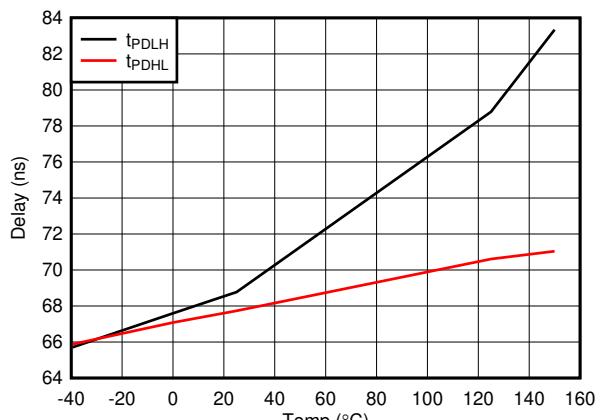


图 6-7. Propagation delay versus Temperature

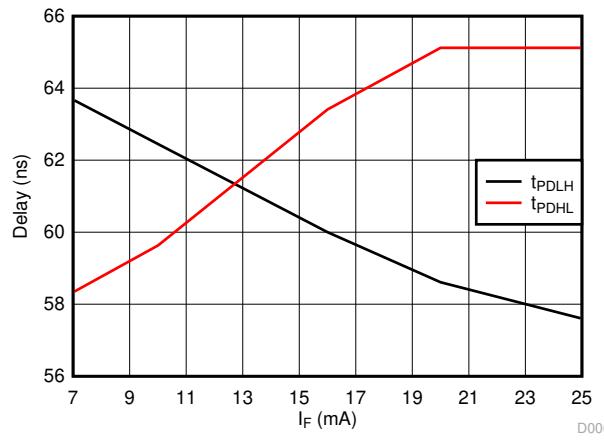


图 6-8. Propagation delay versus Forward current

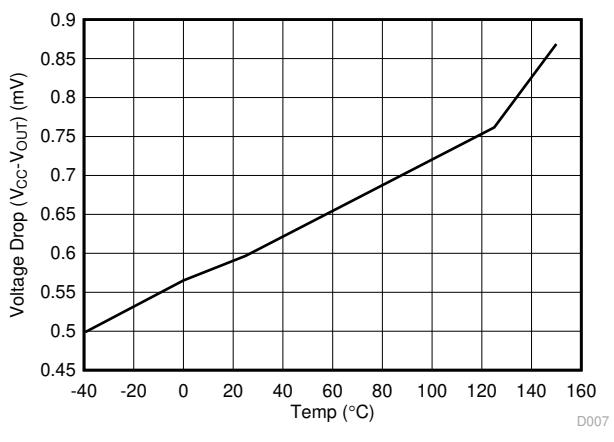


图 6-9.  $V_{OH}$  (No Load) versus Temperature

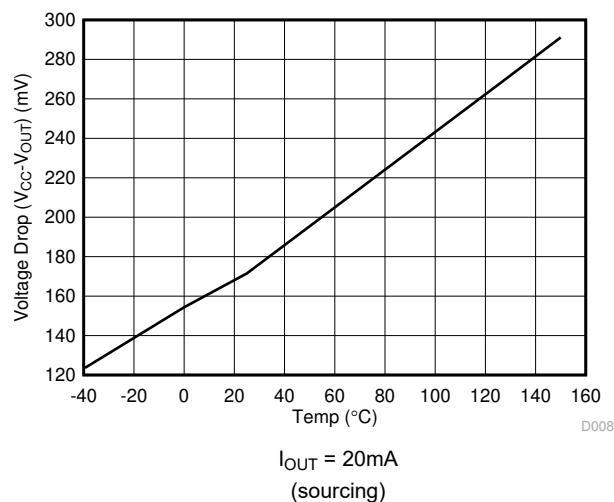


图 6-10.  $V_{OH}$  (20mA Load) versus Temperature

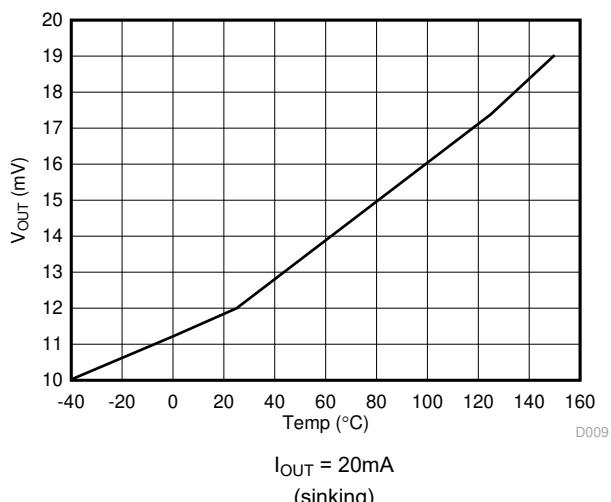


图 6-11.  $V_{OL}$  versus Temperature

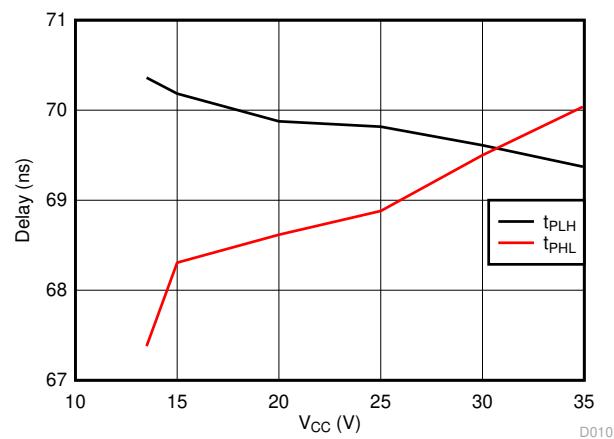


图 6-12. Propagation delay versus Supply voltage

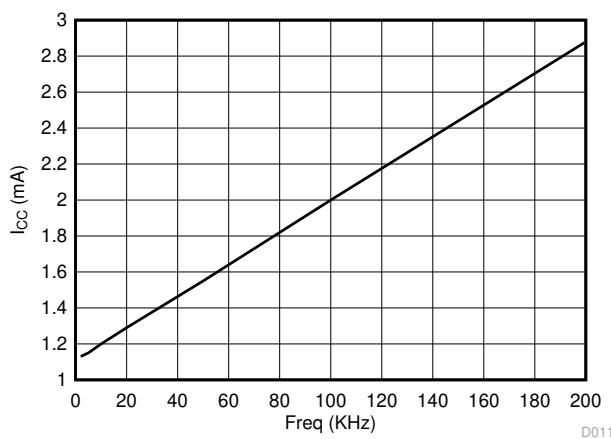


图 6-13. Supply current versus Frequency

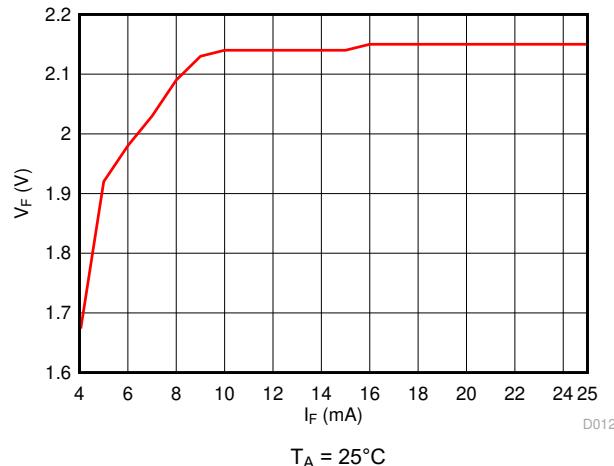


图 6-14. Forward current versus Forward voltage drop

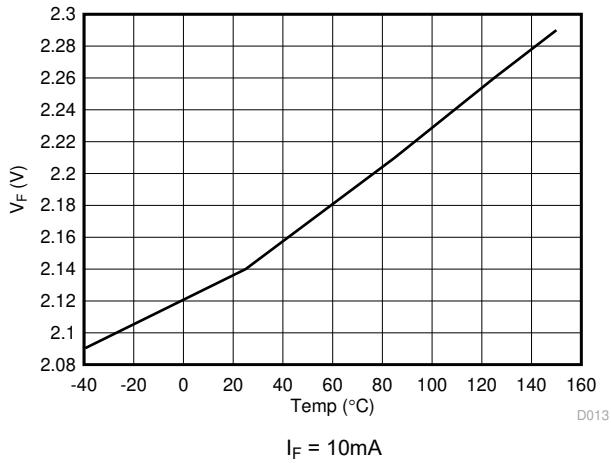


图 6-15. Forward voltage drop versus Temperature

## 7 Parameter Measurement Information

### 7.1 Propagation Delay, rise time and fall time

图 7-1 shows the propagation delay from the input forward current  $I_F$ , to  $V_{OUT}$ . This figure also shows the circuit used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times and the propagation delays  $t_{PD,LH}$  and  $t_{PD,HL}$ .

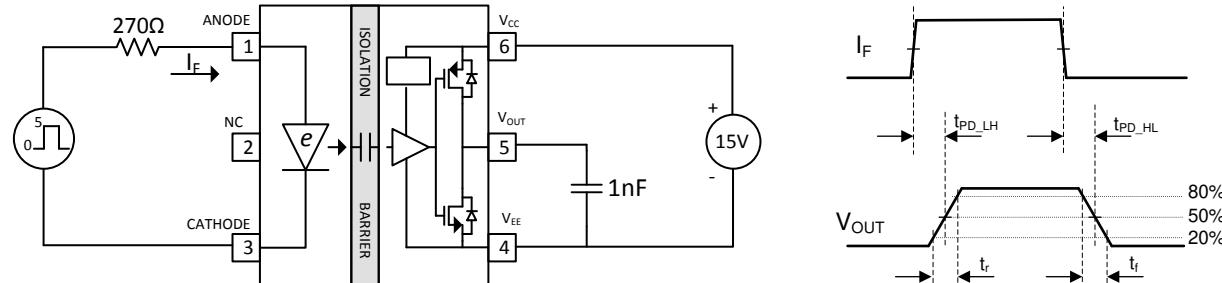


图 7-1.  $I_F$  to  $V_{OUT}$  Propagation Delay, Rise Time and Fall Time

### 7.2 $I_{OH}$ and $I_{OL}$ testing

图 7-2 shows the circuit used to measure the output drive currents  $I_{OH}$  and  $I_{OL}$ . A series resistor of  $6\ \Omega$  and a load capacitance of  $180\ nF$  are used at the output. The peak  $dv/dt$  of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

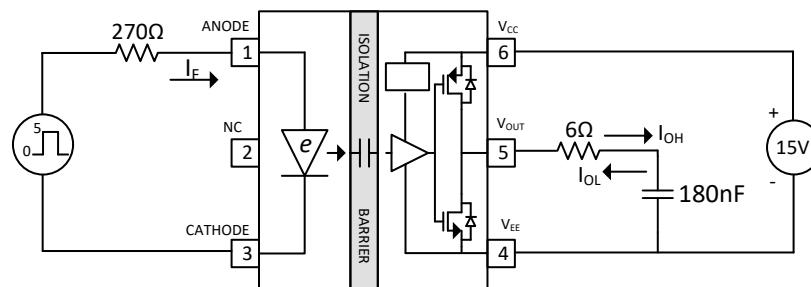


图 7-2.  $I_{OH}$  and  $I_{OL}$

### 7.3 CMTI Testing

图 7-3 is the simplified diagram of the CMTI testing. Common mode voltage is set to  $1500V$ . The test is performed with  $I_F = 6\text{mA}$  ( $V_{OUT} = \text{High}$ ) and  $I_F = 0\text{mA}$  ( $V_{OUT} = \text{Low}$ ). The diagram also shows the fail criteria for both cases. During the application on the CMTI pulse with  $I_F = 6\text{mA}$ , if  $V_{OUT}$  drops from  $V_{CC}$  to  $\frac{1}{2}V_{CC}$  it is considered as a failure. With  $I_F = 0\text{mA}$ , if  $V_{OUT}$  rises above  $1V$ , it is considered as a failure.

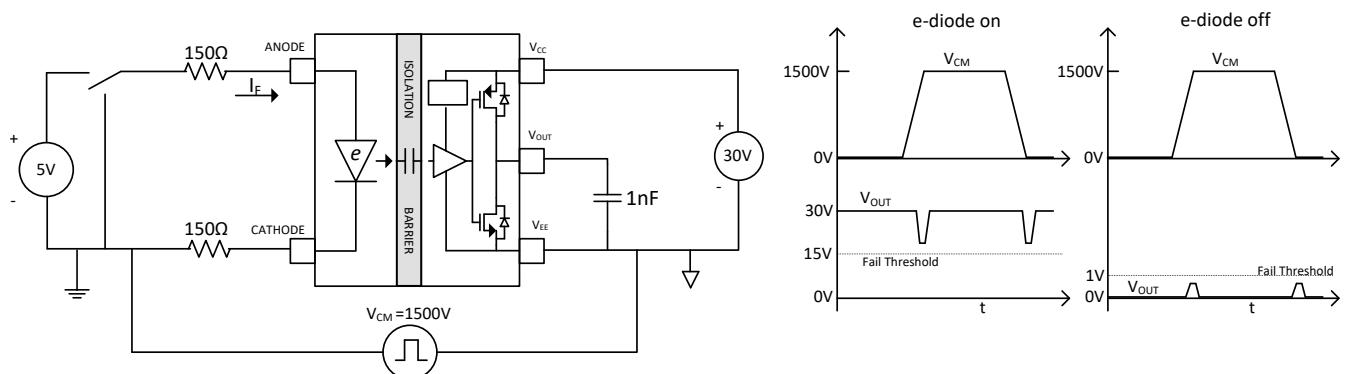


图 7-3. CMTI Test Circuit for UCC23511-Q1

## 8 Detailed Description

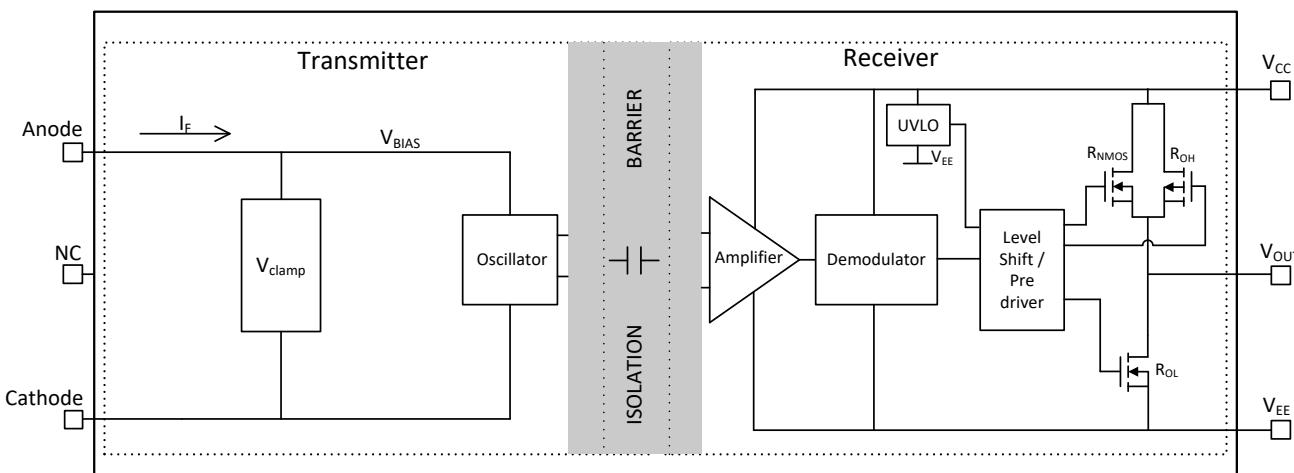
### 8.1 Overview

UCC23511-Q1 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs, MOSFETs and SiC FETs. It has 1.5-A source and 2-A sink peak output current capability with max output driver supply voltage of 33V. The inputs and the outputs are galvanically isolated. UCC23511-Q1 is offered in an industry standard 6 pin (SO6) package with >8.5mm creepage and clearance. It has a working voltage of 1500-V<sub>RMS</sub>, reinforced isolation rating of 5.7-kV<sub>RMS</sub> for 60s and a surge rating of 8-kV<sub>PK</sub>. It is pin-to-pin compatible with standard opto isolated gate drivers. While standard opto isolated gate drivers use an LED as the input stage, UCC23511-Q1 uses an emulated diode (or "e-diode") as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV SiO<sub>2</sub> capacitors in full differential configuration that not only provides reinforced isolation but also offers best-in-class common mode transient immunity of >150kV/us. The e-diode input stage along with capacitive isolation technology gives UCC23511-Q1 several performance advantages over standard opto isolated gate drivers. They are as follows:

1. Since the e-diode does not use light emission for its operation, the reliability and aging characteristics of UCC23511-Q1 are naturally superior to those of standard opto isolated gate drivers.
2. Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto isolated gate drivers
3. The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature.
4. Higher common mode transient immunity than opto isolated gate drivers
5. Smaller propagation delay than opto isolated gate drivers
6. Due to superior process controls achievable in capacitive isolation compared to opto isolation, there is less part-to-part skew in the prop delay, making the system design simpler and more robust
7. Smaller pulse width distortion than opto isolated gate drivers

The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see [图 8-1](#)). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC23511-Q1 also incorporates advanced circuit techniques to maximize the CMOS performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. [图 8-2](#) shows conceptual detail of how the OOK scheme works.

### 8.2 Functional Block Diagram



**图 8-1. Conceptual Block Diagram of a Isolated Gate Driver with an Opto Emulated Input Stage (SO6 pkg)**

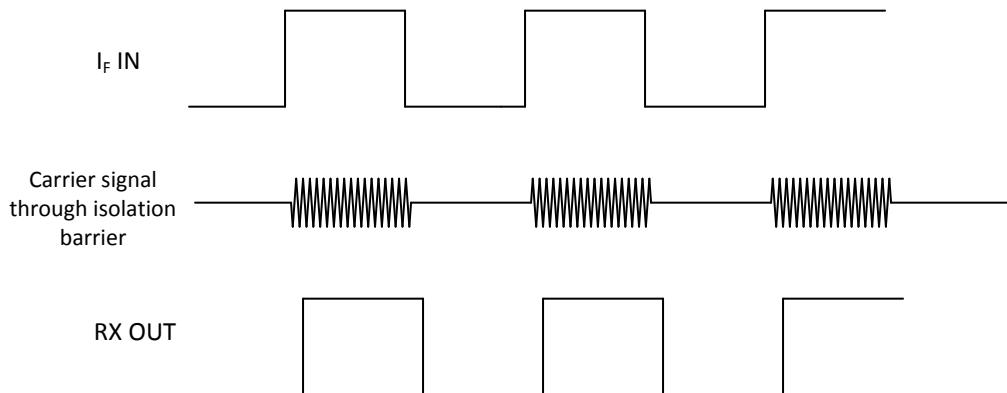


图 8-2. On-Off Keying (OOK) Based Modulation Scheme

## 8.3 Feature Description

### 8.3.1 Power Supply

Since the input stage is an emulated diode, no power supply is needed at the input.

The output supply,  $V_{CC}$ , supports a voltage range from 14V to 33V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the  $V_{CC}$  and  $V_{EE}$  output supplies for bipolar operation are 15V and -8V with respect to GND for IGBTs, and 20V and -5V for SiC MOSFETs.

For operation with unipolar supply, the  $V_{CC}$  supply is connected to 15V with respect to GND for IGBTs, and 20V for SiC MOSFETs. The  $V_{EE}$  supply is connected to 0V.

### 8.3.2 Input Stage

The input stage of UCC23511-Q1 is simply the e-diode and therefore has an Anode (Pin 1) and a Cathode (Pin 3). Pin 2 has no internal connection and can be left open or connected to ground. The input stage does not have a power and ground pin. When the e-diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current  $I_F$  flows into the e-diode. The forward voltage drop across the e-diode is 2.1V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7mA to 16mA. When  $I_F$  exceeds the threshold current  $I_{FLH}$  (2.8mA typ.) a high frequency signal is transmitted across the isolation barrier through the high voltage  $\text{SiO}_2$  capacitors. The HF signal is detected by the receiver and  $V_{OUT}$  is driven high. See [节 10.2.2.1](#) for information on selecting the input resistor. The dynamic impedance of the e-diode is very small (<1.0 $\Omega$ ) and the temperature coefficient of the e-diode forward voltage drop is <1.35mV/ $^{\circ}\text{C}$ . This leads to excellent stability of the forward current  $I_F$  across all operating conditions. If the Anode voltage drops below  $V_{F\_HL}$  (0.9V), or reverse biased, the gate driver output is driven low. The reverse breakdown voltage of the e-diode is >15V. So for normal operation, a reverse bias of up to 13V is allowed. The large reverse breakdown voltage of the e-diode enables UCC23511-Q1 to be operated in interlock architecture (see example in [图 8-3](#)) where  $V_{SUP}$  can be as high as 12V. The system designer has the flexibility to choose a 3.3V, 5.0V or up to 12V PWM signal source to drive the input stage of UCC23511-Q1 using an appropriate input resistor. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

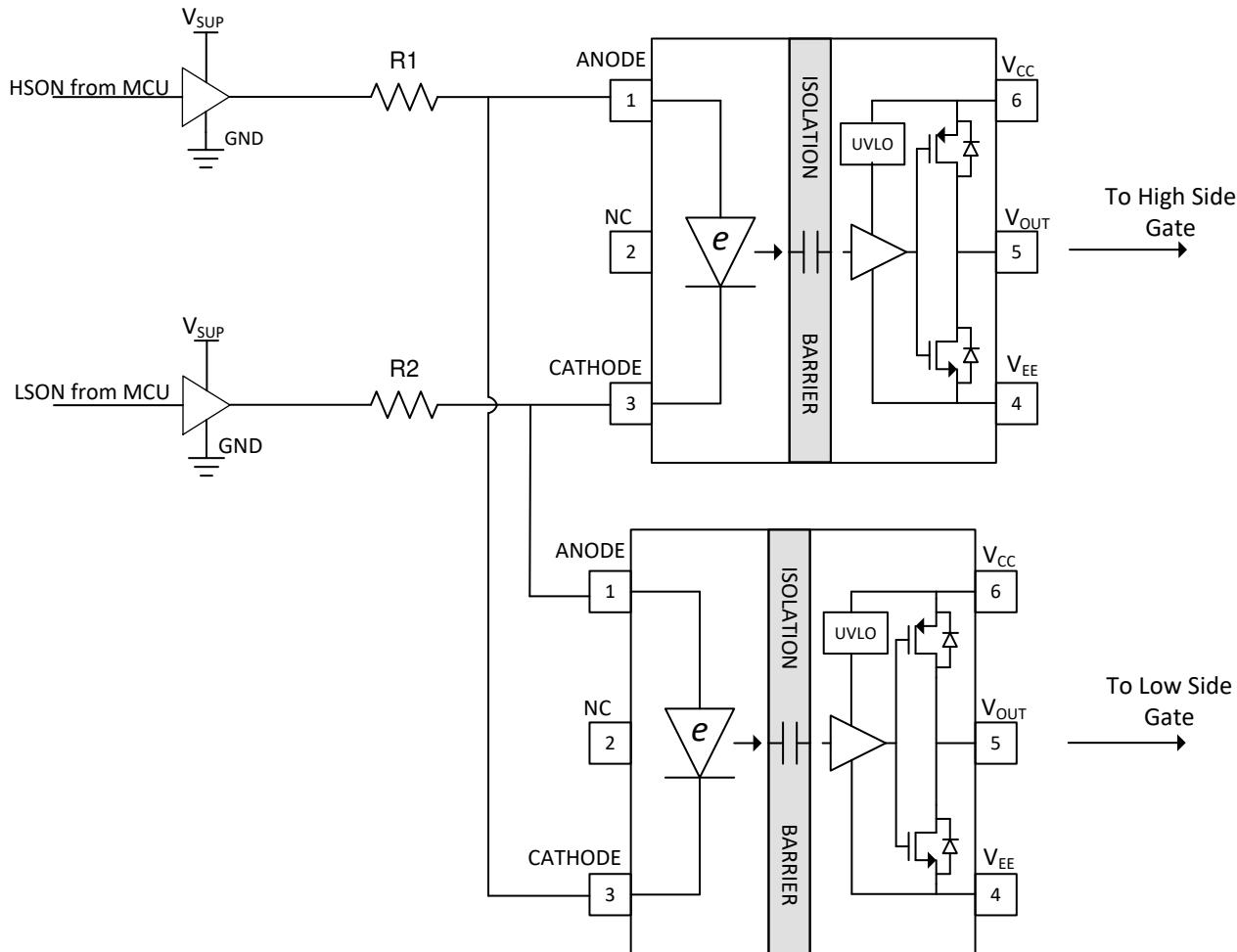


图 8-3. Interlock

### 8.3.3 Output Stage

The output stages of the UCC23511-Q1 family feature a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences  $dV/dt$ ). The output stage pullup structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turnon. Fast turnon is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ( $R_{NMOS}$ ) is approximately  $5.1\ \Omega$  when activated.

表 8-1. UCC23511-Q1 On-Resistance

$R_{NMOS}$	$R_{OH}$	$R_{OL}$	UNIT
5.1	9.5	0.40	$\Omega$

The  $R_{OH}$  parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device because the pullup N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC23511-Q1 pullup stage during this brief turnon phase is much lower than what is represented by the  $R_{OH}$  parameter, yielding a faster turn on. The turnon-phase output resistance is the parallel combination  $R_{OH} \parallel R_{NMOS}$ .

The pulldown structure in the UCC23511-Q1 is simply composed of an N-channel MOSFET. The output voltage swing between  $V_{CC}$  and  $V_{EE}$  provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

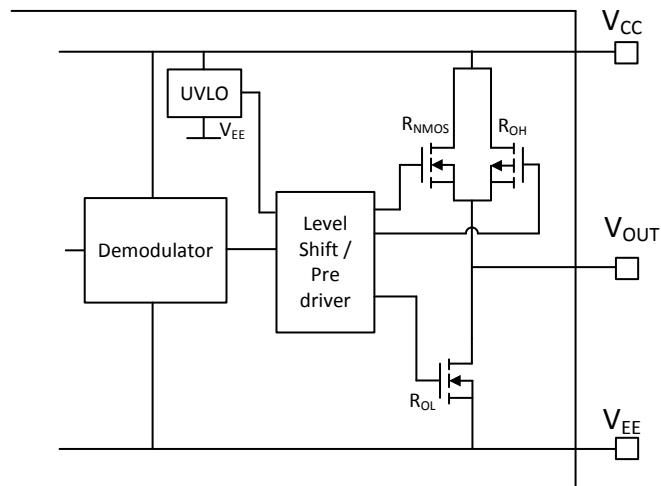


图 8-4. Output Stage

### 8.3.4 Protection Features

#### 8.3.4.1 Undervoltage Lockout (UVLO)

UVLO function is implemented for  $V_{CC}$  and  $V_{EE}$  pins to prevent an under-driven condition on IGBTs and MOSFETs. When  $V_{CC}$  is lower than  $UVLO_R$  at device start-up or lower than  $UVLO_F$  after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input forward current as shown in 表 9-1. The  $V_{CC}$  UVLO protection has a hysteresis feature ( $UVLO_{hys}$ ). This hysteresis prevents chatter when the power supply produces ground noise which allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly.

When  $V_{CC}$  drops below  $UVLO_F$ , a delay,  $t_{UVLO\_rec}$  occurs on the output when the supply voltage rises above  $UVLO_R$  again.

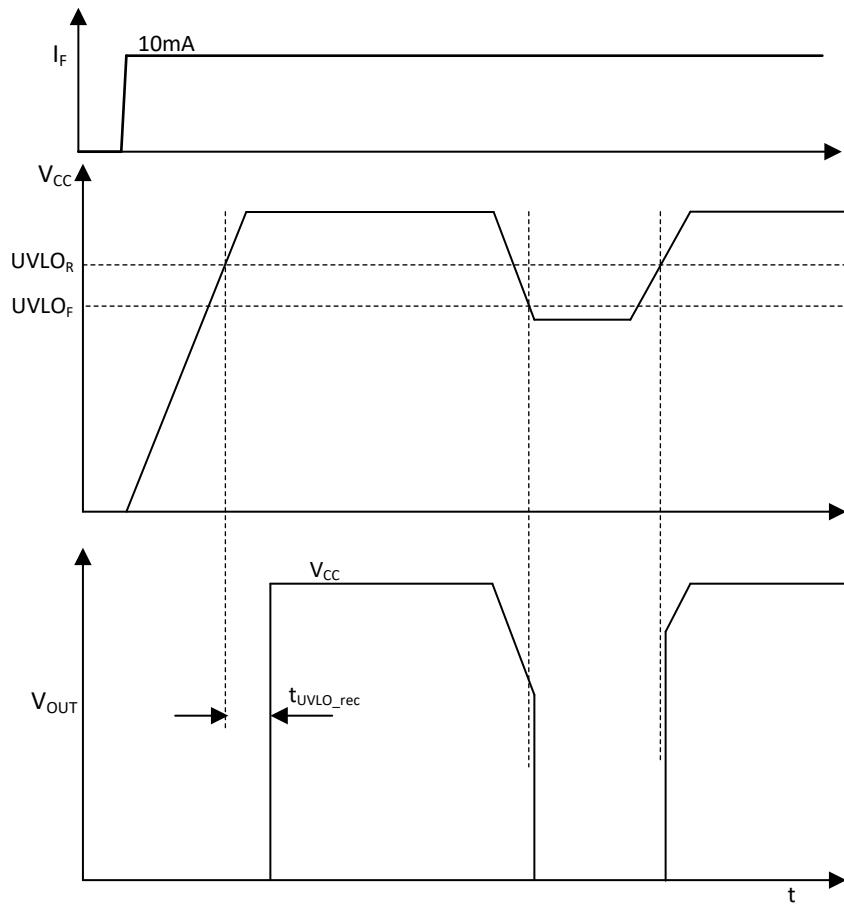


图 8-5. UVLO functionality

#### 8.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the  $V_{CC}$  supply. This feature prevents false IGBT and MOSFET turn-on by clamping  $V_{OUT}$  pin to approximately 2V.

When the output stage of the driver is in an unbiased condition ( $V_{CC}$  floating), the driver outputs (see [图 8-4](#)) are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS & NMOS are held off while the lower NMOS gate is tied to the driver output through an internal 500-k $\Omega$  resistor. In this configuration, the lower NMOS device effectively clamps the output ( $V_{OUT}$ ) to less than 2V.

#### 8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the output pin  $V_{OUT}$  slightly higher than the  $V_{CC}$  voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the  $V_{CC}$  pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10  $\mu$ s and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

## 9 Device Functional Modes

表 9-1 lists the functional modes for UCC23511-Q1

表 9-1. Function Table for UCC23511-Q1 with VCC Rising

e-diode	VCC	V <sub>OUT</sub>
OFF ( $I_F < I_{FLH}$ )	0V - 33V	Low
ON ( $I_F > I_{FLH}$ )	0V - UVLO <sub>R</sub>	Low
ON ( $I_F > I_{FLH}$ )	UVLO <sub>R</sub> - 33V	High

表 9-2. Function Table for UCC23511-Q1 with VCC Falling

e-diode	VCC	V <sub>OUT</sub>
OFF ( $I_F < I_{FLH}$ )	0V - 33V	Low
ON ( $I_F > I_{FLH}$ )	UVLO <sub>F</sub> - 0V	Low
ON ( $I_F > I_{FLH}$ )	33V - UVLO <sub>F</sub>	High

### 9.1 ESD Structure

图 9-1 shows the multiple diodes involved in the ESD protection components of the UCC23511-Q1 device. This provides pictorial representation of the absolute maximum rating for the device.

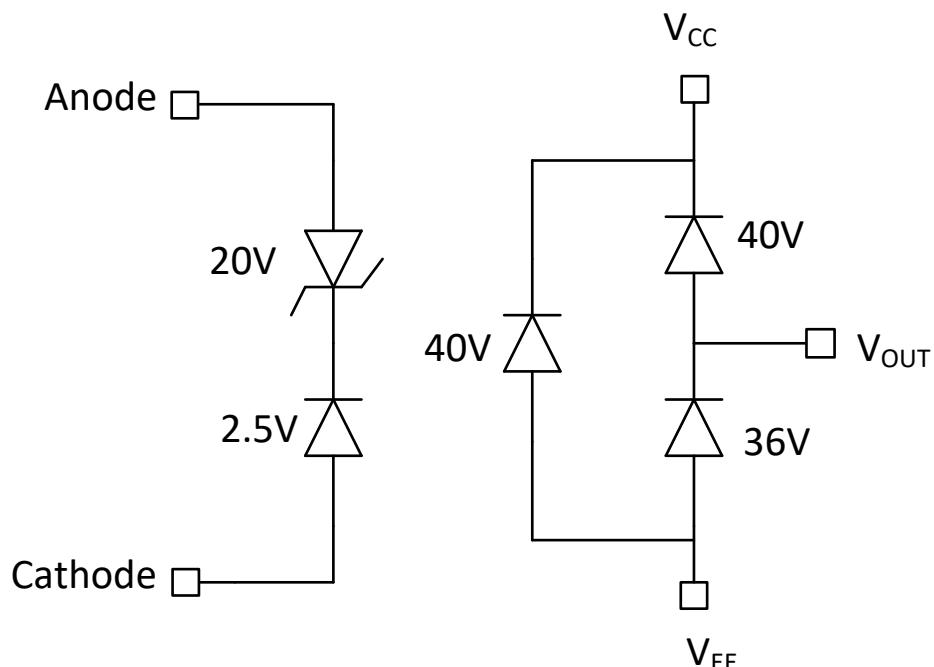


图 9-1. ESD Structure

## 10 Application and Implementation

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### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 10.1 Application Information

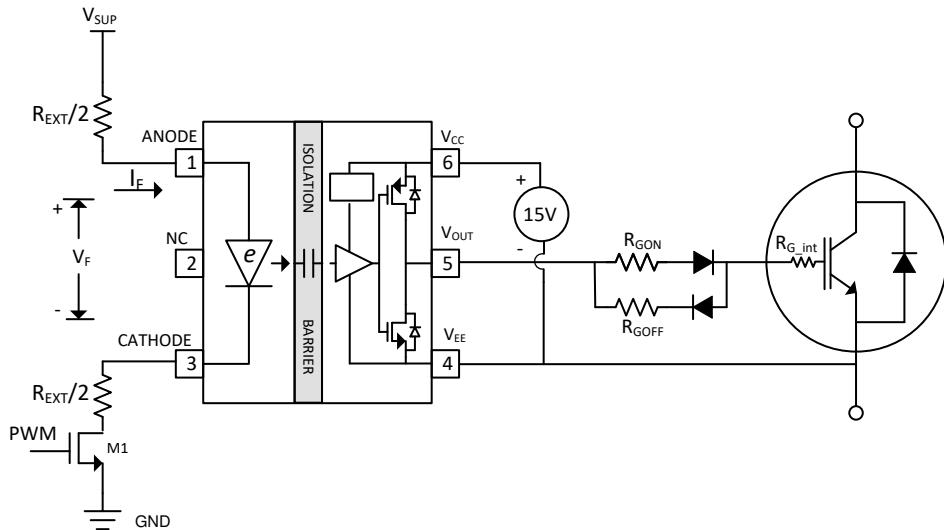
UCC23511-Q1 is a single channel, isolated gate driver with opto-compatible input for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. It is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies. It differs from standard opto isolated gate drivers as it does not have an LED input stage. Instead of an LED, it has an emulated diode (e-diode). To turn the e-diode "ON", a forward current in the range of 7mA to 16mA should be driven into the Anode. This will drive the gate driver output High and turn on the power FET. Typically, MCU's are not capable of providing the required forward current. Hence a buffer has to be used between the MCU and the input stage of UCC23511-Q1. Typical buffer power supplies are either 5V or 3.3V. A resistor is needed between the buffer and the input stage of UCC23511-Q1 to limit the current. It is simple, but important to choose the right value of resistance. The resistor tolerance, buffer supply voltage tolerance and output impedance of the buffer, have to be considered in the resistor selection. This will ensure that the e-diode forward current stays within the recommended range of 7mA to 16mA. Detailed design recommendations are given in the [节 10.1](#). The current driven input stage offers excellent noise immunity that is need in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. UCC23511-Q1 offers best in class CMTI performance of >150kV/us at 1500V common mode voltages.

The e-diode is capable of 25mA continuous in the forward direction. The forward voltage drop of the e-diode has a very tight part to part variation (1.8V min to 2.4V max). The temperature coefficient of the forward drop is  $<1.35\text{mV/}^{\circ}\text{C}$ . The dynamic impedance of the e-diode in the forward biased region is  $\sim 1\Omega$ . All of these factors contribute in excellent stability of the e-diode forward current. To turn the e-diode "OFF", the Anode - Cathode voltage should be  $<0.8\text{V}$ , or  $I_F$  should be  $<I_{FLH}$ . The e-diode can also be reverse biased up to 13V (14V abs max) in order to turn it off and bring the gate driver output low. The large reverse breakdown voltage of the input stage provides system designers the flexibility to drive the input stage with 12V PWM signals without the need for an additional clamping circuit on the Anode and Cathode pin.

The output power supply for UCC23511-Q1 can be as high as 33V (35V abs max). The output power supply can be configured externally as a single isolated supply up to 33V or isolated bipolar supply such that  $V_{CC}-V_{EE}$  does not exceed 33V, or it can be bootstrapped (with external diode & capacitor) if the system uses a single power supply with respect to the power ground. Typical quiescent power supply current from  $V_{CC}$  is 1.2mA (max 2.2mA).

## 10.2 Typical Application

The circuit in [图 10-1](#), shows a typical application for driving IGBTs.



**图 10-1. Typical Application Circuit for UCC23511-Q1 to Drive IGBT**

### 10.2.1 Design Requirements

[表 10-1](#) lists the recommended conditions to observe the input and output of the UCC23511-Q1 gate driver.

**表 10-1. UCC23511-Q1 Design Requirements**

PARAMETER	VALUE	UNIT
V <sub>CC</sub>	15	V
I <sub>F</sub>	10	mA
Switching frequency	8	kHz

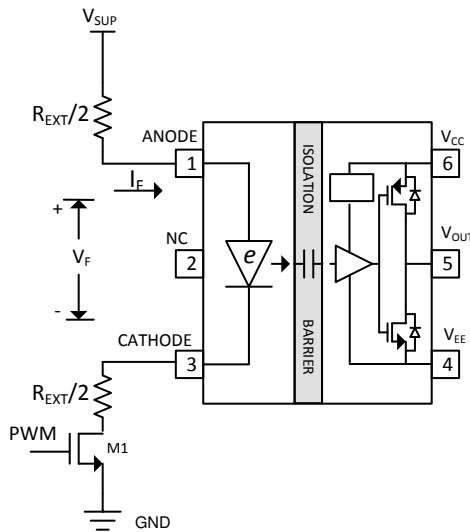
## 10.2.2 Detailed Design Procedure

### 10.2.2.1 Selecting the Input Resistor

The input resistor limits the current that flows into the e-diode when it is forward biased. The threshold current  $I_{FLH}$  is 2.8 mA typ. The recommended operating range for the forward current is 7 mA to 16 mA (e-diode ON). All the electrical specifications are guaranteed in this range. The resistor should be selected such that for typical operating conditions,  $I_F$  is 10 mA. Following are the list of factors that will affect the exact value of this current:

1. Supply Voltage  $V_{SUP}$  variation
2. Manufacturer's tolerance for the resistor and variation due to temperature
3. e-diode forward voltage drop variation (at  $I_F=10$  mA,  $V_F$  = typ 2.1 V, min 1.8 V, max 2.4 V, with a temperature coefficient <1.35 mV/°C and dynamic impedance < 1 Ω)

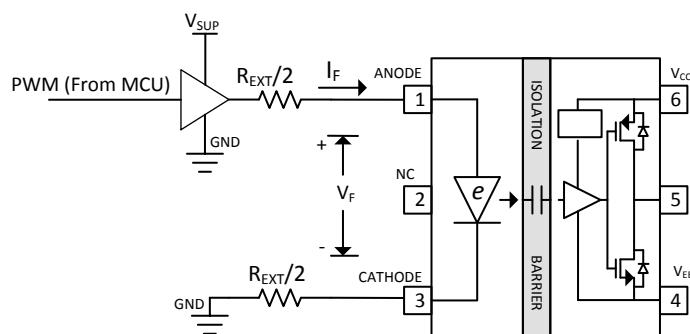
See [图 10-2](#) for the schematic using a single NMOS and split resistor combination to drive the input stage of UCC23511-Q1. The input resistor can be selected using the equation shown.



$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{M1}$$

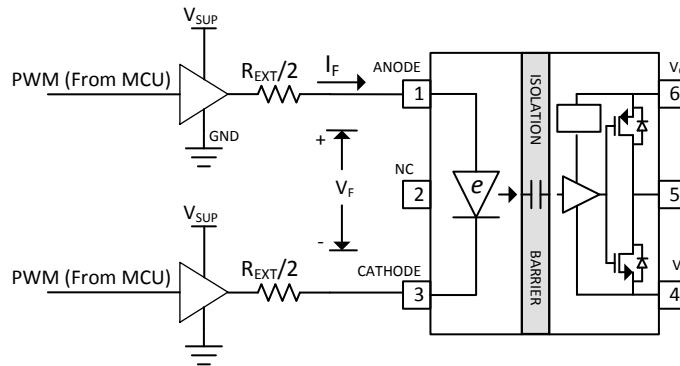
**图 10-2. Configuration 1: Driving the input stage of UCC23511-Q1 with a single NMOS and split resistors**

Driving the input stage of UCC23511-Q1 using a single buffer is shown in [图 10-3](#) and using 2 buffers is shown in [图 10-4](#)



$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH\_buf}$$

**图 10-3. Configuration 2: Driving the input stage of UCC23511-Q1 with one Buffer and split resistors**



$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - (R_{OH\_buf} + R_{OL\_buf})$$

图 10-4. Configuration 3: Driving the input stage of UCC23511-Q1 with 2 buffers and split resistors

表 10-2 shows the range of values for  $R_{EXT}$  for the 3 different configurations shown in 图 10-2, 图 10-3 and 图 10-4. The assumptions used in deriving the range for  $R_{EXT}$  are as follows:

1. Target forward current  $I_F$  is 7mA min, 10mA typ and 16mA max
2. e-diode forward voltage drop is 1.8V to 2.4V
3.  $V_{SUP}$  (Buffer supply voltage) is 5V with  $\pm 5\%$  tolerance
4. Manufacturer's tolerance for  $R_{EXT}$  is 1%
5. NMOS resistance is 0.25  $\Omega$  to 1.0  $\Omega$  (for configuration 1)
6.  $R_{OH}$  (buffer output impedance in output "High" state) is 13  $\Omega$  min, 18  $\Omega$  typ and 22  $\Omega$  max
7.  $R_{OL}$  (buffer output impedance in "Low" state) is 10  $\Omega$  min, 14  $\Omega$  typ and 17  $\Omega$  max

表 10-2.  $R_{EXT}$  Values to Drive The Input Stage

	$R_{EXT}$ $\Omega$		
Configuration	Min	Typ	Max
Single NMOS and $R_{EXT}$	218	290	331
Single Buffer and $R_{EXT}$	204	272	311
Two Buffers and $R_{EXT}$	194	259	294

### 10.2.2.2 Gate Driver Output Resistor

The external gate-driver resistors,  $R_{G(ON)}$  and  $R_{G(OFF)}$  are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching  $dv/dt$ ,  $di/dt$ , and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage of UCC23511-Q1 has a pull up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel, as shown in 图 8-4. The N-channel MOSFET provides the peak current that charges the gate of the IGBT (or power switch) while the P-channel MOSFET ensures that  $V_{OUT}$  will go all the way up to  $V_{CC}$ . 图 10-1 shows the internal gate resistance,  $R_{G\_int}$  of the power switch.  $R_{G\_int}$  is usually specified in the datasheet of the power switch. When turning the power switch "on", the gate driver sees a total gate resistance  $R_{G\_total} = R_{GON} + R_{G\_int}$  and when turning the power switch "off", the gate driver sees a total gate resistance  $R_{G\_total} = R_{GOFF} + R_{G\_int}$  in series with the gate capacitance where,

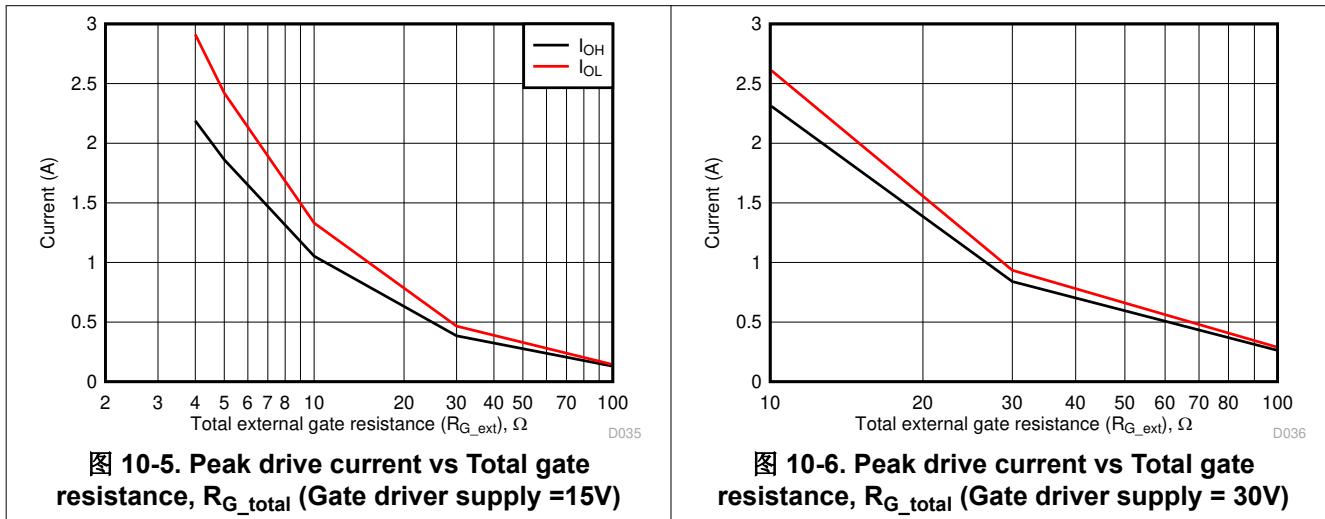
- $R_{GON}$  is the external resistance on the PCB for turn "on"
- $R_{GOFF}$  is the external resistance on the PCB for turn "off"

- $R_{G\_int}$  is the internal gate resistance of the power switch that can be found in the data sheet of the power switch
- Ideal diodes — zero resistance and zero voltage drop — are assumed on both the turn-on and turn-off paths, for simplicity.

To illustrate the procedure to select  $R_{GON}$  and  $R_{GOFF}$ , let us consider the following example with the assumptions listed below:

1. Power switch internal gate resistance is 2 ohms
2. Desired charging current is 1.5A
3. Desired discharging current is 1.7A
4. Gate driver supply is 15 V

For this example, since  $V_{CC}=15V$ , use the typical curves shown in [图 10-5](#). It can be seen that we need a total turn on resistance of 7 ohms (peak charging current of 1.5A) and a total turn off resistance of 8 ohms (peak discharging current of 1.7A). Subtracting the internal gate resistance of the power switch, we get  $R_{GON}= 7$  ohms - 2 ohms = 5 ohms, and  $R_{GOFF}= 8$  ohms - 2 ohms = 6 ohms.



Use [表 10-3](#) to find the minimum gate resistance to be used with UCC23511-Q1 when driving a power switch. The values shown includes the power switch internal gate resistance  $R_{G\_int}$ . Hence,  $R_{G\_int}$  must be subtracted from the values shown to determine the value of the resistor to populate on the printed circuit board.

**表 10-3. Minimum gate resistor (Ω)**

Gate driver supply $V_{CC}-V_{EE}$ (V)	Minimum total gate resistance (Ω) = $(R_{GON}+ R_{G\_int})$ or $(R_{GOFF}+ R_{G\_int})$
15	4
23	7
30	10

The diodes shown in series with each,  $R_{GON}$  and  $R_{GOFF}$ , in [图 10-1](#) ensure the gate drive current flows through the intended path, respectively, during turn-on and turn-off. Note that the diode forward drop will reduce the voltage level at the gate of the power switch. To achieve rail-to-rail gate voltage levels, add a resistor from the  $V_{OUT}$  pin to the power switch gate, with a resistance value approximately 20 times higher than  $R_{GON}$  and  $R_{GOFF}$ . For the examples described in this section, a good choice is 100 Ω to 200 Ω.

### Note

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

#### 10.2.2.3 Estimate Gate-Driver Power Loss

The total loss,  $P_G$ , in the gate-driver subsystem includes the power losses ( $P_{GD}$ ) of the UCC23511-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The  $P_{GD}$  value is the key power loss which determines the thermal safety-related limits of the UCC23511-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss,  $P_{GDQ}$ , which includes power dissipated in the input stage ( $P_{GDQ\_IN}$ ) as well as the quiescent power dissipated in the output stage ( $P_{GDQ\_OUT}$ ) when operating with a certain switching frequency under no load.  $P_{GDQ\_IN}$  is determined by  $I_F$  and  $V_F$  and is given by [方程式 1](#). The  $P_{GDQ\_OUT}$  parameter is measured on the bench with no load connected to  $V_{OUT}$  pin at a given  $V_{CC}$ , switching frequency, and ambient temperature. In this example,  $V_{CC}$  is 15 V. The current on the power supply, with PWM switching at 10 kHz, is measured to be  $I_{CC} = 1.33$  mA. Therefore, use [方程式 2](#) to calculate  $P_{GDQ\_OUT}$ .

$$P_{GDQ\_IN} = \frac{1}{2} * V_F * I_F \quad (1)$$

$$P_{GDQ\_OUT} = V_{CC} * I_{CC} \quad (2)$$

The total quiescent power (without any load capacitance) dissipated in the gate driver is given by the sum of [方程式 1](#) and [方程式 2](#) as shown in [方程式 3](#)

$$P_{GDQ} = P_{GDQ\_IN} + P_{GDQ\_OUT} = 10 \text{ mW} + 20 \text{ mW} = 30 \text{ mW} \quad (3)$$

The second component is the switching operation loss,  $P_{GDSW}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use [方程式 4](#) to calculate the total dynamic loss from load switching,  $P_{GSW}$ .

$$P_{GSW} = V_{CC2} \times Q_G \times f_{SW} \quad (4)$$

where

- $Q_G$  is the gate charge of the power transistor at  $V_{CC}$ .

So, for this example application the total dynamic loss from load switching is approximately 18 mW as calculated in [方程式 5](#).

$$P_{GSW} = 15 \text{ V} \times 120 \text{ nC} \times 10 \text{ kHz} = 18 \text{ mW} \quad (5)$$

$Q_G$  represents the total gate charge of the power transistor switching 520 V at 50 A, and is subject to change with different testing conditions. The UCC23511-Q1 gate-driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  is equal to  $P_{GSW}$  if the external gate-driver resistance and power-transistor internal resistance are 0  $\Omega$ , and all the gate driver-loss will be dissipated inside the UCC23511-Q1. If an external turn-on and turn-off

resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 1.5A/2.0A, however, it will be non-linear if the source/sink current is saturated. Therefore,  $P_{GDO}$  is different in these two scenarios.

**Case 1 - Linear Pull-Up/Down Resistor:**

$$P_{GDO} = \frac{P_{GSW}}{2} \left[ \frac{R_{OH} || R_{NMOS}}{R_{OH} || R_{NMOS} + R_{GON} + R_{GFET\_int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET\_int}} \right] \quad (6)$$

In this design example, all the predicted source and sink currents are less than 1.5 A and 2.0 A, therefore, use [方程式 7](#) to estimate the UCC23511-Q1 gate-driver loss.

$$P_{GDO} = \frac{18 \text{ mW}}{2} \left[ \frac{9.5\Omega || 5.1\Omega}{9.5\Omega || 5.1\Omega + 5.1\Omega + 0\Omega} + \frac{0.4\Omega}{0.4\Omega + 10\Omega + 0\Omega} \right] = 3.9 \text{ mW} \quad (7)$$

**Case 2 - Nonlinear Pull-Up/Down Resistor:**

$$P_{GDO} = f_{sw} x \left[ 4.5A x \int_0^{T_{R\_Sys}} (V_{CC} - V_{OUT}(t)) dt + 5.3A x \int_0^{T_{F\_Sys}} V_{OUT}(t) dt \right] \quad (8)$$

where

- $V_{OUT(t)}$  is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (1.5 A at turnon and 2.0 A at turnoff) charging or discharging a load capacitor. Then, the  $V_{OUT(t)}$  waveform will be linear and the  $T_{R\_Sys}$  and  $T_{F\_Sys}$  can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the  $P_{GDO}$  is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use [方程式 9](#) to calculate the total gate-driver loss dissipated in the UCC23511-Q1 gate driver,  $P_{GD}$ .

$$P_{GD} = P_{GDQ} + P_{GDO} = 30\text{mW} + 3.9\text{mW} = 33.9\text{mW} \quad (9)$$

#### 10.2.2.4 Estimating Junction Temperature

Use [方程式 10](#) to estimate the junction temperature ( $T_J$ ) of UCC23511-Q1.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (10)$$

where

- $T_C$  is the UCC23511-Q1 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$  is the junction-to-top characterization parameter from the table.

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance ( $R_{\theta JC}$ ) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The  $R_{\theta JC}$  resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of  $R_{\theta JC}$  will

inaccurately estimate the true junction temperature. The  $\Psi_{JT}$  parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

#### 10.2.2.5 Selecting $V_{CC}$ Capacitor

Bypass capacitors for  $V_{CC}$  is essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances. A 50-V, 10- $\mu$ F MLCC and a 50-V, 0.22- $\mu$ F MLCC are selected for the  $C_{VCC}$  capacitor. If the bias power supply output is located a relatively long distance from the  $V_{CC}$  pin, a tantalum or electrolytic capacitor with a value greater than 10  $\mu$ F should be used in parallel with  $C_{VCC}$ .

#### Note

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1- $\mu$ F X7R capacitor is measured to be only 500 nF when a DC bias of 15-V<sub>DC</sub> is applied.

#### 10.2.3 Application Performance Plots

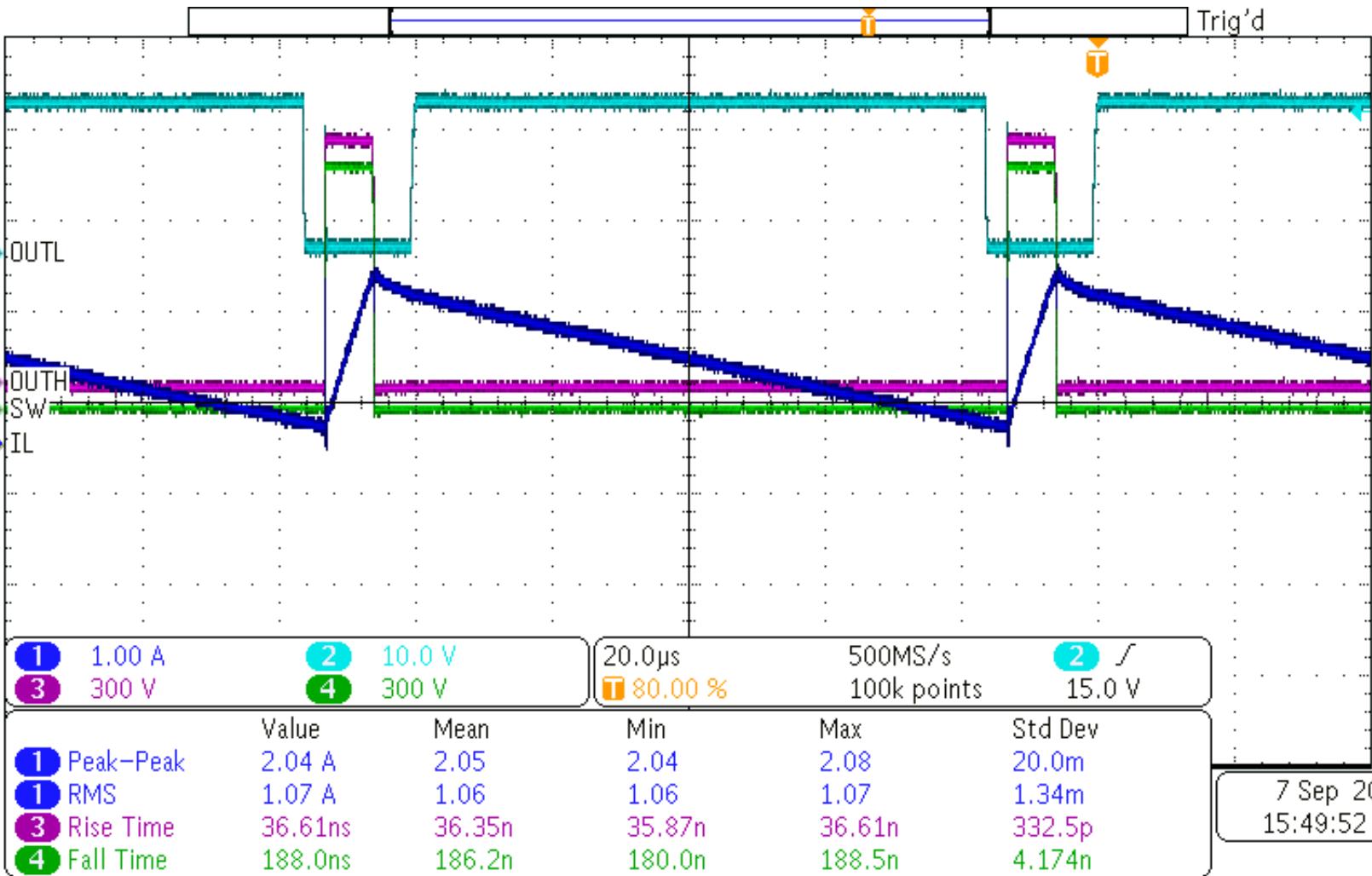


图 10-7. 1-A Load Performance Data

## 11 Power Supply Recommendations

The recommended input supply voltage ( $V_{CC}$ ) for the UCC23511-Q1 device is from 14V to 33V. The lower limit of the range of output bias-supply voltage ( $V_{CC}$ ) is determined by the internal UVLO protection feature of the device.  $V_{CC}$  voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low for more than 20  $\mu$ s by the UVLO protection feature. The higher limit of the  $V_{CC}$  range depends on the maximum gate voltage of the power device that is driven by the UCC23511-Q1 device, and should not exceed the recommended maximum  $V_{CC}$  of 33 V. A local bypass capacitor should be placed between the  $V_{CC}$  and  $V_{EE}$  pins, with a value of 220-nF to 10- $\mu$ F for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' [SN6501](#) or [SN6505A](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#) and [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

## 12 Layout

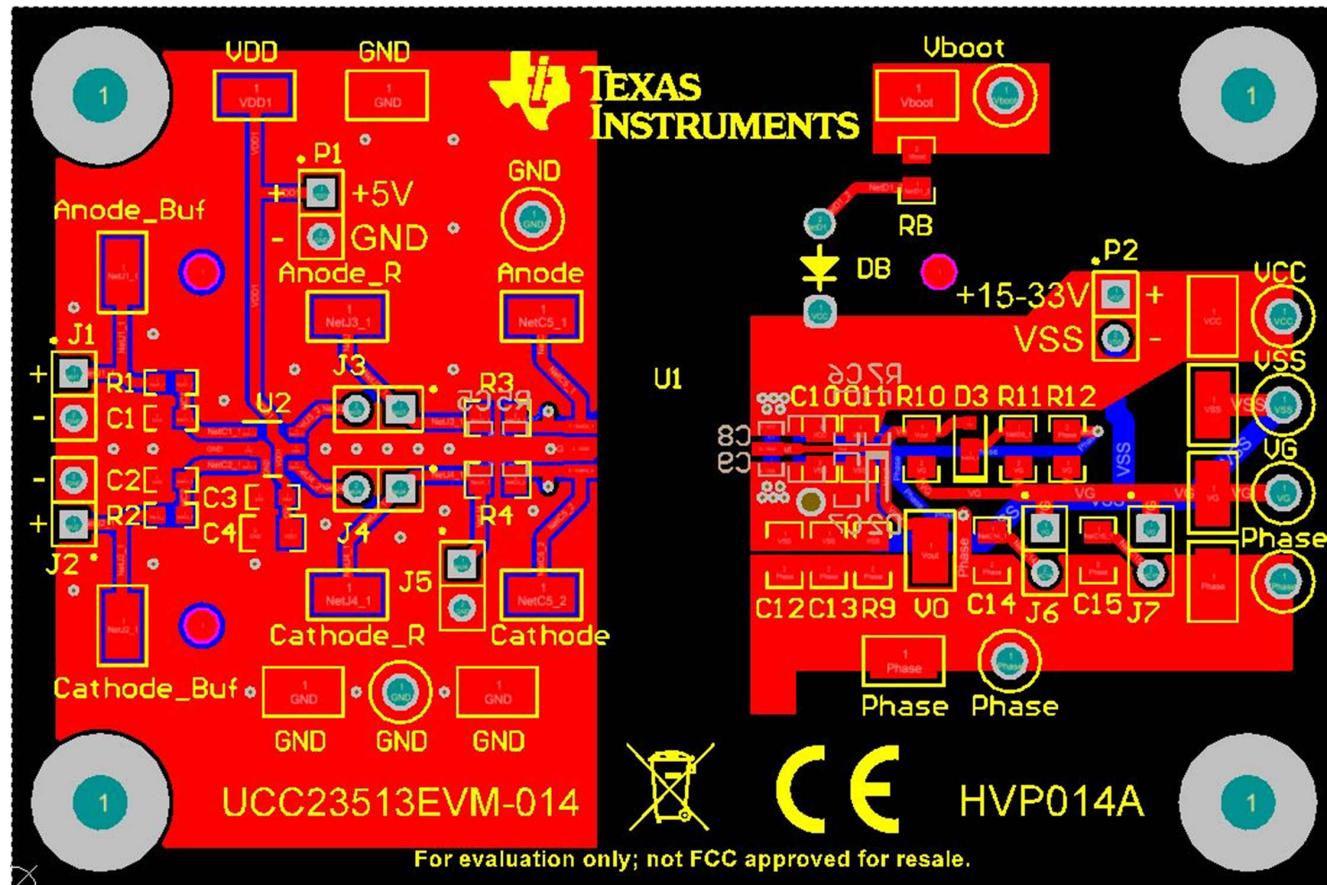
### 12.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC23511-Q1. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the  $V_{CC}$  and  $V_{EE}$  pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the  $V_{EE}$  pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC23511-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ( $\theta_{JB}$ ).
  - Increasing the PCB copper connecting to the  $V_{CC}$  and  $V_{EE}$  pins is recommended, with priority on maximizing the connection to  $V_{EE}$ . However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the  $V_{CC}$  and  $V_{EE}$  pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

## 12.2 Layout Example

图 12-1 shows a PCB layout example with the signals and key components labeled.



A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

图 12-1. Layout Example

图 12-2 and 图 12-3 show the top and bottom layer traces and copper.

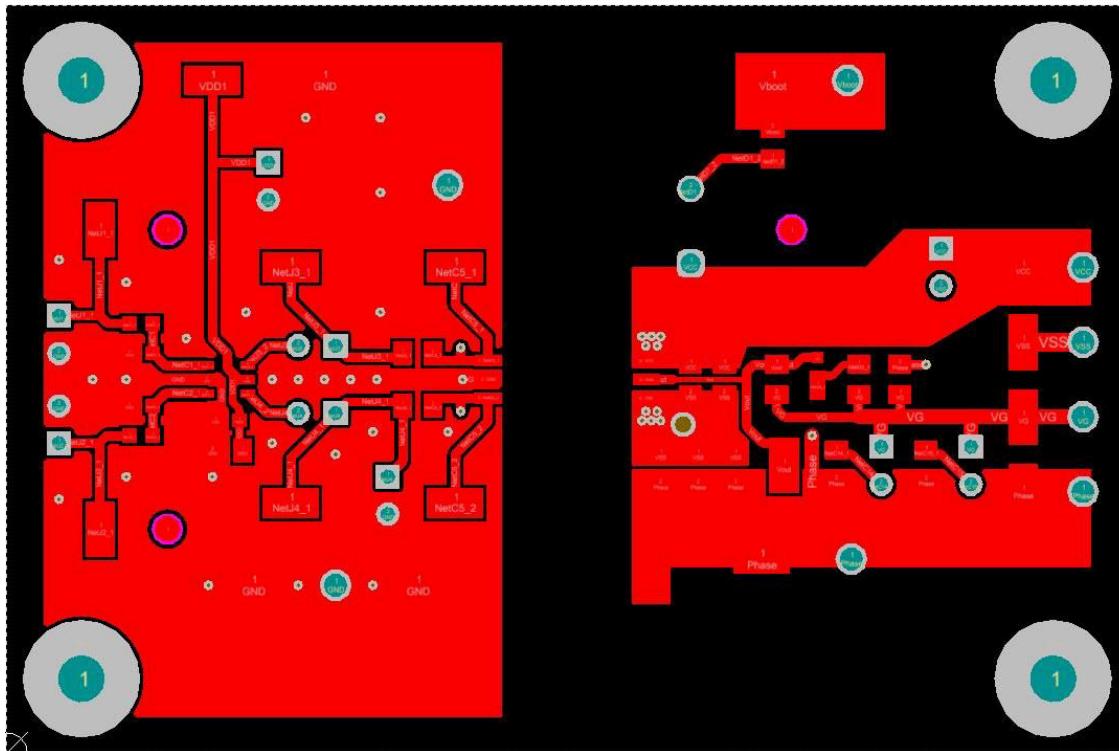


图 12-2. Top-Layer Traces and Copper

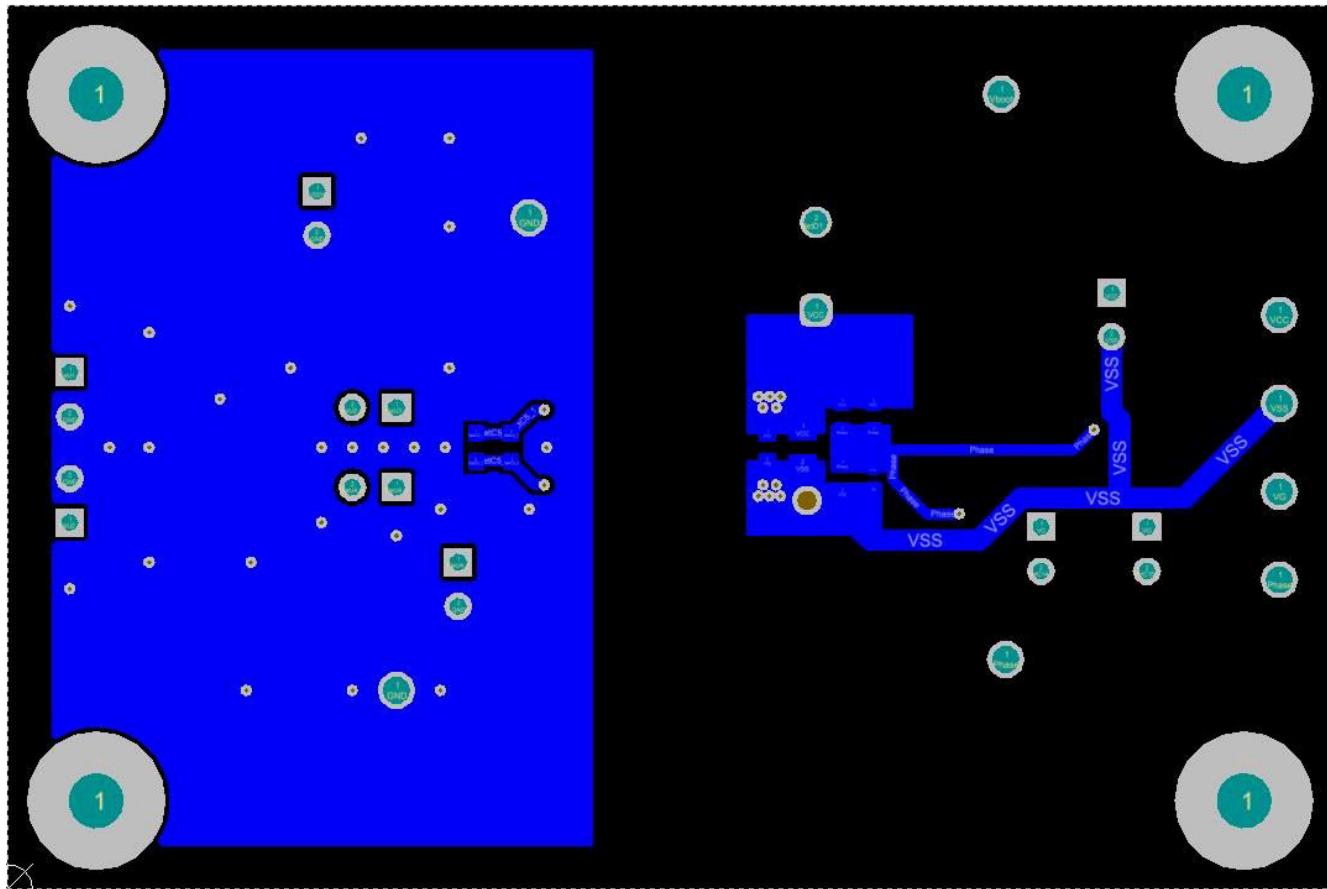
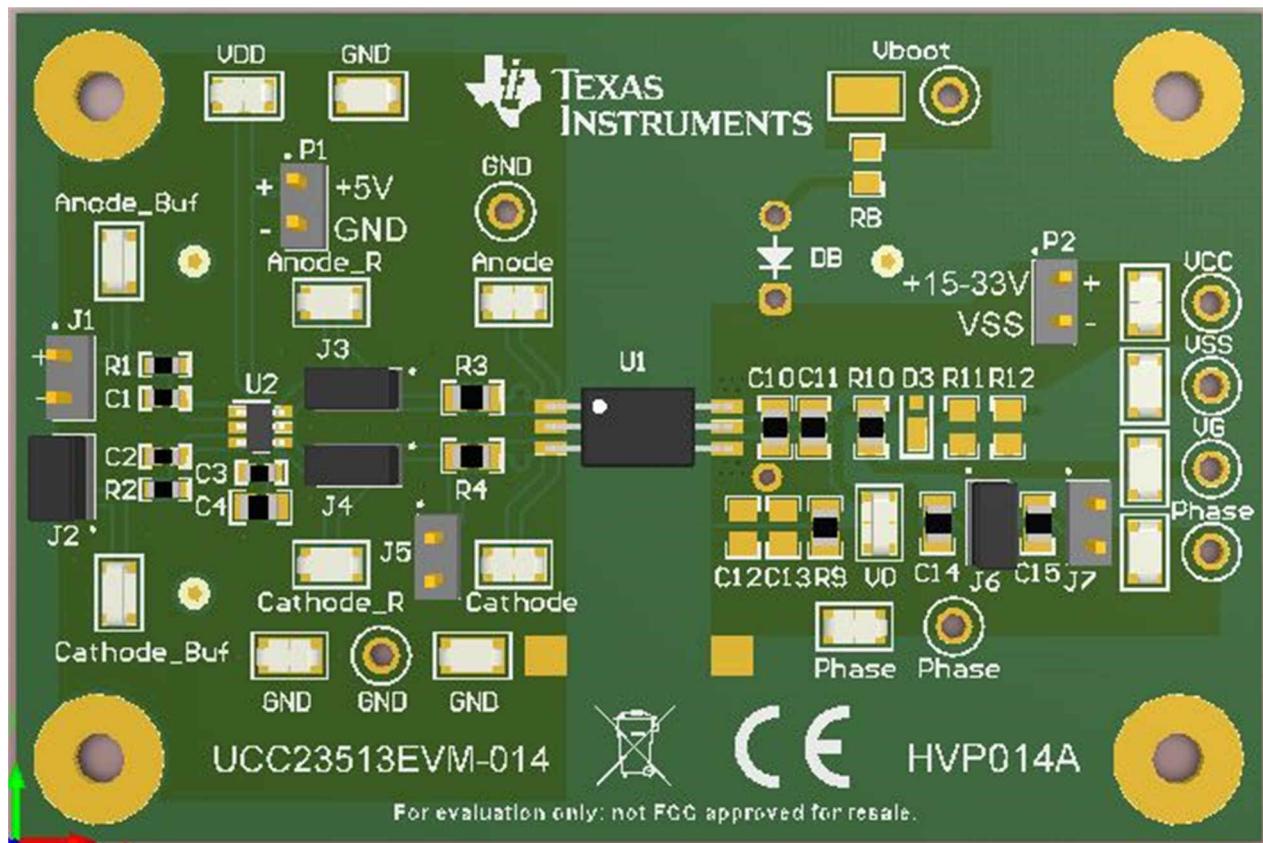


图 12-3. Bottom-Layer Traces and Copper (Flipped)

图 12-4 shows the 3D layout of the top view of the PCB.



A. The location of the PCB cutout between primary side and secondary sides ensures isolation performance.

图 12-4. 3-D PCB View

### 12.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC23511QDWYQ1	Obsolete	Production	SOIC (DWY)   6	-	-	Call TI	Call TI	-40 to 125	UC23511Q
UCC23511QDWYRQ1	Active	Production	SOIC (DWY)   6	850   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(C23511Q, UC23511Q )
UCC23511QDWYRQ1.A	Active	Production	SOIC (DWY)   6	850   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(C23511Q, UC23511Q )

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF UCC23511-Q1 :**

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- Catalog : [UCC23511](#)

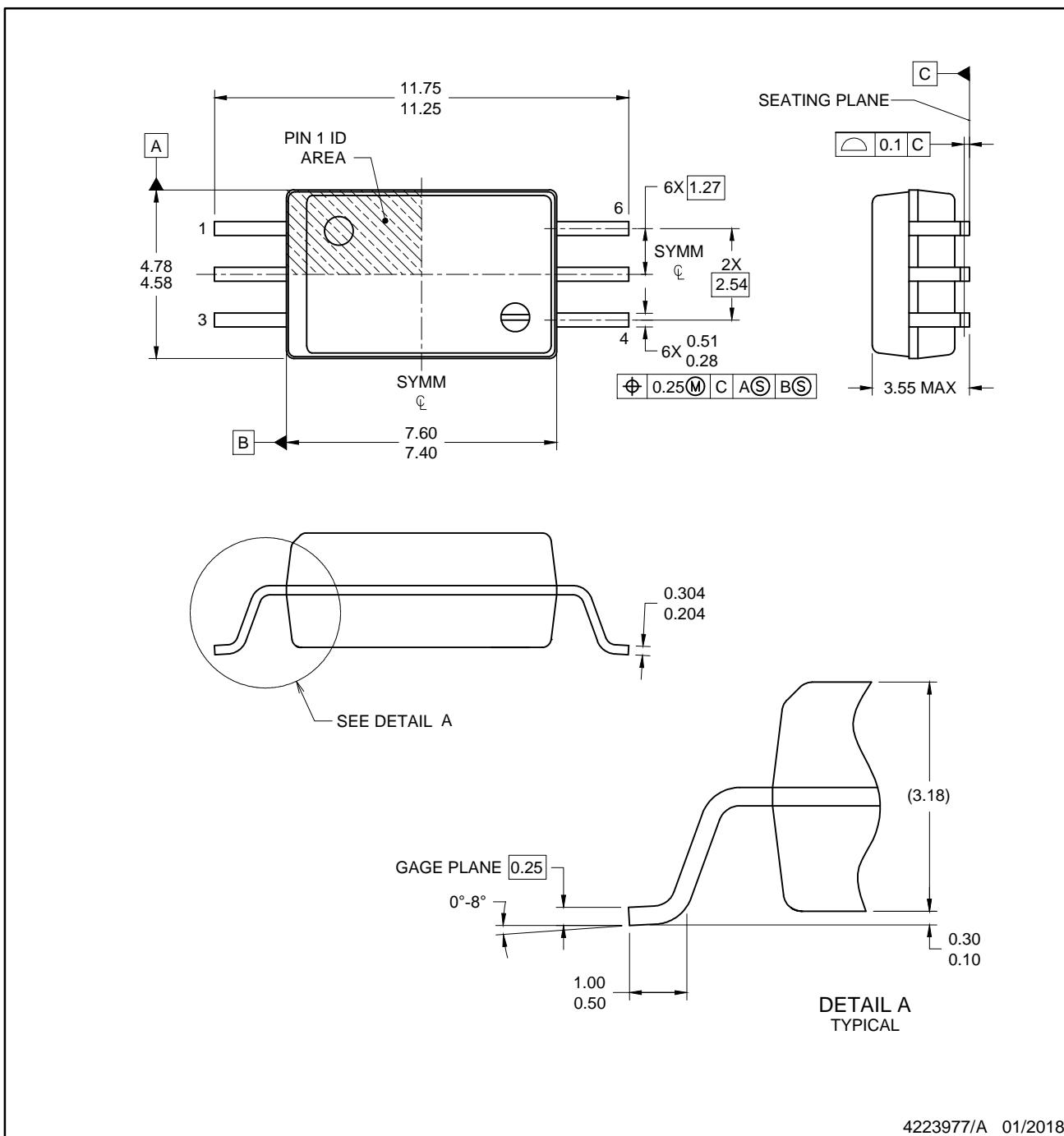
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## PACKAGE OUTLINE

**SOIC -3.55 mm max height**

SOIC



4223977/A 01/2018

## NOTES:

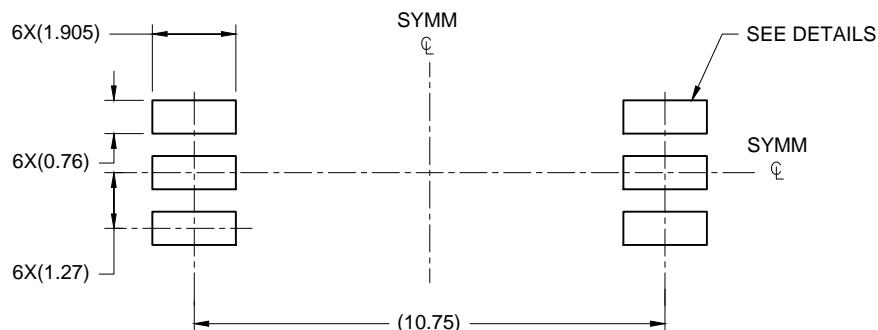
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.70 per side.

# EXAMPLE BOARD LAYOUT

DWY0006A

SOIC - 3.55 mm max height

SOIC



LAND PATTERN EXAMPLE

SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

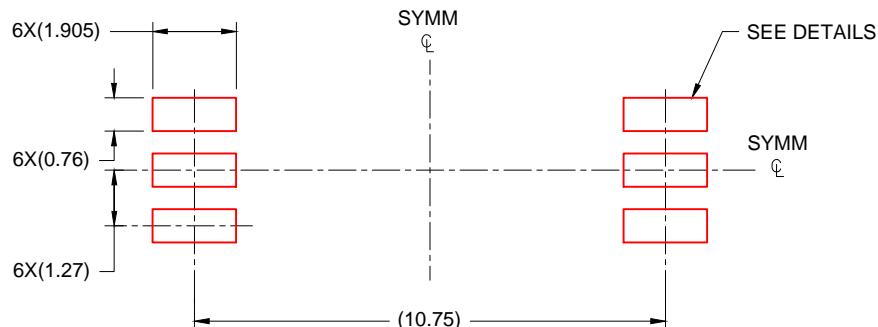
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DWY0006A

SOIC - 3.55 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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