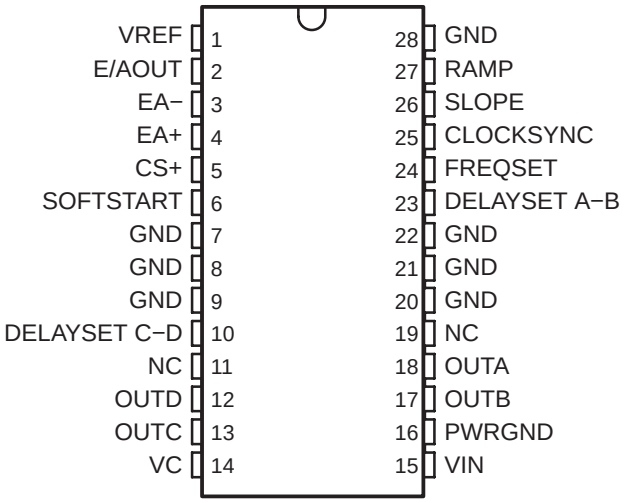
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −25°C to 110°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Zero to 100% Duty Cycle Control**
- **Programmable Output Turn-On Delay**
- **Compatible with Voltage or Current Mode Topologies**
- **Practical Operation at Switching Frequencies to 1 MHz**
- **Four 2 A Totem Pole Outputs**
- **10 MHz Error Amplifier**
- **Under-Voltage Lockout**
- **Low Startup Current −150 μA**
- **Outputs Active Low During UVLO**
- **Soft-Start Control**
- **Latched Over-Current Comparator With Full Cycle Restart**
- **Trimmed Reference**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DW PACKAGE
(TOP VIEW)



NC = No Connect

description/ordering information

The UC2875 integrated circuit implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This circuit may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A−B, C−D).

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−25°C to 110°C	SOP − DW	Tape and reel	UC2875SDWREP	UC2875SEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information

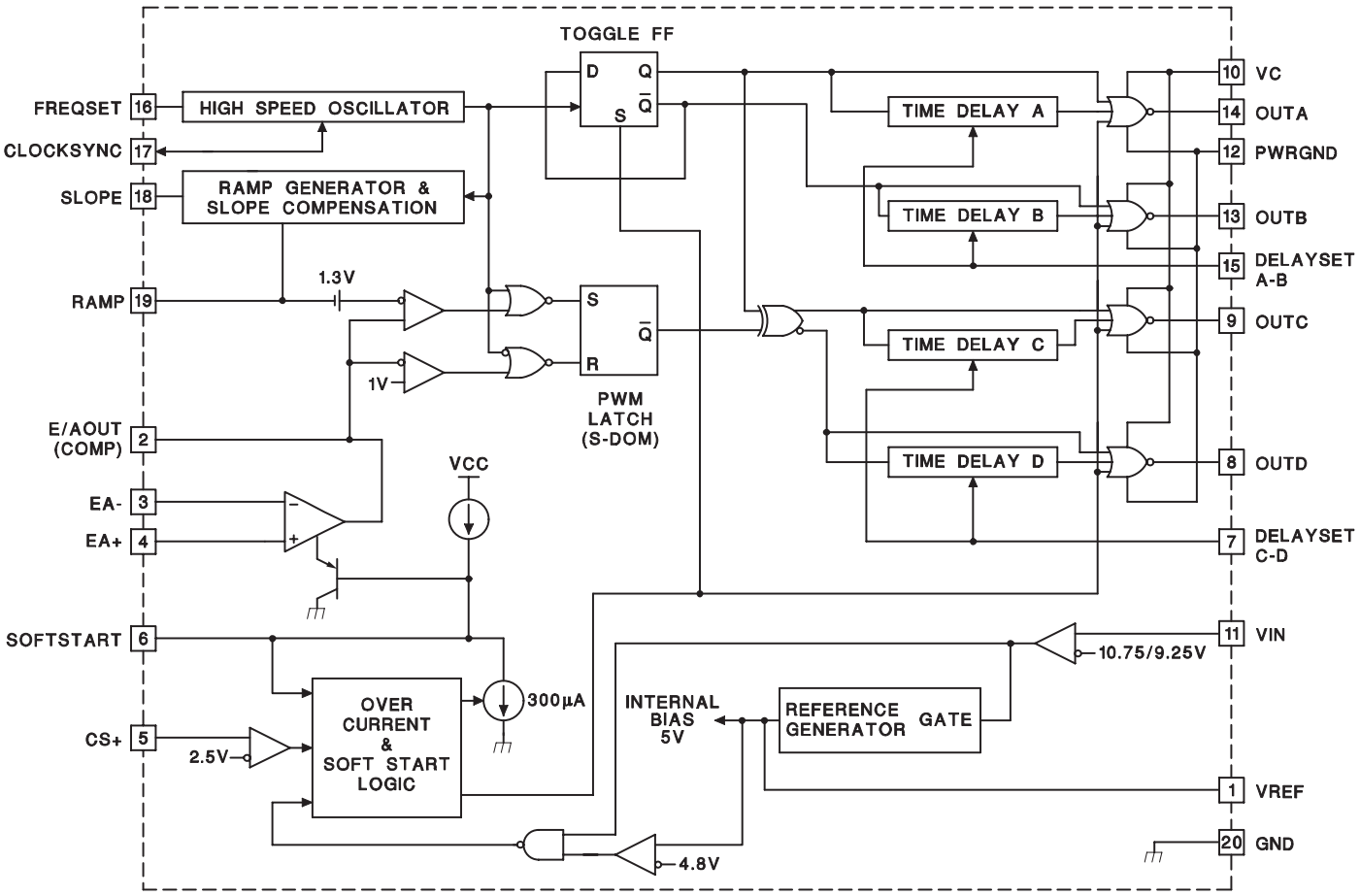
With the oscillator capable of operation at frequencies in excess of 2 MHz, overall switching frequencies to 1 MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75 V threshold. 1.5 V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided, and will latch the outputs in the OFF state within 70 ns of a fault. The current-fault circuitry implements full-cycle restart operation.

Additional features include an error amplifier with band-width in excess of 7 MHz, a 5 V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

This device is available in 28-pin “bat-wing” SOIC plastic package for operation over −25°C to +110°C operation.

block diagram



Ordering Information

UC 287 5 S DW R EP

- EP — ENHANCED PLASTIC INDICATOR
- R — TAPE and REEL INDICATOR
- DW — PACKAGE
  - DW = Plastic SOIC
- S — TEMPERATURE INDICATOR
  - S = −25°C to 110°C
- 5 — PRODUCT OPTION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply voltage (VC, VIN) . . . . . 20 V
Output current (sink or source), I_O, DC . . . . . 0.50 A
Pulse (0.5 μs) . . . . . 3 A
Analog I/O voltage . . . . . −0.3 V to 5.3 V
Operating jucntion temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

electrical characteristics, T_A = −25°C to 110°C, VC = VIN = 12 V, $R_{FREQSET}$ = 12 kΩ, $C_{FREQSET}$ = 330 pF, R_{SLOPE} = 12 kΩ, C_{RAMP} = 200 pF, $C_{DELAYSET\ A–B}$ = $C_{DELAYSET\ C–D}$ = 0.01 μF, $I_{DELAYSET\ A–B}$ = $I_{DELAYSET\ C–D}$ = −500 μA, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start threshold			10.75	11.75	V
UVLO hysteresis		0.5	1.25	2	V
Supply Current					
Supply current, I_{IN} startup	VIN = 8 V, VC = 20 V, R_{SLOPE} open, I_{DELAY} = 0		150	600	μA
Supply current, I_C startup	VIN = 8 V, VC = 20 V, R_{SLOPE} open, I_{DELAY} = 0		10	100	μA
Supply current, I_{IN}			30	44	mA
Supply current, I_C			15	30	mA
Voltage Reference					
Output voltage	T_J = 25°C	4.92	5	5.08	V
Line regulation voltage	VIN = 11 V to 20 V		1	10	mV
Load regulation voltage	I_{VREF} = −10 mA		5	20	mV
Total variation	Line, Load, Temperature	4.9		5.1	V
Noise voltage	10 Hz to 10 kHz		50		μVrms
Long term stability	1000 hours, T_J = 125°C		2.5		mV
Short circuit current	VREF = 0 V, T_J = 25°C		60		mA
Error Amplifier					
Offset voltage			5	15	mV
Input bias current			0.6	3	μA
Open loop voltage gain (A_{VOL})	$V_{E/AOUT}$ = 1 V to 4 V	60	90		dB
Common mode rejection ratio (CMRR)	V_{CM} = 1.5 V to 5.5 V	75	95		dB
PSRR	VIN = 11 V to 20 V	85	100		dB
Output sink current	$V_{E/AOUT}$ = 1 V	1	2.5		mA
Output source current	$V_{E/AOUT}$ = 4 V		−1.3	−0.5	mA
High-level output voltage (V_{OH})	$I_{E/AOUT}$ = −0.5 mA	4	4.7	5	V
Low-level output voltage (V_{OL})	$I_{E/AOUT}$ = 1 mA	0	0.5	1	V
Unity gain bandwidth		7	11		MHz
Slew rate		6	11		V/μsec

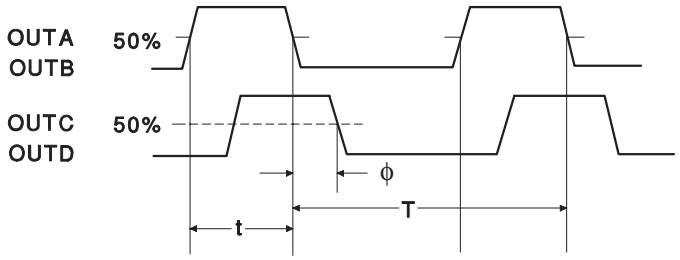
electrical characteristics, T_A = −25°C to 110°C, VC = VIN = 12 V, $R_{FREQSET}$ = 12 kΩ, $C_{FREQSET}$ = 330 pF, R_{SLOPE} = 12 kΩ, C_{RAMP} = 200 pF, $C_{DELAYSET\ A–B}$ = $C_{DELAYSET\ C–D}$ = 0.01 μF, $I_{DELAYSET\ A–B}$ = $I_{DELAYSET\ C–D}$ = −500 μA, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Comparator					
Ramp offset voltage	T_J = 25°C, See Note 3		1.3		V
Zero phase shift voltage	See Note 4	0.55	0.9		V
PWM phase shift (See Note 1)	$V_{E/AOUT}$ > (Ramp Peak + Ramp Offset)	98	99.5	102	%
	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	
Output Skew (See Note 1)	$V_{E/AOUT}$ < 1 V		5	±20	ns
Ramp to output delay	See Note 6		65	125	ns
Oscillator					
Initial accuracy	T_J = 25°C	0.85	1	1.15	MHz
Voltage stability	VIN = 11 V to 20 V		0.2	2	%
Total variation	Line, Temperature	0.80		1.20	MHz
Sync pin threshold	T_J = 25°C		3.8		V
Clock out peak	T_J = 25°C		4.3		V
Clock out low	T_J = 25°C		3.3		V
Clock out pulse width	$R_{CLOCKSYNC}$ = 3.9 kΩ		30	100	ns
Maximum frequency	$R_{FREQSET}$ = 5 kΩ	2			MHz
Ramp Generator/Slope Compensation					
Minimum ramp current	I_{SLOPE} = 10 μA, $V_{FREQSET}$ = VREF		−11	−14	μA
Maximum ramp current	I_{SLOPE} = 1 mA, $V_{FREQSET}$ = VREF	−0.8	−0.95		mA
Ramp valley			0		V
Ramp peak − clamping level	$R_{FREQSET}$ = 100 kΩ		3.8	4.1	V
Current Limit					
Input bias current	V_{CS}+ = 3 V		2	5	μA
Threshold voltage		2.4	2.5	2.6	V
Delay to output			85	150	ns
Soft-Start/Reset Delay					
Charge current	$V_{SOFTSTART}$ = 0.5 V	−20	−9	−3	μA
Discharge current	$V_{SOFTSTART}$ = 1 V	120	230		μA
Restart threshold		4.3	4.7		V
Discharge level			300		mV

electrical characteristics, T_A = −25°C to 110°C, VC = VIN = 12 V, $R_{FREQSET}$ = 12 kΩ, $C_{FREQSET}$ = 330 pF, R_{SLOPE} = 12 kΩ, C_{RAMP} = 200 pF, $C_{DELAYSET\ A-B}$ = $C_{DELAYSET\ C-D}$ = 0.01 μF, $I_{DELAYSET\ A-B}$ = $I_{DELAYSET\ C-D}$ = −500 μA, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Drivers					
Output low level	I_{OUT} = 50 mA		0.2	0.4	V
	I_{OUT} = 500 mA		1.2	2.6	
Output high level	I_{OUT} = −50 mA		1.5	2.5	V
	I_{OUT} = −500 mA		1.7	2.6	
Delay Set					
Delay set voltage	I_{DELAY} = −500 μA	2.3	2.4	2.6	V
Delay time	I_{DELAY} = −250 μA, See Notes 2 and 5	150	250	600	ns

NOTES:
1. Phase shift percentage (0% = 0°, 100% = 180°) is defined as θ = 200/T Φ% , where θ is the phase shift, and Φ and T are defined in Figure 1. At 0% phase shift, Φ is the output skew.
2. Delay time is defined as delay = T (1/2−(duty cycle)), where T is defined in Figure 1.
3. Ramp offset voltage has a temperature coefficient of about 4.0 mV/°C.
4. Zero phase shift voltage has a temperature coefficient of about 2.0 mV/°C.
5. Delay time can be programmed via resistors from the delay set pins to ground. Delay time ≈ $(62.5 \times 10^{-12}) / I_{DELAY}$ sec where I_{DELAY} = Delay set voltage / R_{DELAY}. The recommended range for I_{DELAY} is 25 μA ≤ I_{DELAY} ≤ 1 mA
6. Ramp delay to output time is defined in NO TAG.



Duty Cycle = t/T Period = T
T_{DHL}(A to C) = T_{DHL}(B to D) = ϕ
Phase Shift, Output Skew, and Delay Time Definitions

Figure 1. Phase Shift and Output Skew

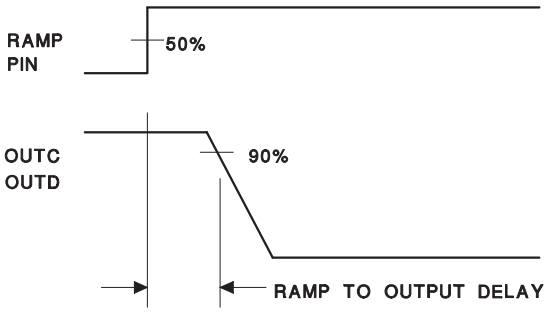


Figure 2. Delay Time

APPLICATION AND OPERATION INFORMATION

Pin Descriptions

CLOCKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (error amplifier output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (current sense):The non-inverting input to the current- fault comparator whose reference is set internally to a fixed 2.5 V (separate from VREF). When the voltage at this pin exceeds 2.5 V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise −− this condition will not prematurely deliver power to the load.

FREQSET (oscillator frequency set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELAYSET A−B, DELAYSET C−D (output delay control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA− (error amplifier inverting input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (error amplifier non-inverting input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (signal ground):All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on V_{IN} and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA−OUTD (outputs A−D): The outputs are 2 A totem- pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A−B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C−D pair will drive the other half-bridge with switching phase shifted with respect to the A−B outputs.

PWRGND (power ground):VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (voltage ramp):This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{SenseVoltage}}{R_{SLOPE} \times C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

APPLICATION AND OPERATION INFORMATION

Because of the 1.3 V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

SLOPE (set ramp slope/slope compensation): A resistor from this pin to V_{CC} will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

SOFTSTART (soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8 V by an internal 9 μA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5 V), SOFTSTART will be pulled to GND and them ramp to 4.8 V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

VC (output switch supply voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors.

VIN (primary chip supply voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12 V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100 μA to a current in excess of 20 μA. If the UC2875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

VREF: This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75 V. For best results bypass VREF with a 0.1 μF, low ESR, low ESL, capacitor to the GND pin.

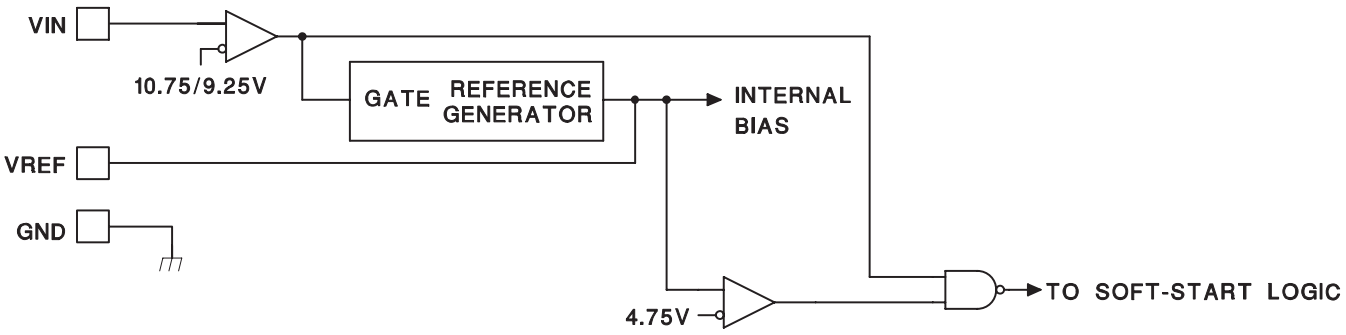


Figure 3. Undervoltage Lockout

When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600 μA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75 V.

APPLICATION AND OPERATION INFORMATION

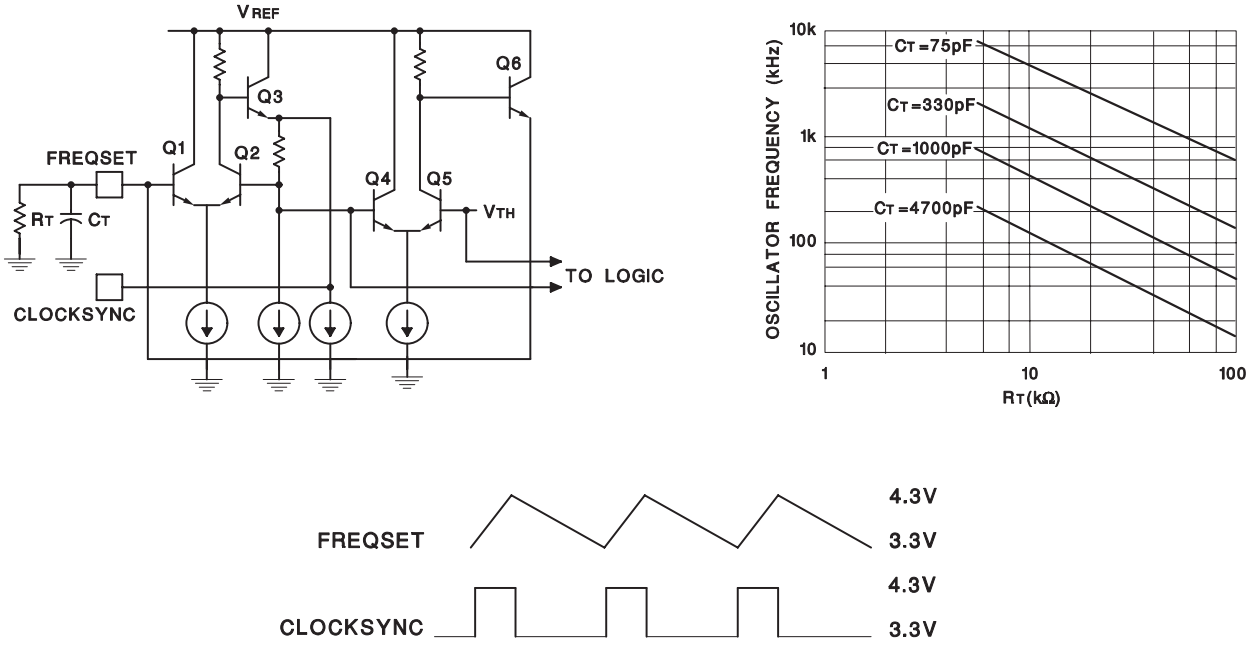


Figure 4. Oscillator Schematic, Frequency vs Resistance Graph, and Timing Diagram

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC2875 devices simply by connecting the CLOCKSYNC of each UC2875 to the others as in Figure 5.

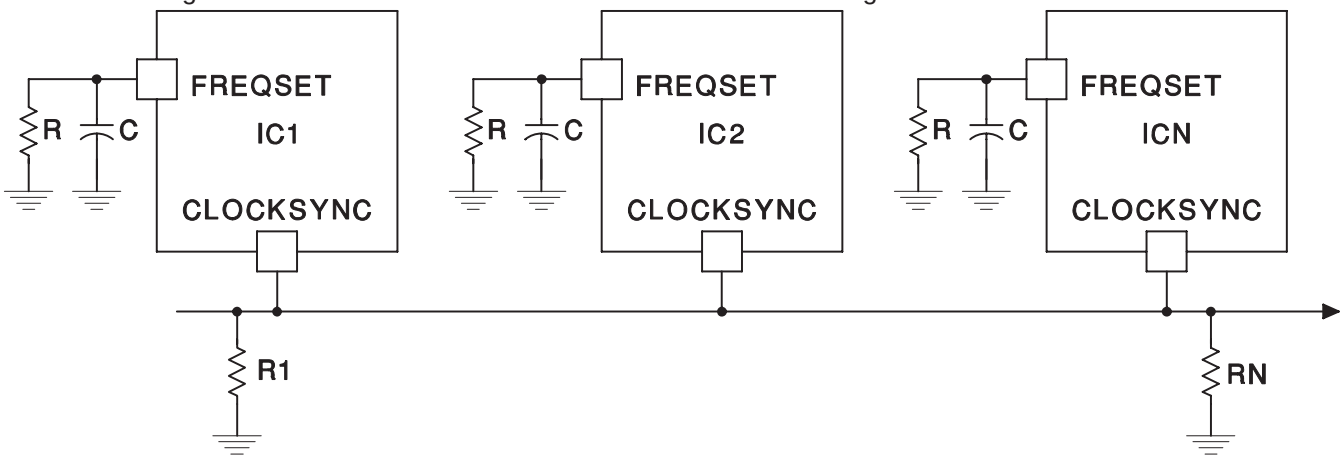


Figure 5. Synchronizing Multiple UC2875−EP Devices

All ICs will sync to chip with the fastest local oscillator.

R1 & RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 & RN may also be needed to properly terminate R_{SYNC} line.

APPLICATION AND OPERATION INFORMATION

Syncing to External TTL/CMOS

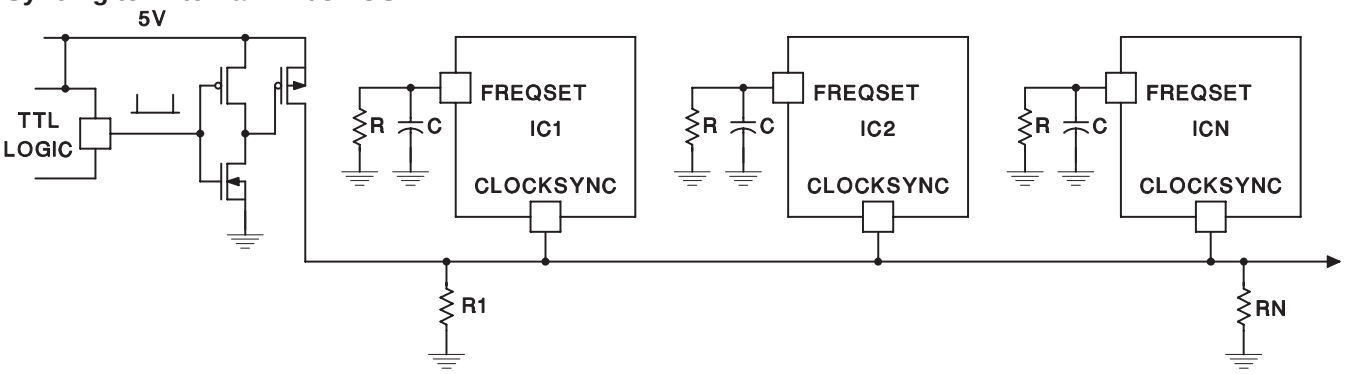


Figure 6. Snychronizing to an External TTL/CMOS Clock Signal

ICs will sync to fastest chip or TTL clock if it is higher frequency.

R and RN may be needed for same reasons as above.

Although each UC2875 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in Figure 6.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

Delay Blocks and Output Stages

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

APPLICATION AND OPERATION INFORMATION

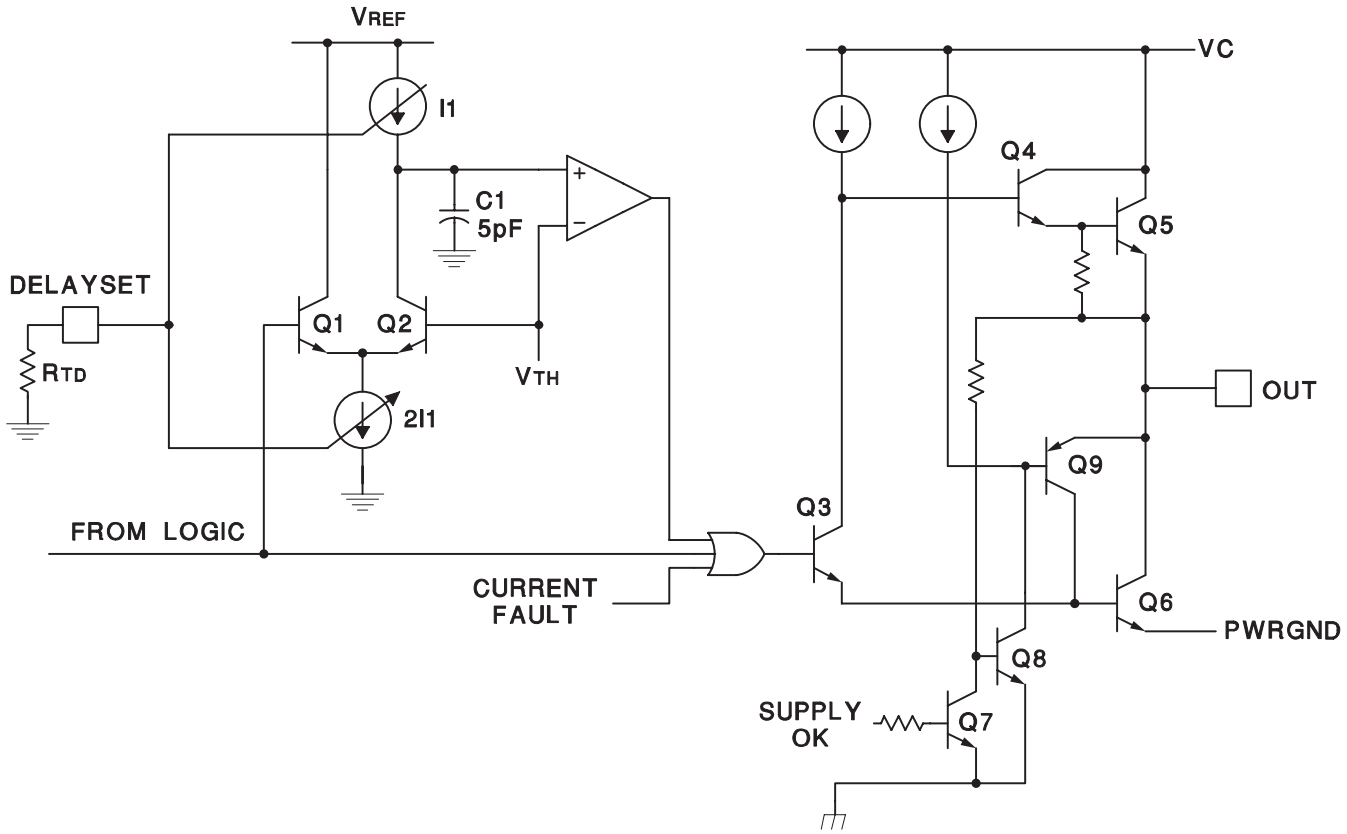


Figure 7. Delay Blocks and Output Stages

The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD} . The voltage on the Delay Set pins is internally regulated to 2.5 V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuitry, and the delay time must be programmed.

Output Switch Orientation

The four outputs of the UC2875 interface to the full bridge converter switches as shown in Figure 8.

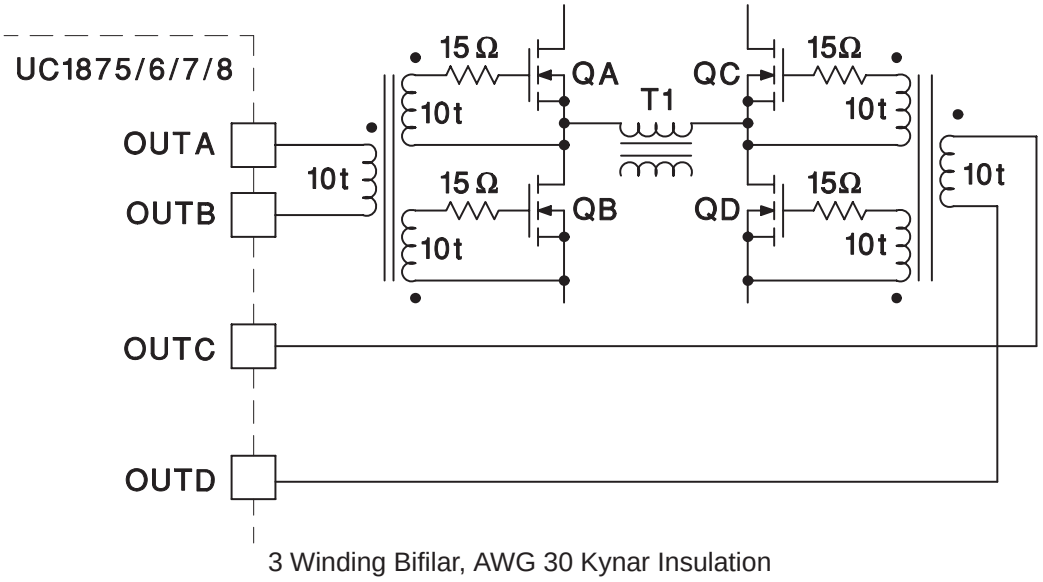


Figure 8. Output Switch Orientation

APPLICATION AND OPERATION INFORMATION

Fault/Soft-Start

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT−START capacitor.

The fault logic insures that a continuous fault will institute a low frequency “hiccup” retry cycle by forcing the SOFT−START capacitor to charge through its full cycle between each restart attempt.

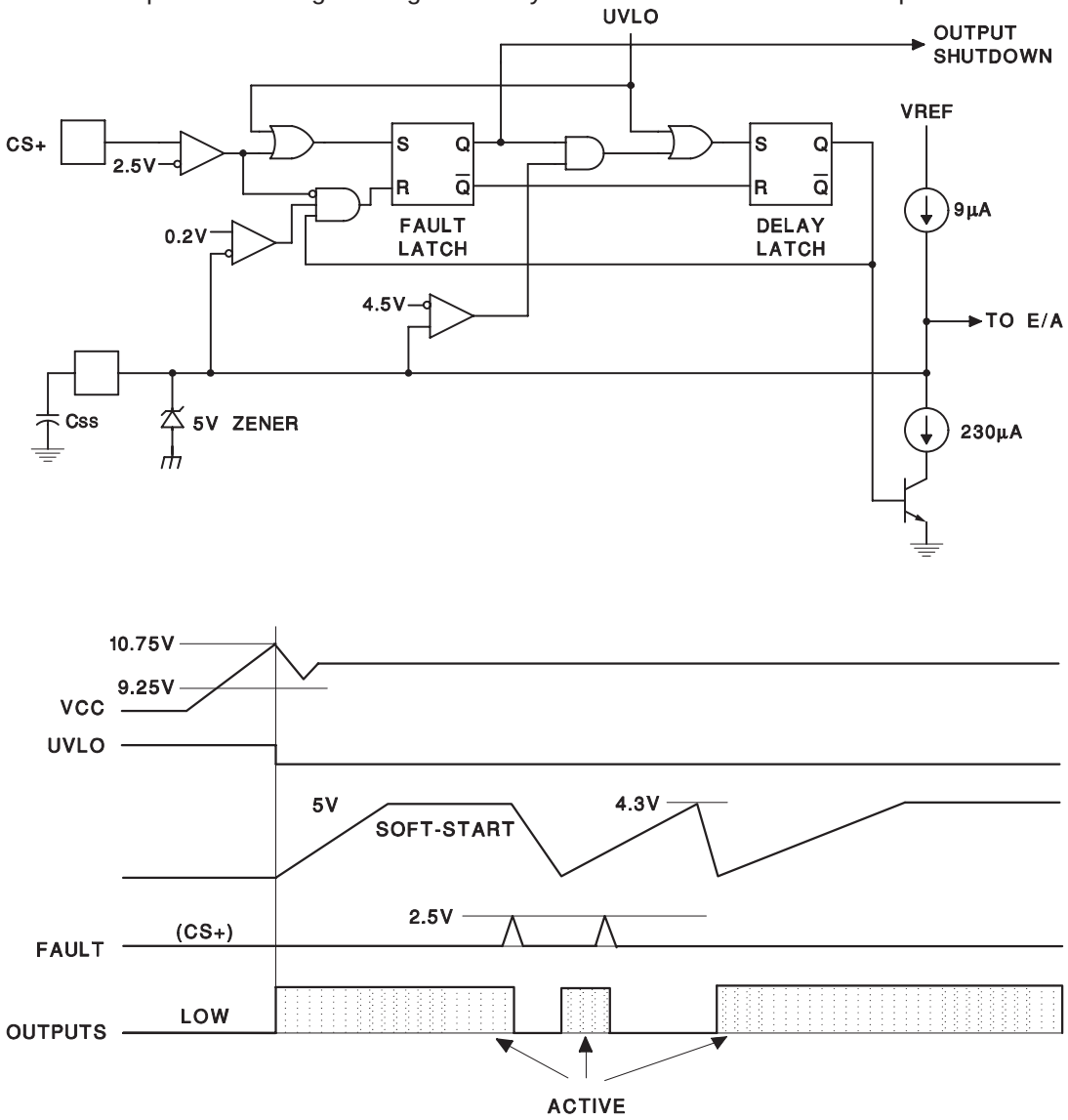


Figure 9. Fault/Soft-Start

APPLICATION AND OPERATION INFORMATION

Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

Figure 10 shows a voltage-mode configuration. With R_{SLOPE} tied to a stable voltage source, the waveform on C_{RAMP} will be a constant-slope ramp, providing conventional voltage-mode control. If R_{SLOPE} is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

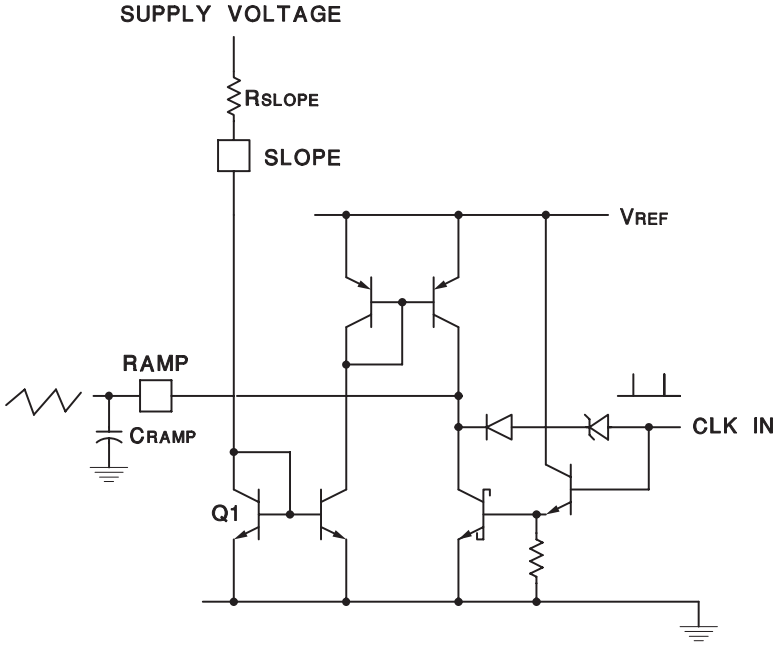


Figure 10. Slope/Ramp Pins

1. Simple voltage mode operation achieved by placing R_{SLOPE} between VIN and SLOPE.
2. Voltage Feedforward achieved by placing R_{SLOPE} between supply voltage and SLOPE pin of UC2875.

RAMP

$$\frac{dV}{dT} \approx \frac{V_{Rslope}}{R_{SLOPE} \times C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2875SDWREP	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	-25 to 110	UC2875SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UC2875-EP :

- Catalog : UC2875

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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