UC1846-EP
CURRENT-MODE PWM CONTROLLER

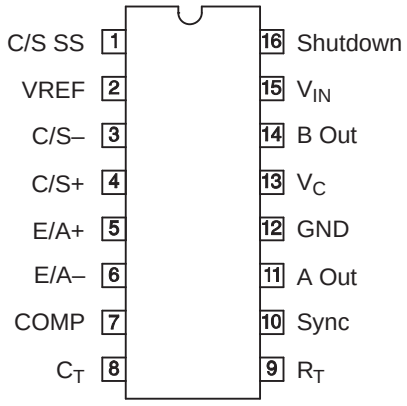
SGLS329 – MAY 2006

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Automatic Feed-Forward Compensation**
- **Programmable Pulse-by-Pulse Current Limiting**
- **Automatic Symmetry Correction in Push-Pull Configuration**
- **Enhanced Load-Response Characteristics**
- **Parallel Operation Capability for Modular Power Systems**
- **Differential Current-Sense Amplifier With Wide Common-Mode Range**
- **Double Pulse Suppression**
- **500-mA (Peak) Totem-Pole Outputs**
- **±1% Bandgap Reference**
- **Undervoltage Lockout**
- **Soft-Start Capability**
- **Shutdown Terminal**
- **500-kHz Operation**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The UC1846-EP control IC provides all of the necessary features to implement fixed-frequency, current-mode control schemes, while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load-response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current-limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel power modules, while maintaining equal current sharing.

Protection circuitry includes built-in undervoltage lockout and programmable current limit, in addition to soft-start capability. A shutdown function is also available, which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846-EP features low outputs in the OFF state.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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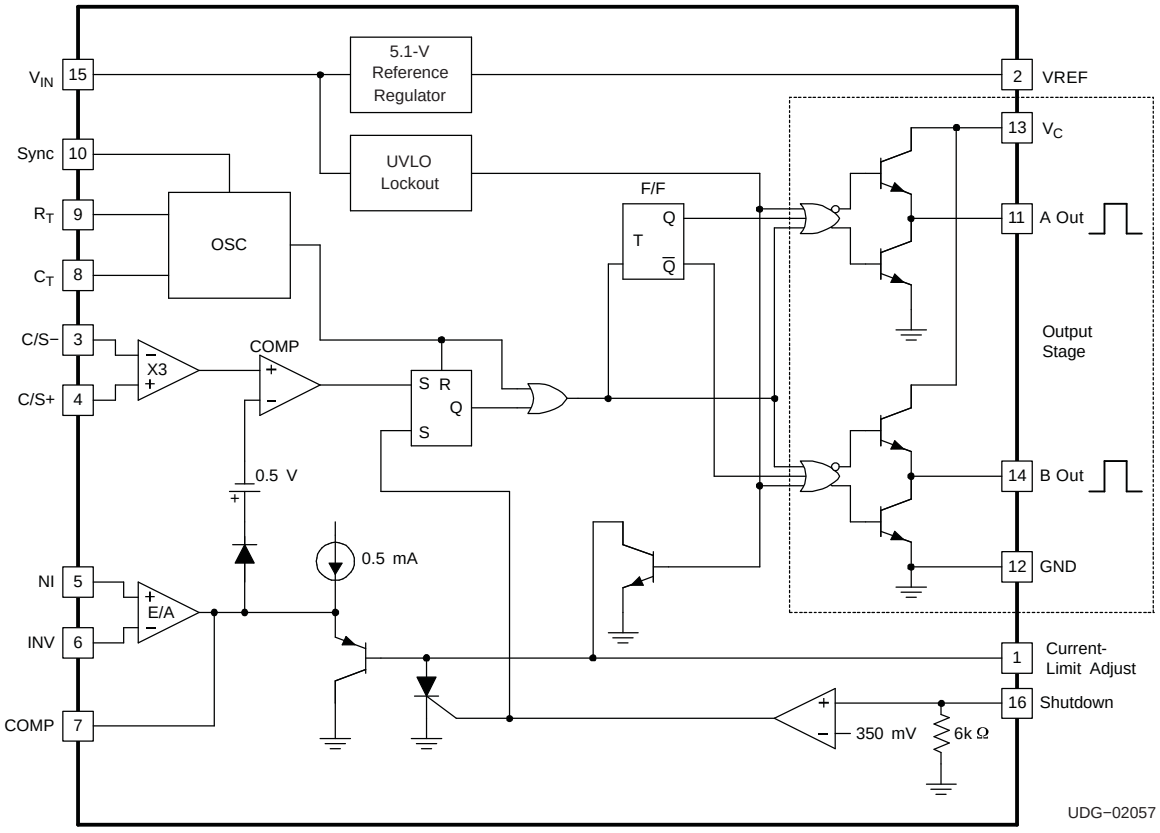
ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – DW	UC1846MDWREP	UC1846MEP

BLOCK DIAGRAM



Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
Supply voltage (pin 15)			40	V
Collector supply voltage (pin 13)			40	V
Output current, source or sink (pins 11, 14)			500	mA
Analog inputs (pins 3, 4, 5, 6, 16)		–0.3	V_{IN}	V
Reference output current (pin 2)			–30	mA
Sync output current (pin 10)			–5	mA
Error amplifier output current (pin 7)			–5	mA
Soft-start sink current (pin 1)			50	mA
Oscillator charging current (pin 9)			5	mA
Power dissipation	T_A = 25°C		1000	mW
	T_C = 25°C		2000	
Storage temperature range		–65	150	°C
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, pin 13. Currents are positive into, negative out of the specified terminal.

Electrical Characteristics

T_A = –55°C to 125°C, V_{IN} = 15 V, R_T = 10 k, C_T = 4.7 nF, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference					
Output voltage	T_J = 25°C, I_O = 1 mA	5.05	5.1	5.15	V
Line regulation	V_{IN} = 8 V to 40 V		5	20	mV
Load regulation	I_L = 1 mA to 10 mA		3	15	mV
Temperature stability	Over operating range(1)		0.4		mV/°C
Total output variation	Line, load, and temperature(1)	5		5.2	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C(1)		100		μV
Long-term stability	T_J = 125°C, 1000 h		5		mV
Short-circuit output current	V_{REF} = 0 V	–10	–45		mA
Oscillator					
Initial accuracy	T_J = 25°C	39	43	47	kHz
Voltage stability	V_{IN} = 8 V to 40 V		–1	2	%
Temperature stability	Over operating range(1)		–1		%
Sync output high level		3.9	4.35		V
Sync output low level			2.3	2.5	V
Sync input high level	Pin 8 = 0 V	3.9			V
Sync input low level	Pin 8 = 0 V			2.5	V
Sync input current	Sync voltage = 3.9 V, Pin 8 = 0 V		1.3	1.5	mA
Error Amplifier					
Input offset voltage			0.5	5	mV
Input bias current			–0.6	–1	μA
Input offset current			40	250	nA
Common-mode range	V_{IN} = 8 V to 40 V	0		V_{IN} – 2	V
Open-loop voltage gain	ΔV_O = 1.2 V to 3 V, V_{CM} = 2 V	80	105		dB
Unity gain bandwidth	T_J = 25°C(1)	0.7	1		MHz
CMRR	V_{CM} = 0 V to 38 V, V_{IN} = 40 V	75	100		dB
PSRR	V_{IN} = 8 V to 40 V	80	105		dB
Output sink current	V_{ID} = –15 mV to –5 V, V_{PIN7} = 1.2 V	2	6		mA
Output source current	V_{ID} = 15 mV to 5 V, V_{PIN7} = 2.5 V	–0.4	–0.5		mA
High-level output voltage	R_L = 15 kΩ (pin 7)	4.3	4.6		V
Low-level output voltage	R_L = 15 kΩ (pin 7)		0.7	1	V

(1) These parameters, although specified over the recommended operating conditions, are not 100% tested in production.

Electrical Characteristics (continued)

T_A = –55°C to 125°C, V_{IN} = 15 V, R_T = 10 k, C_T = 4.7 nF, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current-Sense Amplifier					
Amplifier gain	V_{PIN3} = 0 V, Pin 1 open(2)(3)	2.5	2.75	3	V
Maximum differential input signal (V_{PIN4} – V_{PIN3})	Pin 1 open,(2) R_L (pin 7) = 15 kW	1.1	1.2		V
Input offset voltage	V_{PIN1} = 0.5 V, Pin 7 open(2)		5	25	mV
CMRR	V_{CM} = 1 V to 12 V	60	83		dB
PSRR	V_{IN} = 8 V to 40 V	60	84		dB
Input bias current	V_{PIN1} = 0.5 V, Pin 7 open(2)		–2.5	–10	µA
Input offset current	V_{PIN1} = 0.5 V, Pin 7 open(2)		0.08	1	µA
Input common-mode range		0		V_{IN} – 3	V
Delay to outputs	T_J = 25°C(4)		200	500	ns
Current-Limit Adjust					
Current-limit offset	V_{PIN3} = 0 V, V_{PIN4} = 0 V, Pin 7 open(2)	0.45	0.5	0.55	V
Input bias current	V_{PIN5} = V_{REF}, V_{PIN6} = 0 V		–10	–30	µA
Shutdown Terminal					
Threshold voltage		250	350	400	mV
Input voltage range		0		V_{IN}	V
Minimum latching current (I_{PIN1})(5)		3	1.5		mA
Maximum nonlatching current (I_{PIN1})(6)			1.5	0.8	mA
Delay to outputs	T_J = 25°C(4)		300	600	ns
Output					
Collector-emitter voltage		40			V
Collector leakage current	V_C = 40 V			200	µA
Output low level	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 100 mA		0.4	2.1	
Output high level	I_{SOURCE} = 20 mA	13	13.5		V
	I_{SOURCE} = 100 mA	12	13.5		
Rise time	C_L = 1 nF, T_J = 25°C(4)		50	300	ns
Fall time	C_L = 1 nF, T_J = 25°C(4)		50	300	ns
Undervoltage Lockout					
Start-up threshold			7.7	8	V
Threshold hysteresis			0.75		V
Total Standby Current					
Supply current			17	21	mA

(2) Parameter measured at trip point of latch with V_{PIN5} = V_{REF}, V_{PIN6} = 0 V.
(3) Amplifier gain defined as:

$$G = \frac{(\Delta V_{PIN7})}{(\Delta V_{PIN4})}$$

where V_{PIN4} = 0 to 1 V
(4) These parameters, although specified over the recommended operating conditions, are not 100% tested in production.
(5) Current into pin 1 is ensured to latch circuit in shutdown state.
(6) Current into pin 1 is ensured not to latch circuit in shutdown state.

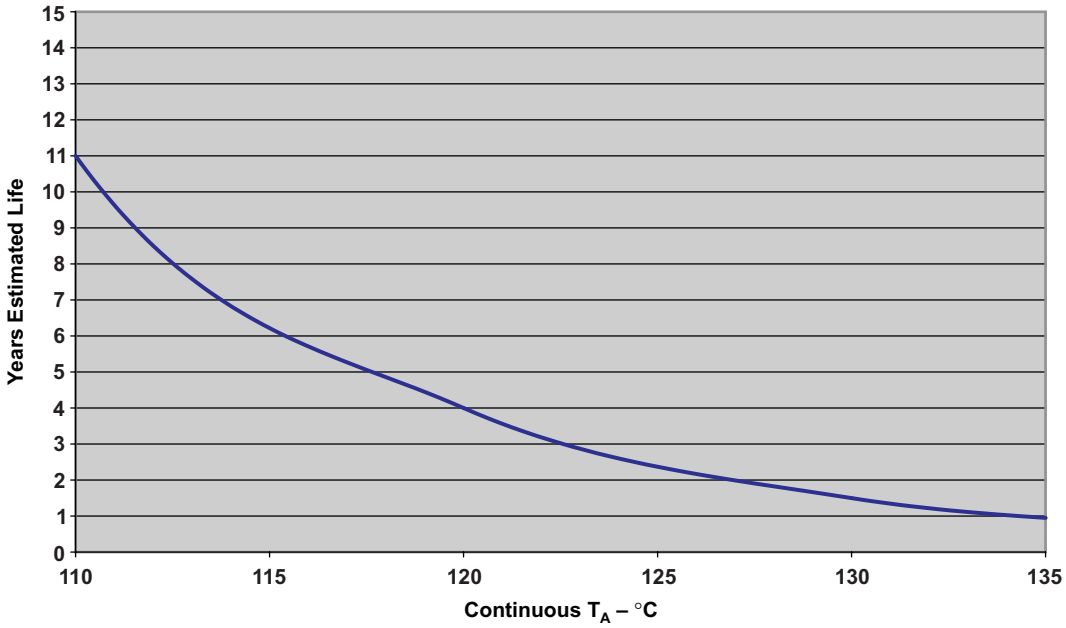
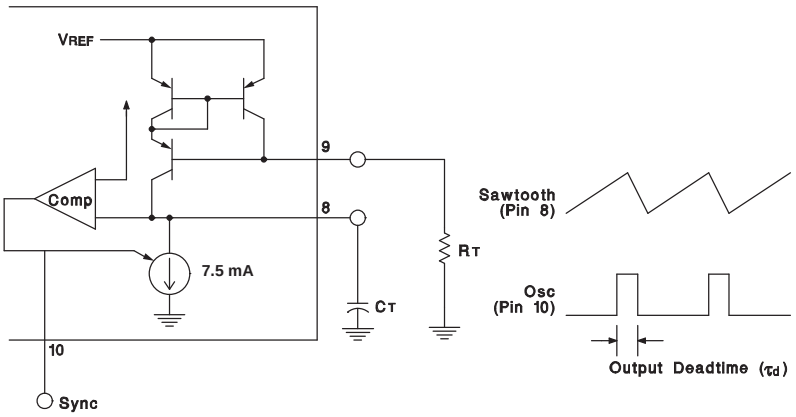


Figure 1. UC1846MDWREP Estimated Device Life at Elevated Temperatures Wirebond Voiding Fail Modes

APPLICATION INFORMATION



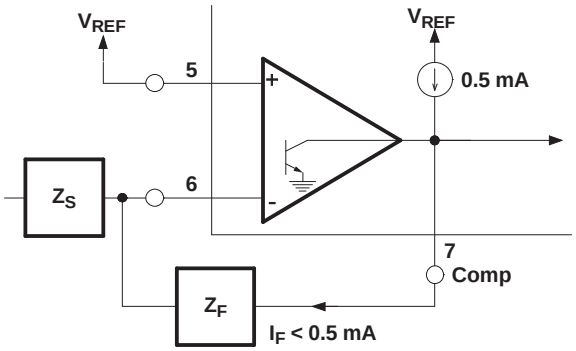
Output deadtime is determined by the external capacitor, C_T, according to the formula:

$$\tau d\ (\mu s) = 145 C_T\ (\mu f) \frac{ID}{ID - \frac{3.6}{R_T\ (k\Omega)}}$$

I_D = Oscillator discharge current at 25°C is typically 7.5 mA.
For large values of R_T: $\tau d\ (\mu s) \approx 145 C_T\ (\mu f)$

Oscillator frequency is approximated by the formula: $f_T\ (kHz) \approx \frac{2.2}{R_T\ (k\Omega) \times C_T\ (\mu f)}$

Figure 2. Oscillator Circuit



Error amplifier can source up to 0.5 mA.

Figure 3. Error-Amplifier Output Configuration

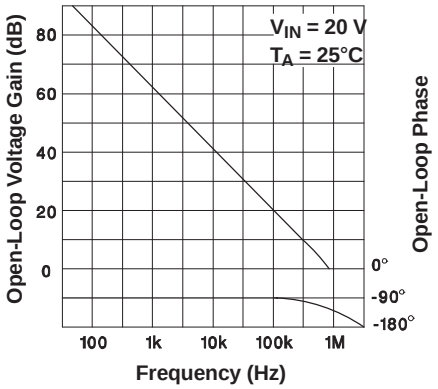


Figure 4. Error-Amplifier Gain and Phase vs Frequency

APPLICATION INFORMATION (continued)

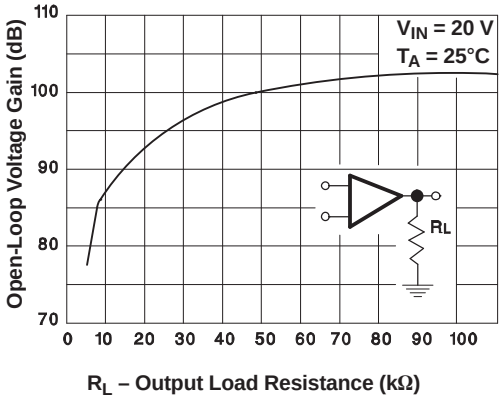
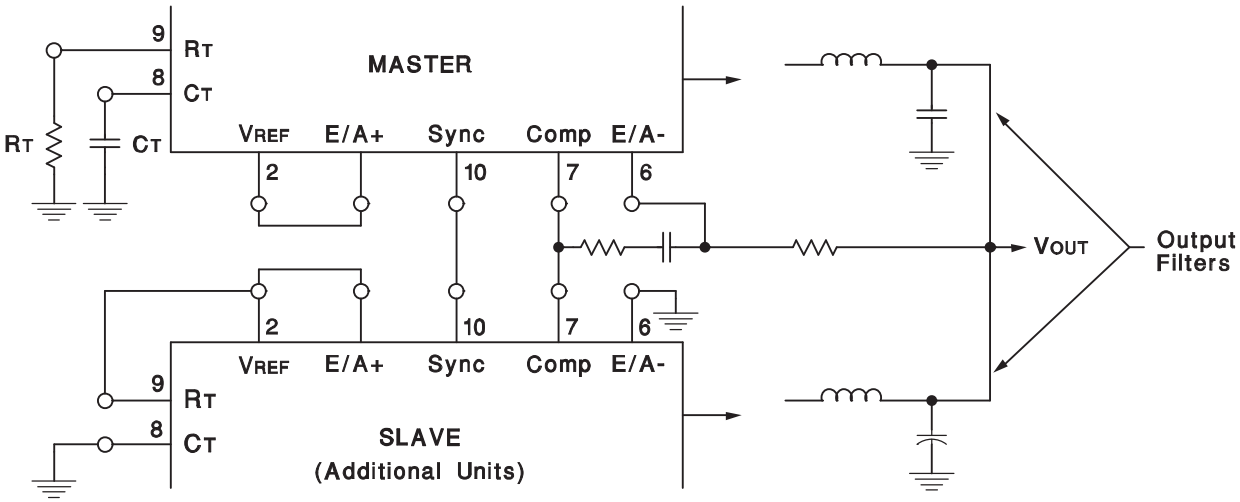


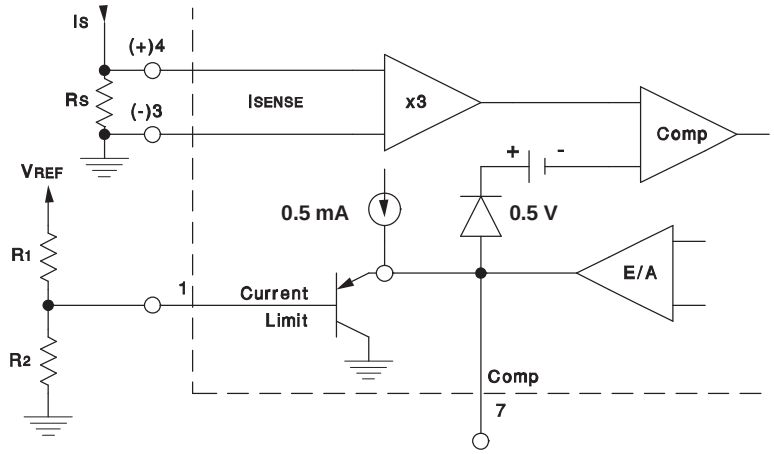
Figure 5. Error-Amplifier Open-Logic DC Gain vs Load Resistance



Slaving allows parallel operation of two or more units with equal current sharing.

Figure 6. Parallel Operation

APPLICATION INFORMATION (continued)



Peak current (IS) is determined by the formula: $I_S = \dfrac{\dfrac{R2\ V_{REF}}{R1 + R2} - 0.5}{3RS}$

Figure 7. Pulse-by-Pulse Current Limiting

APPLICATION INFORMATION (continued)

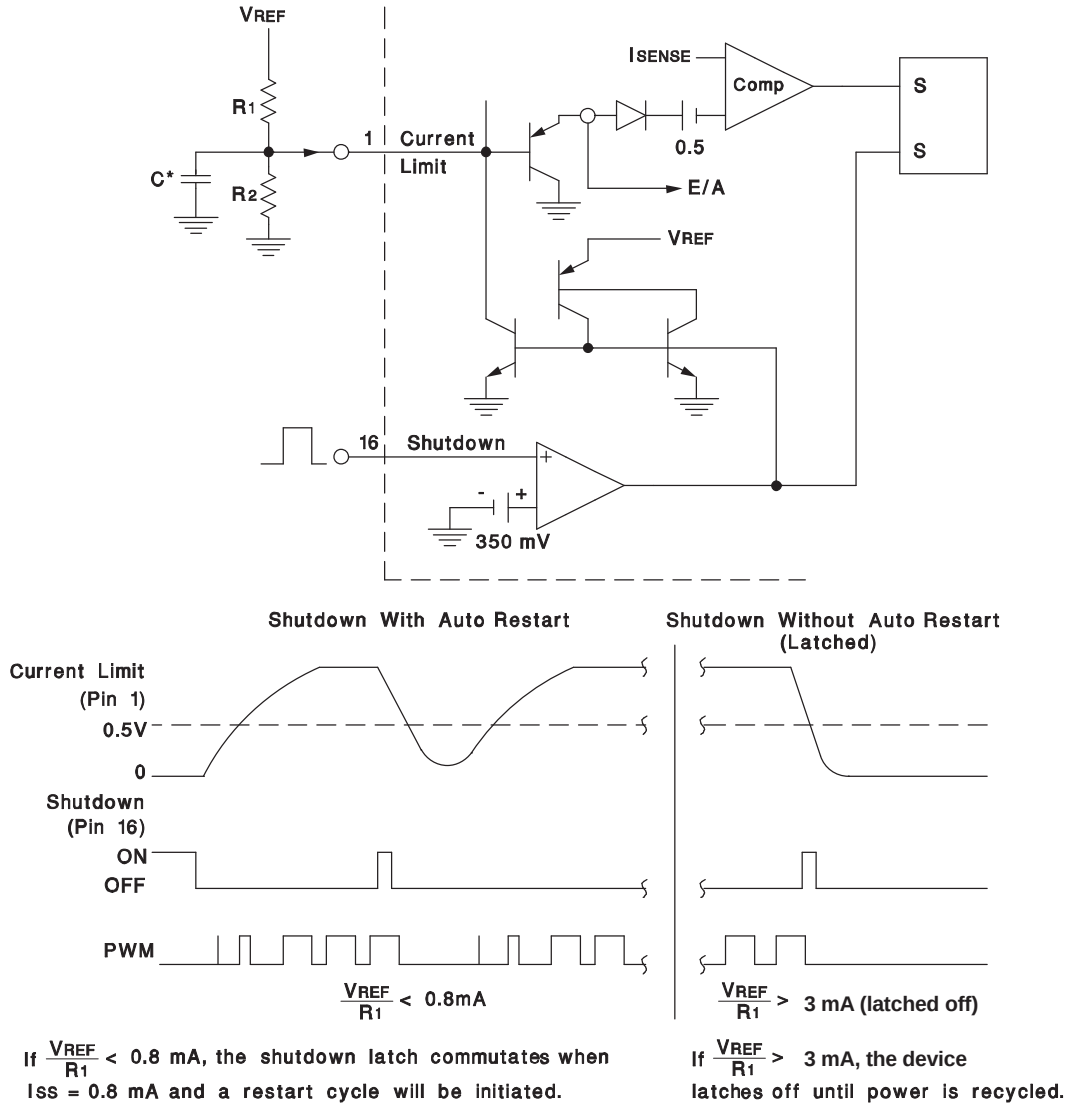
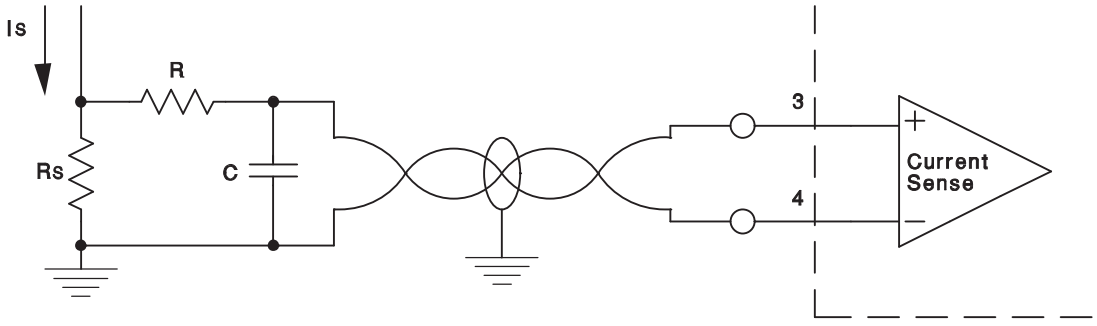


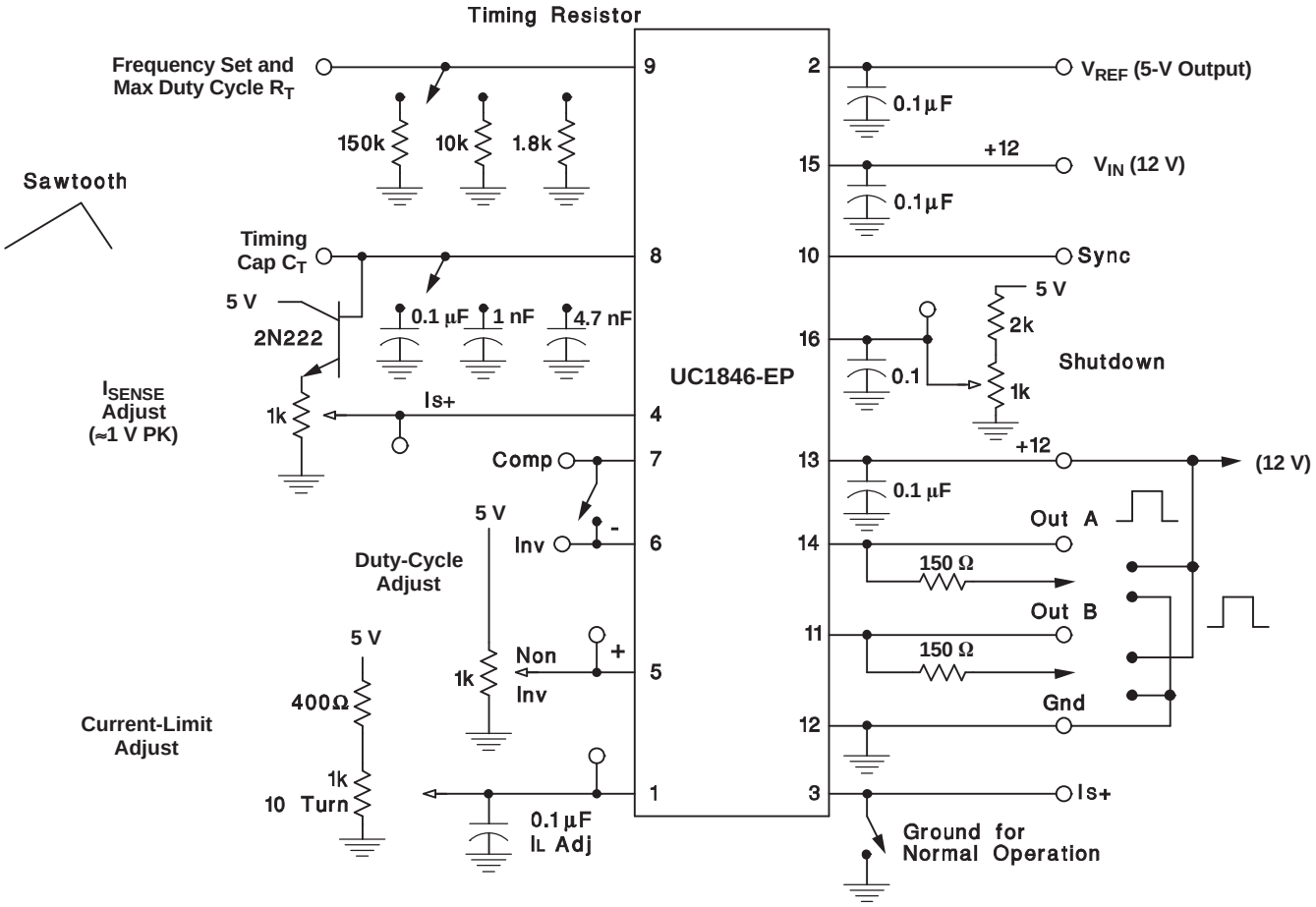
Figure 8. Soft-Start and Shutdown/Restart Functions



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote noise-free sensing.

Figure 9. Current-Sense Amplifier Connection

APPLICATION INFORMATION (continued)



–Bypass capacitance should be low ESR and ESL type.
–Short pins 6 and 7 for unity gain testing.

Figure 10. Open-Loop Test Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC1846MDWREP	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC1846MEP
UC1846MDWREP.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC1846MEP
V62/06606-01XE	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC1846MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1846-EP :

- Catalog : UC1846

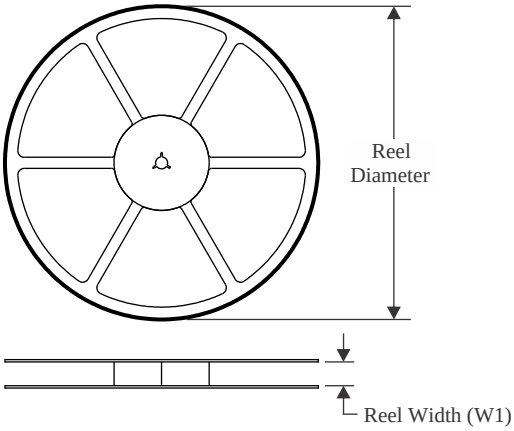
- Space : UC1846-SP

NOTE: Qualified Version Definitions:

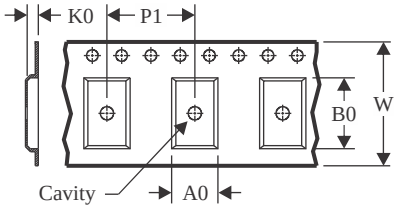
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

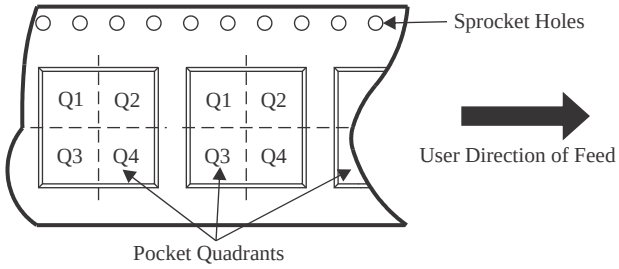


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

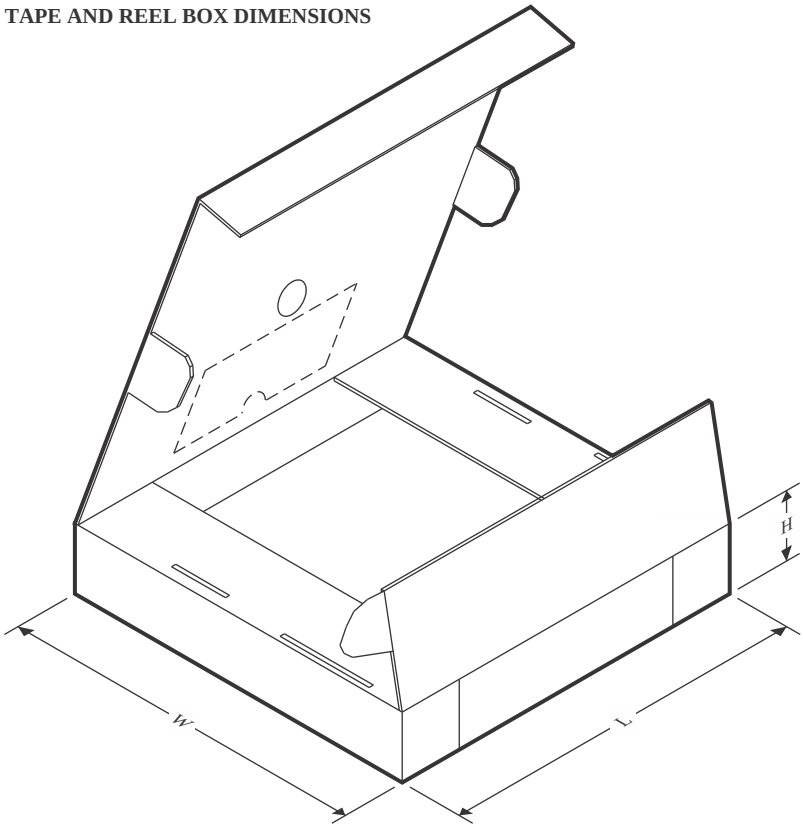
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC1846MDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC1846MDWREP	SOIC	DW	16	2000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

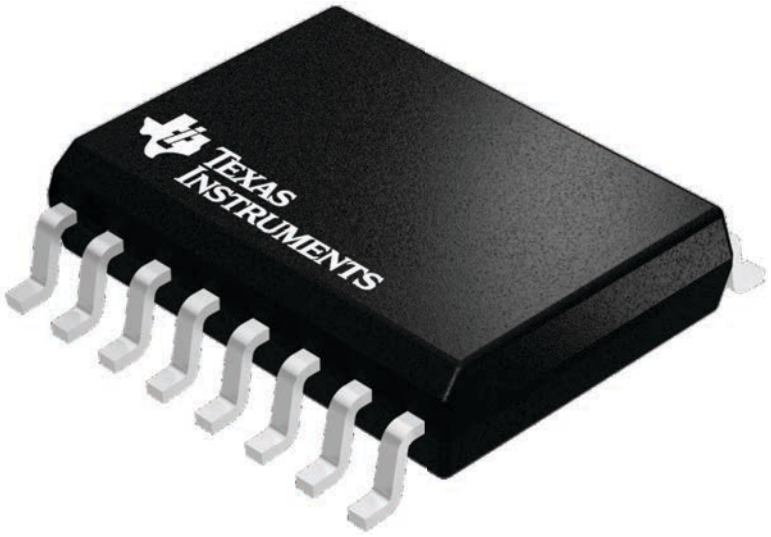
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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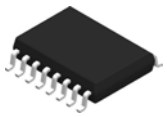
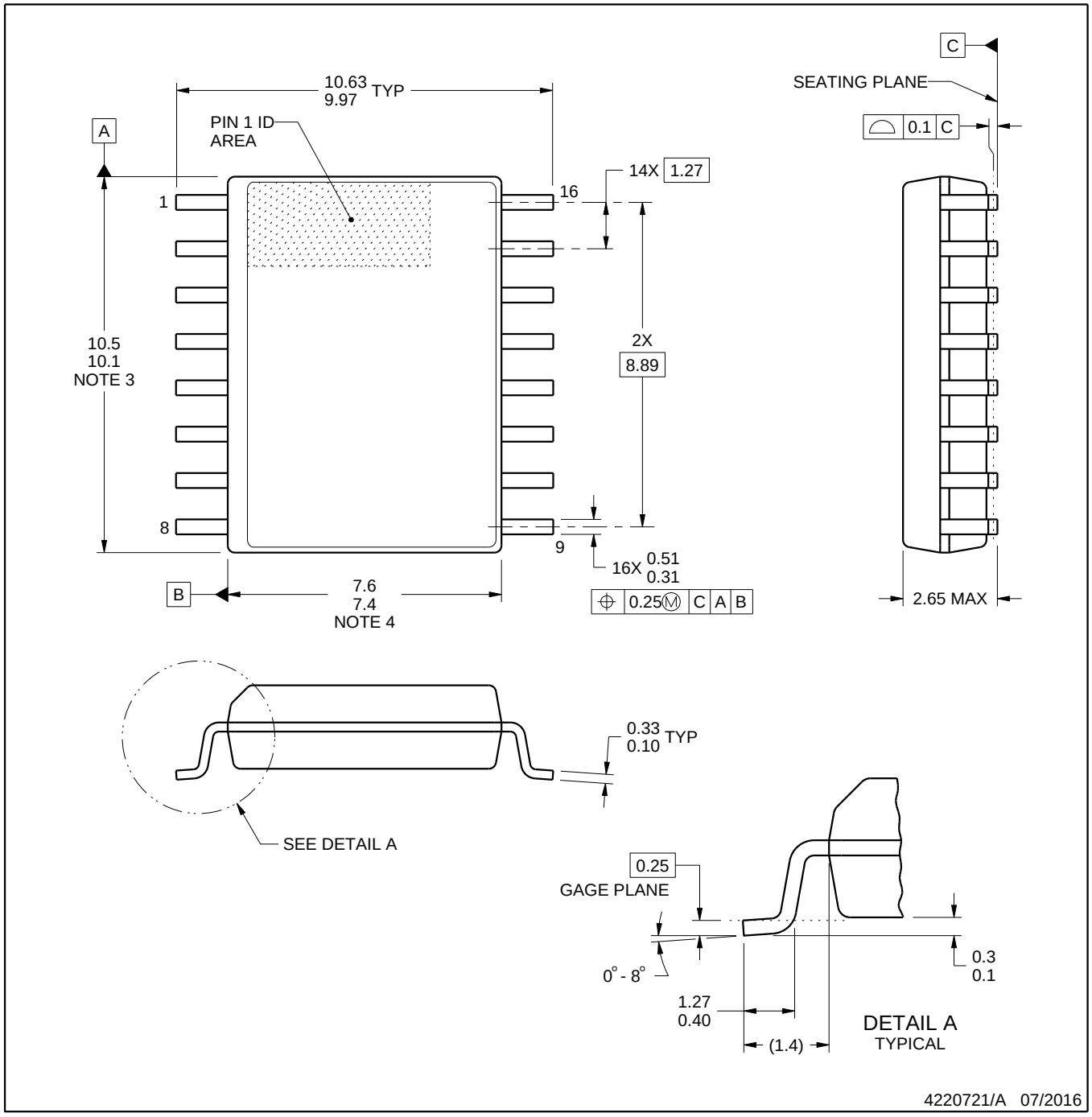


PACKAGE OUTLINE

DW0016A

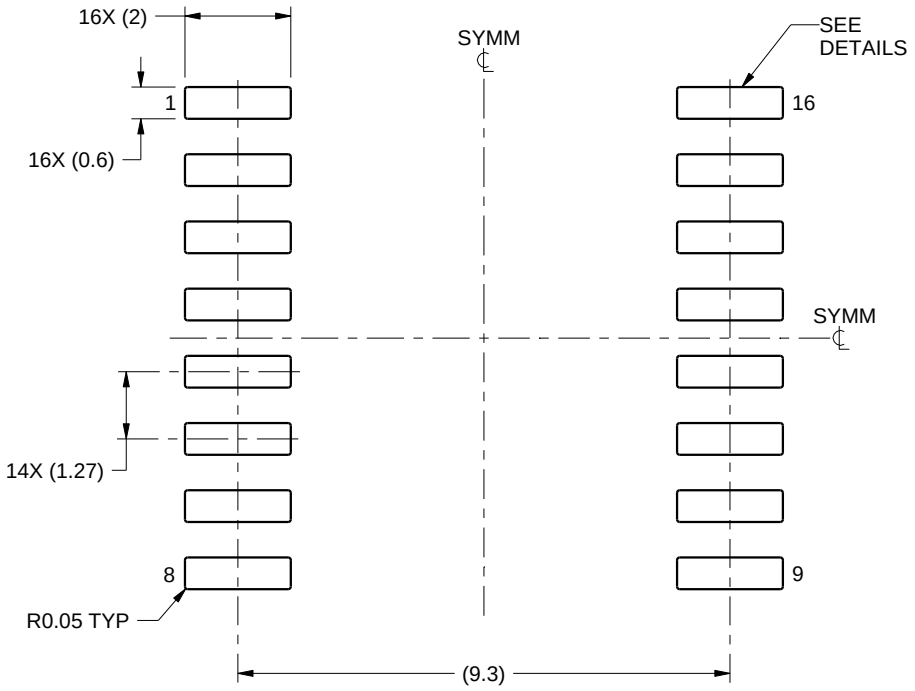
SOIC - 2.65 mm max height

SOIC

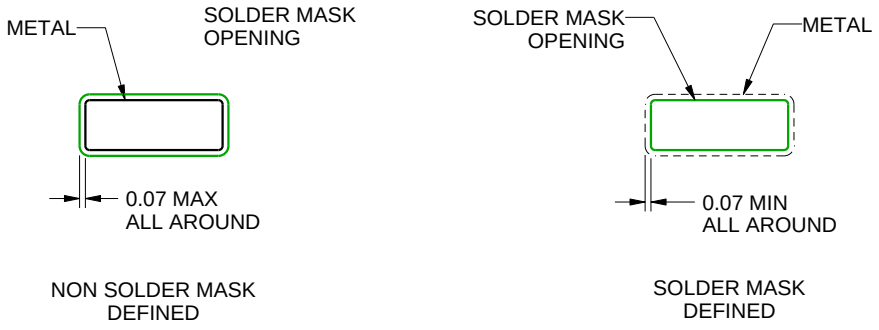


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

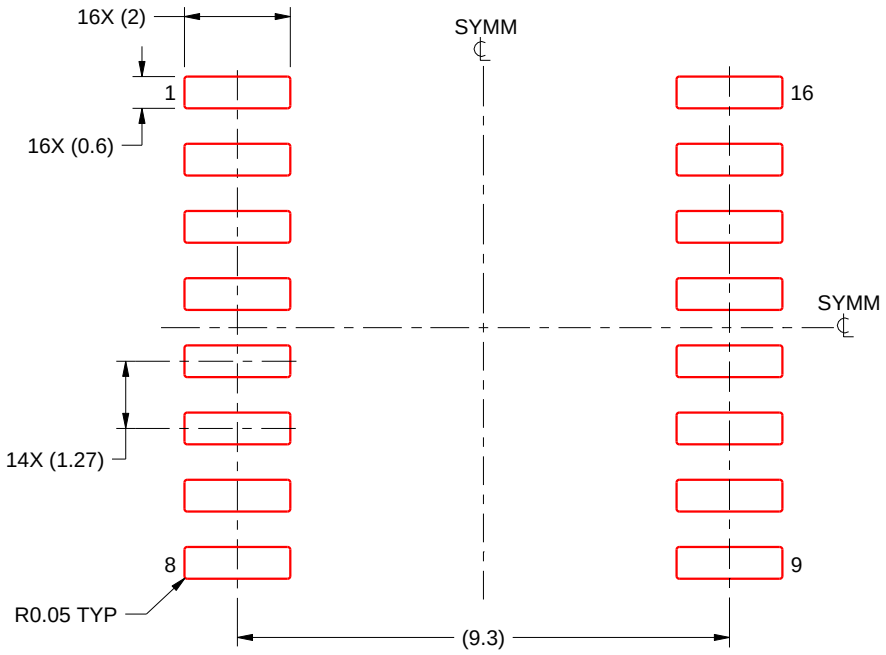


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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