

TXB0101 具有自动方向检测和 ±15kV ESD 保护功能的 1 位双向电平转换和电压转换器

1 特性

- 采用德州仪器 (TI) NanoFree™ 封装
- A 端口支持 1.2V 至 3.6V 的电压，B 端口支持 1.65V 至 5.5V 的电压 ($V_{CCA} \leq V_{CCB}$)
- V_{CC} 隔离特性 - 如果任何一个 V_{CC} 输入接地 (GND)，否则所有输出均处于高阻抗状态
- OE 输入电路以 V_{CCA} 为基准
- 低功耗， I_{CC} 最大值为 5 μ A
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
 - A 端口
 - 2000V 人体放电模型 (A114-B)
 - 250 V 机器模型 (A115-A)
 - 1500 V 充电器件模型 (C101)
 - B 端口
 - 15kV 人体放电模型 (A114-B)
 - 250 V 机器模型 (A115-A)
 - 1500 V 充电器件模型 (C101)

2 应用

- 手持终端
- 智能手机
- 平板电脑
- 台式计算机

3 说明

这个 1 位同相转换器使用两个独立的可配置电源轨。A 端口设计用于跟踪 V_{CCA} 。 V_{CCA} 支持从 1.2V 到 3.6V 范围内的任一电源电压。B 端口设计用于跟踪 V_{CCB} 。 V_{CCB} 支持从 1.65V 到 5.5V 范围内的任意电源电压。这使得该器件可在 1.2V、1.5V、1.8V、2.5V、3.3V 和 5V 电压节点之间任意进行通用低压双向转换。 V_{CCA} 不应超过 V_{CCB} 。

当输出使能端 (OE) 输入为低电平时，所有输出都被置于高阻态。

该器件完全符合使用 I_{off} 的部分断电应用的规范要求。 I_{off} 电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

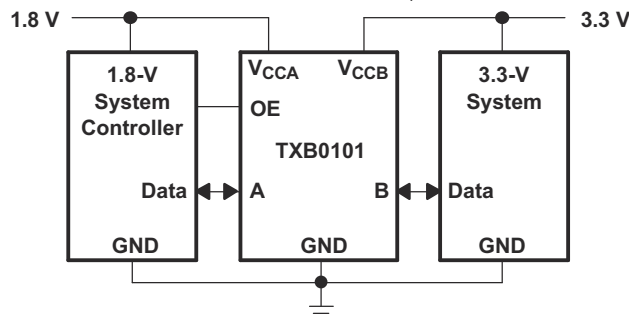
为确保在上电或掉电期间均处于高阻抗状态，应将 OE 通过下拉电阻器接地；该电阻器的最小值取决于驱动器的拉电流能力。

NanoFree™ 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TXB0101	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
	DSBGA (YZP) (6)	0.90mm × 1.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型工作电路



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2017) to Revision E (March 2023)	Page
• 将 YZP 封装的尺寸从 1.1mm × 1.20mm 更改为 0.9mm × 1.40mm (在封装信息表中)	1
• Changed Note 1 in the <i>Absolute Maximum Ratings</i>	4

Changes from Revision C (June 2015) to Revision D (March 2017)	Page
• Added Absolute maximum junction temperature, T_J in <i>Absolute Maximum Ratings</i>	4
• Added TXB0101 Port A and Port B specifications in <i>ESD Ratings</i> table.....	4
• Added <i>Receiving Notification of Documentation Updates</i> section.....	19

Changes from Revision B (May 2012) to Revision C (June 2015)	Page
• 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 删除了订购信息表.....	1

Changes from Revision A (November 2008) to Revision B (March 2012)	Page
• Added notes to pin out graphics.....	3

5 Pin Configuration and Functions

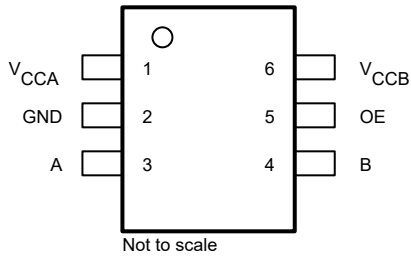


图 5-1. DBV Package, 6-Pin SOT-23 (Top View)

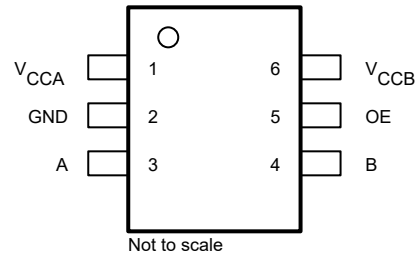


图 5-2. DCK Package, 6-Pin SC70 (Top View)

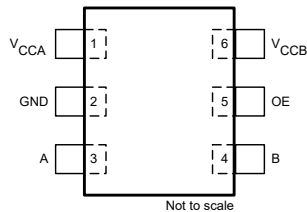


图 5-3. DRL Package, 6-Pin SOT (Top View)

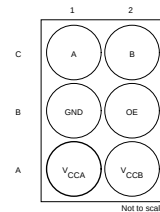


图 5-4. YZP Package, 6-Ball DSBGA (Bottom View)

- A. See mechanical drawings for dimensions.
- B. Pullup resistors are not required on both sides for Logic I/O.
- C. If pullup or pulldown resistors are needed, the resistor value must be over 50 k Ω .
- D. 50 k Ω is a safe recommended value, if the customer can accept higher V_{OL} or lower V_{OH} , smaller pullup or pulldown resistor is allowed, the draft estimation is $V_{OL} = V_{CCOUT} \times 4.5 \text{ k} / (4.5 \text{ k} + R_{PU})$ and $V_{OH} = V_{CCOUT} \times R_{DW} / (4.5 \text{ k} + R_{DW})$.
- E. If pull up resistors are needed, please refer to the TXS0101 or contact TI.
- F. For detailed information, please refer to application note [SCEA043](#).

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{CCA}	—	A-port supply voltage. $1.2 \text{ V} \leq V_{CCA} \leq 3.6 \text{ V}$ and $V_{CCA} \leq V_{CCB}$
2	GND	—	Ground
3	A	I/O	Input/output A. Referenced to V_{CCA} .
4	B	I/O	Input/output B. Referenced to V_{CCB} .
5	OE	I	3-state output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .
6	V_{CCB}	—	B-port supply voltage. $1.65 \text{ V} \leq V_{CCB} \leq 5.5 \text{ V}$

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CCA}	Supply voltage	- 0.5	4.6	V	
V _{CCB}	Supply voltage	- 0.5	6.5		
V _I	Input voltage ⁽²⁾	- 0.5	6.5	V	
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	- 0.5	6.5	V	
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}	A port	- 0.5	V _{CCA} + 0.5	V
		B port	- 0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0	- 50	mA	
I _{OK}	Output clamp current	V _O < 0	- 50	mA	
I _O	Continuous output current		±50	mA	
	Continuous current through V _{CCA} , V _{CCB} , or GND		±100	mA	
T _{JMAX}	Absolute maximum junction temperature		150	°C	
T _{stg}	Storage temperature	- 65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT	
TXB0101 Port A				
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
TXB0101 Port B				
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±15	kV
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1) (2).

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}					1.65	5.5	
V _{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCI} × 0.65 ⁽³⁾	V _{CCI}	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCA} × 0.65	5.5	
V _{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V _{CCI} × 0.35 ⁽³⁾	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	0	V _{CCA} × 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs		1.65 V to 3.6 V		40	
				1.2 V to 3.6 V	4.5 V to 5.5 V		
T _A	Operating free-air temperature				- 40	85	°C

- (1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
- (2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
- (3) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TXB0101				UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	YZP (DSBGA)	
	6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA} Junction-to-ambient thermal resistance	192.3	266.9	204.2	105.8	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	164.8	80.4	76.4	1.6	°C/W
R _{θJB} Junction-to-board thermal resistance	38.6	99.1	38.7	10.8	°C/W
ψ _{JT} Junction-to-top characterization parameter	43.7	1.5	3.4	3.1	°C/W
ψ _{JB} Junction-to-board characterization parameter	38.1	98.3	38.5	10.8	°C/W
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			- 40°C to 85°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{OHA}		I _{OH} = - 20 μA	1.2 V		1.1			V _{CCA} - 0.4			V
			1.4 V to 3.6 V								
V _{OLA}		I _{OL} = 20 μA	1.2 V		0.9			0.4			V
			1.4 V to 3.6 V								
V _{OHB}		I _{OH} = - 20 μA		1.65 V to 5.5 V				V _{CCB} - 0.4			V
V _{OLB}		I _{OL} = 20 μA		1.65 V to 5.5 V				0.4			V
I _I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2			μA
I _{off}	A port		0 V	0 V to 5.5 V	±1			±2			μA
	B port		0 V to 3.6 V	0 V	±1			±2			
I _{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2			μA
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	0.06						μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	3						
			3.6 V	0 V	2						
			0 V	5.5 V	- 2						
I _{CCB}		V _I = V _{CCB} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.4						μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5						
			3.6 V	0 V	- 2						
			0 V	5.5 V	2						
I _{CCA} + I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.5						μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	8						
I _{CCZA}		V _I = V _{CCI} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	0.05						μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	3						
I _{CCZB}		V _I = V _{CCB} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	3.3						μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5						
C _i	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	2.5			3			pF
C _{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V	5			6			pF
	B port				11			13			

(1) V_{CCI} is the supply voltage associated with the input port.

(2) V_{CCO} is the supply voltage associated with the output port.

6.6 Timing Requirements, $V_{CCA} = 1.2\text{ V}$

$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{ V}$

		$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	ns

6.7 Timing Requirements, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (unless otherwise noted)

		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		40		40		40		40		Mbps
t_w	Pulse duration	Data inputs	25	25	25	25	25	25	ns	

6.8 Timing Requirements, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted)

		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		60		60		60		60		Mbps
t_w	Pulse duration	Data inputs	17	17	17	17	17	17	ns	

6.9 Timing Requirements, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		100		100		100		Mbps
t_w	Pulse duration	Data inputs	10	10	10	10	ns	

6.10 Timing Requirements, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
Data rate		100		100		Mbps
t_w	Pulse duration	Data inputs	10	10	10	ns

6.11 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
t_{en}	OE	A	1	1	1	1	μs
		B	1	1	1	1	
t_{dis}	OE	A	18	15	14	14	ns
		B	20	17	16	16	
t_{rA} , t_{fA}	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
t_{rB} , t_{fB}	B-port rise and fall times		2.1	1.5	1.2	1.1	ns
Max data rate			20	20	20	20	Mbps

6.12 Switching Characteristics, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t_{dis}	OE	A	5.9	31	5.7	25.9	5.6	23	5.7	22.4	ns
		B	5.4	30.3	4.9	22.8	4.8	20	4.9	19.5	
t_{rA} , t_{fA}	A-port rise and fall times		1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
t_{rB} , t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			40		40		40		40		Mbps

6.13 Switching Characteristics, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
t_{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t_{dis}	OE	A	5.9	31	5.1	21.3	5	19.3	5	17.4	ns
		B	5.4	30.3	4.4	20.8	4.2	17.9	4.3	16.3	
t_{rA} , t_{fA}	A-port rise and fall times		1	4.2	1.1	4.1	1.1	4.1	1.1	4.1	ns
t_{rB} , t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			60		60		60		60		Mbps

6.14 Switching Characteristics, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.3	1	5.2	0.9	4.7	ns
	B	A	1.2	6.6	1.1	5.1	0.9	4.4	
t_{en}	OE	A		1		1		1	μs
		B		1		1		1	
t_{dis}	OE	A	5.1	21.3	4.6	15.2	4.6	13.2	ns
		B	4.4	20.8	3.8	16	3.9	13.9	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3	0.8	3	0.8	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3	0.5	2.8	0.4	2.7	ns
Max data rate			100		100		100		Mbps

6.15 Switching Characteristics, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.7	0.8	4	ns
	B	A	1	4.9	0.9	4.5	
t_{en}	OE	A		1		1	μs
		B		1		1	
t_{dis}	OE	A	4.6	15.2	4.3	12.1	ns
		B	3.8	16	3.4	13.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	2.5	0.7	2.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.5	2.3	0.4	2.7	ns
Max data rate			100		100		Mbps

6.16 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CCA}							UNIT	
		1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
		V_{CCB}								
		5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP		
C_{pdA}	A-port input, B-port output	$C_L = 0, f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns},$ $OE = V_{CCA}$ (outputs enabled)	7.8	8	8	7	7	8	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		38.1	28	29	29	29	29	30	
	B-port input, A-port output		25.4	18	17	17	18	20	21	

6.16 Operating Characteristics (continued)

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT	
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
			V_{CCB}								
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V		
			TYP	TYP	TYP	TYP	TYP	TYP	TYP		
C_{pdA}	A-port input, B-port output	$C_L = 0$, $f = 10$ MHz, $t_r = t_f = 1$ ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01		
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01		0.02
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01		0.03

6.17 Typical Characteristics

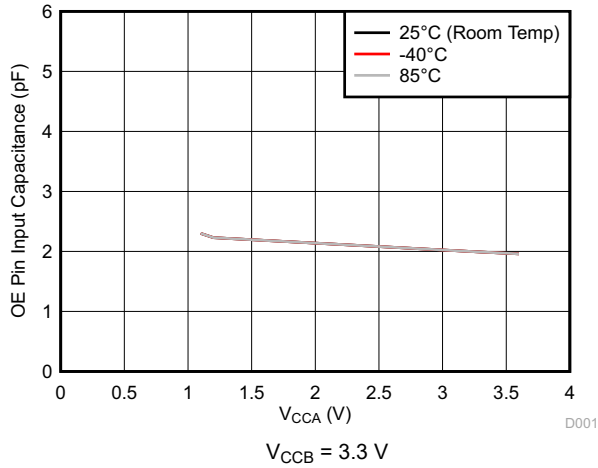


图 6-1. Input Capacitance for OE pin (C_I) vs Power Supply (V_{CCA})

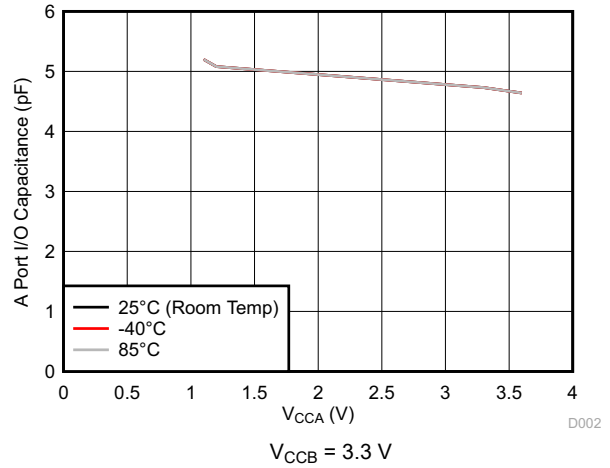


图 6-2. Capacitance for A Port I/O Pins (C_{IO}) vs Power Supply (V_{CCA})

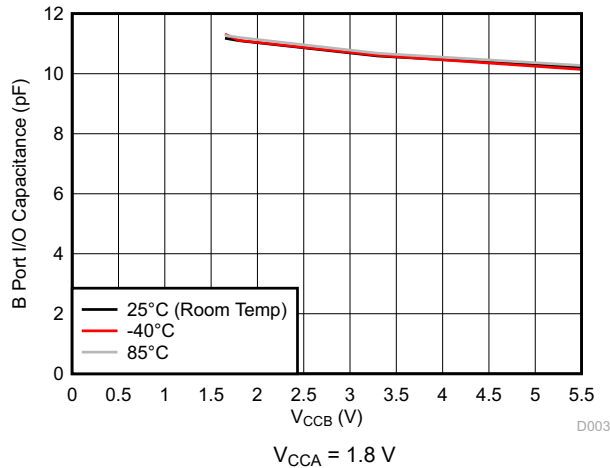
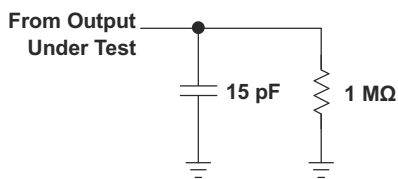
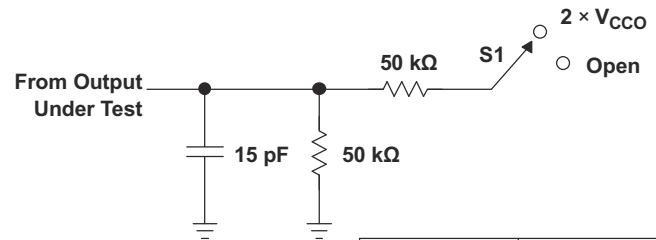


图 6-3. Capacitance for B Port I/O Pins (C_{IO}) vs Power Supply (V_{CCB})

Parameter Measurement Information

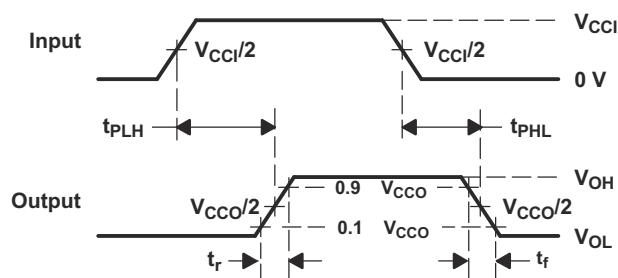


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

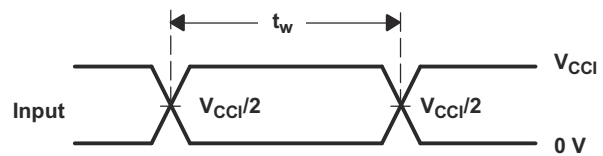


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

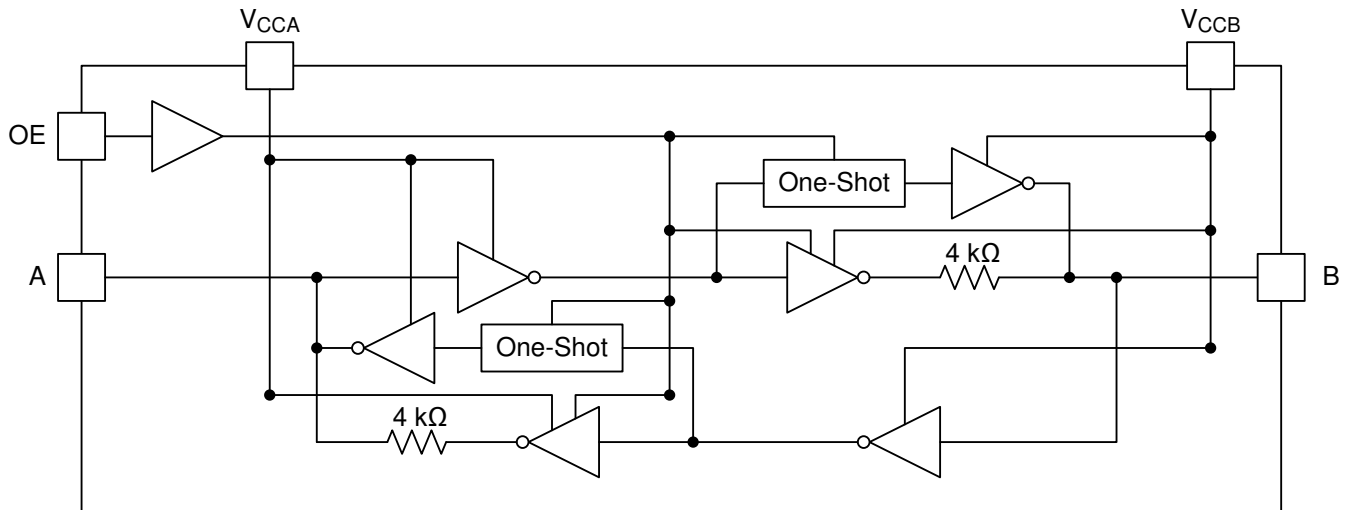
图 7-1. Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TXB0101 device is a 1-bit directionless level-shifting and voltage translator specifically designed for translating logic voltage levels. The A port accepts I/O voltages ranging from 1.2 V to 3.6 V, while the B port is able to accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, see TI [TXS010X](#) products.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXB0101 architecture (see [图 7-1](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0101 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at $V_{CCO} = 1.2$ V to 1.8 V, 50 Ω at $V_{CCO} = 1.8$ V to 3.3 V, and 40 Ω at $V_{CCO} = 3.3$ V to 5 V.

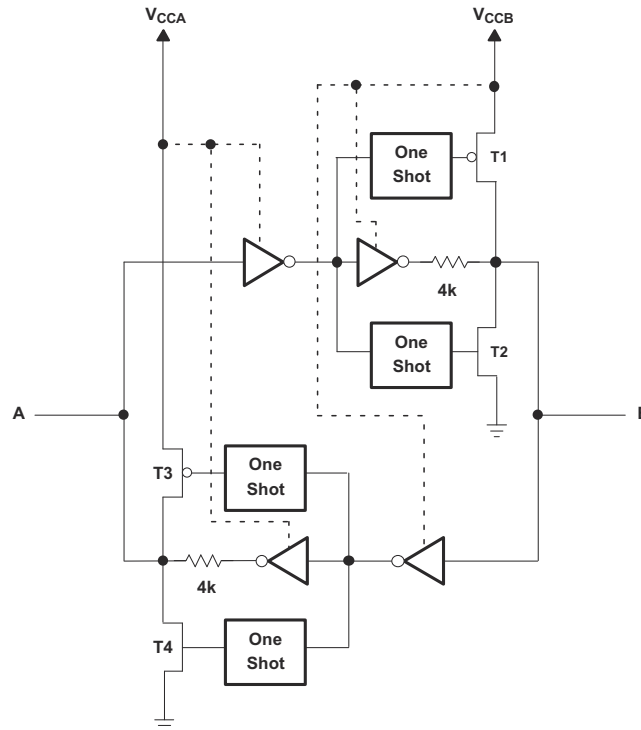


图 7-1. Architecture of TXB0101 I/O Cell

7.3.2 Power Up

During operation, make sure that $V_{CCA} \leq V_{CCB}$ at all times. During power up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0101 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0\text{ V}$) and are placed in high-impedance state.

7.3.3 Enable and Disable

The TXB0101 has an OE input that is used to disable the device by setting $OE = \text{low}$, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs are actually disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.4 Pullup or Pulldown Resistors on I/O Lines

The TXB0101 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0101 have low-DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to make sure they do not contend with the output drivers of the TXB0101.

For the same reason, the TXB0101 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI [TXS010X](#) series of level translators.

7.4 Device Functional Modes

The TXB0101 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high-impedance state. Setting the OE input high enables the device.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TXB0101 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, see TI [TXS010X](#) products. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

8.2 Typical Application

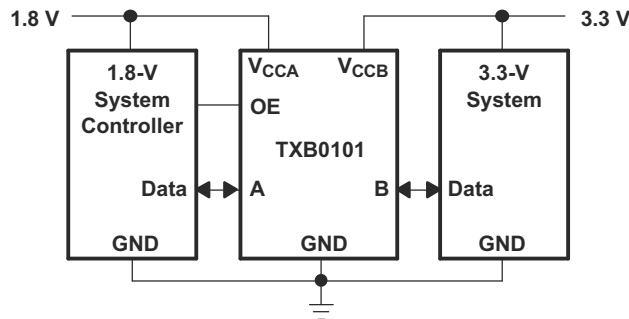


图 8-1. Typical Application Circuit

8.2.1 Design Requirements

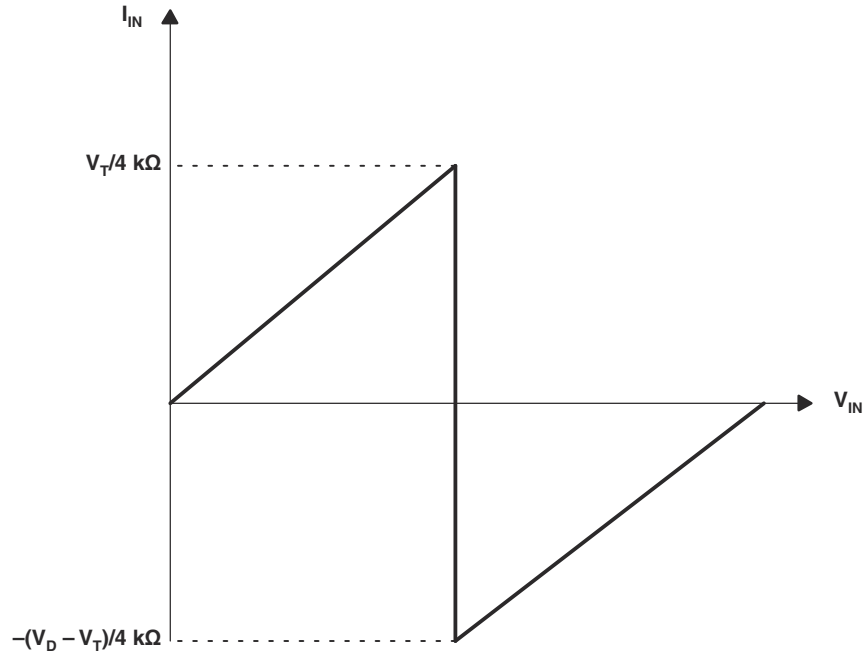
For this design example, use the parameters listed in [表 8-1](#). And make sure that $V_{CCA} \leq V_{CCB}$.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

8.2.1.1 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0101 are shown in [图 8-2](#). For proper operation, the device driving the data I/Os of the TXB0101 must have drive strength of at least ± 2 mA.



- A. V_T is the input threshold voltage of the TXB0101 (typically $V_{CC}/2$).
 B. V_D is the supply voltage of the external driver.

图 8-2. Typical I_{IN} vs V_{IN} Curve

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXB0101 device to determine the input voltage range. For a valid logic HIGH the value must exceed the V_{IH} of the input port. For a valid logic LOW the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXB0101 device is driving to determine the output voltage range.
 - External pullup or pulldown resistors are not recommended. If mandatory, TI recommends the value should be larger than $50\text{ k}\Omega$.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL} . Use 方程式 1 and 方程式 2 to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\text{ k}\Omega) \quad (1)$$

$$V_{OL} = V_{CCx} \times 4.5\text{ k}\Omega / (R_{PU} + 4.5\text{ k}\Omega) \quad (2)$$

where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pulldown resistor
- R_{PU} is the value of the external pullup resistor
- $4.5\text{ k}\Omega$ is the counting the variation of the serial resistor $4\text{ k}\Omega$ in the I/O line.

8.2.3 Application Curve

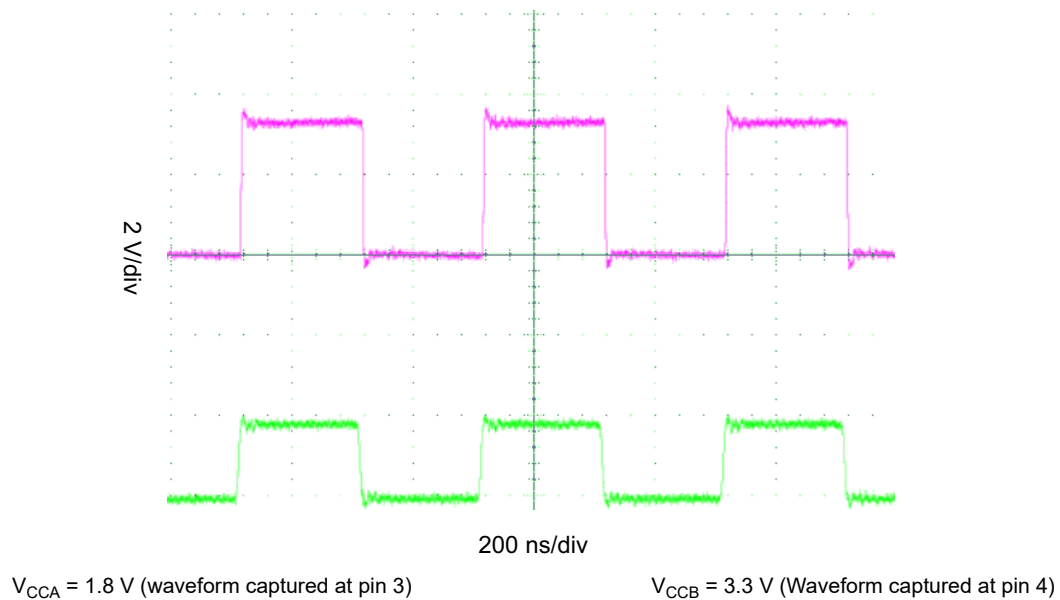


图 8-3. Level-Translation of a 2.5-MHz Signal

8.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0101 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0\text{ V}$). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, the following common printed-circuit board layout guidelines are recommended.

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CCA} , V_{CCB} pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 10 ns, making sure that any reflection encounters low impedance at the source driver.

8.4.2 Layout Example

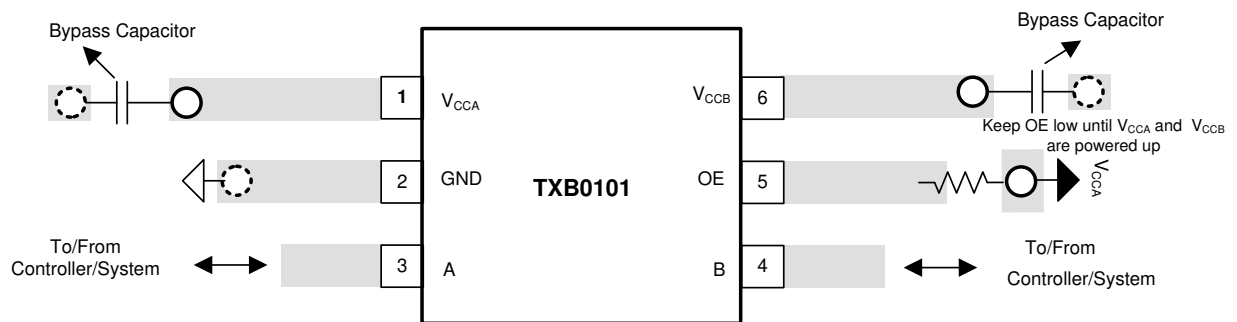
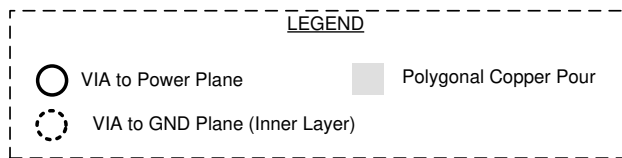


图 8-4. Layout Example Recommendation

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.

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9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0101DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	Samples
TXB0101DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	Samples
TXB0101DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	Samples
TXB0101DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	Samples
TXB0101DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	Samples
TXB0101DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		27O	Samples
TXB0101DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	Samples
TXB0101DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	27R	Samples
TXB0101DRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	27R	Samples
TXB0101YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	27N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101DRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0101DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TXB0101DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TXB0101DCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TXB0101DCKT	SC70	DCK	6	250	203.0	203.0	35.0
TXB0101DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
TXB0101DRLT	SOT-5X3	DRL	6	250	202.0	201.0	28.0
TXB0101YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

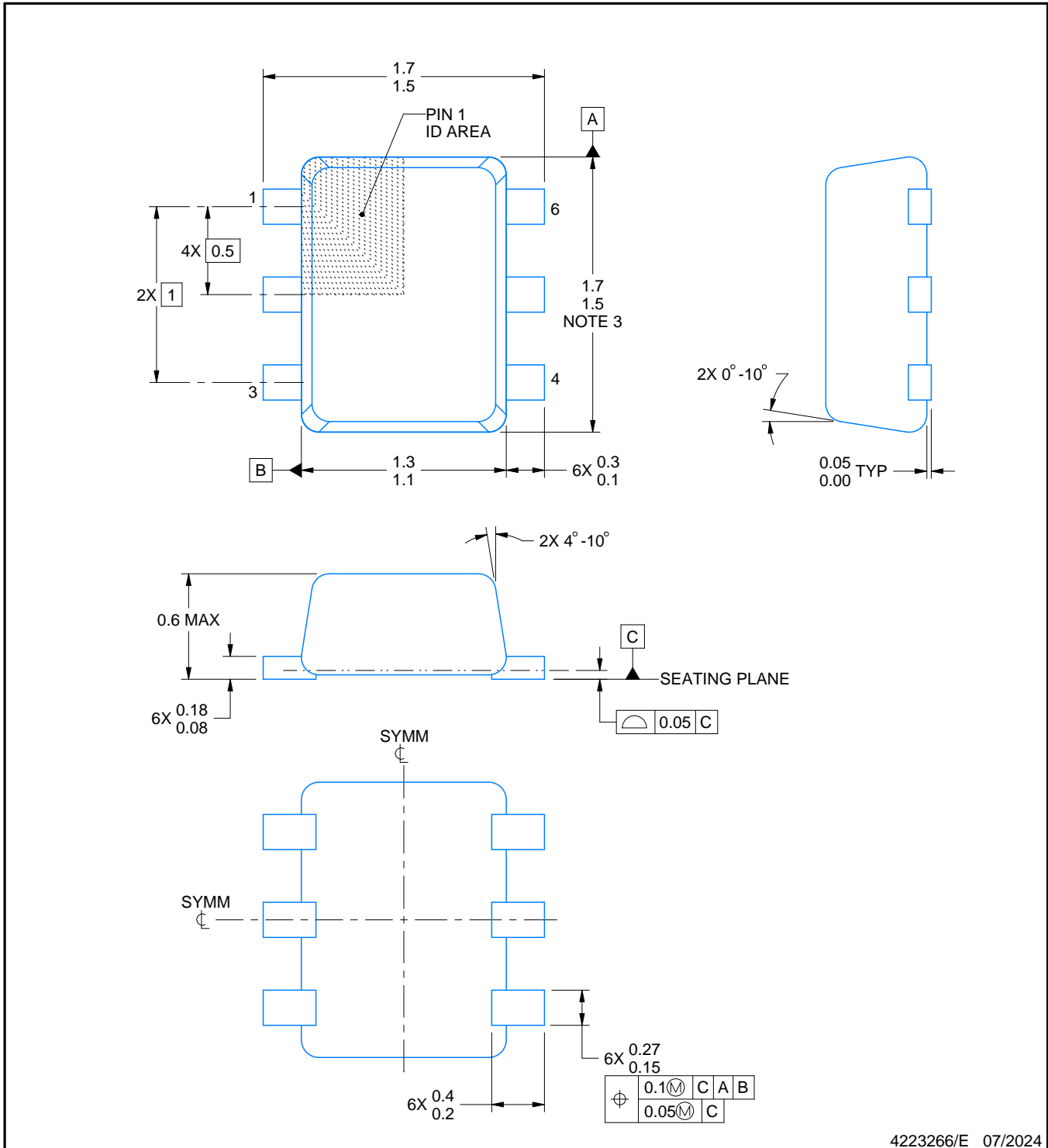
DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/E 07/2024

NOTES:

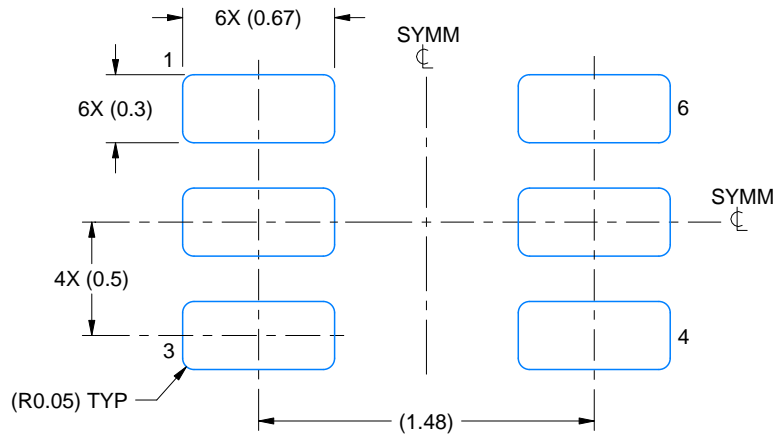
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

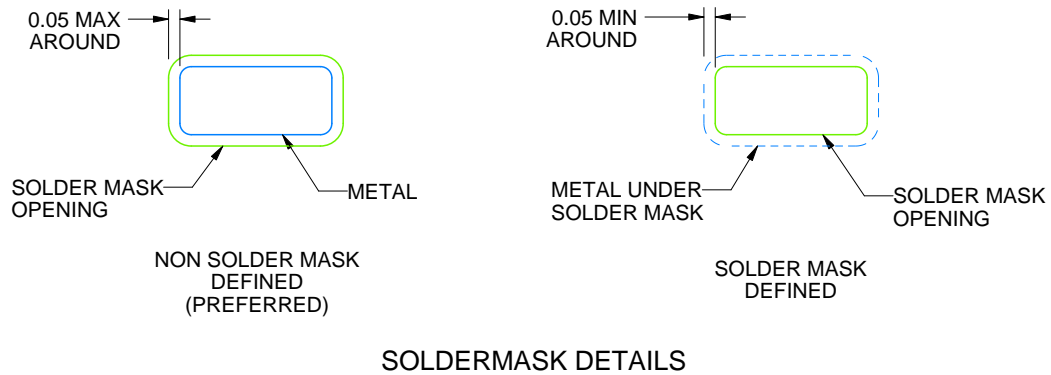
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

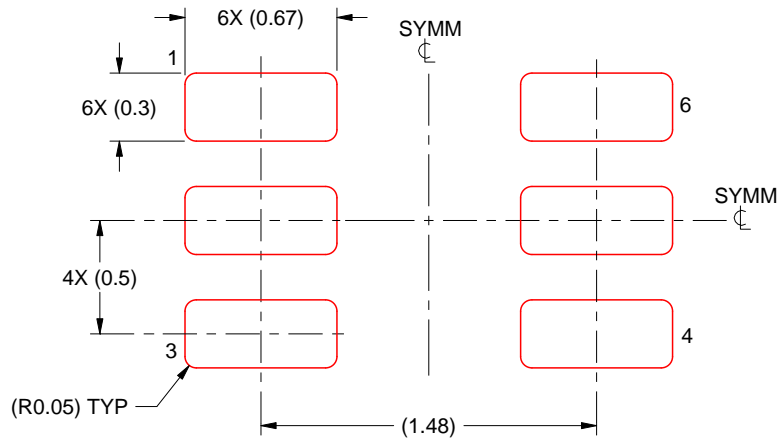
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

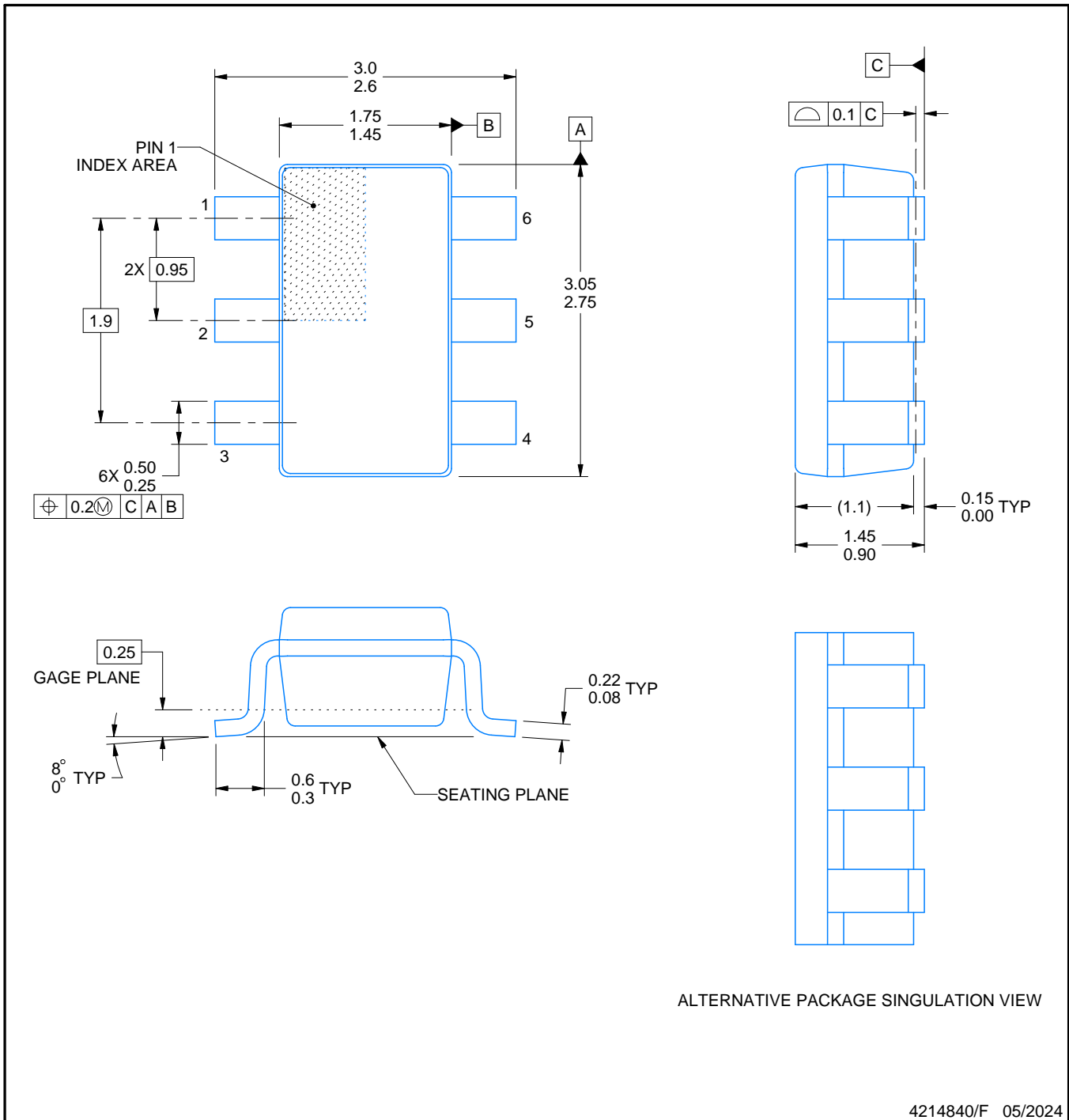
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

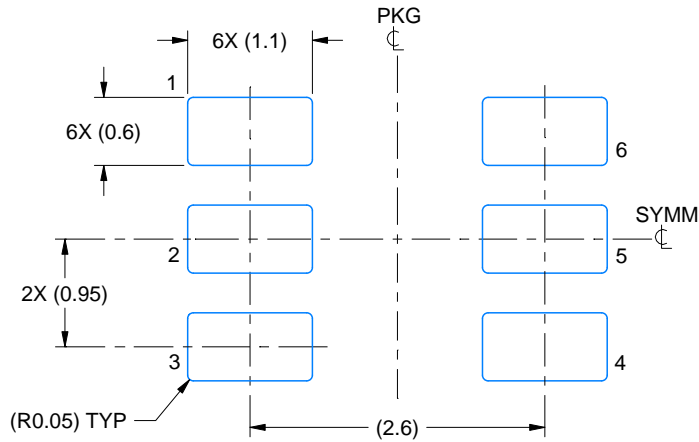
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

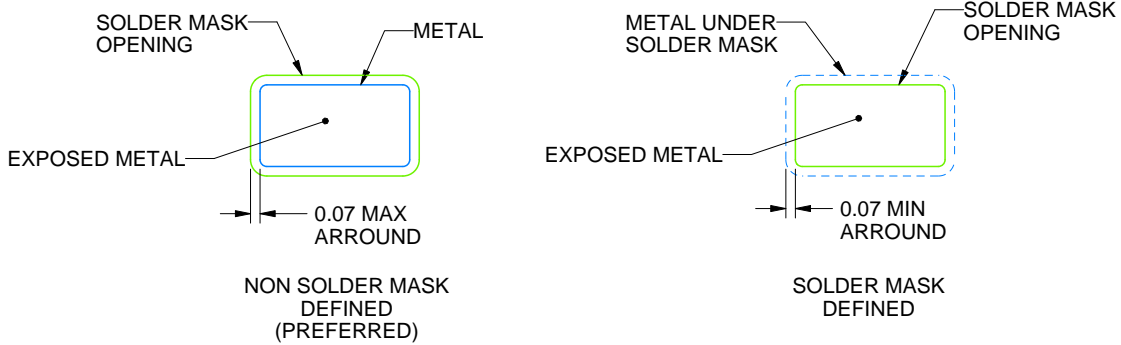
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

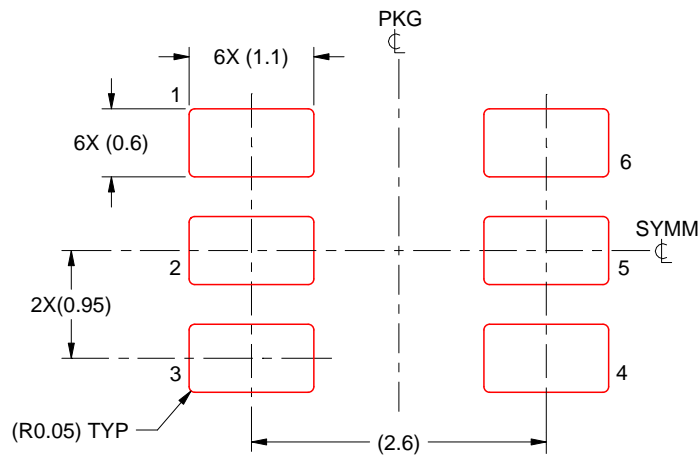
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

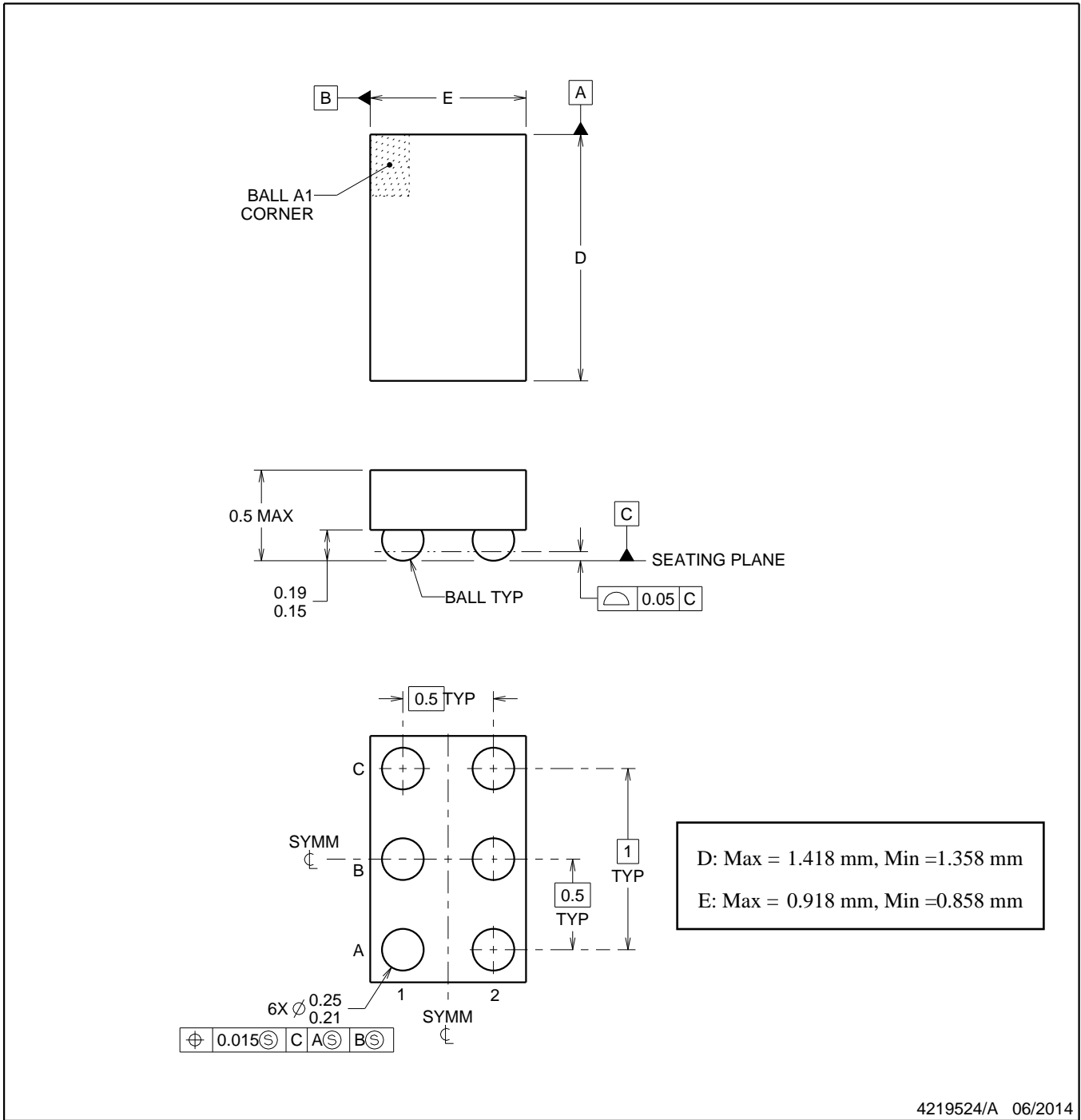
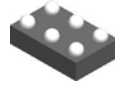


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

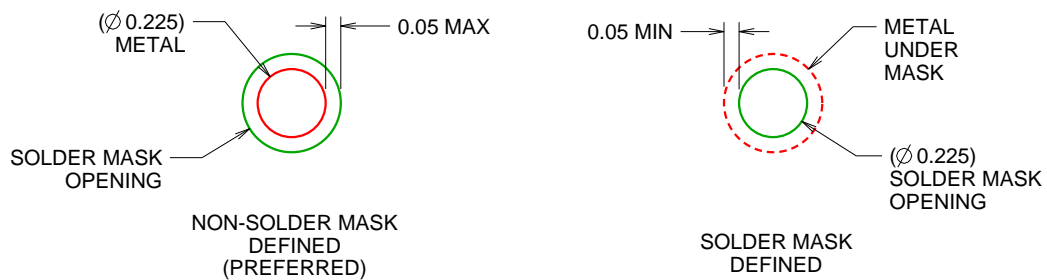
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

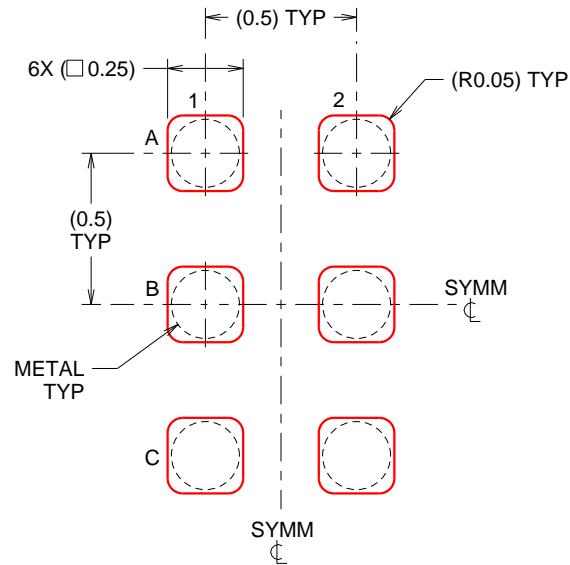
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

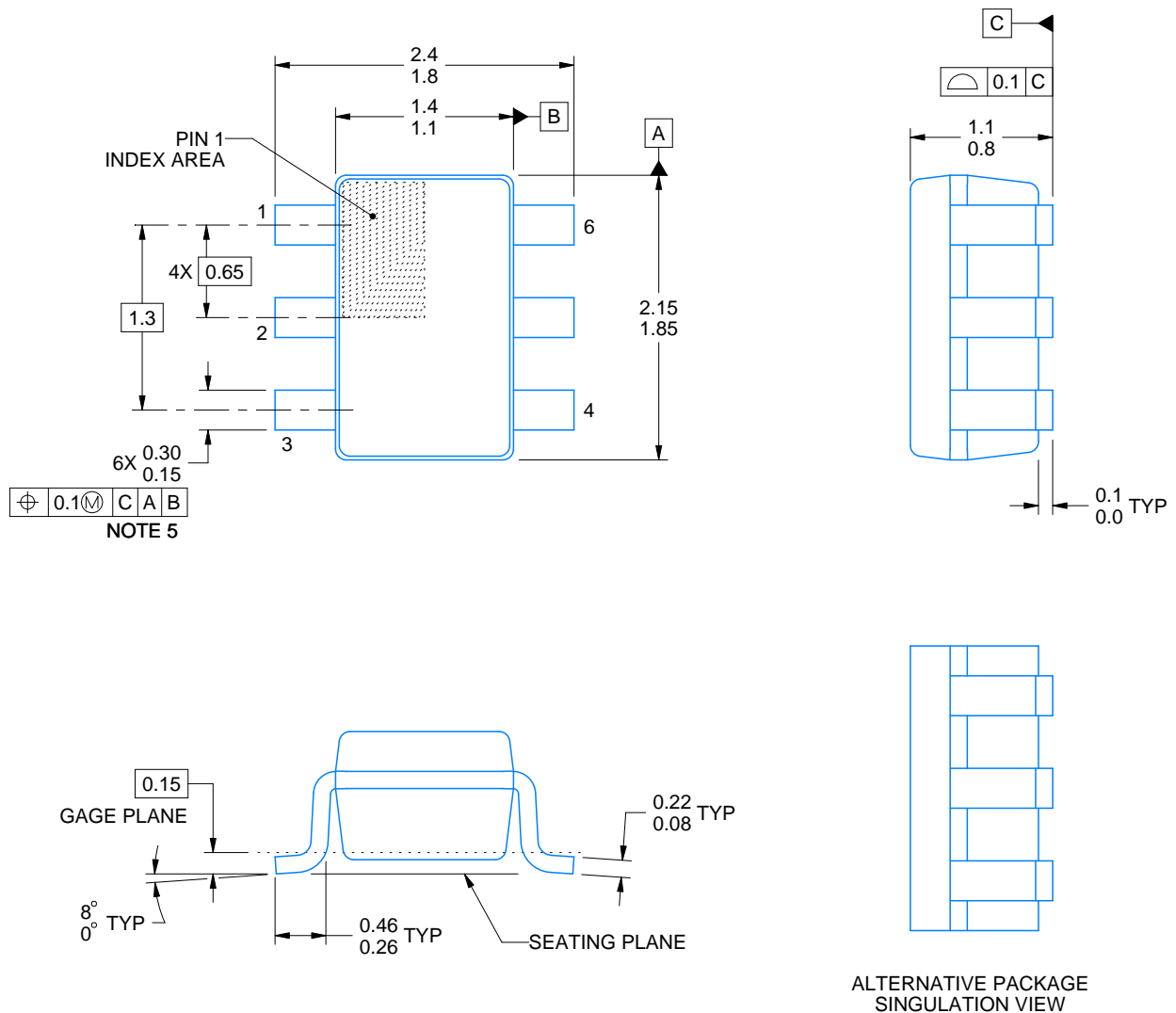
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

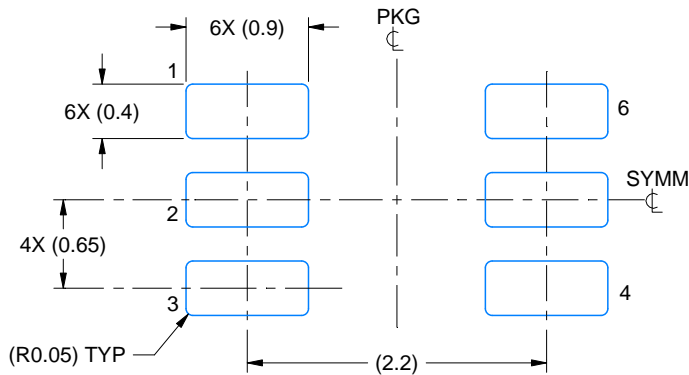
SMALL OUTLINE TRANSISTOR



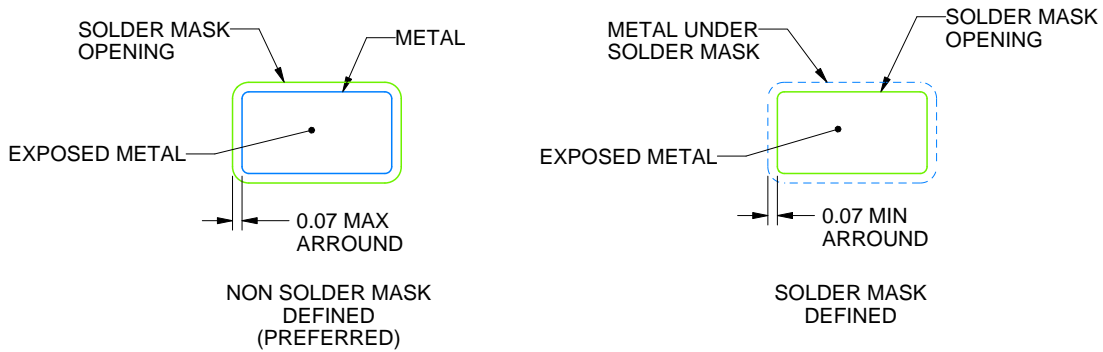
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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