TVB1440 具有均衡功能的 4 通道视频转接驱动器

ECCN：3E991

1 特性

- 兼容电视聚合视频信号发送设备
- 兼容 FPD-Link II 接口
- 适合于数字电视芯片组和 TCON 板
- 四通道转接驱动器，支持 600Mbps 至 5Gbps 范围内的数据速率
- 采用 3.3V 和 1.1V 电源，可实现低功耗运行
- 4 通道操作下的运行功耗为 175mW
- 2mW 关断功耗
- 高度可配置的输入均衡功能，有 8 种控制设置
  - 0dB 至 15dB
- 4 种预加强控制设置
  - 0、3、6 和 9dB
- 4 种输出电压摆幅控制设置
  - 350、500、700 和 1000mV
- 通过 I^2C 控制来配置器件以实现最佳性能
- 扩展温度范围为 -40℃ 至 85°C
- 2kV 人体模型 (HBM) 和 500V 充电器件模型 (CDM) 静电放电 (ESD) 保护
- 48 引脚四方扁平无引线 (QFN) 封装 (7mm x 7mm)

2 应用

- 数字电视
- 摄像机
- 吞吐量要求较高的视频接口

3 说明

TVB1440 是一款针对电视应用的 4 通道转接驱动器信号调节器，能够实现 TV 芯片组与 TCON 板之间的信号完整性。 I^2C 控制可在较宽范围内灵活配置器件以实现最优信号调节，从而使视频输出设备与接收设备之间的视频数据链路具备高保真性。 TVB1440 具备出色的去抖能力，可延长视频输出设备与接收设备之间的距离。

该器件可通过 I2C 对接收均衡功能进行多种可选控制，以补偿其输入端走线或电缆的严重损耗，从而提升输出信号的视觉效果。 每个通道中的发送器有 4 种预加强级别设置和 4 种输出电压摆幅级别设置，可使从 TVB1440 发送到下游接收器的视频信号达到最佳效果。

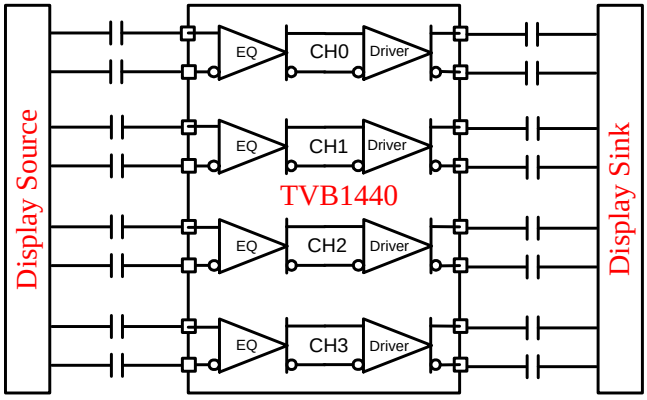
TVB1440 针对功耗要求较高的应用进行了优化。 TVB1440 不仅运行功耗较低，而且在数据链路输入端配有一个活动检测电路，当不存在有效输入信号时会切换至低功耗输出禁用模式。 可以根据需要禁用此活动检测电路。 该器件还具有一个关断模式，可使功耗降至 2mW。

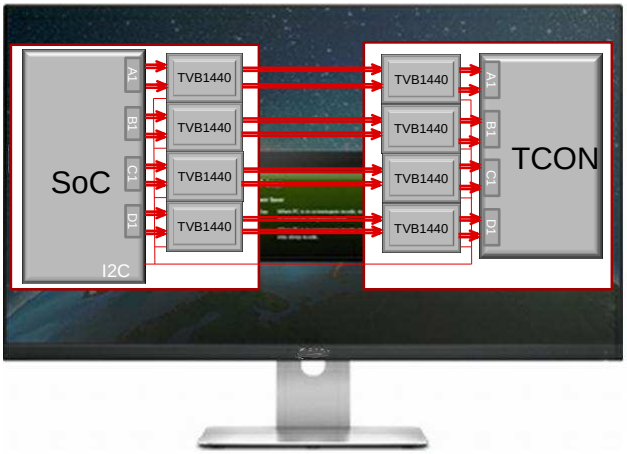
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TVB1440	VQFN (48)	7.00mm x 7.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图





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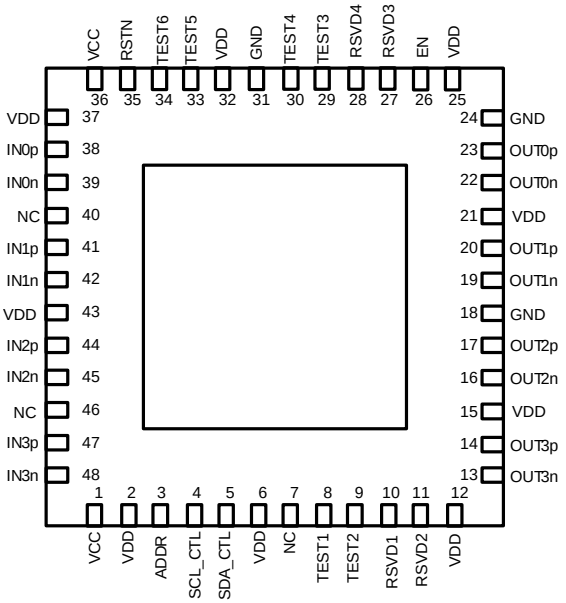
5 修订历史记录

Changes from Original (November 2014) to Revision A **Page**

- Changed text in the *Package Specific* section From: "The TVB1440 package has a 5.6 mm x 5.6 mm thermal pad." To: "The TVB1440 package has a 4.1 mm x 4.1 mm thermal pad." 21

6 Pin Configuration and Functions

VQFN 0.5 mm Pitch
RGZ 48 Pin
Top View



Pin Functions

PIN			DESCRIPTION
SIGNAL	NO.	I/O	
DATA LANES PINS			
IN0p, IN0n	38, 39	Input (100Ω diff)	Lane 0 Differential Input
IN1p, IN1n	41, 42		Lane 1 Differential Input
IN2p, IN2n	44, 45		Lane 2 Differential Input
IN3p, IN3n	47, 48		Lane 3 Differential Input
OUT0p, OUT0n	23, 22	Output (100Ω diff)	Lane 0 Differential Output
OUT1p, OUT1n	20, 19		Lane 1 Differential Output
OUT2p, OUT2n	17, 16		Lane 2 Differential Output
OUT3p, OUT3n	14, 13		Lane 3 Differential Output
CONTROL PINS			
ADDR	3	3-level Input	I^2C Target Address Select.
EN	26	I	Device Enable. This input incorporates internal pullup of 200 kΩ.
NC	7, 40, 46		No Connect. These terminals may be left un-connected, or connect to GND.
RSTN	35	I	Active Low Device Reset. This is 1.1V input. This input includes a 150kΩ resistor to the V_{DDD} core supply. An external capacitor to GND is recommended on the RSTN input to provide a power-up delay. This signal is used to place the TVB1440 into Shutdown mode for the lowest power consumption. When the RSTN input is asserted, all outputs are high-impedance, and inputs are ignored; all I^2C registers are reset to their default values. At power up, the RSTN input must not be de-asserted until the V_{CC} and V_{DD} supplies have reached at least the minimum recommended supply voltage level.
RSVD1	10	I	Reserved pins. Please connect the pin to GND through 1K resistor.
RSVD2	11	I	Reserved pins. Please connect the pin to VCC through 1K resistor.
RSVD3	27	I	Reserved pins. Please connect the pin to VCC through 1K resistor.
RSVD4	28	I	Reserved pins. Please connect the pin to GND through 1K resistor.
SCL_CTL SDA_CTL	4 5	I/O	Bidirectional I2C interface to configure TVB1440. This interface is active independent of EN input but inactive when RSTN is low.
TEST1-6	8, 9, 29, 30, 33, 34		Test Outputs. Do not connect.

Pin Functions (continued)

PIN			DESCRIPTION
SIGNAL	NO.	I/O	
SUPPLY AND GROUND PINS			
GND	18, 24, 31, PAD		Ground. Reference GND connections include the device package exposed thermal pad.
VDD	2, 6, 12, 15, 21, 25, 32, 37, 43		Low voltage supply for analog and digital core. Nominally 1.1V
VCC	1, 36		3.3V Supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	VCC	–0.3	4	V
	VDD	–0.3	1.3	
Voltage range	HS Link I/O (OUTx, INx) Differential Voltage	–0.3	1.3	V
	RSTN	–0.3	1.3	
	SCL_CTL, SDA_CTL, ADDR, EN	–0.3	4	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	-65	150	·C
Electrostatic discharge	Human body model (HBM) (1)	–2000	2000	V
	Charged-device model (CDM) (2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VCC	Supply Voltage, IO	3		3.6	V
VDD	Supply Voltage, CORE	1		1.26	V
V_{IH}	High-level input voltage for ADDR, EN	1.9		3.6	V
V_{IL}	Low-level input voltage for ADDR, EN	0		0.8	V
$V_{IH,RSTN}$	High-level input voltage for RSTN (typical hysteresis of 80mV)		0.75		V
$V_{IL,RSTN}$	Low-level input voltage for RSTN (typical hysteresis of 80mV)		0.3		V
T_A	Operating free-air temperature	0		85	°C
f_{scl}	I2C CK frequency at SCL_CTL (standard I2C mode (1))			100	kHz

(1) The local interface through SCL_CTL and SDA_CTL should follow standard mode I2C specifications

7.4 Thermal Information

THERMAL METRIC[1]		TVB1440 RGZ (48 Pin)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current 4 lanes operation[1]		130	230	mA
I_{STDN}	Shutdown supply current[1]		1.5	3	mA
I_{OD}	Squelch (output disable) supply current		35	50	mA
V_{OD0}	Output differential voltage swing	238	340	442	mVpp
V_{OD1}		357	510	663	
V_{OD2}		484	690	897	
V_{OD3}		700	1000	1300	
PE_0	Output pre-emphasis		0		dB
PE_1			3		
PE_2			6		
PE_3			9		
R_{OUT}	Driver output impedance		50		Ω
$I_{(TXSHORT)}$	Output pins short circuit current limit			50	mA
$V_{(SQUELCH)}$	Squelch threshold voltage for input signals (default)		80		mVpp

(1) Values are V_{DD} supply measurements; VCC supply measurements are 5 mA (typical) and 8 mA (max), with zero current in shutdown mode.

7.6 Timing Requirements

		MIN	TYP	MAX	UNIT
t_{ramp1}	Time V_{DD} must stable before V_{CC} is applied	10			µS
t_{ramp2}	Time RSTN must remain asserted until V_{CC}/V_{DD} voltage has reached minimum recommended operation	100			µS
t_{ramp3}	Time device will be available for operation after a valid reset	400			mS

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time		300		ps
t_{sk1}	Intra-pair output skew (Figure 1)			20	ps
t_{sk2}	Inter-pair output skew (Figure 1)			100	ps
Δt_{jit}	Total peak-to-peak residual jitter V_{OD0}; PE_0; EQ = 8dB; clean source; minimum input and output cabling; PRBS7 data pattern.			15	ps
t_{sq_enter}	Squelch entry time Time from a loss of valid input signal to ML output off	10		120	µS
t_{sq_exit}	Squelch exit time Time from valid input signal available while in squelch mode to ML outputs on			1	µS

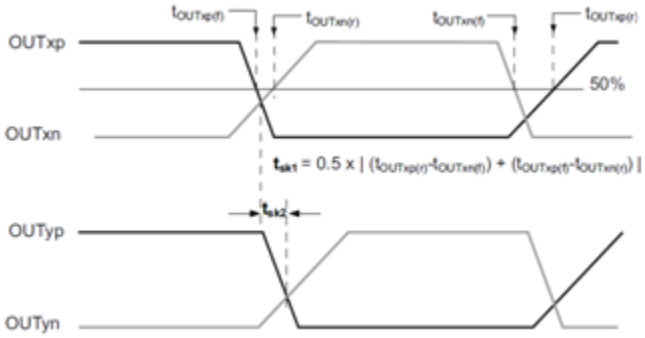


Figure 1. Output Skew Definitions

7.8 Typical Characteristics

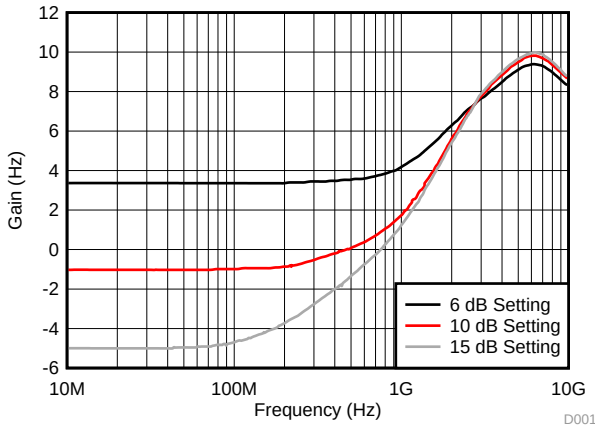


Figure 2. Typical EQ Gain Curves (simulations)

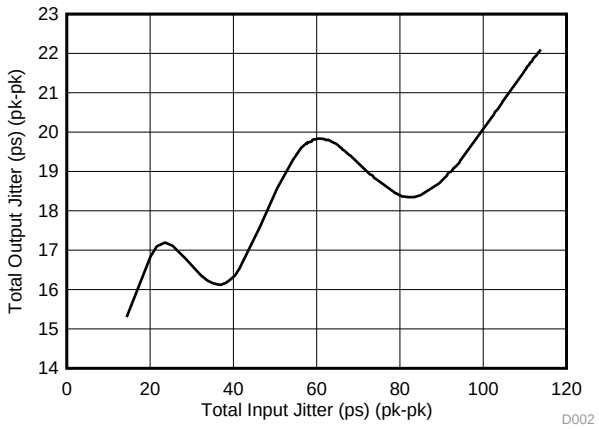


Figure 3. Jitter Performance with Optimal EQ Settings

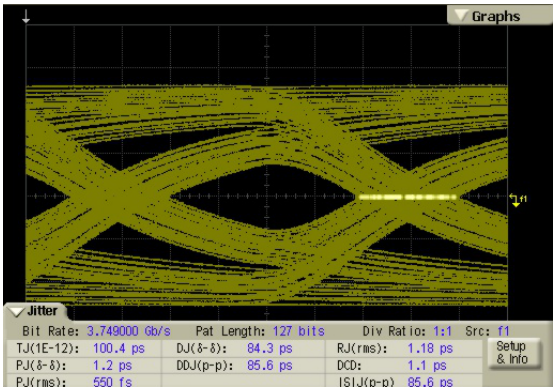


Figure 4. 3.75-Gbps Input With 20 Inch Trace

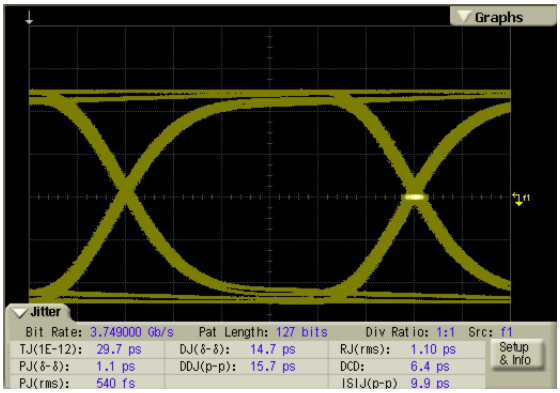


Figure 5. 3.75-Gbps Output with 20 Inch Input Trace and 8-dB EQ Setting

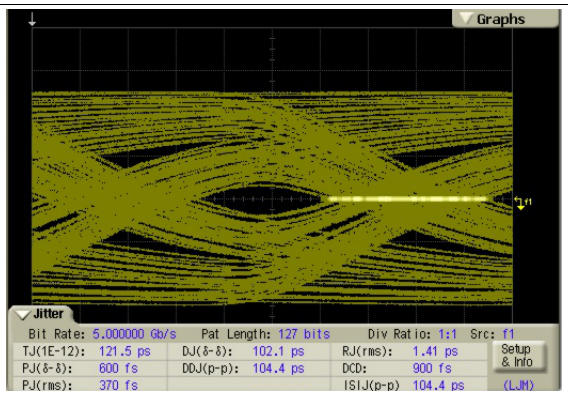


Figure 6. 5-Gbps Input with 20 Inches Trace

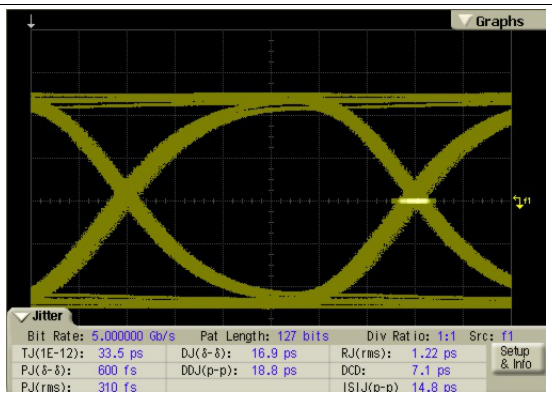


Figure 7. 5-Gbps Output with 20 Inch Input Trace and 13-dB EQ Setting

8 Detailed Description

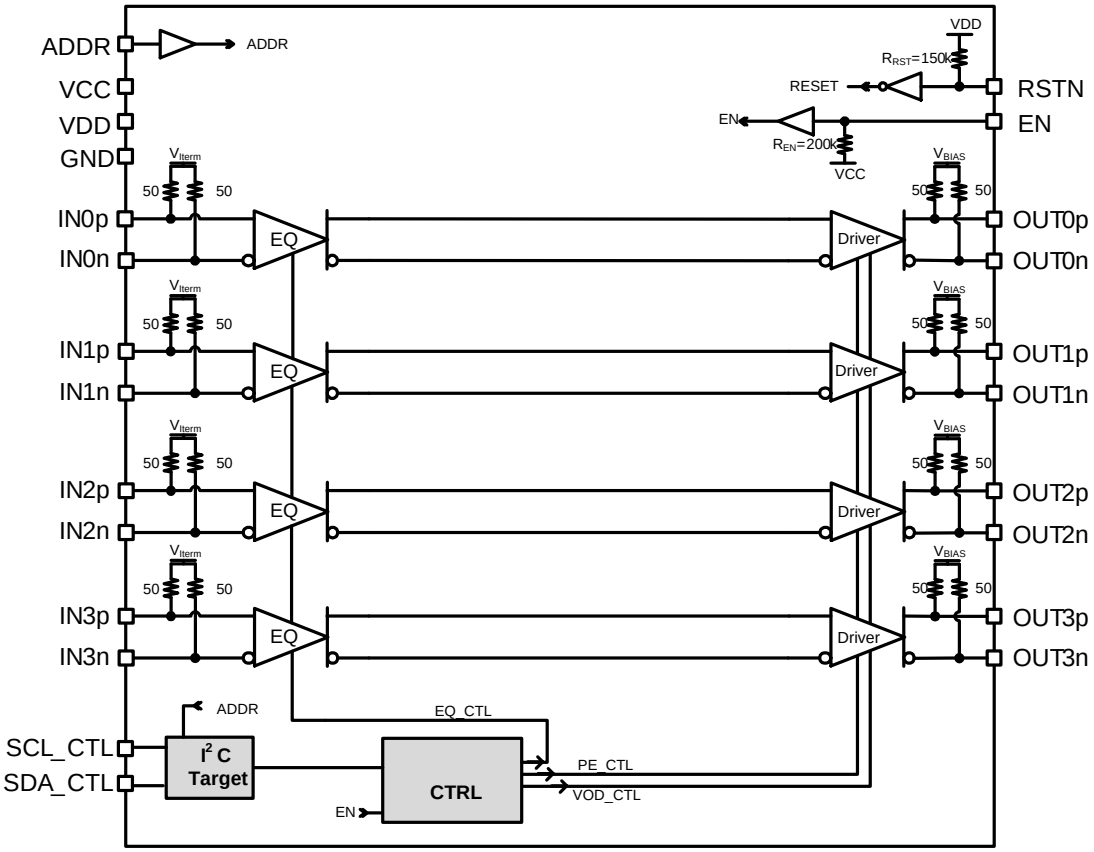
8.1 Overview

TVB1440 is a 4 channel HS re-driver signal conditioner for TV applications. I2C control provides the wide ranges of flexibility to configure the device for optimal signal conditioning so that video data link between a source and sink can achieve high fidelity. TVB1440 allows larger distance between a Chipset and TCON boards through its excellent jitter cleaning capability.

The TVB1440 is optimized for power conscience applications. Apart from its low active power, TVB1440 contains activity detection circuitry on the data link input that transitions to a low-power output disable mode in the absence of a valid input signal. This activity detect circuit can be disabled if desired. The device also has a shutdown mode when exercised results in 2 mW.

The TVB1440 receiver and driver provide input and output common mode voltage bias. It is required that both receive and transmit end of the device is ac coupled in application use cases. Suggested value for the ac coupling capacitors is 75-200 nF.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Equalization

TVB1440 provides flexible continuous time linear equalization (CTLE) to compensate for large trace or cable loss at its input resulting improved eye at the output signals. It has selectable control for receive equalization accessible through I^2C.

8.3.2 Configurable Output

Transmitter in each channel has 4 levels of pre-emphasis and 4 levels of output voltage swing settings which enable optimum video signal performance from the TVB1440 to downstream receiver.

8.3.3 Squelch

TVB1440 has active Squelch feature that allows automatic shutdown of output drivers when it does not have valid input signal. The feature can be disabled through I2C if not desired.

8.4 Device Functional Modes

8.4.1 Active Mode

Normal operation mode. The data lanes of TVB1440 work normally.

8.4.2 Shutdown Mode

Device is in lowest power mode. This mode is invoked by de-asserting RSTN or EN low.

8.4.3 Squelch Mode

The device does not have valid input signal. Output drivers are turned off.

8.5 Programming

8.5.1 Local I^2C Interface

It is required to use the TVB1440's local I^2C interface to configure the TVB1440's receivers (IN[3:0]P/N) and transmitters (OUT[3:0]P/N). The TVB1440's internal registers are accessed through the SCL_CTL pin and SDA_CTL pin. The 7-bit I^2C slave address of the TVB1440 is determined by the ADDR pin.

Table 1. TVB1440 I^2C Slave Address Options

ADDR	7-BIT I^2C SLAVE ADDRESS	READ SLAVE ADDRESS	WRITE SLAVE ADDRESS
Low (VIL)	7'b0101100	'h59	'h58
V_{CC}/2 (VIM)	7'b0101101	'h5B	'h5A
High (VIH)	7'b0101110	'h5D	'h5C

Before adjusting the TVB1440's registers, a writing a zero to bit 2 of address 04h is required to enable the receiver and transmitter adjustments.

8.5.2 Receiver (IN[3:0]P/N) Adjustments

8.5.2.1 Equalization Level

It is recommended to use the TVB1440 local I^2C interface to configure the TVB1440 receiver equalization level. Software should then enable equalization control by writing a one to EQ_I2C_ENABLE bit (bit 7 at address 05h). After EQ_I2C_ENABLE is set, then software can program the equalization for each lane (IN[3:0]) to the appropriate value. Refer to Table 2 for details on equalization settings for each lane.

Table 2. TVB1440 Equalization Levels

Address	Bits(s)	Description	Access
04h	2	Receiver and transmitter adjustment. 0 – configure receiver and transmitter using I2C (required) 1 – reserved (default)	RW
05h	2:0	EQ_LEVEL_LANE0. This field selects the EQ gain level for Lane 0 (IN0P/N). 000 – 0 dB 001 – 2 dB (3.75Gbps); 2.5 dB (5Gbps) 010 – 3.5 dB (3.75Gbps); 5 dB (5Gbps) 011 – 5 dB (3.75Gbps); 6 dB (5Gbps) 100 – 6.5 dB (3.75Gbps); 8 dB (5Gbps) 101 – 8 dB (3.75Gbps); 11 dB (5Gbps) 110 – 9.5 dB (3.75Gbps); 13 dB (5Gbps) 111 – 12 dB (3.75Gbps); 15 dB (5Gbps)	RW
05h	7	EQ_I2C_ENABLE. This field allows EQ control through I2C 0 – reserved (default) 1 – EQ level is set by I2C (required)	RW
07h	2:0	EQ_LEVEL_LANE1. This field selects the EQ gain level for Lane 1 (IN1P/N. Bit definition identical to that of EQ_LEVEL_LANE0.	RW
09h	2:0	EQ_LEVEL_LANE2. This field selects the EQ gain level for Lane 2 (IN2P/N). Bit definition identical to that of EQ_LEVEL_LANE0.	RW
0Bh	2:0	EQ_LEVEL_LANE3. This field selects the EQ gain level for Lane 3 (IN3P/N. Bit definition identical to that of EQ_LEVEL_LANE0.	RW

8.5.2.2 Squelch Level

The TVB1440 squelch level defaults to 80mVpp. If it is necessary to adjust the squelch level, it can be done by changing the SQUELCH_SENSITIVITY register located in the TVB1440's Local I2C register space.

Table 3. Squelch Sensitivity Levels

Address	Bits(s)	Description	Access
03h	5:4	SQUELCH_SENSITIVITY. Main link squelch sensitivity is selected by this field, and determines the transitions to and from the Output Disable mode. 00 – Main Link IN0P/N squelch detection threshold is set to 40mVpp. 01 – Main Link IN0P/N squelch detection threshold is set to 80mVpp. (Default) 10 – Main Link IN0P/N squelch detection threshold is set to 160mVpp. 11 – Main Link IN0P/N squelch detection threshold is set to 250mVpp.	RW
	3	SQUELCH_ENABLE. 0 – Main Link IN0P/N squelch detection is enabled (default) 1 – Main Link IN0P/N squelch detection is disabled.	RW

8.5.3 Main Link Output [OUT[3:0]P/N] Adjustments

The TVB1440 Main link outputs (OUT[3:0]) must be set in link address space by following specified I^2C access method.

8.5.3.1 LINK Address Space

Access to and from the TVB1440 LINK address space is indirectly addressable through the local I^2C registers as illustrated in the Figure 8.

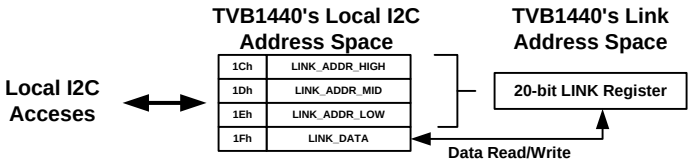


Figure 8. Accessing TVB1440 LINK Registers

The configuration of these registers can be performed through the local I^2C interface, where three registers (from 1Ch to 1Eh) are used as the address to the LINK register and another one (1Fh) as a data to be read/written.

8.5.4 Example Script

The script below is for a Total Phase Aardvark I²C controller. Details on the Total Phase Aardvark I²C controller can be obtained from the Total Phase website. This example is for a 5.0 Gbps data rate with 4 active lanes.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
<i2c_bitrate khz="100"/>

======Program the device=====
<i2c_write addr="0x2D" count="1" radix="16">04 00</i2c_write> />

======Program Link Bandwidth Settings to 5Gbps======LINK 00100h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 14</i2c_write> />


======Program Num of Lanes to 4.s======LINK 00101h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 04</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 0======LINK 00103h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 03</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 1======LINK 00104h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 04</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 2======LINK 00105h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 05</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 3======LINK 00106h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 06</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Set Power Mode to Normal======LINK 00600h=====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 06</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

=====May want to adjust Squelch Level===
<i2c_write addr="0x2D" count="1" radix="16">03 10</i2c_write> />

=====Enable EQ===
<i2c_write addr="0x2D" count="1" radix="16">05 80</i2c_write> />

=====Set EQ level to 11dB(5Gbps) for lane 0===
<i2c_write addr="0x2D" count="1" radix="16">05 85</i2c_write> />

=====Set EQ level to 11dB(5Gbps) for lane 1===
<i2c_write addr="0x2D" count="1" radix="16">07 05</i2c_write> />

=====Set EQ level to 11dB(5Gbps) for lane 2===
<i2c_write addr="0x2D" count="1" radix="16">09 05</i2c_write> />

=====Set EQ level to 11dB(5Gbps) for lane 3===
<i2c_write addr="0x2D" count="1" radix="16">0B 05</i2c_write> />
</aardvark>
```

8.6 Register Maps

Table 4. TVB1440 LINK Registers

LINK Address	NAME	Value Written	Value Read	Description
00100h	LINK_BW_SET	06h	00h	<1.6Gbps per lane
		0Ah	01h	1.6-2.7Gbps per lane
		14h	02h	2.7-5.0Gbps per lane
00101h	LANE_COUNT_SET	00h	00h	All Lanes disabled
		01h	01h	One lane enabled (OUT0).
		02h	03h	Two lanes enabled (OUT[1:0]).
		04h	0Fh	Four lanes enabled (OUT[3:0]).
00103h	LANE0_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT0.
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT0.
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT0.
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT0.
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT0.
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT0.
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT0.
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT0.
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT0.
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT0
00104h	LANE1_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT1.
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT1.
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT1.
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT1.
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT1.
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT1.
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT1.
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT1.
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT1.
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT1
00105h	LANE2_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT2.
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT2.
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT2.
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT2.
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT2.
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT2.
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT2.
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT2.
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT2.
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT2
00106h	LANE3_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT3.
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT3.
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT3.
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT3.
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT3.
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT3.
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT3.
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT3.
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT3.
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT3
00600h	SET_POWER	01h	00h	Normal Mode
		02h	01h	Power-Down mode.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TVB1440 is a signal conditioner especially suited for equalizing channel loss due to traces and flexible cable between digital TV chipset and TCON receiver.

9.1.1 Typical Application

The device can be helpful improving eye diagram by placing it either end of the flexible cable in digital TV chipset or TCON board or at the both. Figure 9 shows a typical application for TV interface.

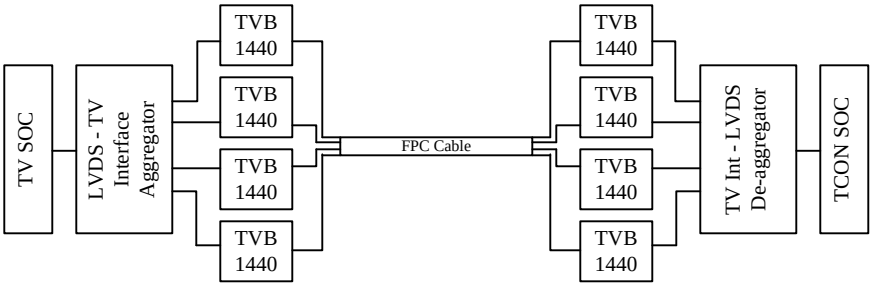


Figure 9. Typical Application of TVB1440 in 4K2K Digital TV Interface

9.1.1.1 Design Requirements

Table 5. Design Parameters

PARAMETER	VALUE
V_{DD} Supply	1.1 V
V_{CC} Supply	3.3 V
TV Max Resolution Requirement	
Pixel Clock (MHz)	1194
Horizontal Active (pixels)	3840
Vertical Active	2160
Color bit Depth (6bpc, 8bpc, 10bpc)	10 (30 bpp)
Refresh Rate	120 Hz
Panel Configuration (A or B)	B
Channel Requirements	
Input Channel Insertion Loss	Up to 12 dB at 3.75 Gbps
Output Channel Insertion Loss	Up to 12 dB at 3.75 Gbps
TVB1440 Settings	
Number of Lanes (1, 2, or 4)	4
Link Rate (Gbps)	3.75
RX EQ Setting (dB)	6.5 dB
TX VOD Setting (Level 0, 1, 2, or 3)	Level 3 (1000 mVpp)
TX Pre-Emphasis Setting (Level 0, 1, 2, or 3)	Level 0 (0 dB)

9.1.1.2 Detailed Design Procedure

9.1.1.2.1 Common 4k2k TV Panel Configuration

A common 4k2k TV is broken into four 1920 x 1080 panels or four 960 x 2160 panels. For this particular implementation, panel configuration B is assumed. It is also assumed that two TVB1440 are used for each panel (one near SOC and one near TCON) for a total of eight TVB1440.

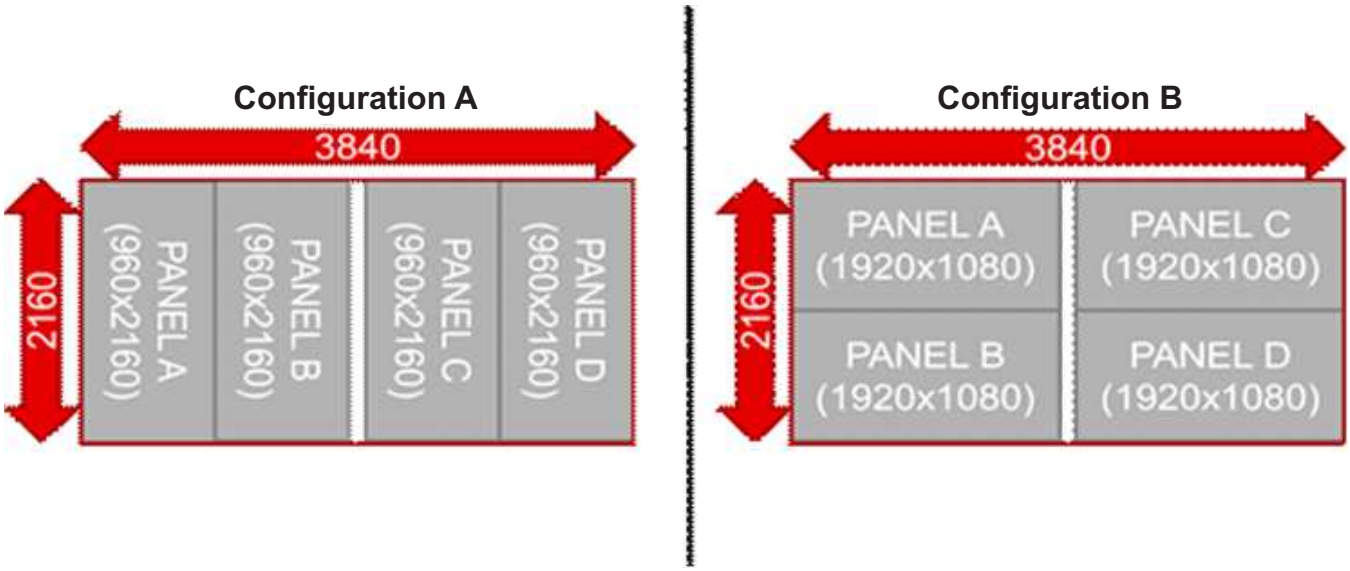


Figure 10. Common Panel Configurations

9.1.1.2.2 1Max Stream Rate

The maximum stream rate can be derived from the maximum TV resolutions pixel clock and color depth. For this example, the maximum pixel clock is 1194 MHz. Because the TV is broken into 4 panels, the actual pixel clock for each panel is 298.5 MHz.

Stream Bit Rate = PixelClock x bpp

Stream Bit Rate = 298.5 x 30

Stream Bit Rate = 8.955 Gbps.

9.1.1.2.3 Encoded Stream Rate

Most high-speed video standards are 8b10b encoded. Because of 8b10b encoding overhead, an additional 20% must be added to the stream bit rate. On top of the 8b10b, there are some additional overhead due to packetization before the 8b10b encode that also must be added to the stream bit rate. For example, a particular video standard may define the actual coded stream rate by the following equation.

Encoded_Stream_Rate = #_of_Bytes_for_bpp x 8 x 1.25 x PixelClock

Encoded_Stream_Rate = #_of_Bytes_for_bpp x 8 x 1.25 x PixelClock

Encoded_Stream_Rate = 11.94Gbps.

9.1.1.2.4 TVB1440 Configuration

The TVB1440 must be configured by the SOC using I2C. Because of the limited number of I2C address available on the TVB1440, an I2C switch needs to be incorporated in order to configure each of the TVB1440. Figure 11 shows an example implement using the Texas Instruments TCA9546A 4-channel I2C switch.

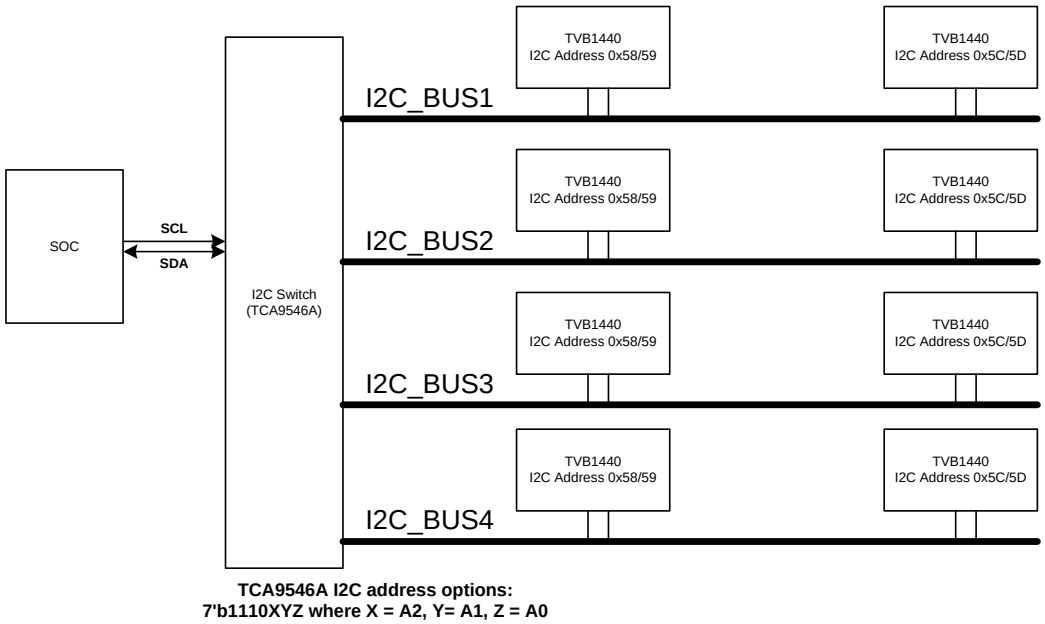
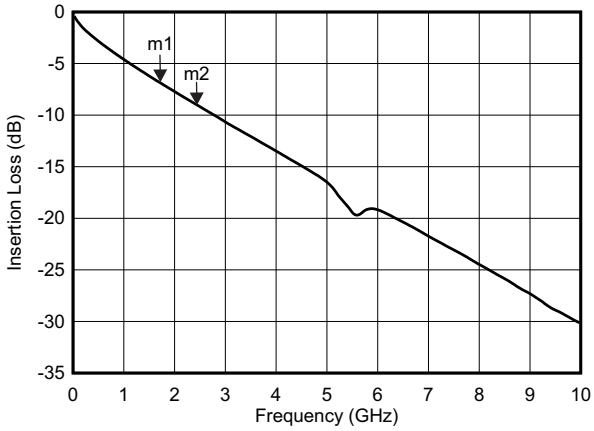


Figure 11. Example I2C Switch Implementation

9.1.1.2.5 Receiver Equalization Setting

The TVB1440 has a receiver equalizer that is adjustable from 0dB to 15 dB at 5 Gbps. The common approach to determine the proper equalizer setting is to measure the insertion loss of the channel at the input of the TVB1440 at the Nyquist frequency of the data rate (1.875 GHz for 3.75 Gbps and 2.5 GHz for 5 Gbps). For example, if the input channel is 20 inches of trace with 4 mil width over FR4, the insertion loss at 3.75 Gbps would be -7.3 dB and at 5 Gbps would be -9.1 dB. The register EQ_LEVEL_LANEx, where X = 0, 1, 2, or 3 should be programmed to 3'b100 for a 3.75 Gbps data rate and should be programmed to 3'b101. The actual setting may need to be adjusted based on the additional channel parasitics from package, vias, and connectors.



m1 frequency = 1.876 GHz I_L = –7.346

m2 frequency = 2.500 GHz I_L = –9.185

Figure 12. Insertion Loss of 20 Inch FR4 Trace With 4-mil Width

9.1.1.2.6 Transmitter Settings

The TVB1440's transmitter controls have four settings for voltage swing and four settings for pre-emphasis. The best transmitter setting to use is a function of the output channel insertion loss and the inputs eye requirement of the device at end of the channel. For the case in which a TVB1440 is at the end of the channel, the output channel's insertion loss should not be greater than the receiver equalization of the TVB1440.

To specify the largest eye opening at the end of the channel, the best voltage swing setting should be either level 2 or level 3. It is also recommended to use either a pre-emphasis level of 0 dB or 3dB. The pre-emphasis setting can be thought of as a way to reduce the amount receiver equalizer required by the device at end channel. For example, a 3.5dB setting could allow for the receive equalization setting for the TVB1440 to be reduced from 12dB to 10dB. If necessary, these settings can be adjusted up or down in order to improve the eye opening at the end of the channel.

9.1.1.2.7 RESET

The TVB1440 RSTN input gives control over the device reset and to place the device into shut-down mode. When RSTN is low, all registers are reset to their default values, which means all HS Link ports are disable. When the RSTN pin is released back to high, the device comes out of the shut-down mode. To turn on the HS Link, it is necessary to provision the device registers through the local I^2C_CTL interface.

It is critical to transition the RSTN input from a low to a high level after both V_{CC} and V_{DD} supply voltages have reached the minimum recommended operating voltage. This is achieved by a control signal to the RSTN input, or by an external capacitor connected between RSTN and GND. To insure that the TVB1440 is properly reset, the RSTN pin must be de-asserted for at least 100 µs before being asserted.

The RSTN input includes a 150k resistor from the input to the V_{DD} supply. An external capacitor connected between RSTN and GND allows delaying the RSTN signal during power up. When implementing the external capacitor the size of the external capacitor depends on the power up ramp of the VCC and VDD supplies; a slower ramp-up results in a larger value external capacitor. Approximately 200 nF capacitor is a reasonable first estimate for the size of the external capacitor for most applications.

Both RSTN implementations are shown in Figure 13.

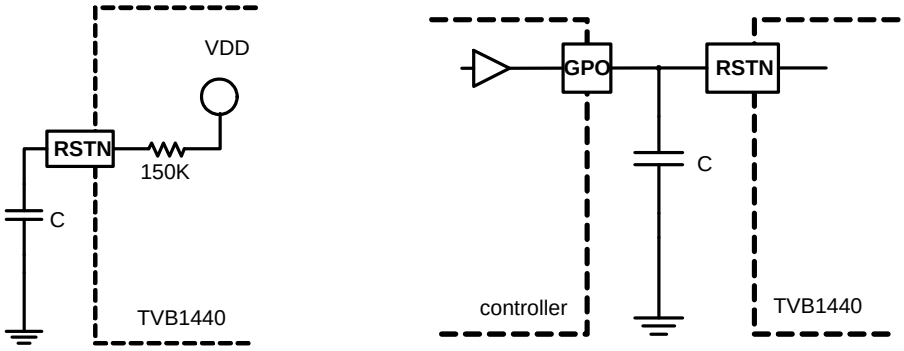


Figure 13. (a) Reset Implementation Using a Capacitor, (b) Microprocessor Drives the Pin

Figure 14 shows a typical schematic implementation either in TV chipset or TCONS receiver board.

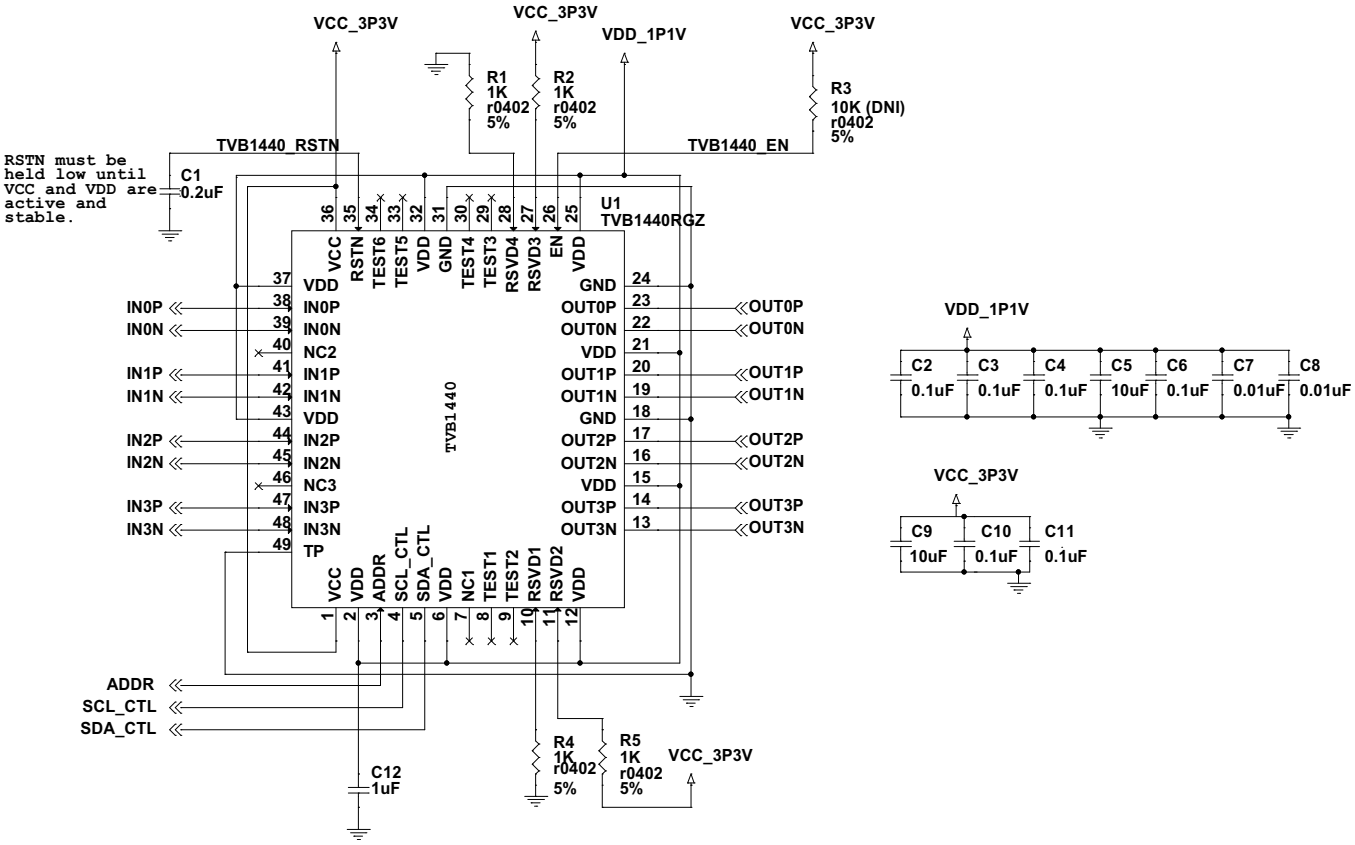


Figure 14. Schematic Implementation of TVB1440

10 Power Supply Recommendations

The following power-up and power-down sequences describe how the RSTN signal is applied to the TVB1440.

10.1 Power-Up Sequence

1. Apply VDD then VCC (recommended both less than 10-ms ramp time). VDD must be asserted first and stable for greater than 10 µs before VCC is applied.
2. RSTN must remain asserted until VCC/VDD voltage has reached minimum recommended operation for more than 100 µs.
3. De-assert RSTN (Note: This RSTN is a 1.1V interface and is internally connected to VDD through a 150-kΩ resistor).
4. Device will be available for operation approximately 400 ms after a valid reset.

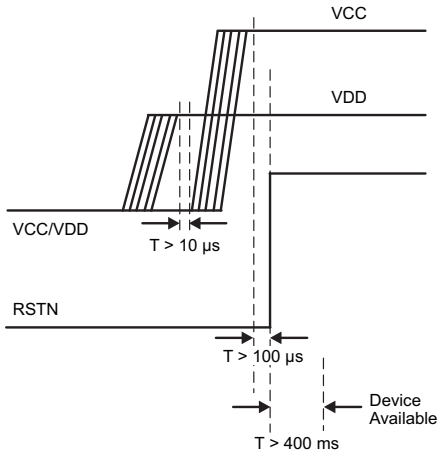


Figure 15. Power-up Sequence

10.2 Power-Down Sequence

There is no power-down sequence required.

11 Layout

11.1 Layout Guidelines

11.1.1 Differential Pairs

This section describes the layout recommendations for all the TVB1440 differential pairs: IN[3:0] and OUT[3:0].

- Must be designed with a differential impedance of 100 Ω ± 10% or 50-Ω single-ended impedance.
- In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity and; therefore, negative impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90 degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This minimizes any length mismatch causes by the bends; and therefore, minimizes the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. Longer trace lengths require very careful routing to assure proper signal integrity.
- Keep intra-pair skew to a minimum in order to minimize EMI. There should be less than 5 mils difference between a differential pair signal and its complement.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. It is recommended to keep the vias count to 2 or less.

11.1.2 Layout Example

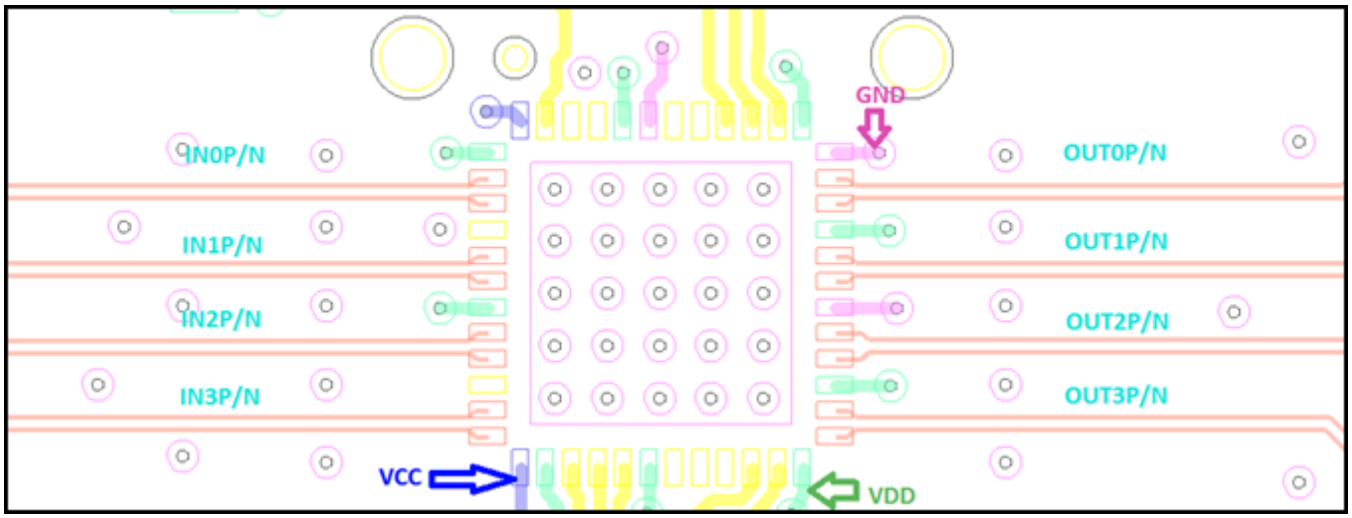


Figure 16. TBV1440 Layout

Layout Guidelines (continued)

11.1.3 Placement

- A 100-nF should be placed as close as possible on each V_{DD} and V_{CC} power pin.
- The 100-nF capacitors on the IN[3:0] and OUT[3:0] nets should be placed close to the connector.
- The ESD and EMI protection devices (if used) should also be placed as possible to the connector.

11.1.4 Package Specific

- The TVB1440 package as a 0.5 mm pin pitch
- The TVB1440 package has a 4.1 mm x 4.1 mm thermal pad. This thermal pad must be connected to ground through a system of vias.
- All vias under device, except for those connected to thermal pad, should be solder masked to avoid any potential issues with thermal pad layouts.

11.1.5 Ground

It is recommended that only one board plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TVB1440 should be connected to this plane through a system of vias.

12 器件和文档支持

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12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVB1440RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TVB1440
TVB1440RGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TVB1440

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

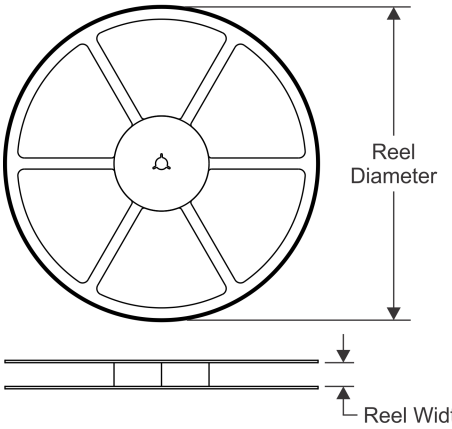
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

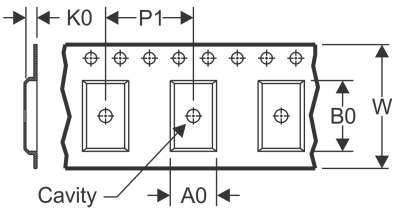
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

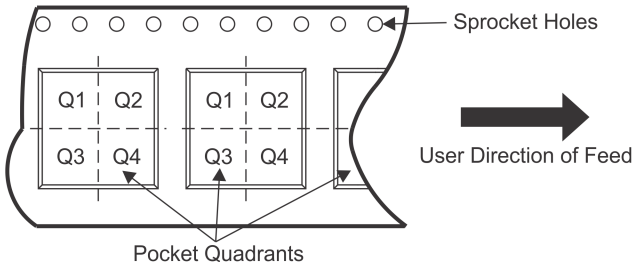


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

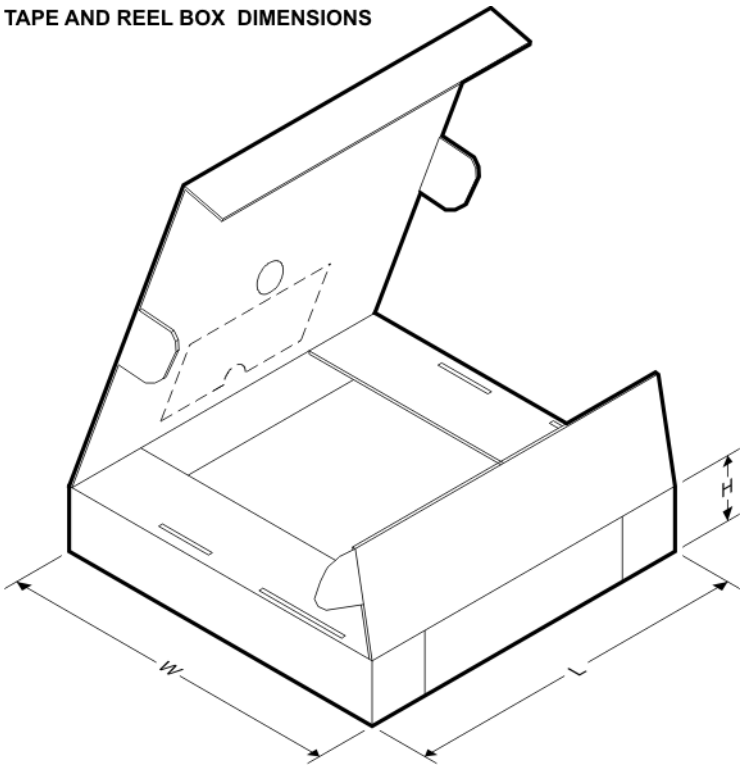
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVB1440RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVB1440RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0

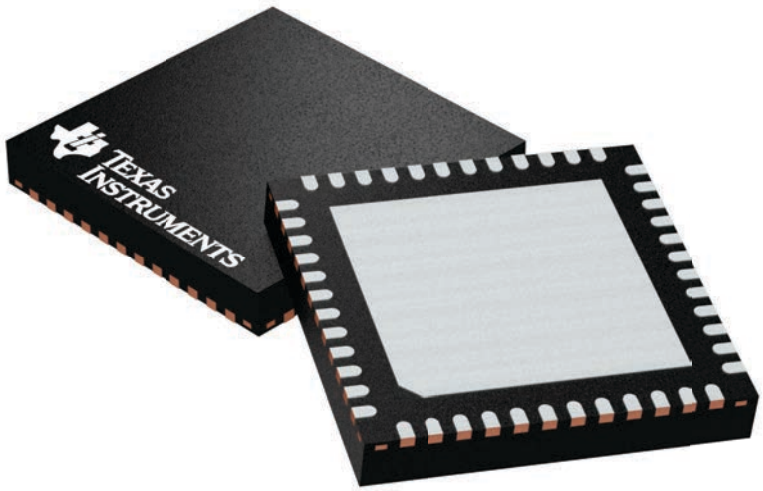
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

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