

# TUSB2161 具有 BC 1.2 控制器的 USB 2.0 高速信号调节器

## 1 特性

- 宽电源电压范围：2.3V 至 6.5V
- 超低 USB 断开和关断功耗
- 可提供 USB 2.0 高速信号调节
- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 支持低速、全速和高速信号传输
- 集成了 BC 1.2 CDP 电池充电控制器
- 主机或器件无关
- 支持长达 5m 的电缆
  - 通过外部下拉电阻器值实现四种可选的信号增强（边沿升压与直流升压）设置
  - 通过上拉或下拉实现三种可选的 RX 灵敏度设置，以补偿高损耗应用中的 ISI 抖动
- 支持长达 10m 的电缆和两台 TUSB2161 器件
- 可扩展解决方案 - 器件可通过菊花链连接用于高损耗应用
- 与 TUSB211A、212、214 和 217A 引脚兼容 (3.3V)

## 2 应用

- 笔记本电脑、台式机或扩展坞
- 便携式电子产品
- 平板电脑
- 手机
- 电视
- 有源电缆、电缆扩展器、背板

## 3 说明

TUSB2161 是第三代 USB 2.0 高速信号调节器，旨在补偿传输通道中的交流损失（由于电容性负载）和直流损失（由于电阻性负载）。

TUSB2161 采用了专利设计，可通过边缘加速器来对 USB 2.0 高速信号的传输边缘进行加速，并通过直流升压功能来提高静态电平。

此外，TUSB2161 还具有预均衡功能，可提高接收器的灵敏度并补偿较长线缆应用中的码间串扰 (ISI) 抖动。USB 低速和全速信号特征不受 TUSB2161 的影响。

TUSB2161 可在不改变数据包计时或不增加传播延迟的情况下提高信号质量。

TUSB2161 可使用长达 5 米的线缆帮助系统通过 USB 2.0 高速近端眼图合规性测试。

TUSB2161 与 USB On-The-Go (OTG) 和电池充电 (BC 1.2) 协议兼容。集成的 BC 1.2 电池充电控制器可通过控制引脚启用。

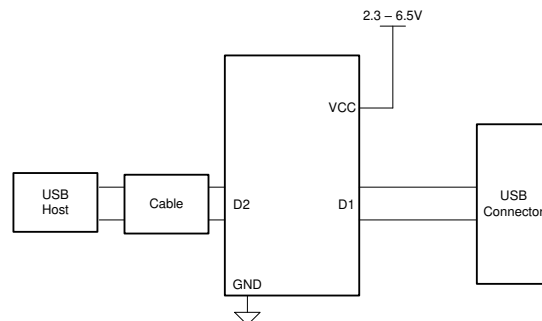
### 器件信息

器件型号 <sup>(1)</sup>	封装 <sup>(2)</sup>	OP TEMP (T <sub>A</sub> ) °C	封装尺寸 <sup>(3)</sup>
TUSB216	RWB ( X2QFN , 12 )	0 至 70	1.6mm x 1.6mm
TUSB216I		-40 至 85	
TUSB216-Q1		-40 至 105	

(1) 请参阅 [器件比较](#)

(2) 有关详细信息，请参阅 [节 11](#)。

(3) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



简化版原理图



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## 4 Device Comparison

	TUSB211A	TUSB212	TUSB214	TUSB216	TUSB217A
Industrial Variant Available	Y	Y	Y	Y	Y
Automotive Variant Available	Y	Y	Y	Y	Y
Supply (V)	2.3 to 6.5	3.3	3.3	2.3 to 6.5	2.3 to 6.5
DC Boost	Tandem with AC Boost	3 levels	3 levels	Tandem with AC Boost	Tandem with AC Boost
I2C Control	N	Y	Y	Y	Y
RX pre-equalization for ISI compensation	N/A	N/A	N/A	3 levels	3 levels
Charging Downstream Port (CDP) controller	N/A	N/A	Always ON	Pin Controlled	Always ON. Dynamically selected by DCP/CDP pin
Dedicated Charging Port (DCP) controller	N/A	N/A	N/A	N/A	Always ON. Dynamically selected by DCP/CDP pin
Cable length compensation for near-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge)	6/3 - 28AWG (10 - 24AWG with one redriver on each end)	4/2 - 28AWG	4/2 - 28AWG	6/3 - 28AWG (10 - 24AWG with one redriver on each end)	6/3 - 28AWG (10 - 24AWG with one redriver on each end)
Cable length compensation for far-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge)	10/8 - 26AWG (10 - 28AWG with one redriver on each end)	8/6 - 28AWG	8/6 - 28AWG	10/8 - 26AWG (10 - 28AWG with one redriver on each end)	10/8 - 26AWG (10 - 28AWG with one redriver on each end)

## 5 Pin Configuration and Functions

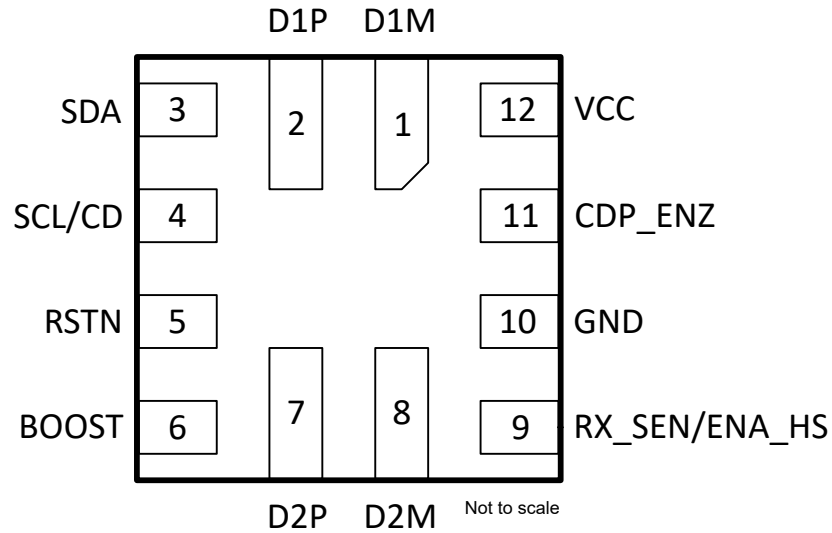


图 5-1. TUSB216I RWB Package, 12-Pin X2QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
BOOST	6	I	N/A	USB High-speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
CDP_ENZ	11	I	500 k $\Omega$ PU	Set CDP_ENZ is low to enable BC 1.2 CDP controller

表 5-1. Pin Functions (续)

PIN		TYPE <sup>(1)</sup>	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
RX_SEN <sup>(3)</sup> /ENA_HS	9	I/O	N/A	<p>In I2C mode: Reserved for TI test purpose.</p> <p>In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High-speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) – high RX sensitivity (high loss channel) M (pin is left floating) – medium RX sensitivity (medium loss channel) L (pin is pulled low) – low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 <math>\mu</math>s – 128 <math>\mu</math>s].</p>
D2P	7	I/O	N/A	USB High-speed positive port.
D2M	8	I/O	N/A	USB High-speed negative port.
GND	10	P	N/A	Ground
D1M	1	I/O	N/A	USB High-speed negative port..
D1P	2	I/O	N/A	USB High-speed positive port.
SDA <sup>(2)</sup>	3	I/O	500 k $\Omega$ PU 1.8 M $\Omega$ PD	<p>I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C].</p> <p>In non I2C mode: Reserved for TI test purpose.</p>
VCC	12	P	N/A	Supply power
RSTN	5	I	500 k $\Omega$ PU 1.8 M $\Omega$ PD	<p>Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-<math>\mu</math>F external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.</p>
SCL <sup>(2)</sup> /CD	4	I/O	When RSTN asserted there is a 500 k $\Omega$ PD	<p>In I2C mode: I2C clock pin [I2C address = 0x2C].</p> <p>Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.</p>

(1) I = input, O = output, P = power

(2) Pull-up resistors for SDA and SCL pins in I<sup>2</sup>C mode should be R<sub>Pull-up</sub> (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I<sup>2</sup>C mode.(3) Pull-down and pull-up resistors for RX\_SEN pin must follow R<sub>RXSEN1</sub> and R<sub>RXSEN2</sub> resistor recommendations in non I<sup>2</sup>C mode.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VCC	- 0.3	7	V
Voltage range USB data	DxP, DxM	- 0.3	5.5	V
Voltage range on BOOST pin	BOOST	-0.3	1.98	V
Voltage range other pins	RX_SEN, CDP_ENZ, SDA, SCL, RSTN	-0.3	5.5	V
Storage temperature, T <sub>stg</sub>		- 65	150	°C
Maximum junction temperature, T <sub>J(max)</sub>			125	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5	6.5	V
T <sub>A</sub>	Operating free-air temperature (Industrial)	- 40		85	°C
T <sub>J</sub>	Junction temperature (Industrial)			105	°C
V <sub>I2C_BUS</sub>	I2C Bus Voltage	1.62		3.6	V
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
DIGITAL	Voltage range other pins (SCL, SDA, RSTN, CDP_ENZ)	0		3.6	V
RX_SEN	Voltage range RX_SEN pin	0		5.0	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RWB (X2QFN)	UNIT
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	137.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>POWER</b>						
$I_{ACTIVE\_HS}$	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. $V_{CC}$ supply stable, with Boost = Max		22	36	mA
$I_{IDLE\_HS}$	High Speed Idle Current	USB channel = HS mode, no traffic. $V_{CC}$ supply stable, Boost = Max		22	36	mA
$I_{HS\_SUSPEND}$	High Speed Suspend Current	USB channel = HS Suspend mode. $V_{CC}$ supply stable		0.75	1.4	mA
$I_{FS}$	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, $V_{CC}$ supply stable		0.75	1.4	mA
$I_{DISCONN}$	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
$I_{SHUTDOWN}$	Shutdown Power	RSTN driven low, $V_{CC}$ supply stable		60	115	$\mu$ A
<b>CONTROL PIN LEAKAGE</b>						
$I_{LKG\_FS}$	Pin failsafe leakage current for SDA, RSTN	$V_{CC} = 0$ V, pin at $V_{IH, max}$		10	15	$\mu$ A
$I_{LKG\_FS}$	Pin failsafe leakage current for RX_SEN	$V_{CC} = 0$ V, pin at $V_{IH, max}$		6	15	$\mu$ A
$I_{LKG\_FS}$	Pin failsafe leakage current for SCL	$V_{CC} = 0$ V, pin at $V_{IH, max}$			70	nA
<b>INPUT RSTN</b>						
$V_{IH}$	High level input voltage		1.5		3.6	V
$V_{IL}$	Low-level input voltage		0		0.5	V
$I_{IH}$	High level input current	$V_{IH} = 3.6$ V, $R_{PU}$ enabled			$\pm 15$	$\mu$ A
$I_{IL}$	Low level input current	$V_{IL} = 0$ V, $R_{PU}$ enabled			$\pm 20$	$\mu$ A
<b>INPUT DIGITAL</b>						
$V_{IH}$	High level input voltage (CDP_ENZ)		1.5		3.6	V
$V_{IL}$	Low-level input voltage (CDP_ENZ)		0		0.5	V
$I_{IL}$	Low level input current	$V_{IL} = 0$ V			$\pm 20$	$\mu$ A
$I_{IH}$	High level input current	$V_{IH} = 3.6$ V			$\pm 15$	$\mu$ A
<b>INPUT RX_SEN (3-level input, for mid level leave pin floating)</b>						
$V_{IH(Max)}$	Maximum High level input voltage	$V_{CC} = 2.3$ V to 6.5 V			5.0	V
$V_{IH(Min)}$	Minimum High level input voltage	$V_{CC} > 4.5$ V		3.3		V
		$V_{CC} = 2.3$ V to 4.5 V (% of $V_{CC}$ )		75		%
$V_{IL}$	Low level input voltage	$V_{CC} > 4.5$ V			0.75	V
		$V_{CC} = 2.3$ V to 4.5 V (% of $V_{CC}$ )			15	%
<b>INPUT BOOST</b>						
$R_{BOOST\_LVL0}$	External pulldown resistor for BOOST Level 0				160	$\Omega$
$R_{BOOST\_LVL1}$	External pulldown resistor for BOOST Level 1		1.5	1.8	2	k $\Omega$
$R_{BOOST\_LVL2}$	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	k $\Omega$
$R_{BOOST\_LVL3}$	External pulldown resistor for BOOST Level 3 to remove upper limit for resistor value, can be left open		7.5			k $\Omega$
<b>OUTPUTS CD, ENA_HS</b>						
$V_{OH}$	High level output voltage for CD and ENA_HS	$I_O = -50$ $\mu$ A, $V_{CC} \geq 3.0$ V	2.5			V
$V_{OH}$	High level output voltage for CD	$I_O = -25$ $\mu$ A, $V_{CC} = 2.3$ V	1.7			V

## 6.5 Electrical Characteristics (续)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	High level output voltage for ENA_HS	I <sub>O</sub> = - 25 μA, V <sub>CC</sub> = 2.3V	1.8			V
V <sub>OL</sub>	Low level output voltage for CD and ENA_HS	I <sub>O</sub> = 50 μA			0.3	V
<b>I<sup>2</sup>C</b>						
C <sub>I2C_BUS</sub>	I <sup>2</sup> C Bus Capacitance		4		150	pF
I <sub>OL</sub>	I <sup>2</sup> C open drain output current	V <sub>OL</sub> = 0.4V	1.5			mA
V <sub>IL</sub>	2.3V ≤ V <sub>CC</sub> ≤ 4.3V, V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IL</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IH</sub>	2.3V ≤ V <sub>CC</sub> ≤ 4.3V, V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>	80			%
V <sub>IH</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>	75			%
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 1.8V +/-10%		1.6	2	2.5	kΩ
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%		2.8	4.7	7	kΩ
SCL Frequency					400	kHz
<b>DxP, DxM</b>						
C <sub>IO_DXX</sub>	Capacitance to GND	Measured with VNA at 240 MHz, V <sub>CC</sub> supply stable, Redriver off		2.5		pF

(1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DxP, DxM USB Signals</b>						
F <sub>BR_DXX</sub>	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V <sub>CC</sub> supply stable			480	Mbps
t <sub>R/F_DXX</sub>	Rise/Fall time		100			ps

(1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>POWER UP TIMING</b>					
$T_{RSTN\_PW}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			$\mu\text{s}$
$T_{STABLE}$	VCC must be stable before RSTN de-assertion	300			$\mu\text{s}$
$T_{READY}$	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	$\mu\text{s}$
$T_{RAMP}$	V <sub>CC</sub> ramp time			100	ms
$T_{RAMP}$	V <sub>CC</sub> ramp time	0.2			ms
<b>I2C (STD)</b>					
$t_{SUSTO}$	Stop setup time, SCL ( $T_r=600\text{ns}-1000\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 100kHz STD	4			$\mu\text{s}$
$t_{HDSTA}$	Start hold time, SCL ( $T_r=600\text{ns}-1000\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 100kHz STD	4			$\mu\text{s}$
$t_{SUSTA}$	Start setup time, SCL ( $T_r=600\text{ns}-1000\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 100kHz STD	4.7			$\mu\text{s}$
$t_{SUDAT}$	Data input or False start/stop, setup time, SCL ( $T_r=600\text{ns}-1000\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 100kHz STD	250			ns
$t_{HDDAT}$	Data input or False start/stop, hold time, SCL ( $T_r=600\text{ns}-1000\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 100kHz STD	5			$\mu\text{s}$
$t_{BUF}$	Bus free time between START and STOP conditions	4.7			$\mu\text{s}$
$t_{LOW}$	Low period of the I2C clock	4.7			$\mu\text{s}$
$t_{HIGH}$	High period of the I2C clock	4			$\mu\text{s}$
$t_F$	Fall time of both SDA and SCL signals			300	ns
$t_R$	Rise time of both SDA and SCL signals			1000	ns
<b>I2C (FM)</b>					
$t_{SUSTO}$	Stop setup time, SCL ( $T_r=180\text{ns}-300\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 400 kHz FM	0.6			$\mu\text{s}$
$t_{HDSTA}$	Start hold time, SCL ( $T_r=180\text{ns}-300\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 400 kHz FM	0.6			$\mu\text{s}$
$t_{SUSTA}$	Start setup time, SCL ( $T_r=180\text{ns}-300\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 400 kHz FM	0.6			$\mu\text{s}$
$t_{SUDAT}$	Data input or False start/stop, setup time, SCL ( $T_r=180\text{ns}-300\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 400 kHz FM	100			ns
$t_{HDDAT}$	Data input or False start/stop, hold time, SCL ( $T_r=180\text{ns}-300\text{ns}$ ), SDA ( $T_f=6.5\text{ns}-106.5\text{ns}$ ), 400 kHz FM	0			$\mu\text{s}$
$t_{BUF}$	Bus free time between START and STOP conditions	1.3			$\mu\text{s}$
$t_{LOW}$	Low period of the I2C clock	1.3			$\mu\text{s}$
$t_{HIGH}$	High period of the I2C clock	0.6			$\mu\text{s}$
$t_F$	Fall time of both SDA and SCL signals			300	ns
$t_R$	Rise time of both SDA and SCL signals			300	ns



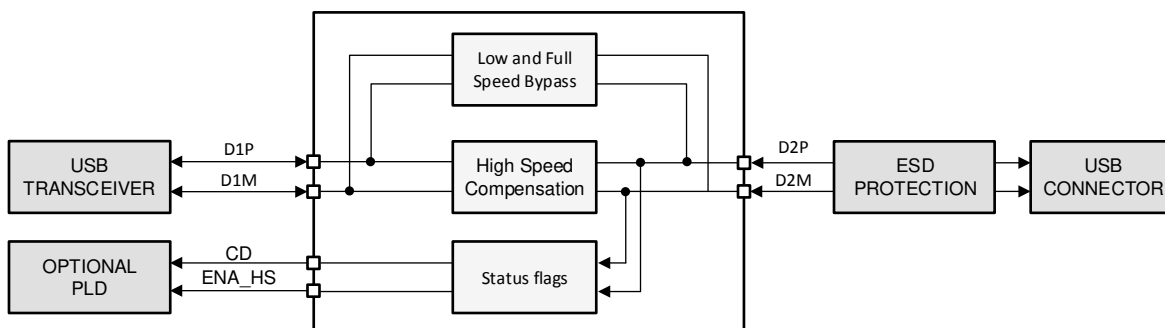
## 7 Detailed Description

### 7.1 Overview

The TUSB2161 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB2161 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB2161 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 High-Speed Boost

The high-speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set through the I2C register according to 节 7.4.6. Internal circuitry of the signal conditioner reduces possible overshoot.

#### 7.3.2 RX Sensitivity

The RX\_SEN pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

### 7.4 Device Functional Modes

#### 7.4.1 Low-Speed (LS) Mode

TUSB2161 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low.

#### 7.4.2 Full-Speed (FS) Mode

TUSB2161 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low

#### 7.4.3 High-Speed (HS) Mode

TUSB2161 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX\_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA\_HS pin are asserted high when high-speed boost is active.

#### 7.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB2161 will detect HS compliance test fixture and enter downstream port high-speed eye diagram test mode. CD pin will be low and ENA\_HS pin is asserted high when TUSB2161 is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB2161 is operating in HS functional mode, TUSB2161 will transition to HS eye compliance test mode and CD asserts low and ENA\_HS remains high. When this occurs signal compensation is enabled.

#### 7.4.5 Shutdown Mode

TUSB2161 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 7-1. CD and ENA\_HS Pins in Different Modes

MODE	CD	ENA_HS
Low-speed	HIGH	LOW
Full-speed	HIGH	LOW
High-speed	HIGH	HIGH
High-speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

#### 7.4.6 I<sup>2</sup>C Mode

TUSB2161 supports 100 and 400 kHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification – STANDARD and FAST MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG\_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high-speed mode.

#### 7.4.7 BC 1.2 Battery Charging Controller

The TUSB2161 main function is a signal conditioner offering the boost and pre-equalization features to the incoming DP/DM signals. For applications in which USB host or hub does not provide USB BC charging controller functionality, the TUSB2161 can perform this task when CDP\_ENZ is low and BC 1.2 CDP Controller is enabled. When battery charging CDP controller feature is enabled (CDP\_ENZ=low) TUSB2161 supports CDP charging downstream port functionality. CDP\_ENZ has an internal pull up when the pin is left unconnected CDP controller will be disabled.

表 7-2. TUSB2161 Battery Charging Controller Modes

Pin 11 (CDP_ENZ)	CDP
High	NO
Low	YES

## 7.5 TUSB216 Registers

表 7-3 lists the memory-mapped registers for the TUSB216 registers. All register offset addresses not listed in 表 7-3 should be considered as reserved locations and the register contents should not be modified.

表 7-3. TUSB216 Registers

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	<a href="#">Go</a>
0x3	CONFIGURATION	This register is selecting device mode.	<a href="#">Go</a>

**表 7-3. TUSB216 Registers (续)**

Offset	Acronym	Register Name	Section
0xE	DC_BOOST	This register is setting DC BOOST level.	<a href="#">Go</a>
0x25	RX_SEN	This register is setting RX Sensitivity level.	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. 表 7-4 shows the codes that are used for access types in this section.

**表 7-4. TUSB216 Access Type Codes**

Access Type	Code	Description
Read Type		
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.5.1 EDGE\_BOOST Register (Offset = 0x1) [reset = X]

EDGE\_BOOST is shown in 图 7-1 and described in 表 7-5.

Return to [Summary Table](#).

This register is setting EDGE BOOST level.

**图 7-1. EDGE\_BOOST Register**

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

**表 7-5. EDGE\_BOOST Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range  0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting)  0x3 = BOOST PIN LEVEL 1  0x6 = BOOST PIN LEVEL 2  0xA = BOOST PIN LEVEL 3  0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

### 7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in 图 7-2 and described in 表 7-6.

Return to [Summary Table](#).

This register is selecting device mode.

图 7-2. CONFIGURATION Register

7	6	5	4	3	2	1	0
RESERVED							CFG_ACTIVE
RH/W-X							RH/W-0x1

表 7-6. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode.  0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

### 7.5.3 DC\_BOOST Register (Offset = 0xE) [reset = X]

DC\_BOOST is shown in 图 7-3 and described in 表 7-7.

Return to [Summary Table](#).

This register is setting DC BOOST level.

图 7-3. DC\_BOOST Register

7	6	5	4	3	2	1	0
RESERVED				DCB_LVL			
RH/W-X				RH/W-X			

表 7-7. DC\_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range  0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting) 0x2 = BOOST PIN LEVEL 1 and 2 0x6 = BOOST PIN LEVEL 3 0xF = (highest dc boost setting)

### 7.5.4 RX\_SEN Register (Offset = 0x25) [reset = X]

RX\_SEN is shown in [图 7-4](#) and described in [表 7-8](#).

Return to [Summary Table](#).

This register is setting RX Sensitivity level.

**图 7-4. RX\_SEN Register**

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

**表 7-8. RX\_SEN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range  0x0 = RX_SEN LEVEL LOW  0x33 = RX_SEN LEVEL MID  0x66 = RX_SEN LEVEL HIGH  0xFF = (highest setting)

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

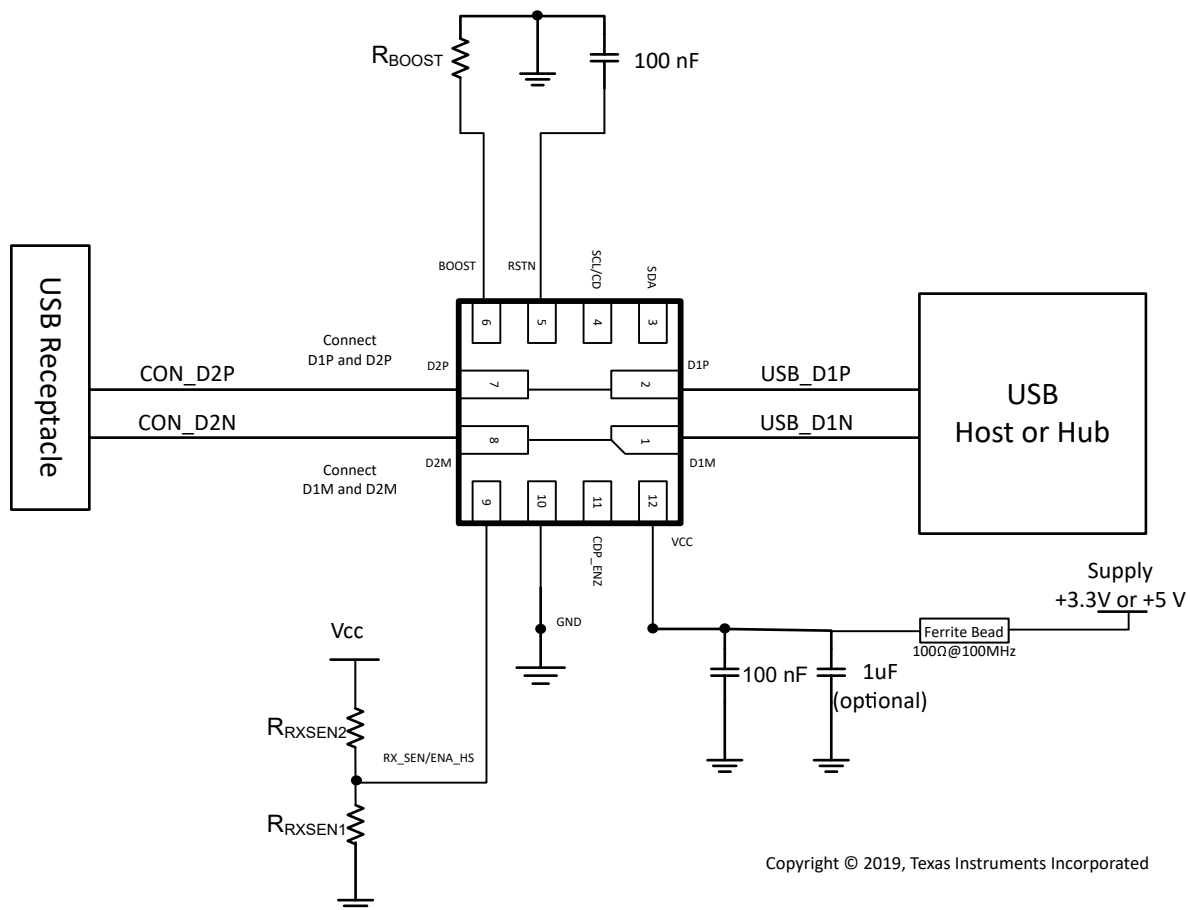
### 8.1 Application Information

The purpose of the TUSB216I is to re-store the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB216I can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB216I to control other blocks on the customer platform, if so desired.

### 8.2 Typical Application

A typical application for TUSB216I is shown in 图 8-1. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



**图 8-1. TUSB216I Reference Schematic (Design Example with CDP disabled), CDP\_ENZ Can Be Left Floating but an Option for a Decoupling Capacitor of 0.1  $\mu$ F is Recommended So the Design is Compatible with Older Devices: TUSB211, TUSB212, TUSB214**

## 8.2.1 Design Requirements

TUSB2161 requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in [表 8-1](#), [表 8-2](#) and [表 8-3](#).

**表 8-1. Design Parameters for 5-V Supply With High Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				5 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>		<b>BOOST Level</b>	Boost Level 1: R <sub>BOOST</sub> = 1.8 kΩ
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
Do Not Install (DNI)		3		
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	High RX Sensitivity Level: R <sub>RXSEN1</sub> = 37.5 kΩ R <sub>RXSEN2</sub> = 12.5 kΩ
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37.5 kΩ <sup>(2)</sup>	12.5 kΩ	High	

- (1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 5 V supply system could be applicable to 3.3 V supply system as well.
- (2) This resistor is needed for a 5 V supply to divide the voltage down so the RX\_SEN pin voltage does not exceed 5.0 V.

**表 8-2. Design Parameters for 3.3-V Supply With Low to Medium Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				3.3 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>		<b>BOOST Level</b>	Boost Level 0: R <sub>BOOST</sub> = 0-Ω
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
Do Not Install (DNI)		3		
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	Medium RX Sensitivity Level: R <sub>RXSEN1</sub> = DNI R <sub>RXSEN2</sub> = DNI
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ - 40 kΩ (27 kΩ typical)	High	

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3 V supply system could be applicable to 5 V supply system as well.

表 8-3. Design Parameters for 2.3-V to 4.3-V VBAT Supply With Low to Medium Loss System

PARAMETER			VALUE <sup>(1)</sup>
V <sub>CC</sub>			2.3 V to 4.3V
I <sup>2</sup> C support required in system (Yes/No)			No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>	<b>BOOST Level</b>	Boost Level 0: R <sub>BOOST</sub> = 0-Ω
	0-Ω	0	
	1.8 kΩ ±1%	1	
	3.6 kΩ ±1%	2	
	Do Not Install (DNI)	3	
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low
	Do Not Install (DNI)	Do Not Install (DNI)	Medium
	37.5 kΩ <sup>(2)</sup>	12.5 kΩ	High
			Medium RX Sensitivity Level: R <sub>RXSEN1</sub> = DNI R <sub>RXSEN2</sub> = DNI

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 2.3 V - 4.3 V supply system could be applicable to 5 V supply system as well.
- (2) This resistor is needed for a VBAT supply (2.3 V - 4.3 V) to divide the voltage down so the RX\_SEN pin voltage does not exceed 5.0 V.

### 8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level Low.

In order for the TUSB216I to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

#### 备注

The TUSB216I compensates for extra attenuation in the signal path according to the configuration of the RX\_SEN pin. This maximum recommended voltage for this pin is 5 V when selecting the highest RX sensitivity level.

Placement of the device is also dependent on the application goal. 表 8-4 summarizes our recommendations.

表 8-4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB216I PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB216Is to improve device enumeration	Midway between each USB interconnect



**表 8-5. Table of Recommended Settings**

BOOST and RX_SEN settings <sup>(1)</sup> for channel loss		
Pre-channel cable length (Between USB PHY and TUSB2161)	BOOST	RX_SEN
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB2161 and inter-connect)	BOOST	RX_SEN
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

### 8.2.2.1 Test Procedure to Construct USB High-speed Eye Diagram

#### 备注

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

#### 8.2.2.1.1 For a Host Side Application

1. Configure the TUSB2161 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB2161
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB2161
4. Enable the host to transmit USB TEST\_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB2161 with a different BOOST setting (must reset to change)

#### 8.2.2.1.2 For a Device Side Application

1. Configure the TUSB2161 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB2161
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB2161. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST\_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB2161 with a different BOOST setting (must reset to change)

### 8.2.3 Application Curves

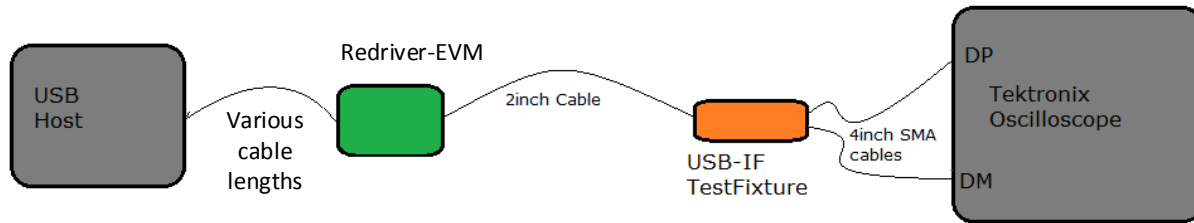


图 8-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

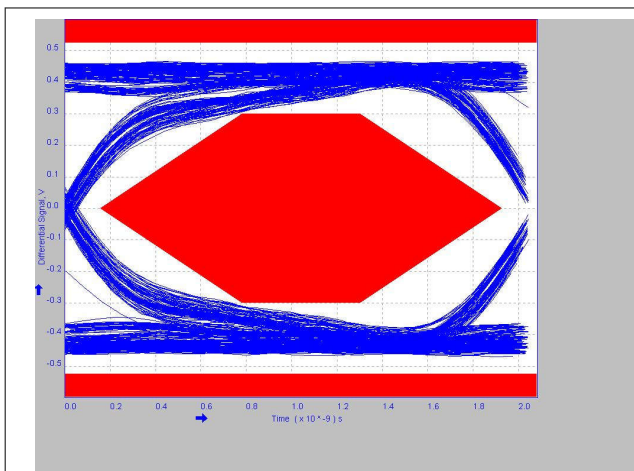


图 8-3. 2 Meter Pre-Channel Without TUSB2161

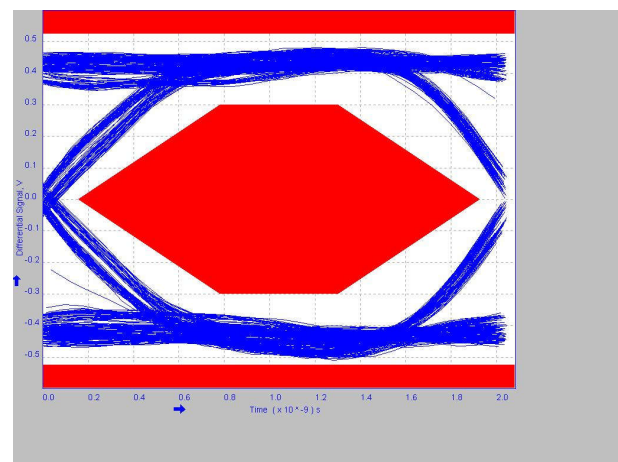


图 8-4. 2 Meter Pre-Channel With TUSB2161 BOOST=1  
RX\_SEN=MED

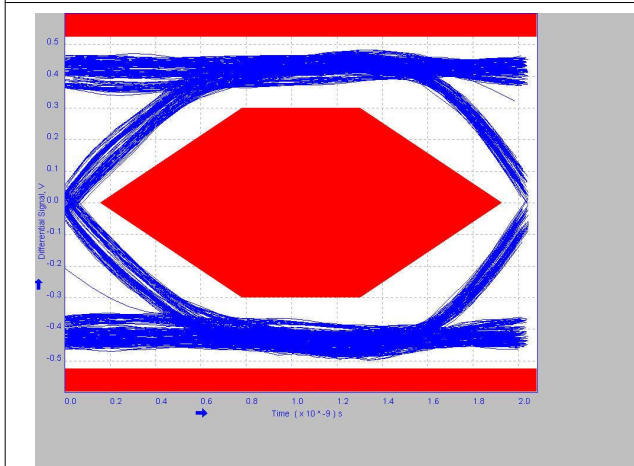


图 8-5. 2 Meter Pre-Channel With TUSB2161 BOOST=0  
RX\_SEN=HIGH

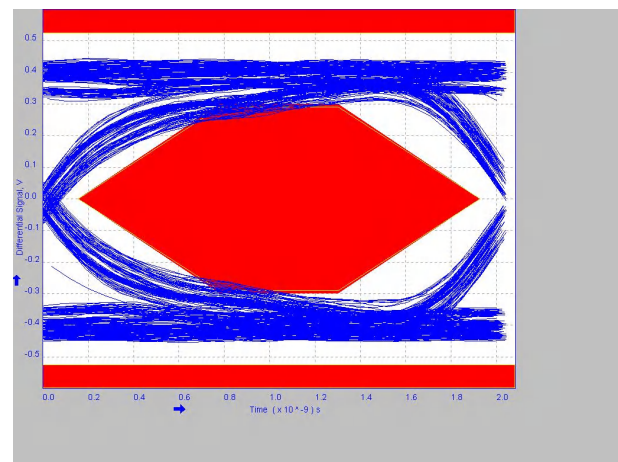


图 8-6. 3 Meter Pre-Channel Without TUSB2161

### 8.2.3 Application Curves (continued)

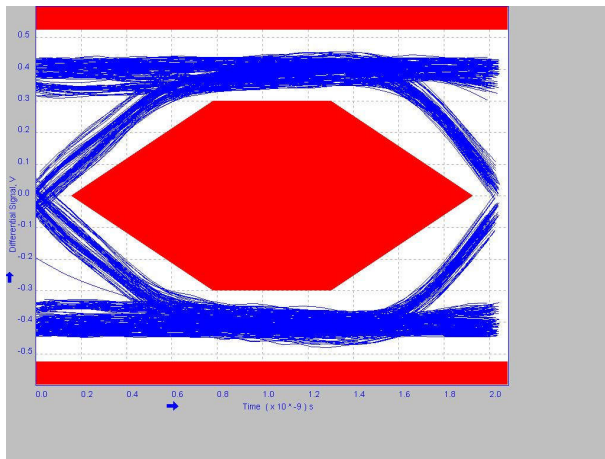


图 8-7. 3 Meter Pre-Channel With TUSB2161 BOOST=0  
RX\_SEN=HIGH

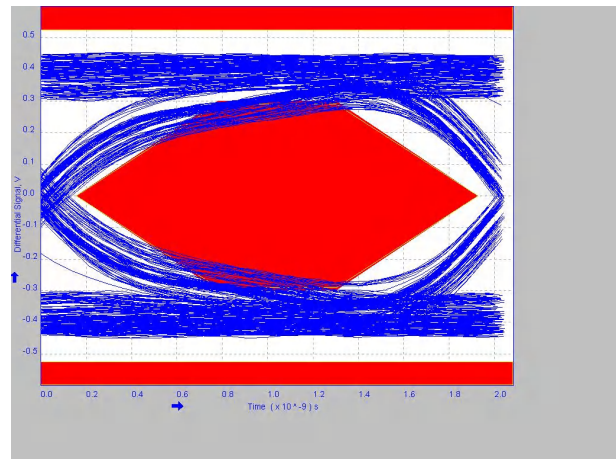


图 8-8. 5 Meter Without TUSB2161

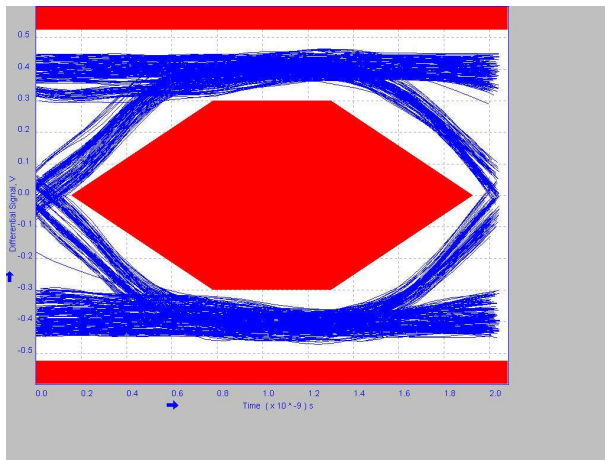


图 8-9. 5 Meter Pre-Channel With TUSB2161 BOOST=1  
RX\_SEN=MED

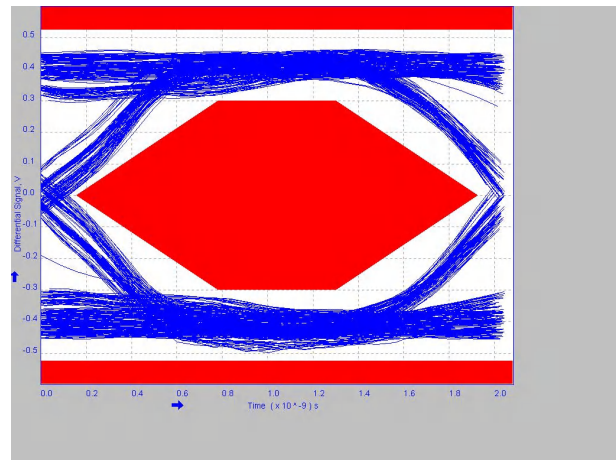


图 8-10. 5 Meter Pre-Channel With TUSB2161 BOOST=2  
RX\_SEN=MED

### 8.2.3 Application Curves

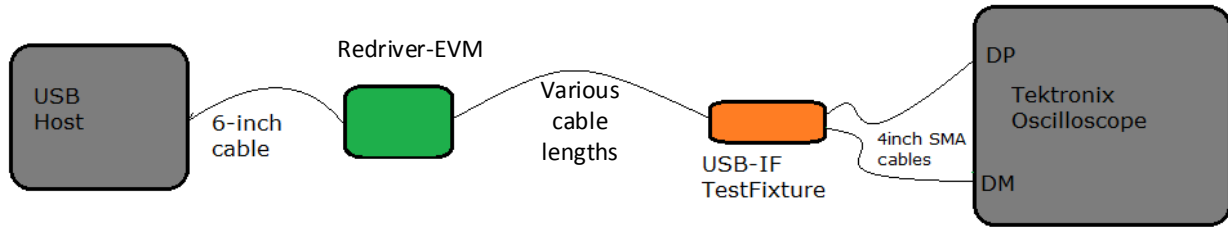


图 8-11. Near End Eye Measurement Set-Up With Post-Channel Cable

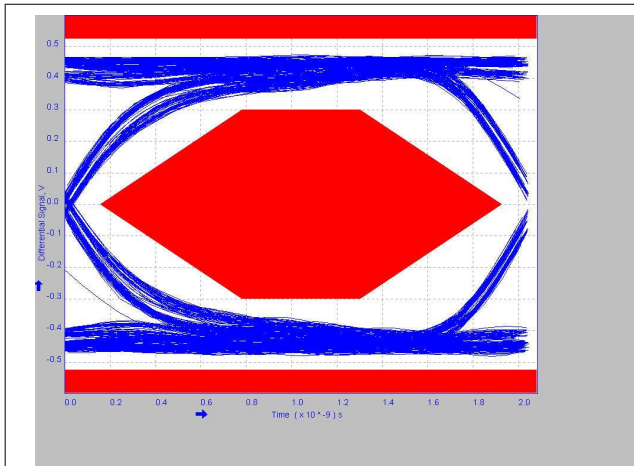


图 8-12. 6 Inches Post Channel Without TUSB2161

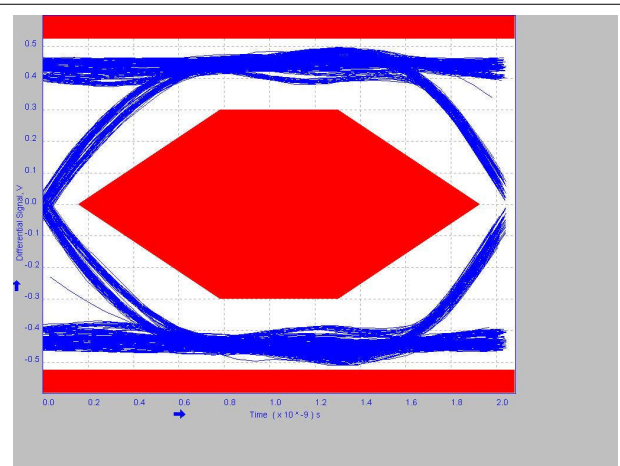


图 8-13. 6 Inches Post-Channel With TUSB2161 BOOST=0  
RX\_SEN=HIGH

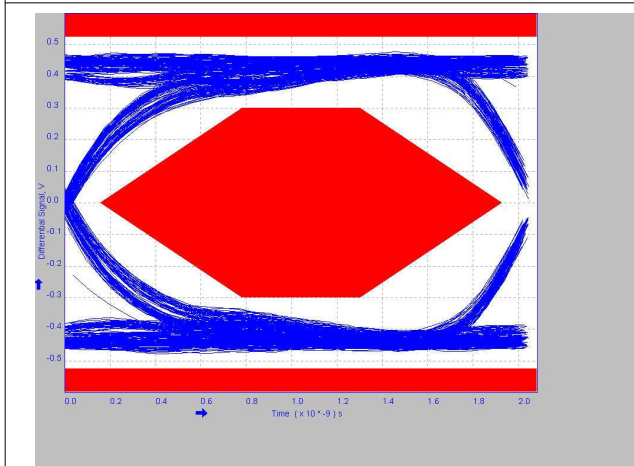


图 8-14. 1 Meter Post-Channel Without TUSB2161

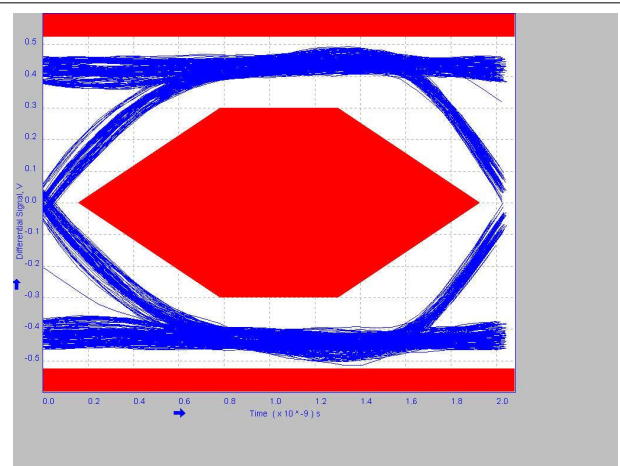


图 8-15. 1 Meter Post-Channel With TUSB2161 BOOST=0  
RX\_SEN=MED

### 8.2.3 Application Curves (continued)

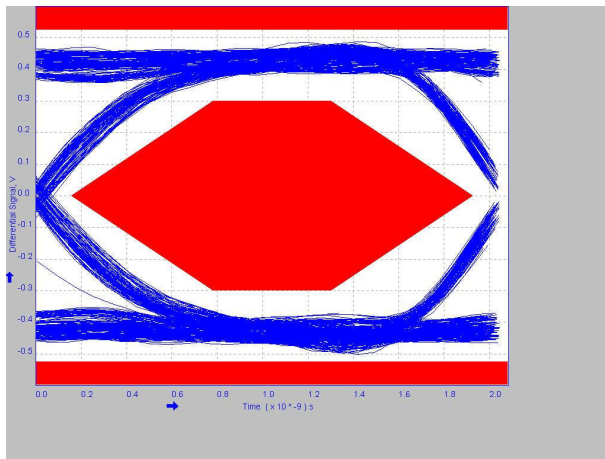


图 8-16. 1 Meter Post-Channel With TUSB2161 BOOST=0 RX\_SEN=HIGH

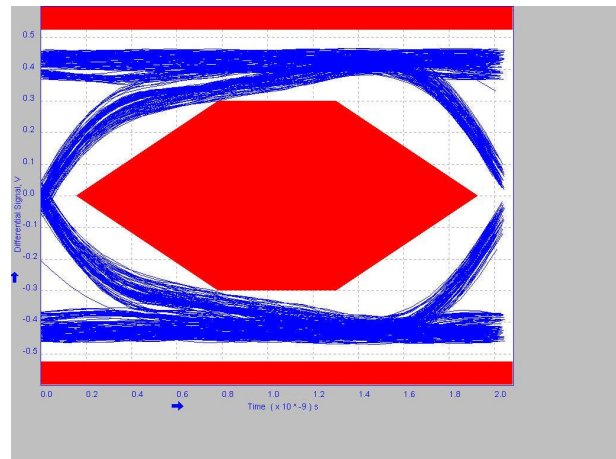


图 8-17. 2 Meter Post-Channel Without TUSB2161

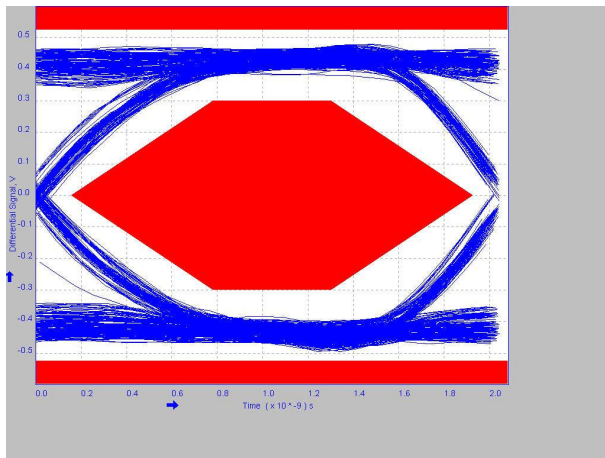


图 8-18. 2 Meter Post-Channel With TUSB2161 BOOST=1 RX\_SEN=MED

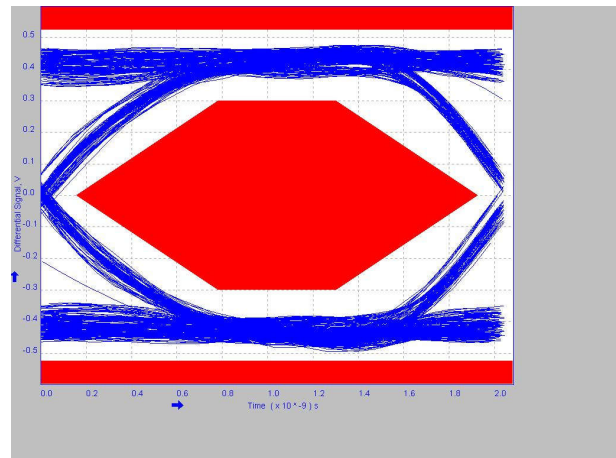


图 8-19. 2 Meter Post-Channel With TUSB2161 BOOST=1 RX\_SEN=HIGH

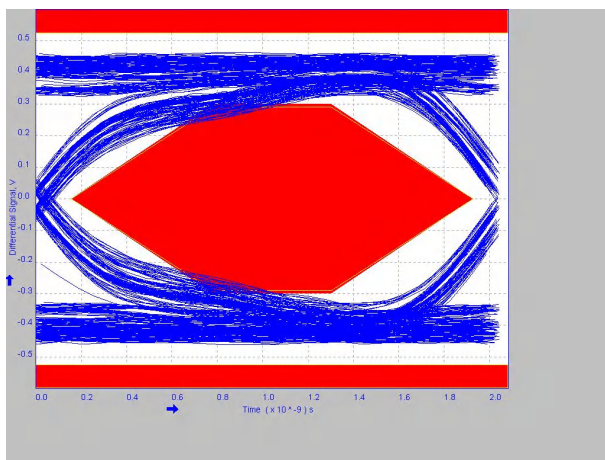


图 8-20. 4 Meter Post-Channel Without TUSB2161

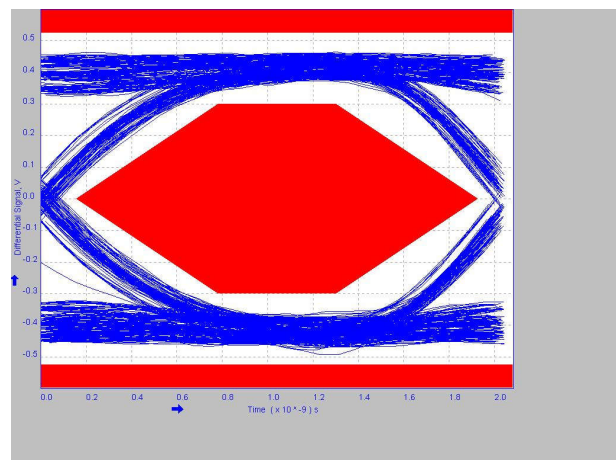


图 8-21. 4 Meter Post-Channel With TUSB2161 BOOST=2 RX\_SEN=MED

### 8.3 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to  $V_{CC}$ ). With a typical internal pullup resistance of 500 k $\Omega$ , the recommended minimum external capacitance is calculated as:

$$[\text{Ramp Time} \times 5] \div [500 \text{ k}\Omega] \quad (1)$$

### 8.4 Layout

#### 8.4.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90  $\Omega$  differential routing underneath the device.

#### 8.4.2 Layout Example

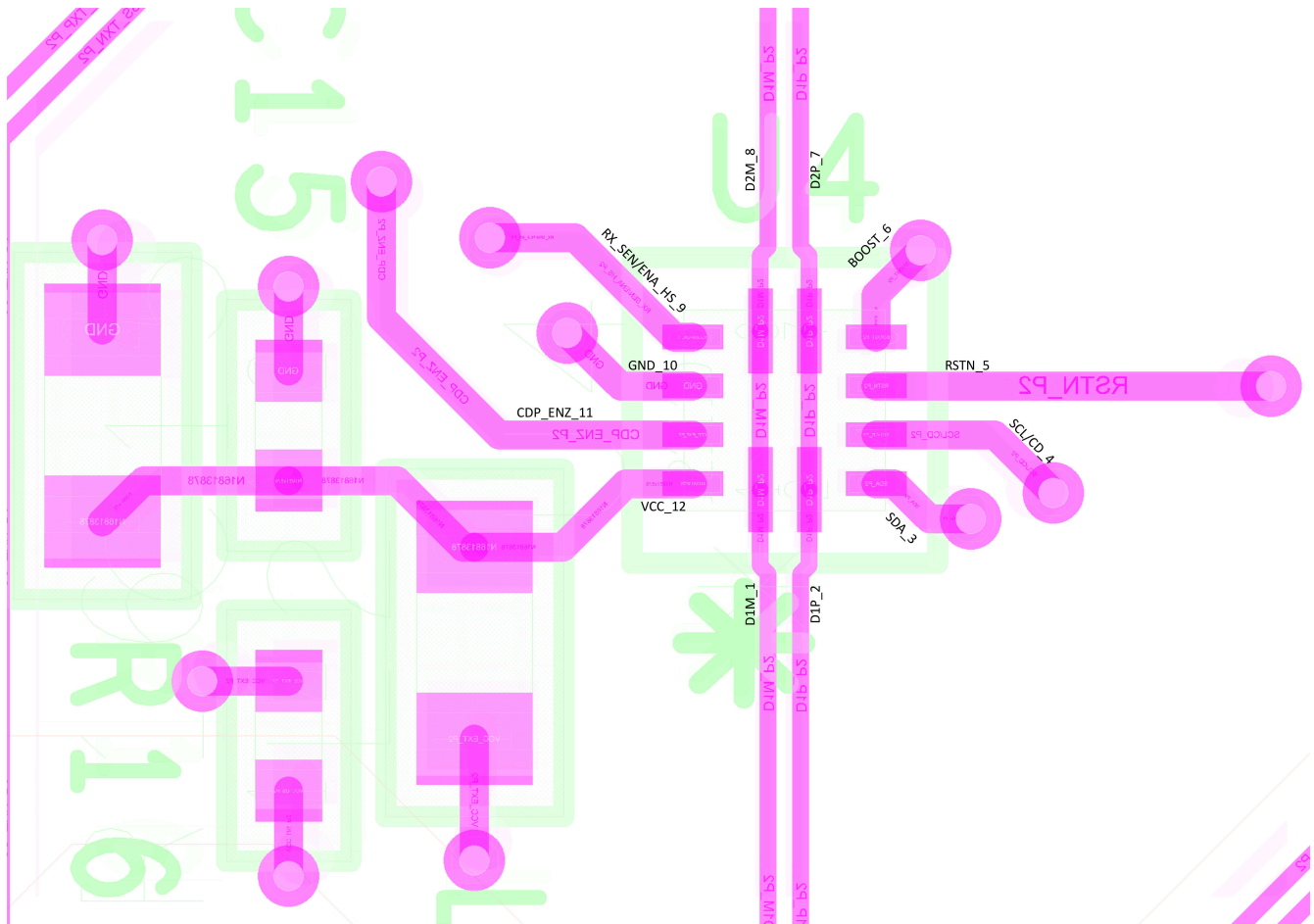


图 8-22. Layout Example

## 9 Device and Documentation Support

### 9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 2021) to Revision A (December 2023)	Page
• Added <i>Device Comparison</i> section.....	2
• Added 400 kHz I2C support.....	6
• Added timing table for 400 kHz I2C Fast Mode.....	8
• Added I2C standard and fast mode support in Detailed Description.....	10

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TUSB216IRWBR</a>	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6l
TUSB216IRWBR.A	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6l
<a href="#">TUSB216IRWBT</a>	Active	Production	X2QFN (RWB)   12	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6l
TUSB216IRWBT.A	Active	Production	X2QFN (RWB)   12	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6l

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

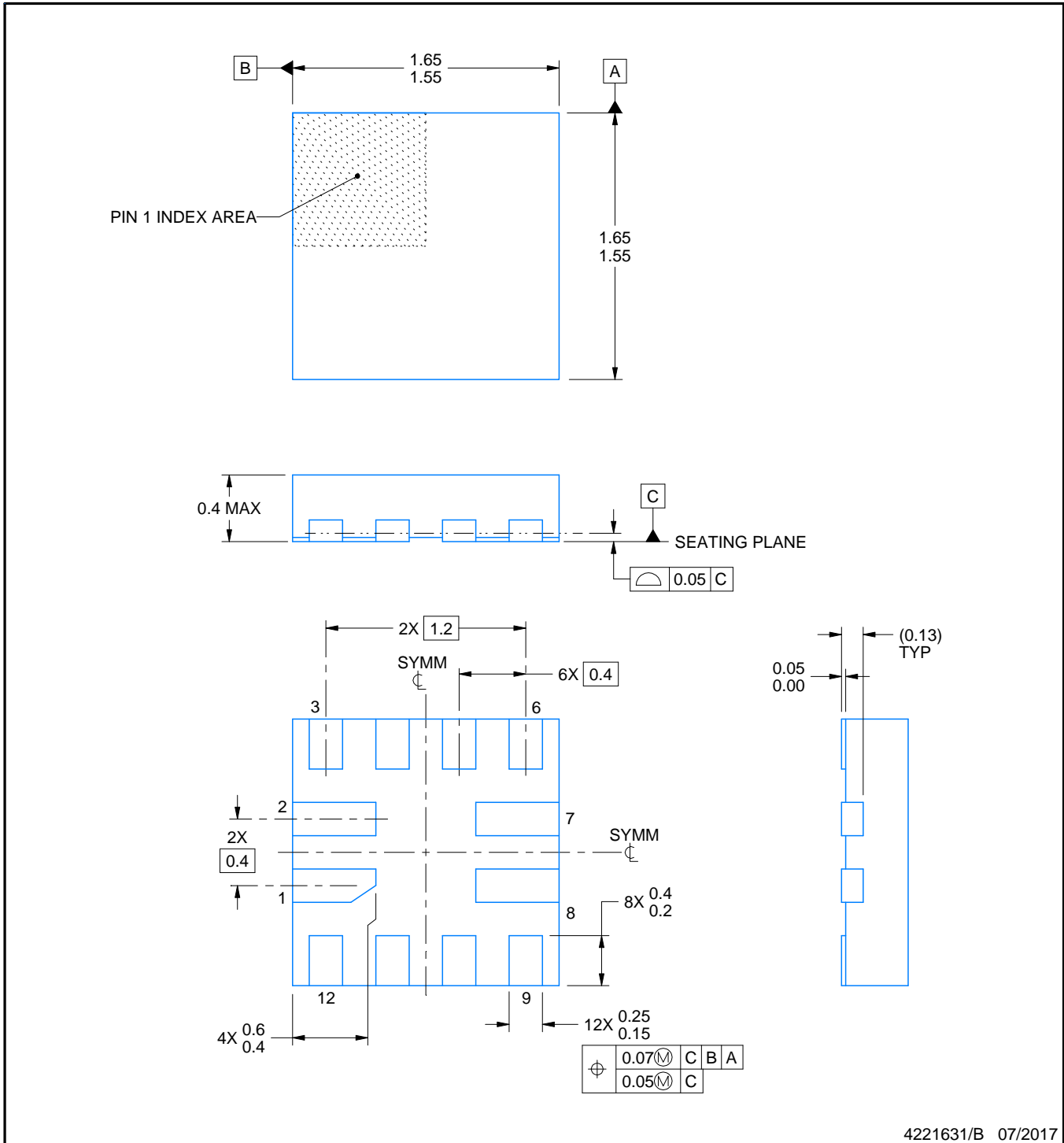

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB216IRWBR	X2QFN	RWB	12	3000	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1
TUSB216IRWBT	X2QFN	RWB	12	250	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q1
TUSB216IRWBT	X2QFN	RWB	12	250	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2161RWBR	X2QFN	RWB	12	3000	189.0	185.0	36.0
TUSB2161RWBT	X2QFN	RWB	12	250	210.0	185.0	35.0
TUSB2161RWBT	X2QFN	RWB	12	250	189.0	185.0	36.0



4221631/B 07/2017

NOTES:

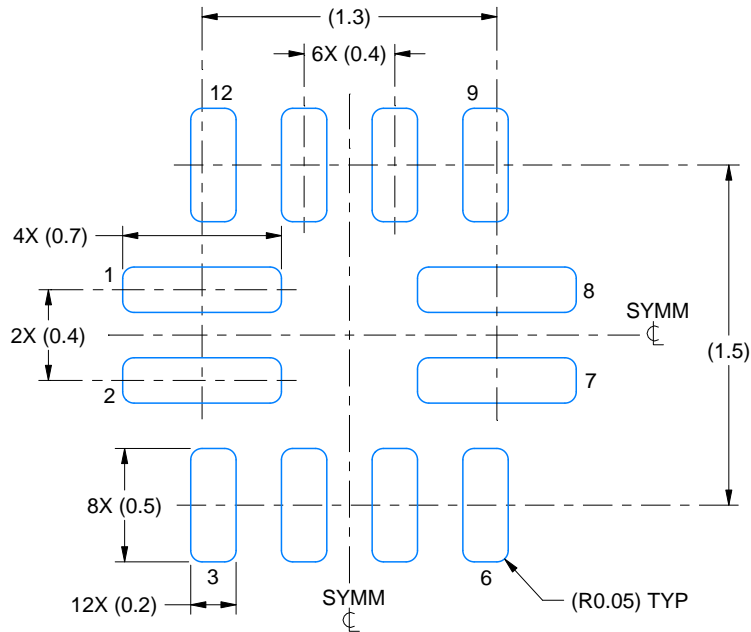
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

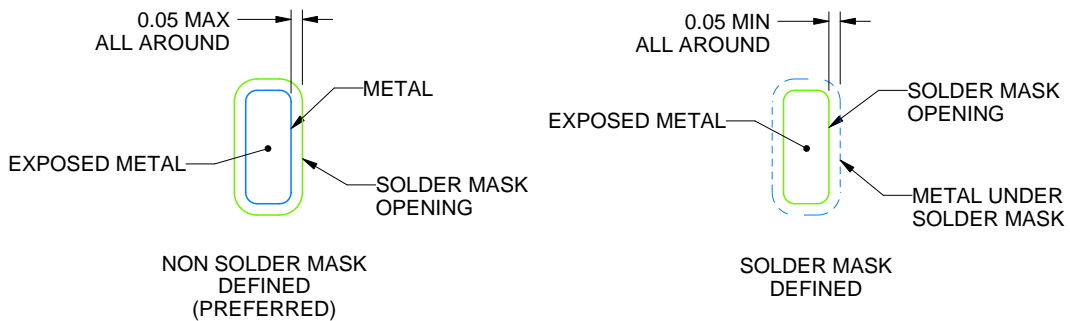
RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

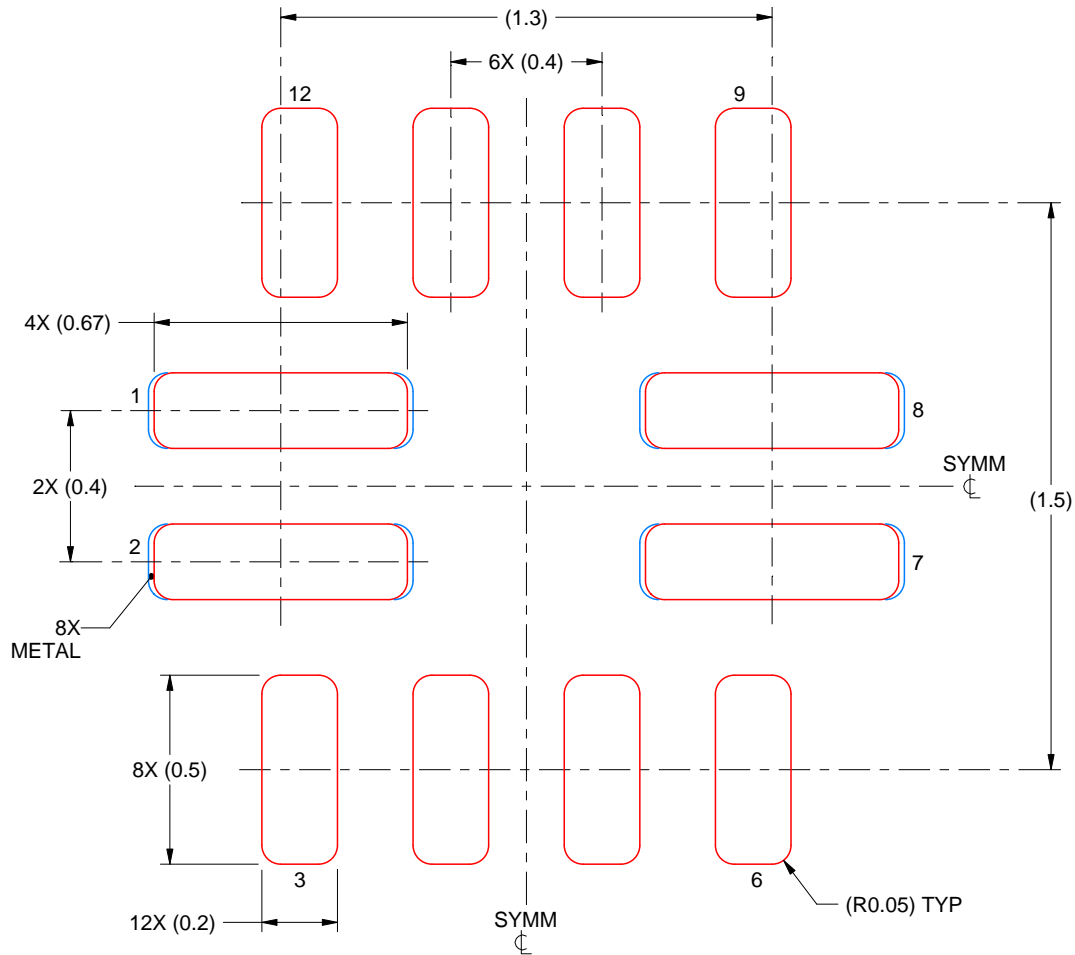
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8  
96% PRINTED SOLDER COVERAGE BY AREA  
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要通知和免责声明

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