TSM36A 采用 SOT-23 封装的浪涌保护器件

1 特性

- 针对工业信号线的 1.7kV 42Ω IEC 61000-4-5 浪涌测试提供单向浪涌保护
- 强大的浪涌保护：
  - IEC61000-4-5 (8/20μs)：41 A
- 对于持续 8/20μs 的 25A 浪涌电流，钳位电压低至 50 V，可保护下游元件
- 工作电压为 36V，用于保护 24V 系统中的信号
- 1μA 低漏电流
- 0.5Ω 低动态电阻
- 集成 4 级 IEC 61000-4-2 ESD 保护
- 30kV ESD 保护 (IEC 61000-4-2)
- SOT-23 (DBZ) 小型、标准、通用封装
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- 工业传感器
- IO link
- PLC I/O 模块
- 24V 电源线或数字输入或输出线
- 4/20mA 环路
- 电器
- 医疗设备
- 电机驱动器

3 说明

TSM36A 是 TI 浪涌保护器件系列的一款产品。TSM36A 可将高达 41A 的 IEC 61000-4-5 故障电流可靠分流，从而保护系统免受高功率瞬态冲击或雷击。该器件为满足常见的工业信号线路 EMC 要求提供了解决方案，可通过 42Ω 电阻进行耦合的方式承受最高 1.7 kV IEC 61000-4-5 开路电压。TSM36A 在浪涌事件期间进行钳制，确保系统在 I_{PP} = 25A 时承受低于 50 V 的电压。

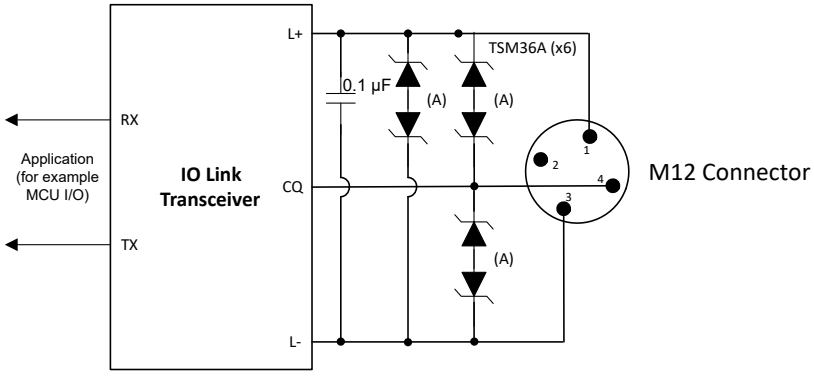
此外，TSM36A 采用小型引线式 SOT-23 (DBZ) 封装，尺寸大概比业界通用 SMA 封装小 50%。器件的漏电流和电容都非常低，可有效减少保护线路所受影响。

更多有关浪涌系列其他器件的信息，请参阅该*链接中的产品*。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TSM36A	DBZ（SOT-23，3）	2.92mm × 1.30mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



A. 该图所示为两个串联堆叠的 TSM36A 单向器件，阳极背靠背连接，从而在各自信号之间实施保护。

工业传感器 IO Link 应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2022) to Revision A (October 2022)	Page
• 将数据表的状态从*预告信息*更改为*量产数据*	1

5 Pin Configuration and Functions

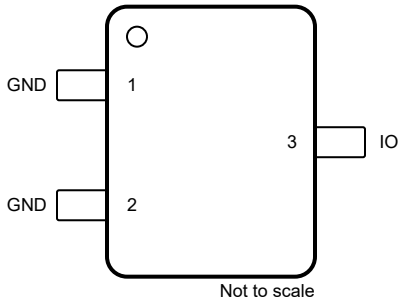


**图 5-1. DBZ Package,
3-Pin SOT-23
(Top View)**

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	3	I/O	Surge and ESD protected IO
GND	1, 2	G	Connect to ground. To achieve the rated performance, it is required to connect pin 1 and 2 together on the PCB as close to the device as possible.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

Parameter		Device	MIN	MAX	UNIT
$P_{pk\_8\_20}$	IEC 61000-4-5 Power (t_p - 8/20 µs)	TSM36A		2000	W
$I_{pp\_8\_20}$	IEC 61000-4-5 Current (t_p - 8/20 µs)	TSM36A		41	A
T_A	Operating free-air temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

6.3 ESD Ratings—IEC Specification

T_A = 25°C (unless otherwise noted)

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		36	V
T_A	Operating free-air temperature	–55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		TSM36A DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Device	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		TSM36A	0		36	V
V_{BRF}	Forward breakdown voltage(1)	I_{IO} = – 10 mA	TSM36A		0.8		V
V_{BRR}	Reverse breakdown voltage(1)	I_{IO} = 10 mA	TSM36A	37.8		44.2	V
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 25A, t_p = 8/20 µs, from IO to GND	TSM36A		50		V
		I_{PP} = 40 A, t_p = 8/20 µs, from IO to GND	TSM36A		57		
I_{LEAK}	Leakage current	V_{IO} = +36 V	TSM36A			1	µA
R_{DYN}	Dynamic resistance	t_p = 8/20 µs, from IO to GND	TSM36A		0.5		Ω
C_{IO-GND}	Line capacitance	V_{IO} = 0 V, f = 1 MHz, V_{p-p} = 30 mV	TSM36A		50	80	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.

6.7 Typical Characteristics

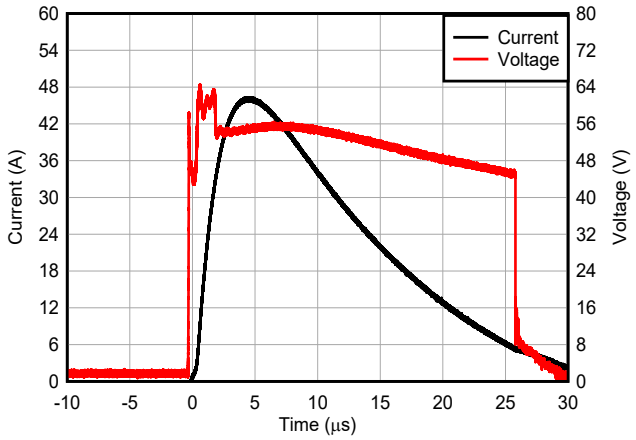


图 6-1. 8/20 µs Surge Response

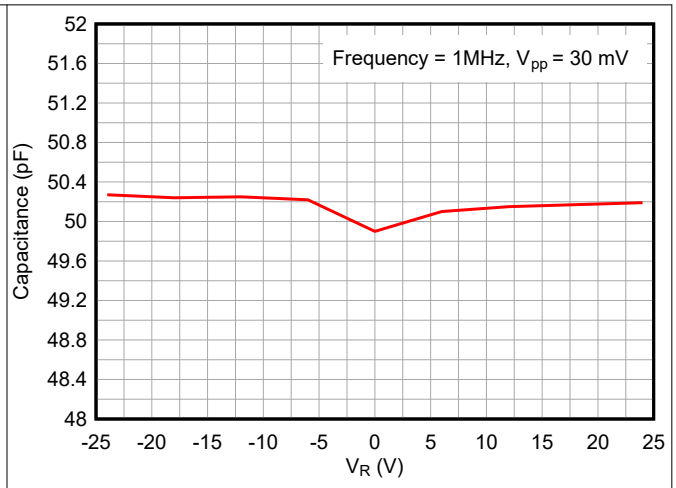


图 6-2. Capacitance vs Bias Voltage

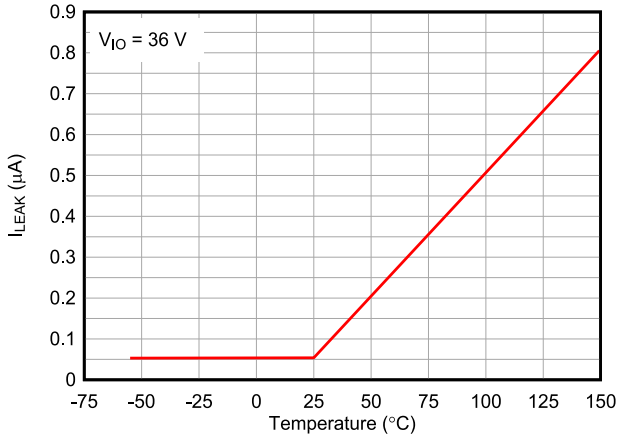


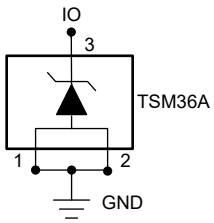
图 6-3. Leakage vs Temperature

7 Detailed Description

7.1 Overview

The TSM36A is a surge protection diode that clamps the voltage during a fault and protects downstream components from overvoltage events.

7.2 Functional Block Diagram



7.3 Feature Description

The TSM36A is a surge protection diode that handles 41 A of IEC 61000-4-5 8/20 µs surge current. The low clamping voltage protects downstream circuits from being stressed during a surge event. The TSM36A has minimal leakage current at the standoff voltage of 36 V, making it a good candidate for applications where low leakage is needed to reduce power dissipation. A 30-kV IEC 61000-4-2 rating makes it a robust protection solution for ESD events as well. The TSM36A has a wide ambient temperature range of –55°C to +150°C which enables it to work in applications requiring an extended temperature range. The small SOT-23 (DBZ) package enables it to save board area compared to other surge protection devices in a traditional SMA package. The leaded SOT-23 (DBZ) package enables automatic optical inspection during the assembly process.

7.4 Device Functional Modes

7.4.1 Protection Specifications

The TSM36A is specified according to both the IEC 61000-4-5 standard. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs.

Additionally, the TSM36A is tested according to IEC 61000-4-5 to pass a ±1.7 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, which is a common test requirement for industrial signal I/O lines. The TSM36A will serve as a protection solution for applications with that requirement.

The TSM36A integrates 30-kV IEC 61000-4-2 rated ESD protection, which ensures that the device can protect against both surge and ESD transient events.

For more information on TI's test method for surge and ESD testing, reference *TI's IEC 61000-4-x Testing* application note.

8 Application and Implementation

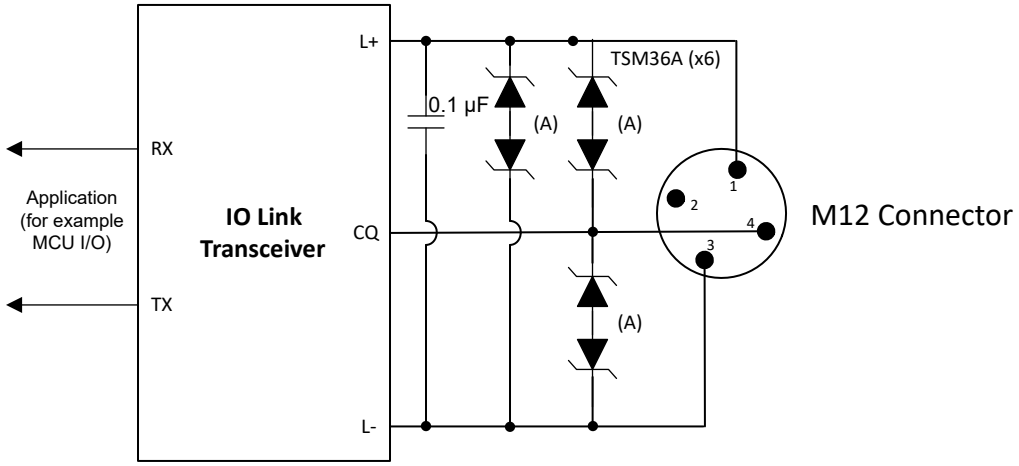
备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TSM36A can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

8.2 Typical Application



A. Diagram shows two TSM36A unidirectional devices stacked in series with the anodes tied back-to-back to protect between the respective signals.

图 8-1. TSM36A Application Schematic

8.2.1 Design Requirements

In the previous example, the TSM36A is protecting an IO Link tranceiver that has a nominal voltage of 24 V and a maximum input voltage of 30 V. Most industrial interfaces such as this require protection against ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, equaling approximately 24 A of surge current. If a surge event caused by lightning, coupling, ringing, or any other fault condition occurs without any input protection, then this input voltage will rise to hundreds of volts in microseconds, which violates the absolute maximum input voltage and will harm the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system.

8.2.2 Detailed Design Procedure

If the TSM36A is protecting the device, then during a surge event the voltage will rise to the breakdown of the diode at 37.8 V (minimum), the TSM36A will turn on and shunt the surge current to ground. With the low dynamic resistance of the TSM36A, large amounts of surge current will have some impact on the clamping voltage. The dynamic resistance of the TSM36A is around 0.5 Ω, which means 24 A of surge current will cause a voltage rise of 24 A × 0.5 Ω = 12 V. Because the device turns on at 37.8 V (minimum), the IO Link transceiver input will be exposed to 37.8 V + 12 V = 49.8 V during surge pulses, which is well within the absolute maximum voltage of the IO Link transceiver input pins (L+, L-, and CQ) and will protect the circuit. The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the SOT-23 package allows the device to be placed extremely close to the input connector, lowering the length of the fault current path through the system compared to larger protection solutions. Finally, the low leakage of the TSM36A will have low input power losses. The device will receive a maximum of 1 µA leakage at 36 V for a constant power dissipation of 36 µW; a small quantity that will minimally effect overall efficiency metrics and heating concerns.

8.2.3 Configuration Options

The TSM36A can either be used in an unidirectional or bidirectional configuration. For bidirectional operation, place two TSM36A devices in series with reverse orientation, which allows a working voltage of ±36 V. TSM36A bidirectional operation is similar to its unidirectional operation, but with a minor increase in breakdown voltage and clamping voltage.

9 Power Supply Recommendations

This is a passive TVS diode-based surge protection device; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- For optimal performance, place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Pin 1 and 2 are not internally connected. To achieve the rated performance, it is required to connect Pin 1 and 2 together on the PCB as close to the device as possible and route the signal to ground. Also use a thick and short trace for this return path.

10.2 Layout Example

The following is a typical example of the layout routing for the TSM36A undirectional device.

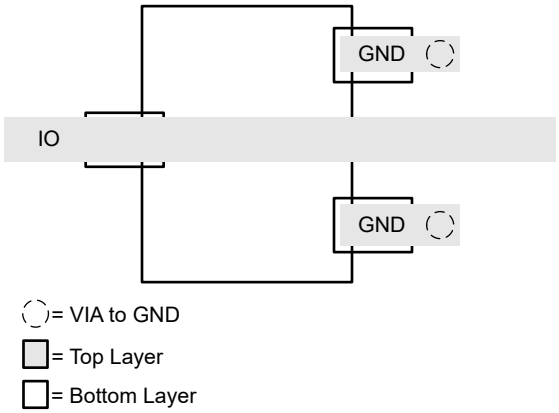


图 10-1. Routing with DBZ Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TI's IEC 61000-4-x Testing* application note
- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSM36ADBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2O98	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

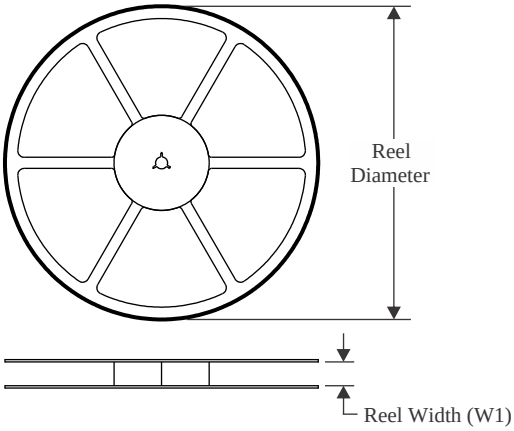
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

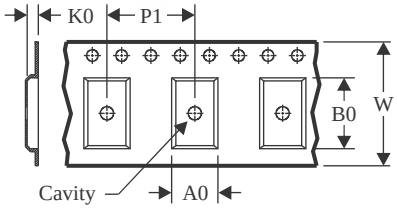
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

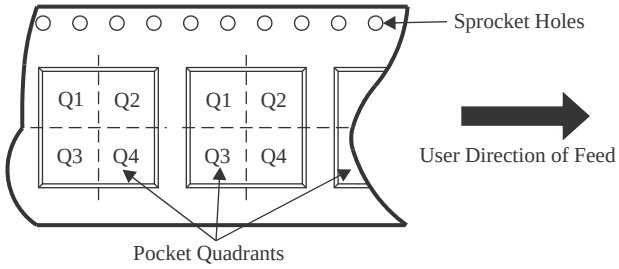


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

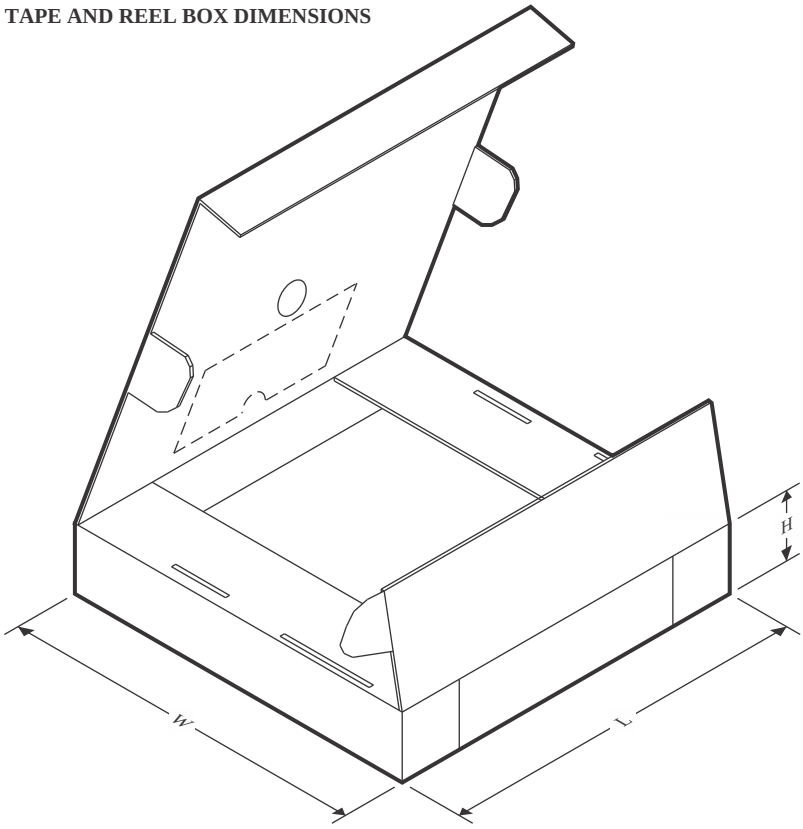
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM36ADBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

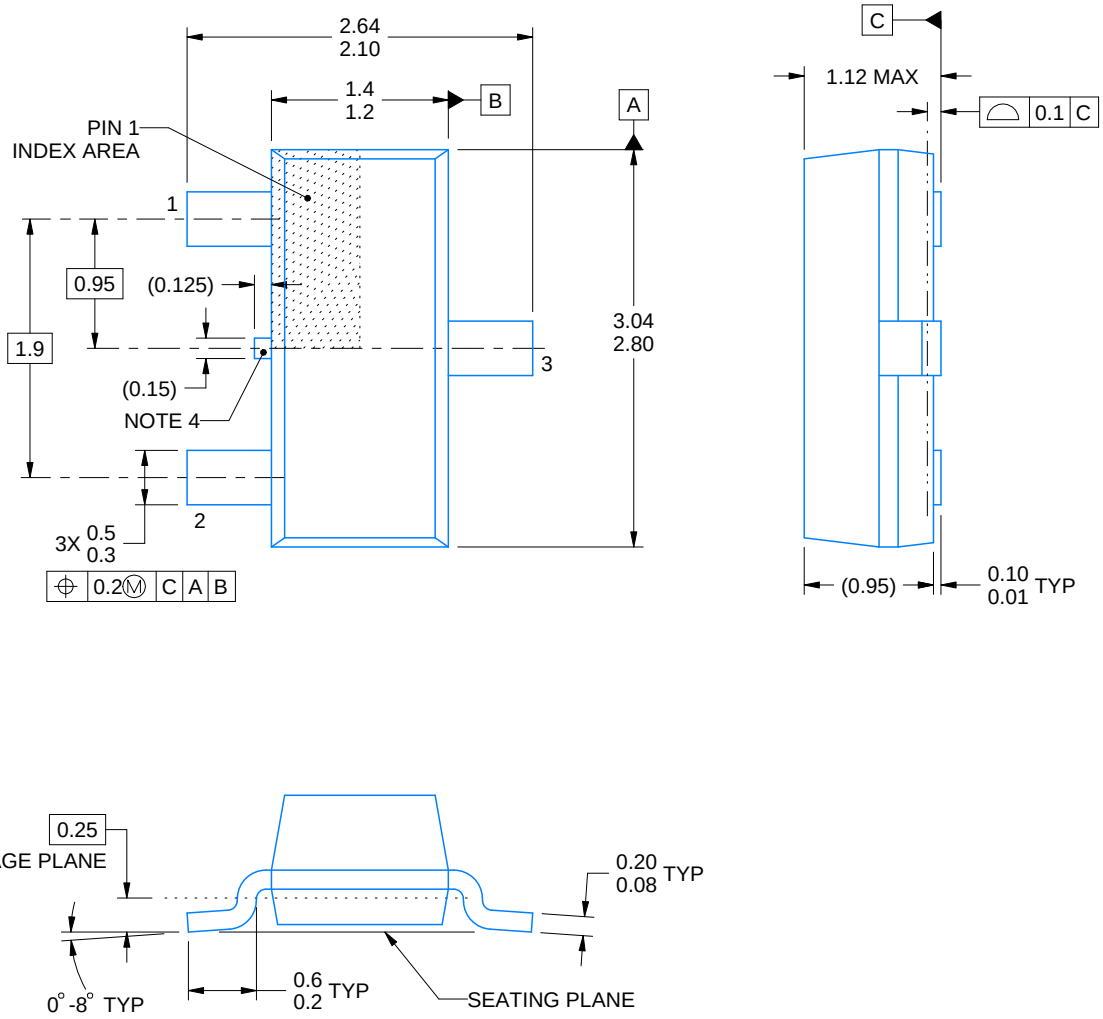
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM36ADBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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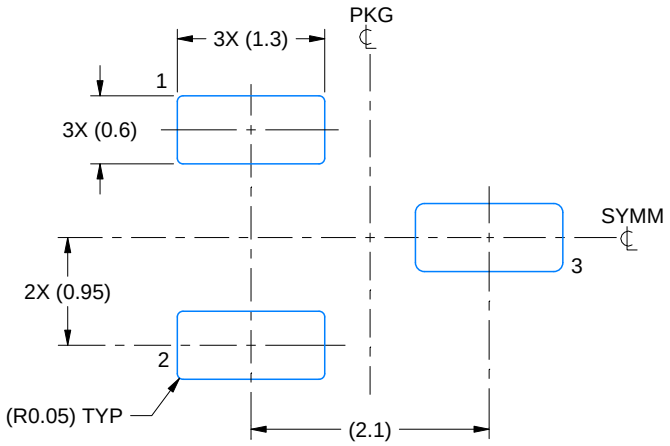
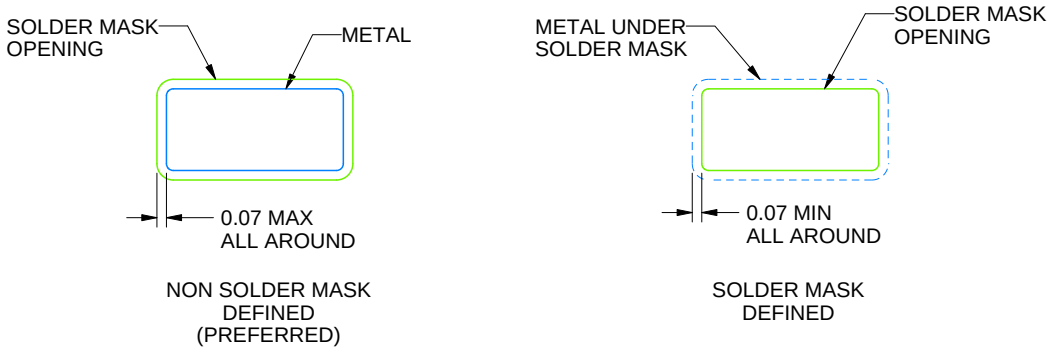
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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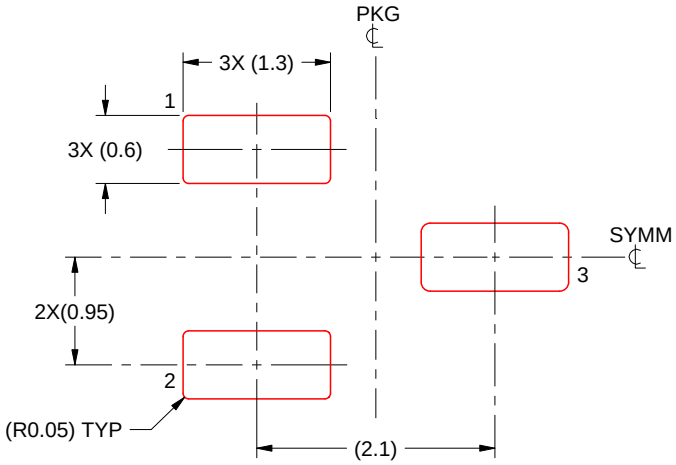
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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