TS5A3160 1-Ω SPDT Analog Switch

1 Features

- Low ON-State Resistance (1 Ω)
- Isolation in the Powered-Off Mode, $V_+ = 0$
- Specified Make-Before-Break Switching
- Control Inputs are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Mobile Phones
- Consumer and Computing
- Portable Instrumentation

3 Description

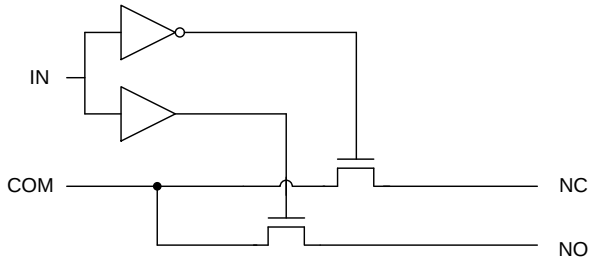
The TS5A3160 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3160DBV	SOT-23 (6)	2.90 mm × 1.60 mm
TS5A3160DCK	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

Changes from Revision D (June 2015) to Revision E **Page**

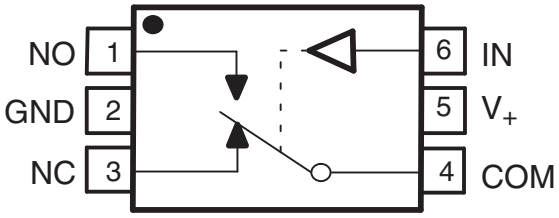
- Changed Input leakage current UNIT value From: μA To: nA in the *Electrical Characteristics for 5-V Supply* table ... 5

Changes from Revision C (March 2012) to Revision D **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

DBV or DCK Packages
6-Pin SOT-23 or SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally open switch port
2	GND	—	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	—	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage(3) (4) (5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–200	200	mA
	On-state peak switch current(6)		–400	400	
V_I	Digital input voltage(3) (4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5A3160		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	4.5 V		0.05	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	4.5 V		0.15		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C			0.1	0.25	
				Full				0.25	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see Figure 14	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{COM} = 0 to 5.5 V, V_{NC} or V_{NO} = 5.5 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.1	1	µA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NC} or V_{NO} = Open, or V_{COM} = 4.5 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
DIGITAL CONTROL INPUT (IN)(2)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2		0.2	nA
				Full		100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	5 V	2	3.5	6	ns
				Full	4.5 V to 5.5 V	1		8	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	5 V	3	8.5	13	ns
				Full	4.5 V to 5.5 V	2		15	
t_{MBB}	Make-before-break time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	5 V	2	7	12	ns
				Full	5 V to 5.5 V	2		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 22	25°C	5 V		36.5		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See Figure 20	25°C	5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 23	25°C	5 V		0.004%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND		25°C	5.5 V		10	50	nA
				Full				500	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	3 V		1.3	1.6	Ω
				Full				2	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	3 V		1.2	1.5	Ω
				Full				1.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C	3 V		0.2		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, see Figure 13	25°C			0.15	0.3	
				Full				0.3	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see Figure 14	25°C	3.6 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see Figure 15	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NC} or V_{NO} = Open, or V_{COM} = 3 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 15	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUT (IN)(2)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	3.3 V	2	4.5	13	ns
				Full	3 V to 3.6 V	1		15	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	3.3 V	3	9	15	ns
				Full	3 V to 3.6 V	2		20	
t_{MBB}	Make-before-break time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	3.3 V	1	7	12	ns
				Full	3 V to 3.6 V	1		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 22	25°C	3.3 V		20		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	3.3 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See Figure 20	25°C	3.3 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 23	25°C	3.3 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND		25°C	3.6 V		10	30	nA
				Full				100	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 13	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 13	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 13	25°C	2.3 V		0.15	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 13	25°C	2.3 V		2.6		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 13	25°C			0.6	1	
				Full				1	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, see Figure 14	25°C	2.3 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, see Figure 15	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{COM} = 0 to 2.7 V, V_{NC} or V_{NO} = 2.7 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NC} or V_{NO} = Open, or V_{COM} = 2.2 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 15	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
DIGITAL CONTROL INPUT (IN)(2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2		2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	2.5 V	2	6.5	15	ns
				Full	2.3 V to 2.7 V	1		17	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	2.5 V	3	11	18	ns
				Full	2.3 V to 2.7 V	2		20	
t_{MBB}	Make-before-break time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	2.5 V	1	8	12	ns
				Full	2.3 V to 2.7 V	1		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 22	25°C	2.5 V		12		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	2.5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See Figure 20	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 23	25°C	2.5 V		0.02%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND		25°C	2.7 V		10	30	nA
				Full				50	

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 13	25°C	1.65 V		5		Ω
				Full				15	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 13	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 13	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 13	25°C	1.65 V		5		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 13	25°C			4.5		
				Full					
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, see Figure 14	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 15	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{COM} = 0 to 1.95 V, V_{NC} or V_{NO} =1.95 V to 0,	Switch OFF, see Figure 14	25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.3 V, V_{NC} or V_{NO} = Open, or V_{COM} = 1.65 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 15	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
DIGITAL CONTROL INPUT (IN)(2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	1.8 V	6	13	24	ns
				Full	2.3 V to 2.7 V	5		27	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	1.8 V	6	15	27	ns
				Full	2.3 V to 2.7 V	5		30	
t_{MBB}	Make-before-break time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	1.8 V	2	7	12	ns
				Full	2.3 V to 2.7 V	2		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 22	25°C	1.8 V		5.5		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	1.8 V		105		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See Figure 20	25°C	1.8 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	1.8 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 23	25°C	1.8 V		0.06%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND		25°C	1.95 V		5	15	nA
				Full				50	

6.9 Typical Characteristics

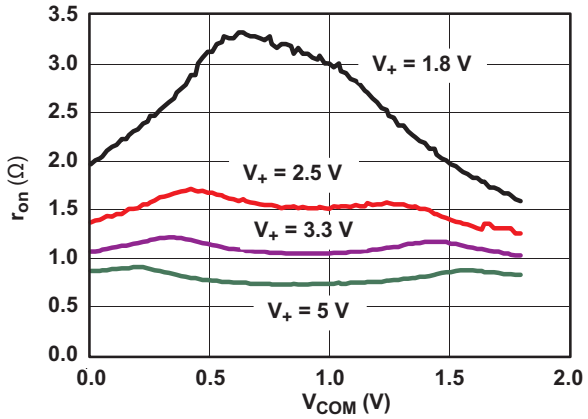


Figure 1. r_{on} vs V_{COM}

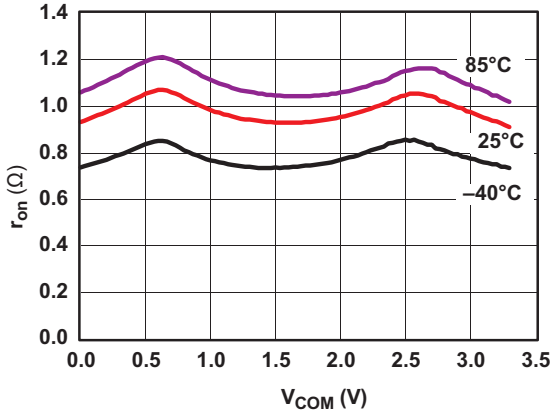


Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

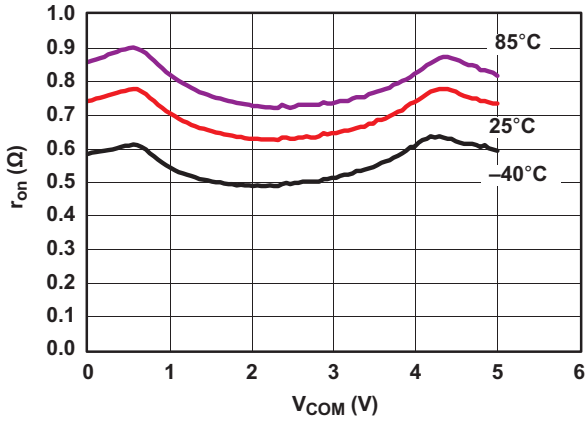


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

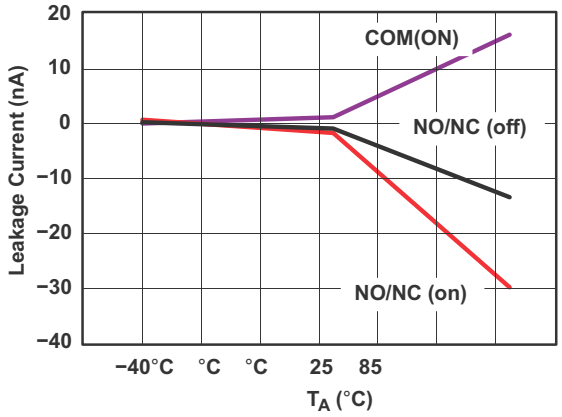


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

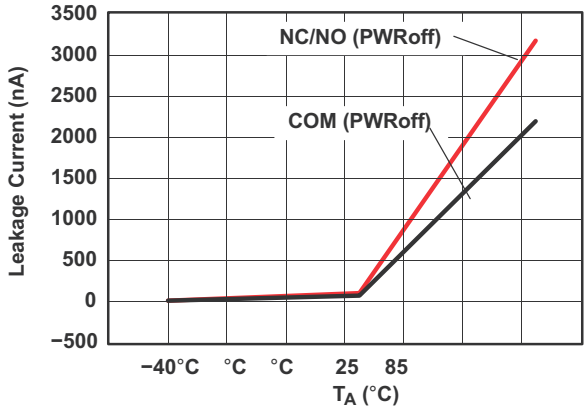


Figure 5. Leakage Current vs Temperature (V_+ = 5 V)

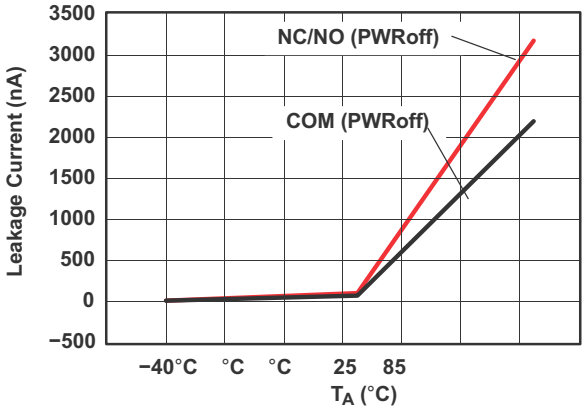


Figure 6. Charge Injection (Q_C) vs V_{COM}

Typical Characteristics (continued)

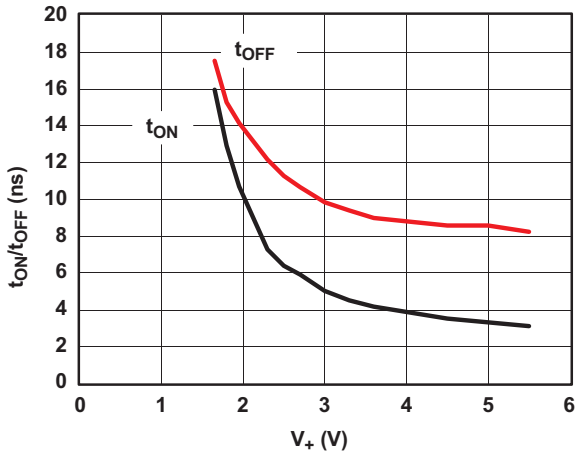


Figure 7. t_{ON} and t_{OFF} vs Supply Voltage

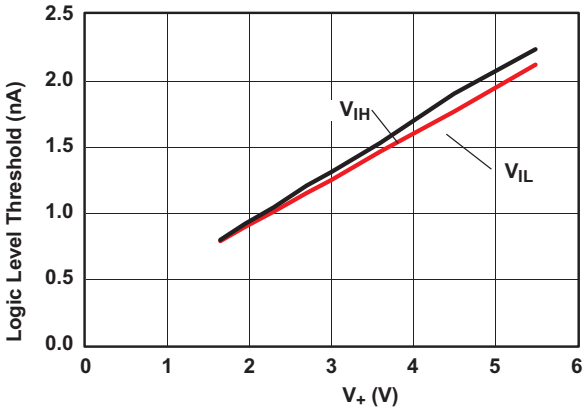


Figure 8. Logic-Level Threshold vs V_+

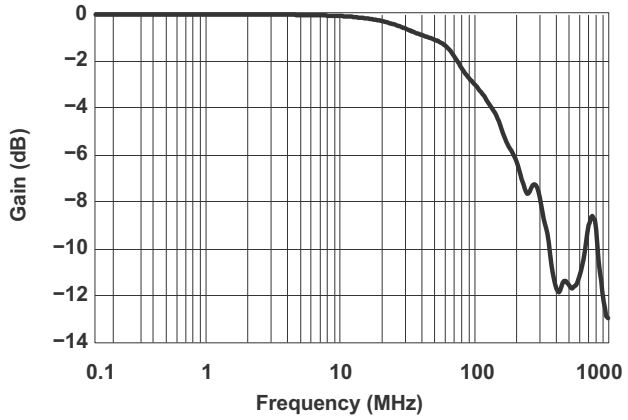


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

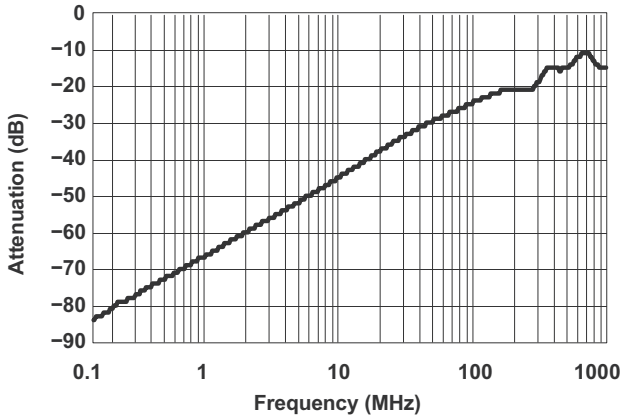


Figure 10. OFF Isolation vs Crosstalk (V_+ = 5 V)

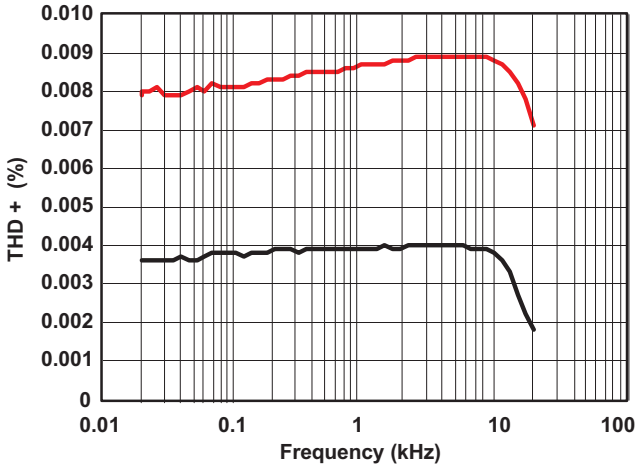


Figure 11. Total Harmonic Distortion vs Frequency

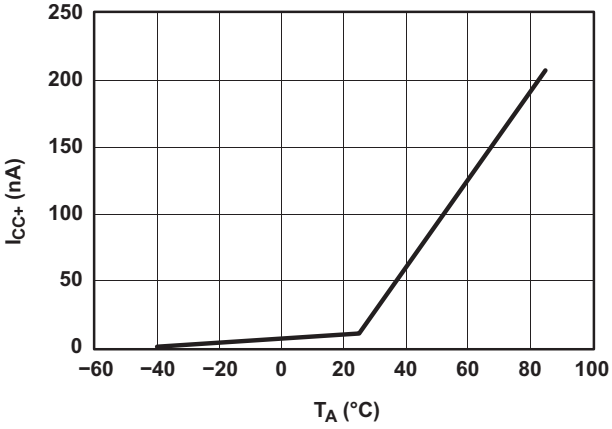


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

7 Parameter Measurement Information

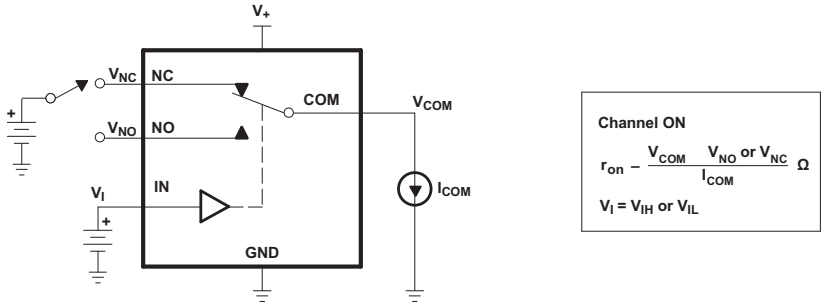


Figure 13. ON-State Resistance (r_{on})

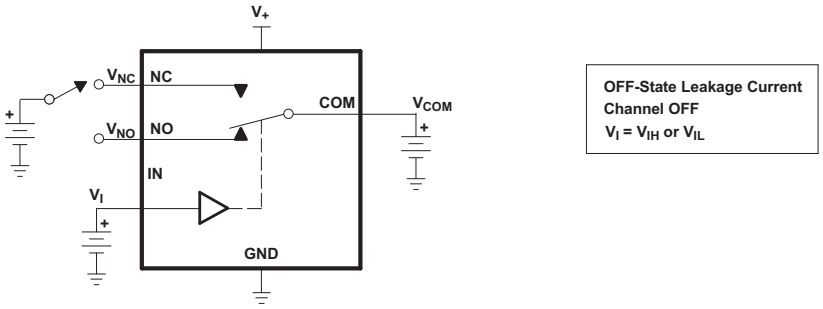


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{COM(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$, $I_{COM(PWROFF)}$)

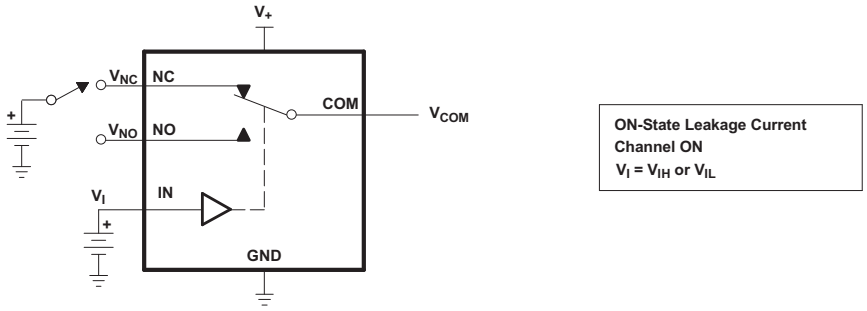


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

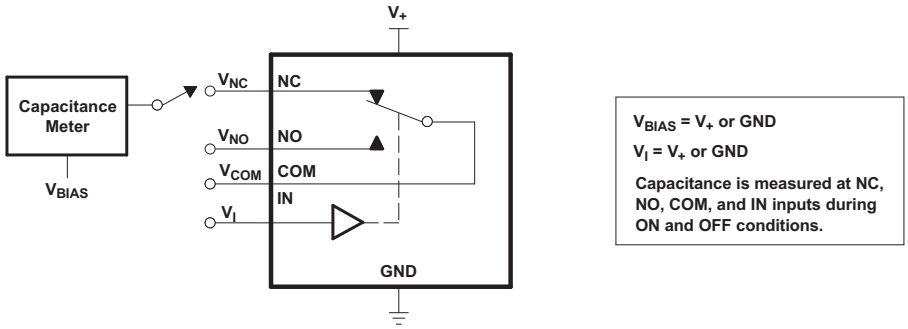
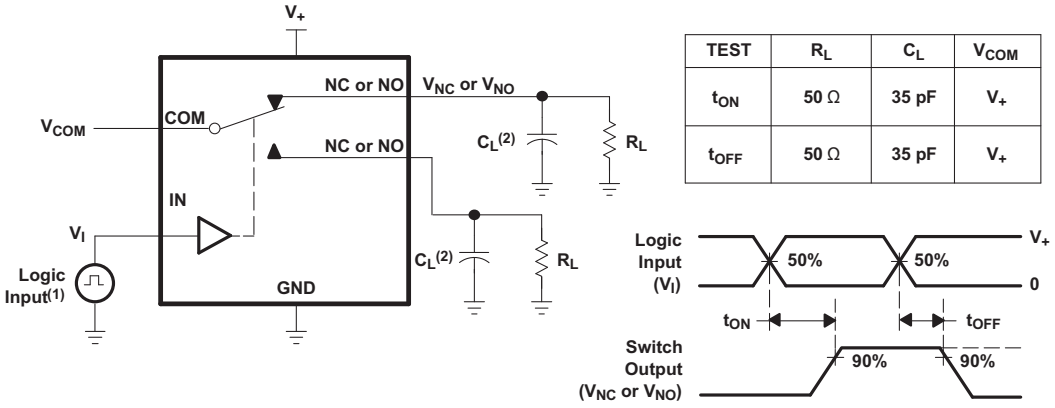


Figure 16. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)

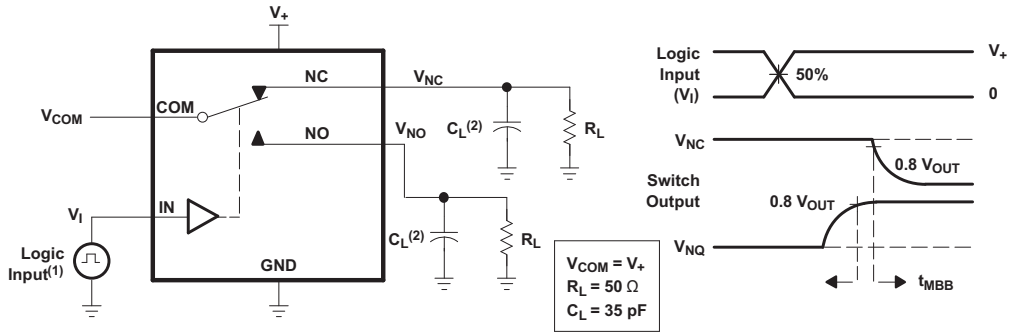


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 17. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 18. Make-Before-Break Time (t_{MBB})

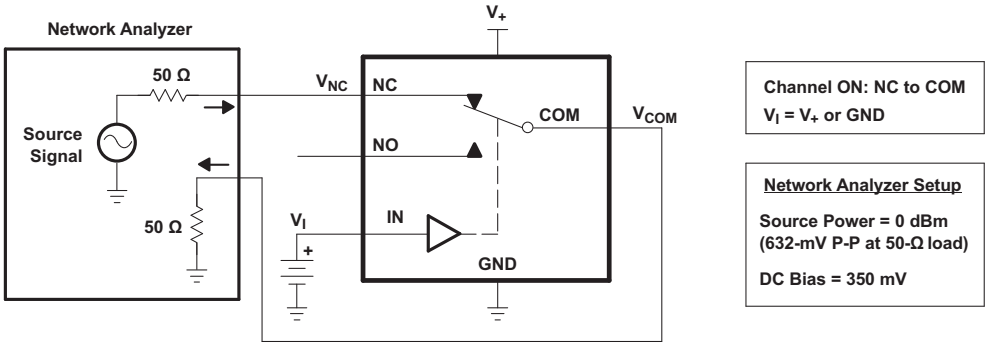


Figure 19. Bandwidth (BW)

Parameter Measurement Information (continued)

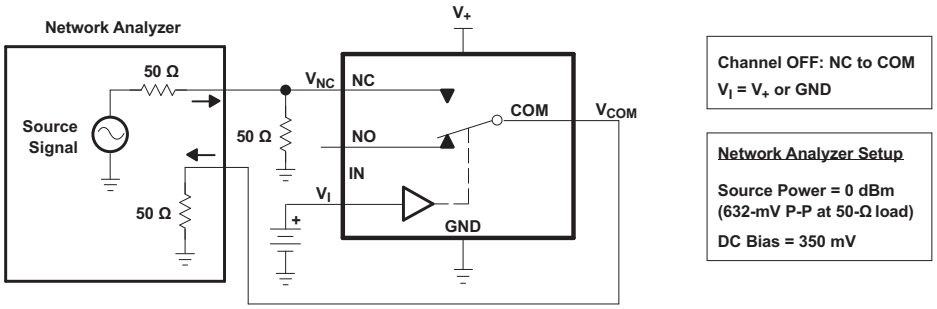


Figure 20. OFF Isolation (OISO)

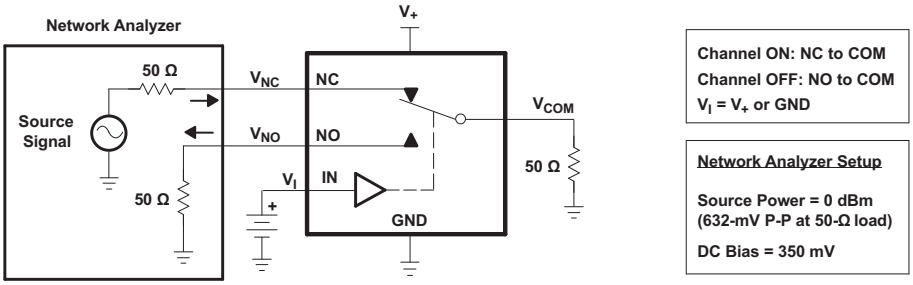
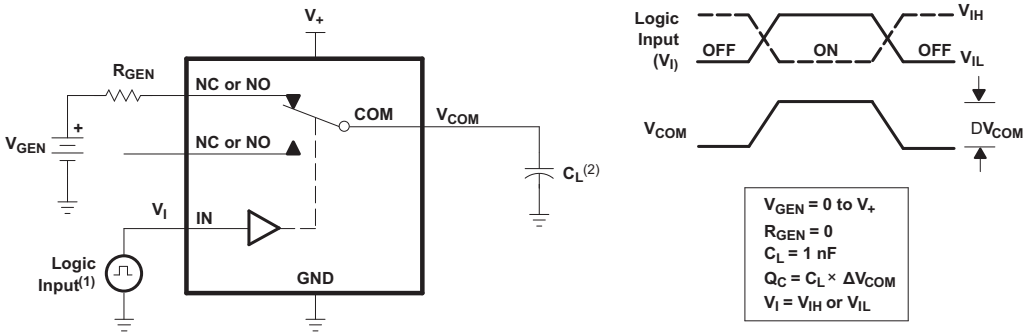


Figure 21. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

A. C_L includes probe and jig capacitance.

Figure 22. Charge Injection (Q_C)

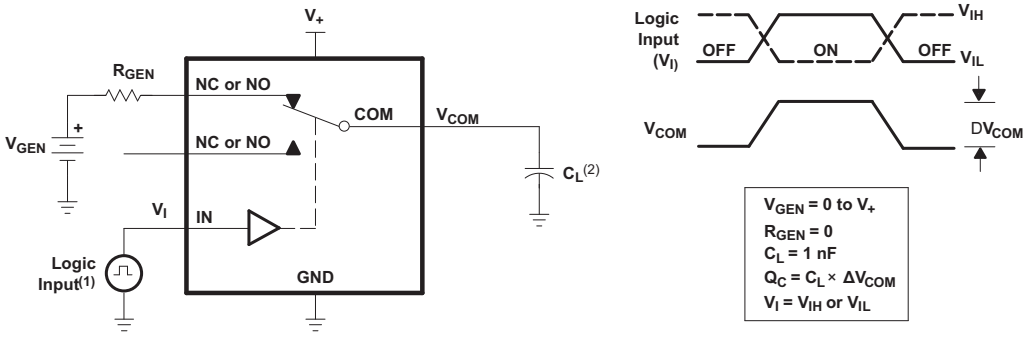


Figure 23. Total Harmonic Distortion (THD)

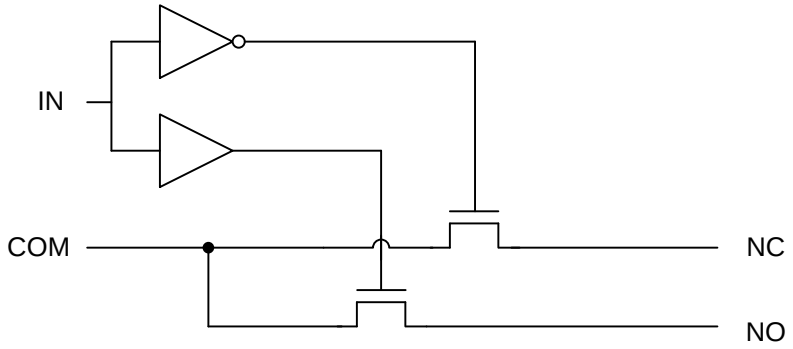
8 Detailed Description

8.1 Overview

The TS5A3160 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3160, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3160 is a make-before-break switch. This means that during switching, a connection is made before the existing connection is broken. During this brief period, the NC and NO pins are connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3160 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1 lists the functional modes for the TS5A3160.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3160 can be used in a variety of customer systems. The TS5A3160 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

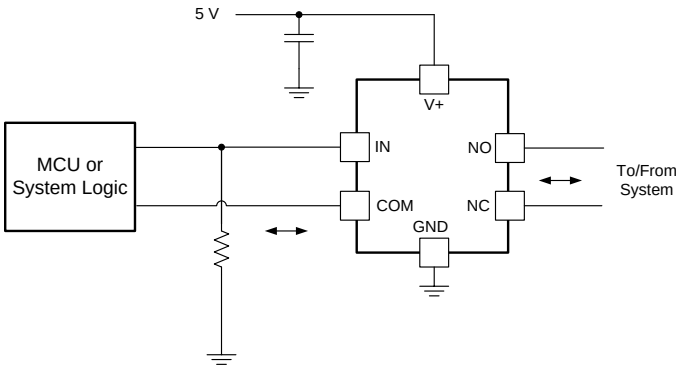


Figure 24. System Schematic for TS5A3160

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

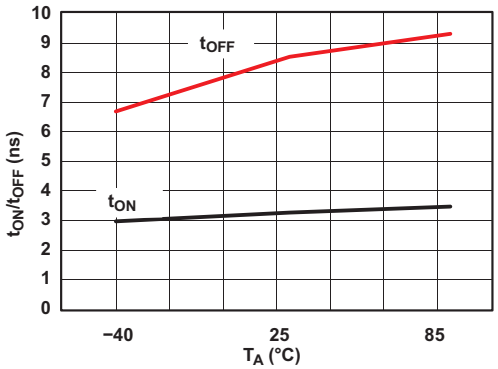


Figure 25. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single-supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

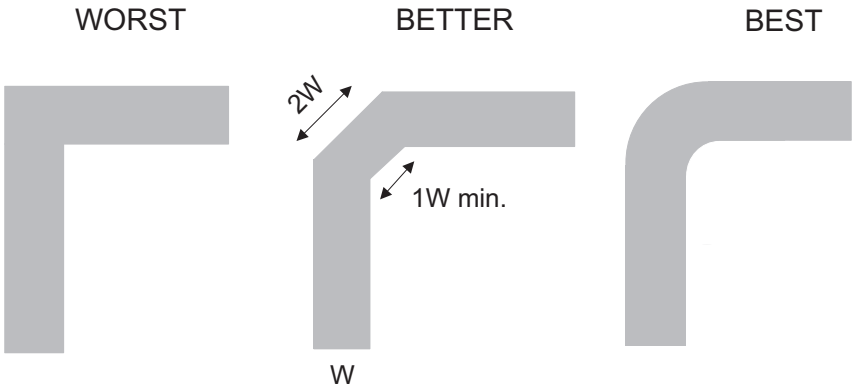


Figure 26. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-off condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-off condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-off condition, $V_+ = 0$
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{MBB}	Make-before-break time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.

Table 2. Parameter Description (continued)

SYMBOL	DESCRIPTION
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3160DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAKR JAKH
TS5A3160DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAKR JAKH
TS5A3160DBVT	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 85	JAKR JAKH
TS5A3160DCKJ	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	(JKK, JKR) JKH
TS5A3160DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JKK, JKR) JKH
TS5A3160DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JKK, JKR) JKH
TS5A3160DCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	(JKK, JKR) JKH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

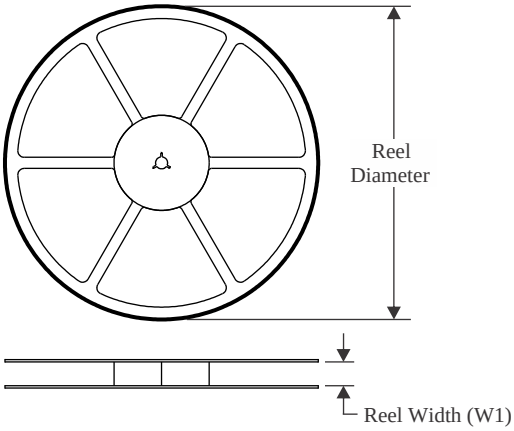
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

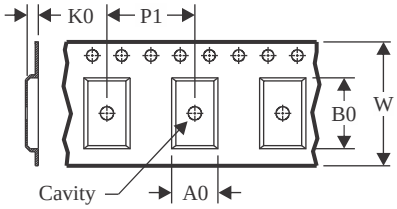
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

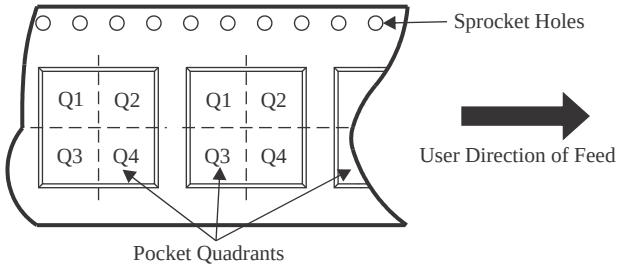


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

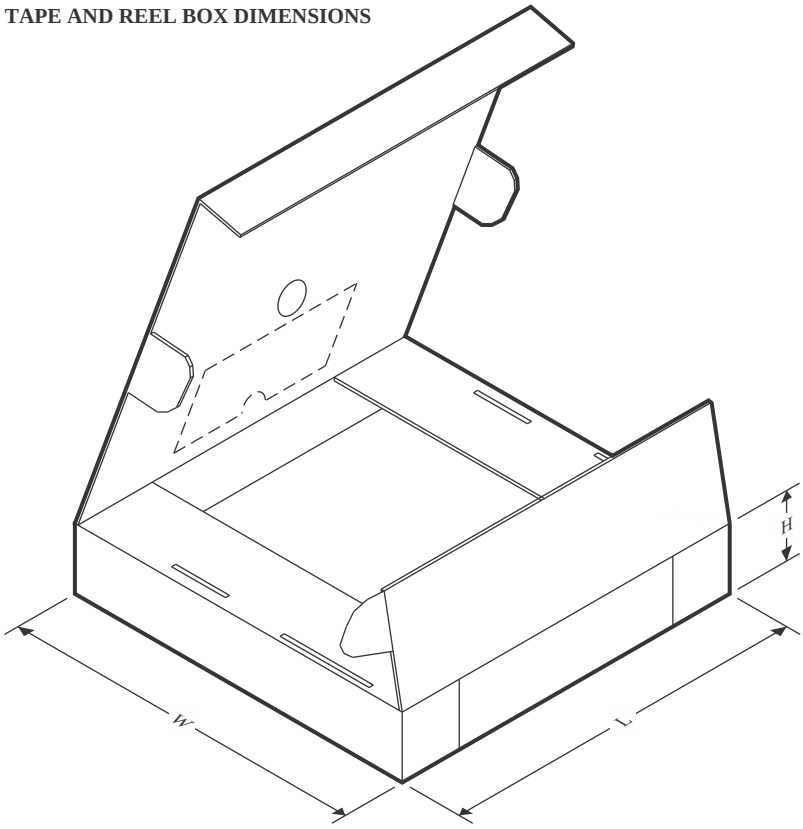
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3160DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3160DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

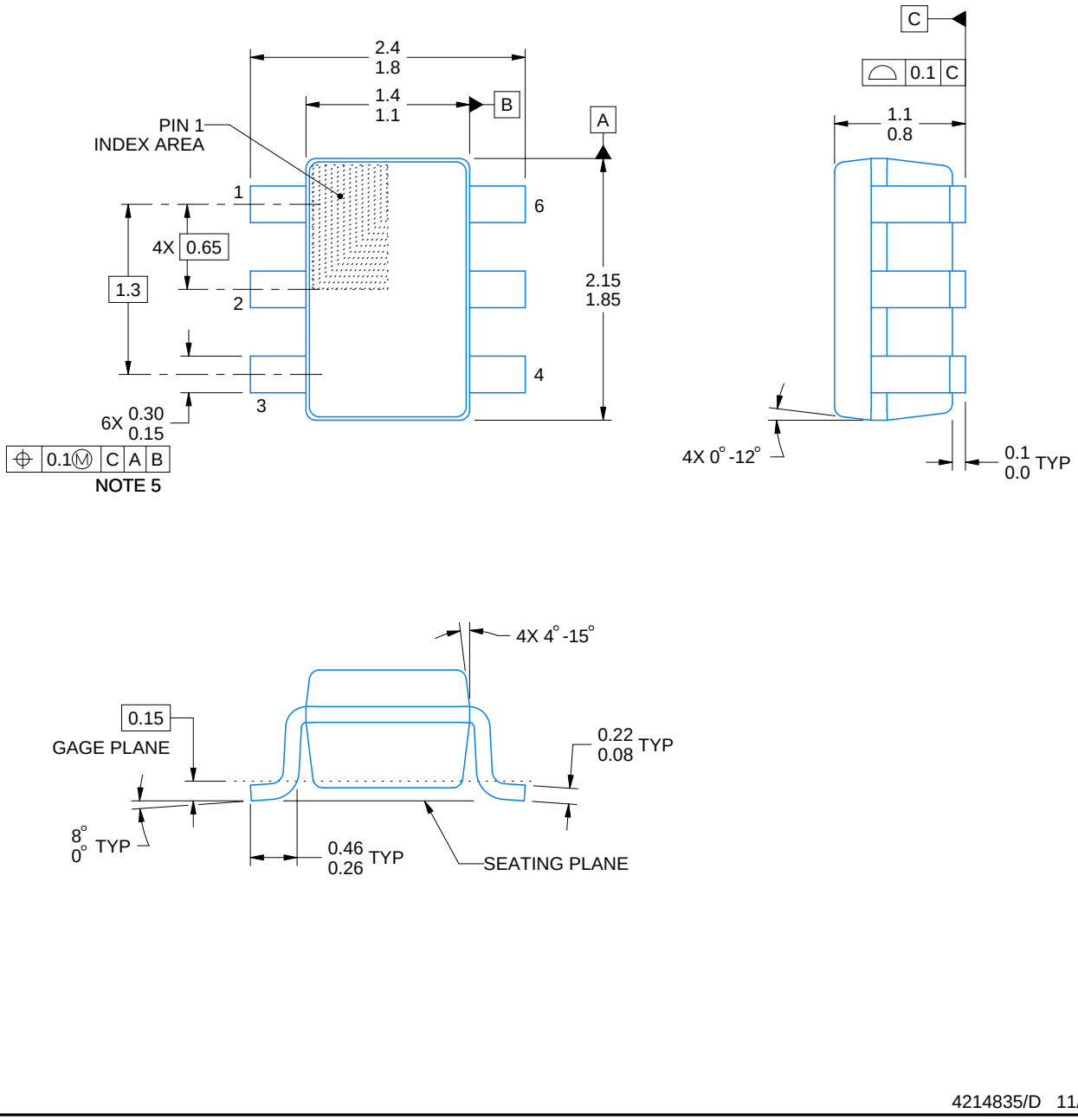
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3160DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3160DCKR	SC70	DCK	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

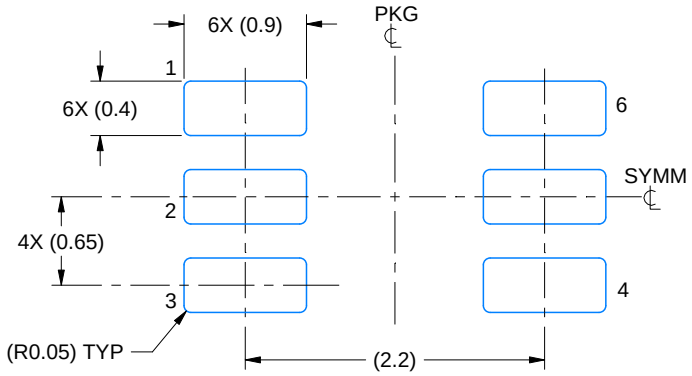
SMALL OUTLINE TRANSISTOR



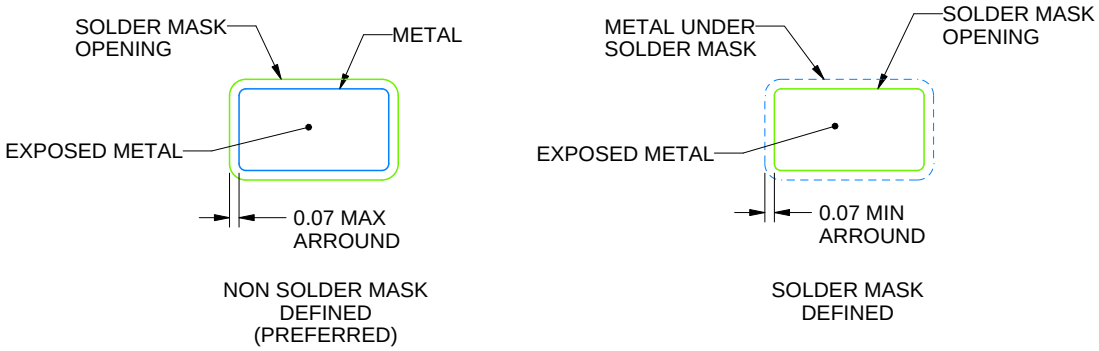
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

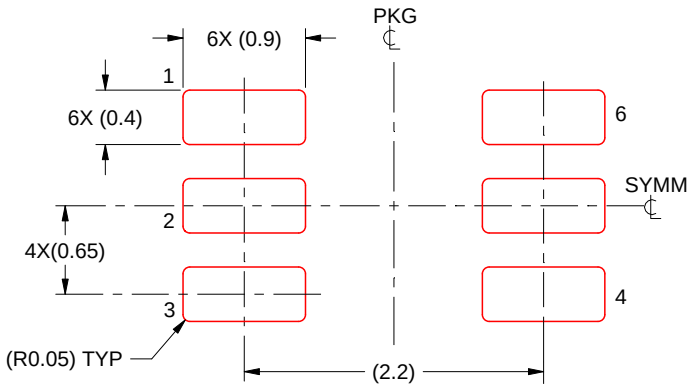


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

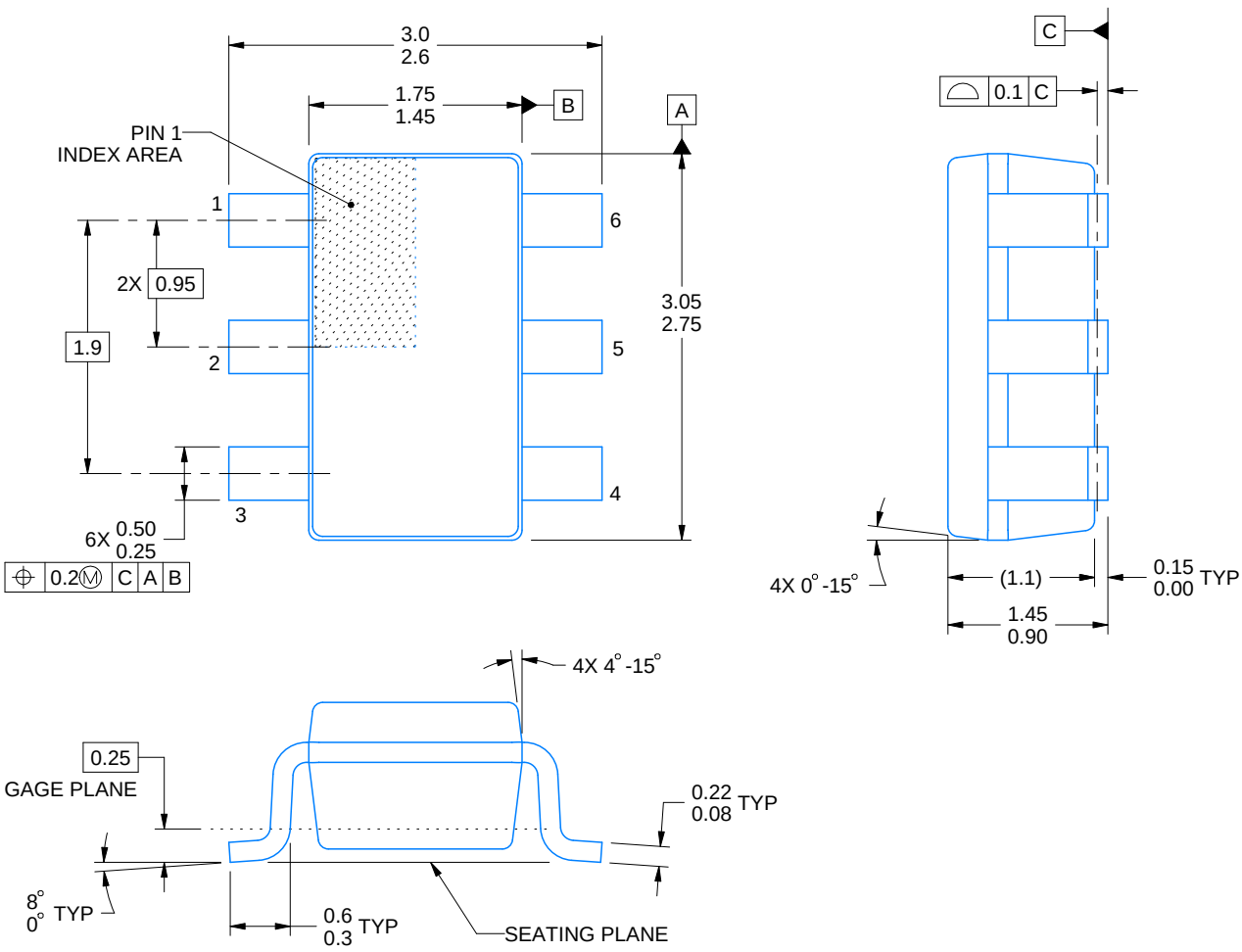
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

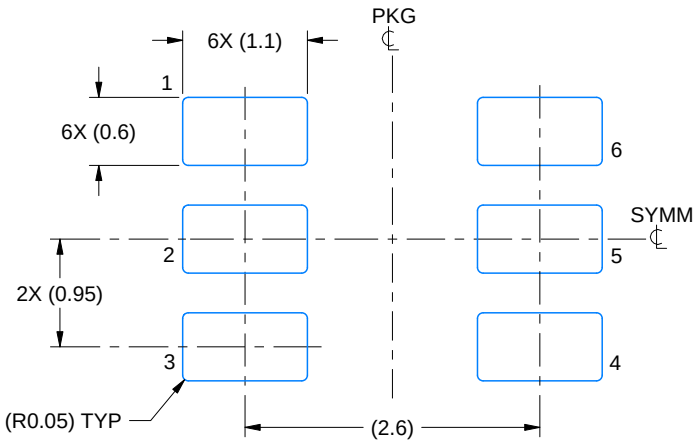
SMALL OUTLINE TRANSISTOR



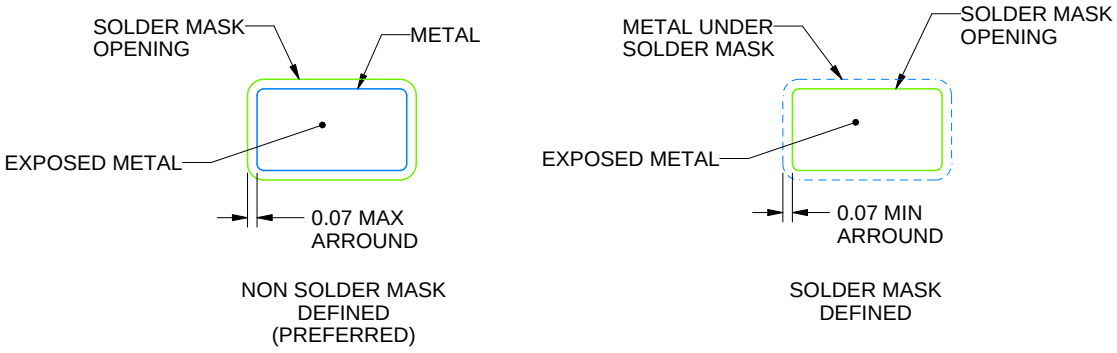
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

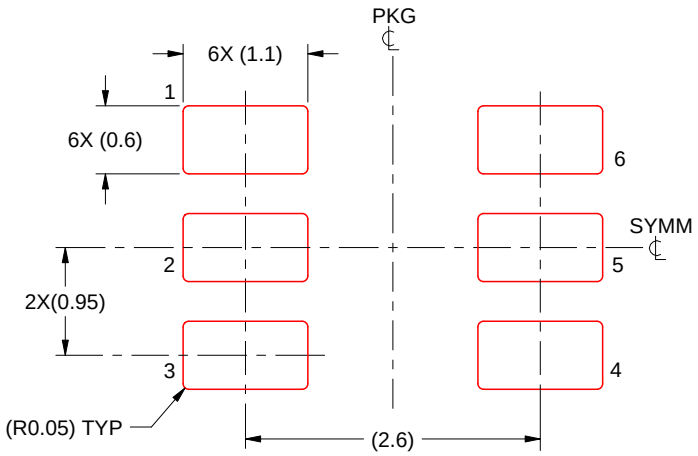


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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