TS5A23157-Q1 双通道 15Ω SPDT 模拟开关

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C4B
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 可支持客户特殊配置控制与重大变更批准
- 指定的先断后合开关
- 低导通电阻 (15Ω)
- 控制输入可承受 5V 电压
- 低电荷注入
- 出色的导通电阻匹配
- 低总计谐波失真
- 1.8V 至 5.5V 单电源运行

2 应用

- 采样保持电路
- 电池供电类设备
- 音频和视频信号路由
- 通信电路

3 描述

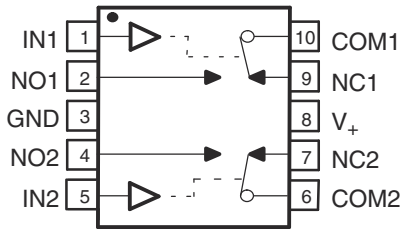
TS5A23157-Q1 是一款双通道单极双投 (SPDT) 模拟开关，其设计工作电压为 1.65V 至 5.5V。该器件可以同时处理数字和模拟信号，并可在任一方向传输高达 5.5V（峰值）的信号。

有关最新的封装和订购信息，请参阅本文档结尾的“封装选项附录”，或访问 TI 网站：www.ti.com。

表 3-1. 器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A23157-Q1	VSSOP (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



TS5A23157-Q1 功能框图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (February 2013) to Revision B (June 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向*特性* 部分添加了“提供功能安全”信息	1

5 Pin Configurations and Functions

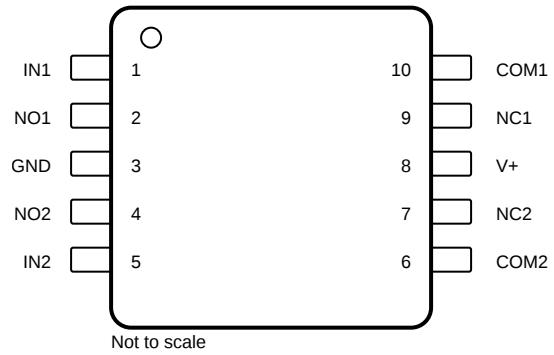


图 5-1. DGS VSSOP (16) Top View

表 5-1. Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
COM1	10	I/O	Common
COM2	6	I/O	Common
GND	3	P	Ground
IN1	1	I	Digital control to connect COM to NO or NC
IN2	5	I	Digital control to connect COM to NO or NC
NC1	9	I/O	Normally closed
NC2	7	I/O	Normally closed
NO1	2	I/O	Normally open
NO2	4	I/O	Normally open
V_+	8	P	Power supply

1. I = input, O = output, I/O = input and output, P = power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(1)		– 0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(1) (2) (3)		– 0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_+		±50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+		±50	mA
V_{IN}	Digital input voltage range(1) (2)		– 0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		– 50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance(4)			165.36	°C/W
T_{stg}	Storage temperature range		– 65	150	°C
ESD	Electrostatic discharge rating	Human-body model H2		2	kV
		Charged-device model C4B		750	V

(1) All voltages are with respect to ground, unless otherwise specified.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = – 40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = – 30 mA,	Switch ON, See 图 8-1	Full	4.5 V			15	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 3.15 V, I_{COM} = – 30 mA,	Switch ON, See 图 8-1	25°C	4.5 V		0.15		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = – 30 mA,	Switch ON, See 图 8-1	25°C	4.5 V		4		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See 图 8-2	25°C	5.5 V	– 1	0.05	1	μA
				Full		– 1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See 图 8-2	25°C	5.5 V	– 0.1		0.1	μA
				Full		– 1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See 图 8-2	25°C	5.5 V	– 0.1		0.1	μA
				Full		– 1		1	
Digital Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.7			V
Input logic low	V_{IL}			Full				V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	5.5 V	– 1	0.05	1	μA
				Full		– 1		1	

6.2 Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	4.5 V to 5.5 V	1.2		8.7	ns
Turnoff time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	4.5 V to 5.5 V	0.5		6.8	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See 图 8-5	25°C	4.5 V to 5.5 V	0.5			ns
Charge injection	Q_C	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	See 图 8-9	25°C	5 V		7		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, See 图 8-3	25°C	5 V		5.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, See 图 8-3	25°C	5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND,	Switch ON, See 图 8-3	25°C	5 V		17.5		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See 图 8-3	25°C	5 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See 图 8-6	25°C	4.5 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See 图 8-7	25°C	4.5 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See 图 8-8	25°C	4.5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See 图 8-10	25°C	4.5 V		0.01		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	µA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	5.5 V			500	µA

(1) T_A = 25°C
(2) Hold all unused digital inputs of the device at V+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.3 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, See 图 8-1	Full	3 V			23	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See 图 8-1	25°C	3 V		0.2		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, See 图 8-1	25°C	3 V		9		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See 图 8-2	25°C	3.6 V	–1	0.05	1	μA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See 图 8-2	25°C	3.6 V	–0.1		0.1	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See 图 8-2	25°C	3.6 V	–0.1		0.1	μA
				Full		–1		1	
Digital Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.7			V
Input logic low	V_{IL}			Full				V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	3.6 V	–1	0.05	1	μA
				Full		–1		1	
Dynamic									
Turnon time	t_{ON}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	3 V to 3.6 V	2.0		10.6	ns
Turnoff time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	3 V to 3.6 V	1.0		8.3	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See 图 8-5	25°C	3 V to 3.6 V	0.5			ns
Charge injection	Q_C	R_L = 50 Ω, CL = 0.1 nF,	See 图 8-9	25°C	3.3 V		3		pC
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 图 8-6	25°C	3 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See 图 8-7	25°C	3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See 图 8-8	25°C	3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See 图 8-10	25°C	3 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	μA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	3.6 V			500	μA

(1) T_A = 25°C

(2) Hold all unused digital inputs of the device at V+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, I_{COM} = –8 mA,	Switch ON, See 图 8-1	Full	2.3 V			50	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, See 图 8-1	25°C	2.3 V		0.5		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, I_{COM} = –8 mA,	Switch ON, See 图 8-1	25°C	2.3 V		27		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See 图 8-2	25°C	2.7 V	–1	0.05	1	μA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See 图 8-2	25°C	2.7 V	–0.1		0.1	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See 图 8-2	25°C	2.7 V	–0.1		0.1	μA
				Full		–1		1	
Digital Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$			V
Input logic low	V_{IL}			Full				$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	2.7 V	–1	0.05	1	μA
				Full		–1		1	
Dynamic									
Turnon time	t_{ON}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	2.3 V to 2.7 V	2.5		17	ns
Turnoff time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	2.3 V to 2.7 V	1.5		10.5	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See 图 8-5	25°C	2.3 V to 2.7 V	0.5			ns
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See 图 8-6	25°C	2.3 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See 图 8-7	25°C	2.3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See 图 8-8	25°C	2.3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See 图 8-10	25°C	2.3 V		0.025		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	2.7 V			500	μA

(1) T_A = 25°C
(2) Hold all unused digital inputs of the device at V+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.5 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, I_{COM} = –4 mA,	Switch ON, See 图 8-1	Full	1.65 V			180	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See 图 8-1	25°C	1.65 V		1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, I_{COM} = –4 mA,	Switch ON, See 图 8-1	25°C	1.65 V		110		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See 图 8-2	25°C	1.95 V	–1	0.05	1	μA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See 图 8-2	25°C	1.95 V	–0.1		0.1	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See 图 8-2	25°C	1.95 V	–0.1		0.1	μA
				Full		–1		1	
Digital Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.75$			V
Input logic low	V_{IL}			Full				$V_+ \times 0.25$	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	1.95 V	–1	0.05	1	μA
				Full		–1		1	
Dynamic									
Turnon time	t_{ON}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	1.65 V to 1.95 V	5.5		27	ns
Turnoff time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+, or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See 图 8-4	Full	1.65 V to 1.95 V	2		16	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See 图 8-5	25°C	1.65 V to 1.95 V	0.5			ns
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See 图 8-6	25°C	1.8 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See 图 8-7	25°C	1.8 V		–60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See 图 8-8	25°C	1.8 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See 图 8-10	25°C	1.8 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	μA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	1.95 V			500	μA

(1) T_A = 25°C
(2) Hold all unused digital inputs of the device at V+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Typical Characteristics

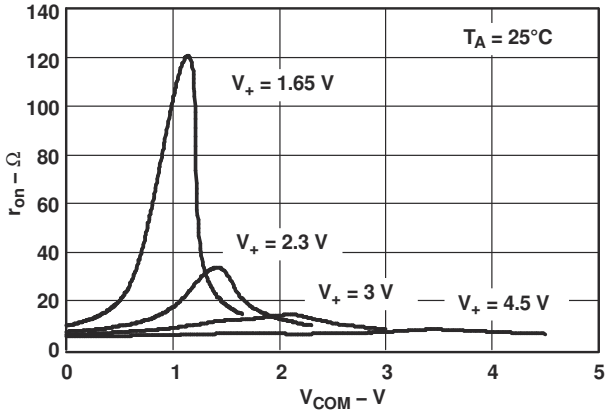


图 6-1. r_{on} versus V_{COM}

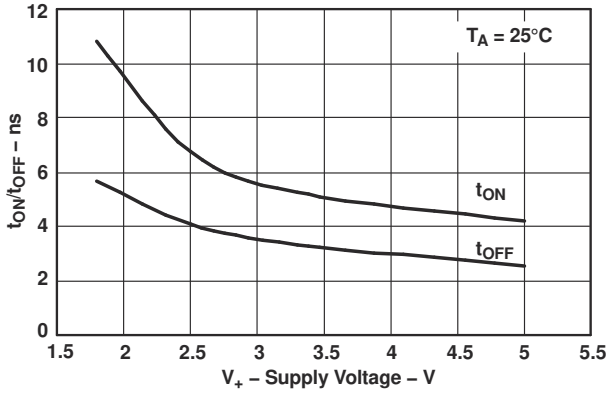


图 6-2. t_{ON} and t_{OFF} versus V_+

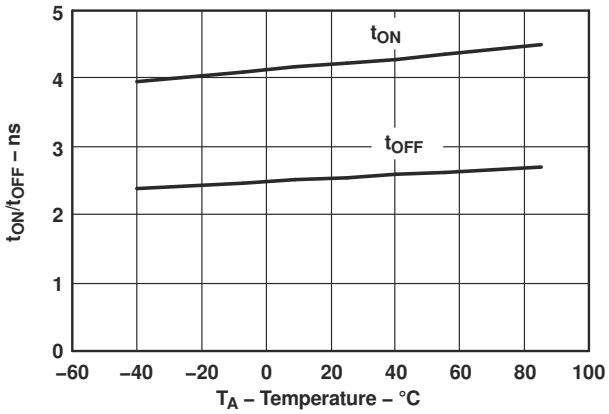


图 6-3. t_{ON} and t_{OFF} versus Temperature (V_+ = 5 V)

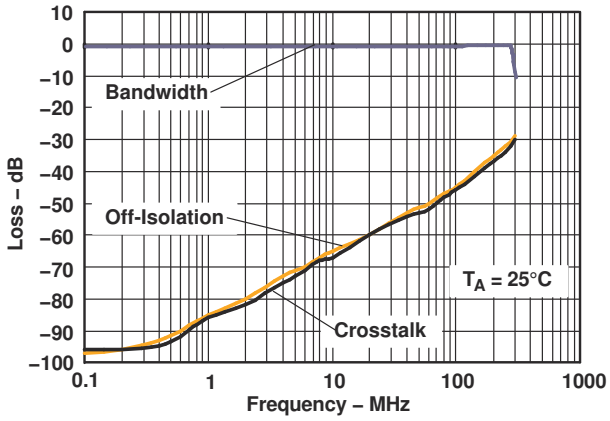


图 6-4. Frequency Response (V_+ = 3 V)

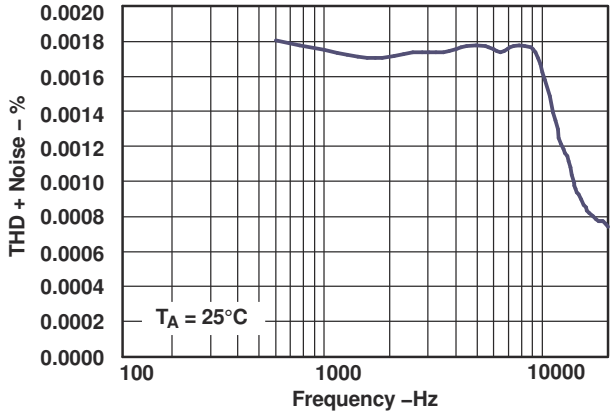
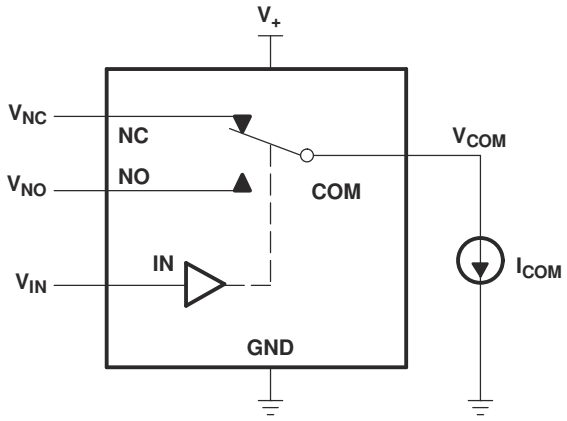


图 6-5. Total Harmonic Distortion (THD) versus Frequency (V_+ = 3 V)

7 Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turnon time for the switch. Measure this parameter under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM/NC/NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. Measure this parameter under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM/NC/NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. Measure this parameter under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This measure is in coulombs (C) and is the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This measure is in dB at a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, O_{ISO} = 20 LOG (V_{NC}/V_{COM}) dB, V_{COM} is the input and V_{NC} is the output.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This measure is at a specific frequency and in dB. Crosstalk, X_{TALK} = 20 log (V_{NC1}/V_{NO1}), V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the dc gain. Gain is measured from the equation, 20 log (V_{NC}/V_{COM}) dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

8 Parameter Measurement Information

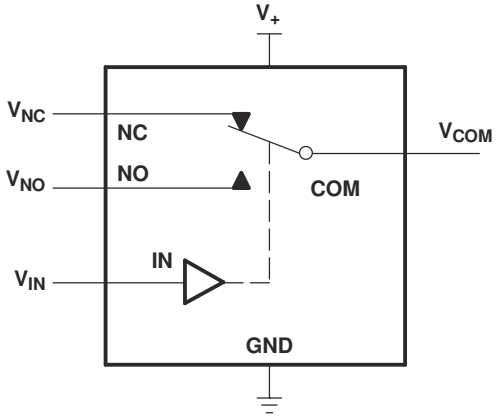


Channel ON

$r_{on} = \frac{V_{COM} - V_{NO/NC}}{I_{COM}}\ \Omega$

$V_{IN} = V_{IH}$ or V_{IL}

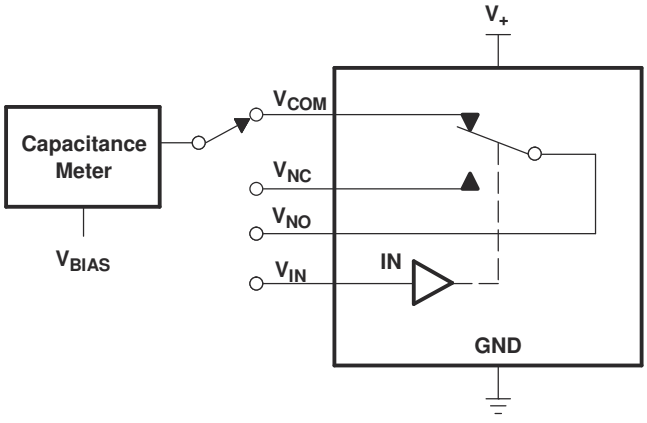
图 8-1. ON-State Resistance (R_{on})



OFF-State Leakage Current
Channel OFF
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+
or
V_{COM} = 0 to V_+

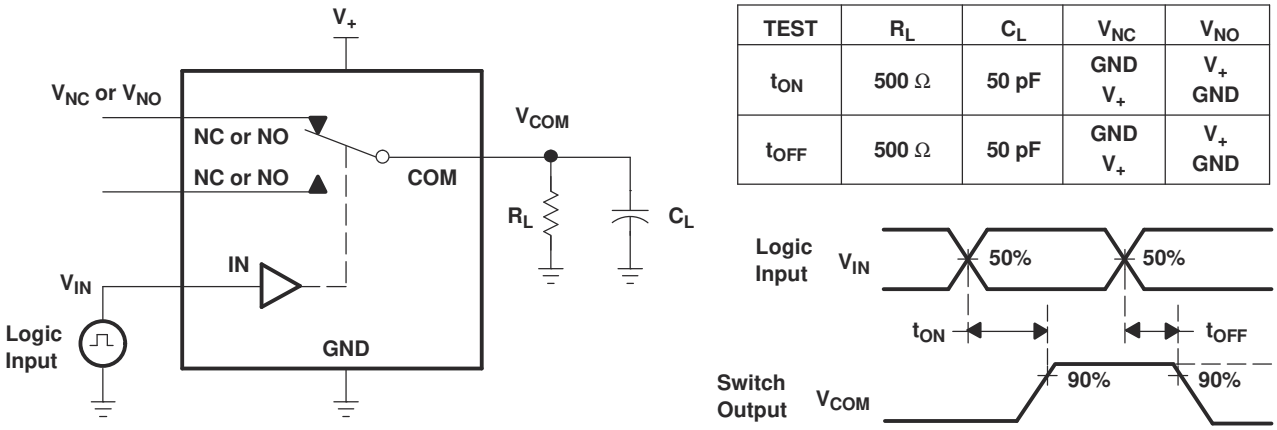
ON-State Leakage Current
Channel ON
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open
or
V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+

图 8-2. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)



$V_{BIAS} = V_+$ or GND
$V_{IN} = V_{IH}$ or V_{IL}
Capacitance is measured at NC, NO, COM, and IN inputs during ON and OFF conditions.

图 8-3. Capacitance (C_{IN}, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{NC}	V_{NO}
t_{ON}	500 Ω	50 pF	GND V_+	V_+ GND
t_{OFF}	500 Ω	50 pF	GND V_+	V_+ GND

图 8-4. Turn-On Time (t_{ON}) and Turn-Off Time (t_{OFF})

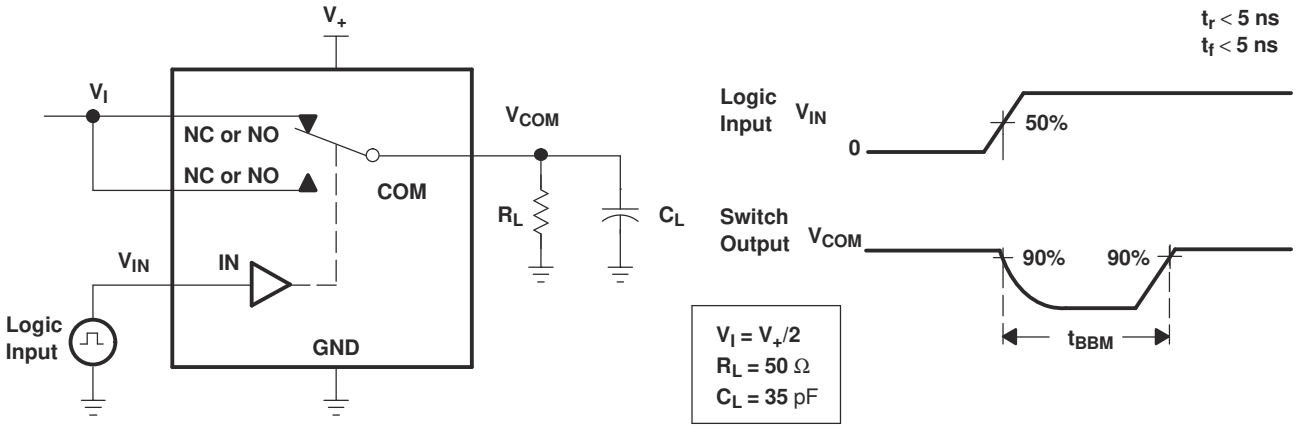


图 8-5. Break-Before-Make Time (t_{BBM})

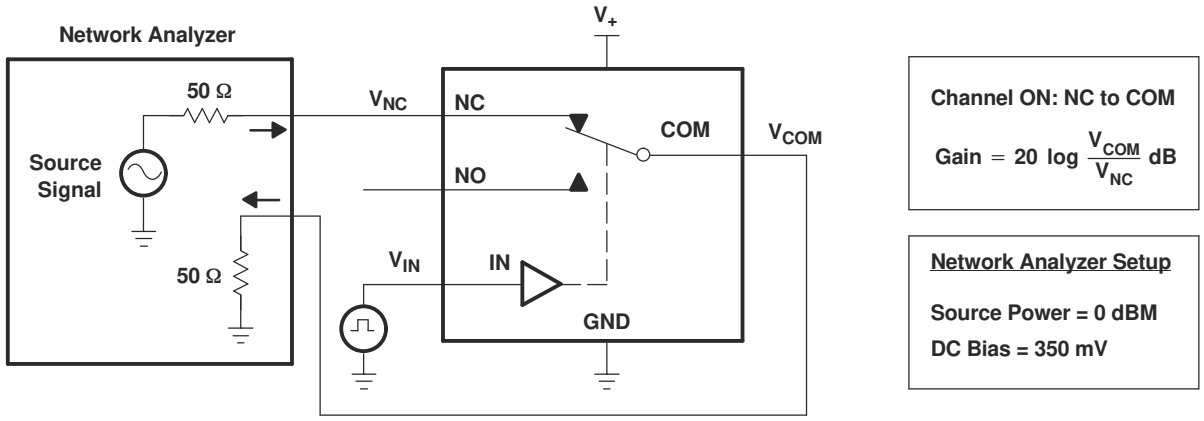


图 8-6. Frequency Response (BW)

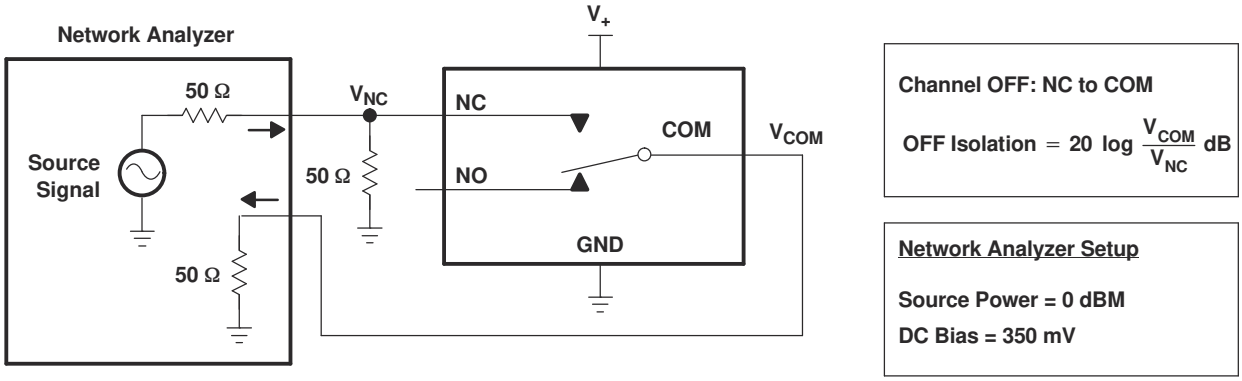


图 8-7. OFF Isolation (O_{ISO})

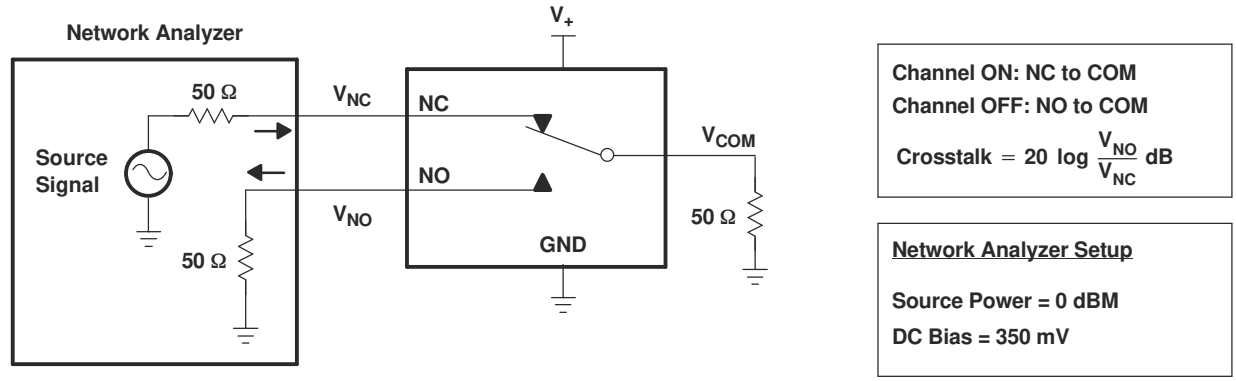


图 8-8. Crosstalk (X_{TALK})

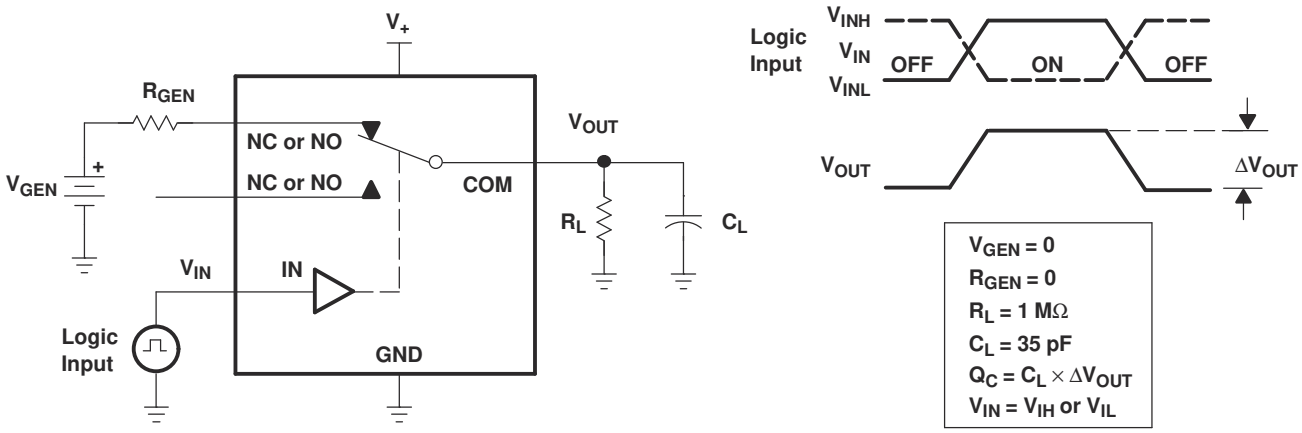


图 8-9. Charge Injection (Q_C)

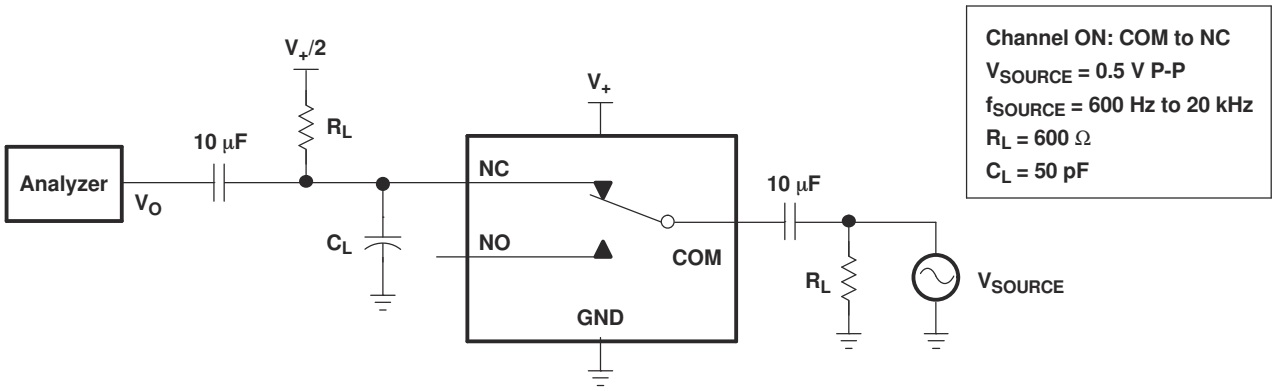


图 8-10. Total Harmonic Distortion (THD)

9 Function and Summary of Characteristics

Input In	NC to COM | COM to NC	NO to COM | COM to NO
L	ON	OFF
H	OFF	ON

表 9-1. Summary of Characteristics

Configuration	2:1 Multiplexer and Demultiplexer (2 × SPDT)
Number of channels	2
r_{on}	15 Ω
Δr_{on}	0.15 Ω
$r_{on(flat)}$	4 Ω
t_{ON}	8.7 ns
t_{OFF}	6.8 ns
t_{BBM}	0.5 ns
Charge injection	7 pC
Bandwidth	220 MHz
OFF isolation	–65 dB at 10 MHz
Crosstalk	–66 dB at 10 MHz
Total harmonic distortion	0.01%
$I_{COM(off)}/I_{NC(OFF)}$	±1 μA
Package option	10-pin DGS

10 Detailed Description

10.1 Overview

The TS5A23157-Q1 is a 2 channel 2:1 switch (SPDT). It has a wide operating supply of 1.8 V to 5.5 V that allows for use in a wide array of applications from sample and hold circuits to communication protocol switching such as I2C or UART. The device supports bidirectional analog and digital signals on the source (NCx and NOx) and drain (COMx) pins.

10.2 Functional Block Diagram

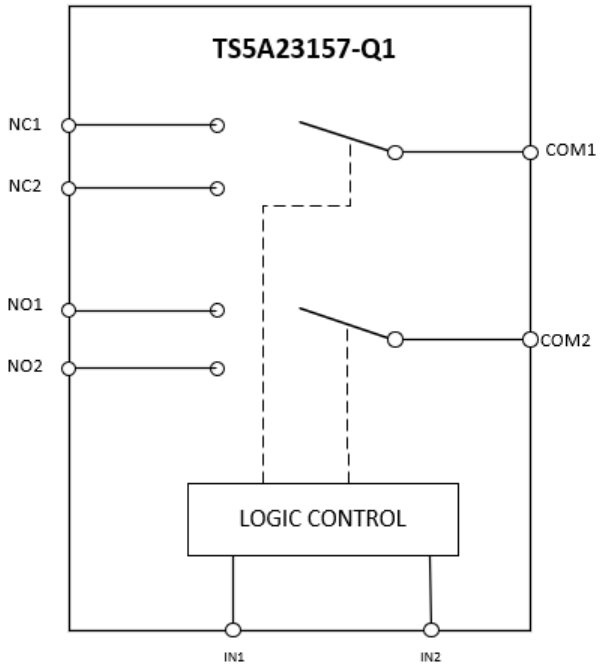


图 10-1. TS5A23157-Q1 Functional Block Diagram

10.3 Feature Description

Bidirectional Operation

The TS5A23157-Q1 conducts equally well from source (NCx and NOx) to drain (COMx) or from drain (COMx) to source (NCx and NOx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

10.4 Device Functional Modes

The digital control pins (IN1 and IN2) are the logic pins that control their respective common connections (COM1 and COM2) with both the normally closed pathways (NC1 and NC2) and the normally open pathways (NO1 and NO2). When either or both digital control pins (IN1 and IN2) are pulled low their respecitive common (COM1 and COM2) and normally closed (NC1 and NC2) pins are connected. When either or both digital control pins (IN1 and IN2) are pulled high their respective common (COM1 and COM2) and normally open (NO1 and NO2) pins are connected.

The TS5A23157-Q1 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins (INx) should be tied to GND or VDD in order to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (NCx, NOx, and COMx) should be connected to GND.

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

Common applications that require the features of the TS5A23157-Q1 include multiplexing various protocols from a processor MCU such as I2C, UART, or standard GPIO signals. With the TS5A23157-Q1's wide operating supply range different variations of signal levels with GPIO, UART, and I2C can all be passed and the supply voltage can vary with the needs of the system designer. A typical UART application is shown in the Typical Application Section.

11.2 Typical Application

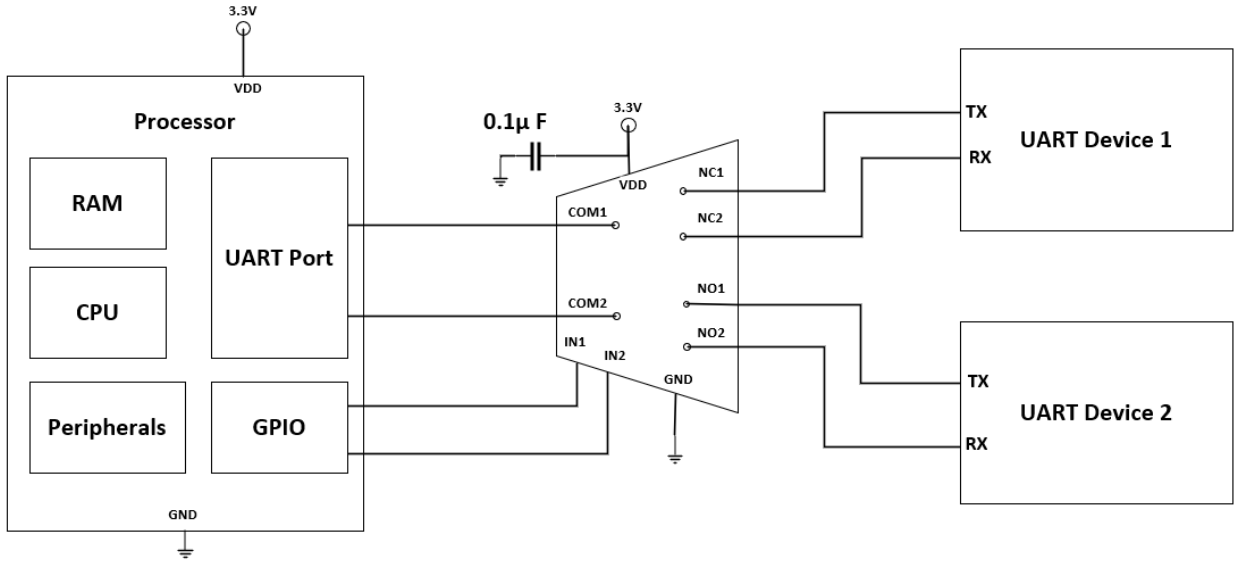


图 11-1. TS5A23157-Q1 Used in UART Application

11.3 Design Requirements

For the typical application shown above - please use the following parameters shown below.

表 11-1. Design Parameters

PARAMETER	VALUE
Supply Voltage	3.3 V
Input / Output Voltage	0 V – 3.3 V
Logic Input High	2.31 V – 3.3 V
Logic Input Low	0 V – 0.99 V

11.4 Detailed Design Procedure

The TS5A23157-Q1 can be operated without any external components except for the supply decoupling capacitors. To ensure known logic states at start up - use pull-down resistors, between 10 KΩ and 100 KΩ, on each control input (INx). All inputs signals passing through the switch must fall within the recommend operating conditions of the TS5A23157-Q1 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. Due to the voltage range and bandwidth of the switch, it can support many applications such as I2C, UART, and GPIO switching.

11.5 Application Performance Plots

Three important parameters when using the TS5A23157-Q1 in any communication protocol / GPIO switching application are the bandwidth of the switch as well as off isolation and cross talk. The below figure shows the typical bandwidth, off isolation, and cross talk versus frequency. When implenmenting this use case of the switch it is crucial to understand the AC error that other signals may create when using this device.

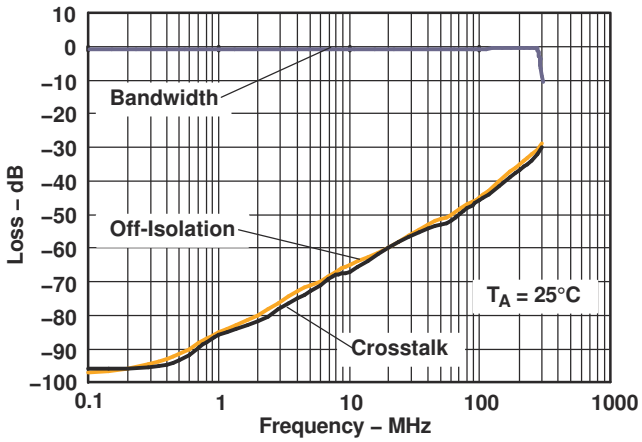


图 11-2. AC Parmeters for TS5A23157-Q1 (V+ = 3V)

12 Power Supply Recommendations

The TS5A23157-Q1 operates across a wide supply range of 1.8 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Power-supply bypassing improves noise margin and prevents switching noise propagation from the VDD supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from VDD to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

13 Layout

13.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.The figure below shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

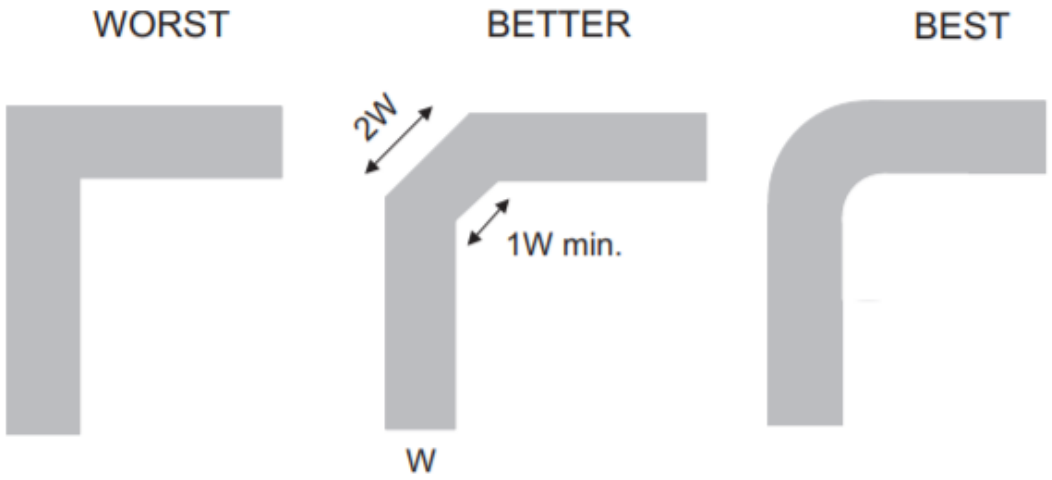


图 13-1. Trace Guidelines for TS5A23157-Q1

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, throughhole pins are not recommended at high frequencies. Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals. Avoid stubs on the high-speed signals traces because they cause signal reflections. Route all high-speed signal traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits. When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown below.

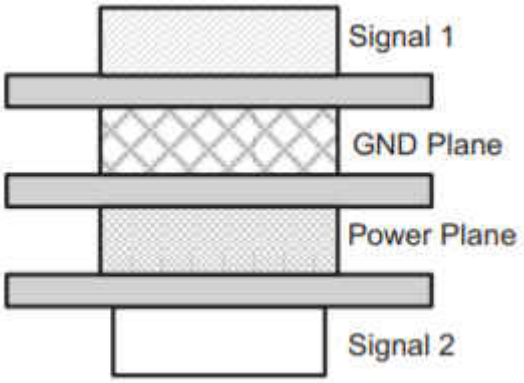


图 13-2. Layer Stack Example for TS5A23157-Q1 device.

13.2 Layout Example

- Decouple the VDD pin with a 0.1 μF capacitor, placed as close to the pin as possible.
- Make sure that the capacitor voltage rating is sufficient for the VDD supply.
- High-speed switches require proper layout and design procedures for optimum performance.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

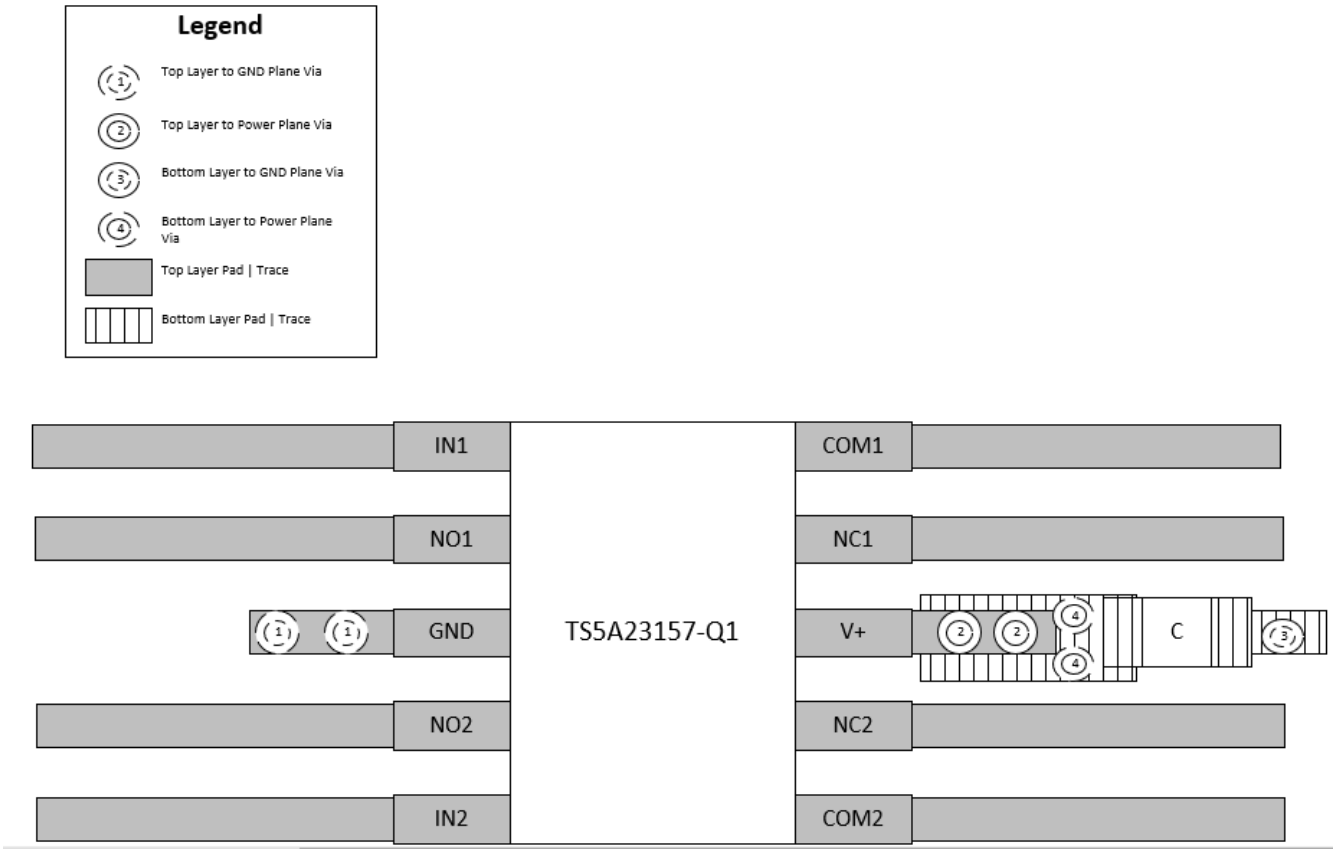


图 13-3. Layout Example of TS5A23157-Q1

14 Device and Documentation Support

14.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

14.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

15.1 Ordering Information

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	VSSOP 10 – (DGS)	Tape and reel	TS5A23157TDGSRQ1	JBR
–40°C to 125°C	VSSOP 10 – (DGS)	Tape and reel	TS5A23157QDGSRQ1	SJC

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23157QDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJC
TS5A23157QDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJC
TS5A23157TDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	JBR
TS5A23157TDGSRQ1.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	JBR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A23157-Q1 :

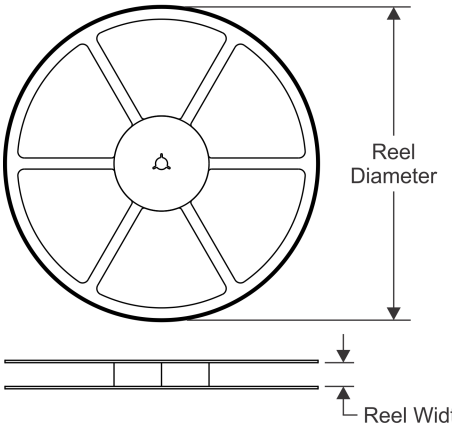
- Catalog : TS5A23157

NOTE: Qualified Version Definitions:

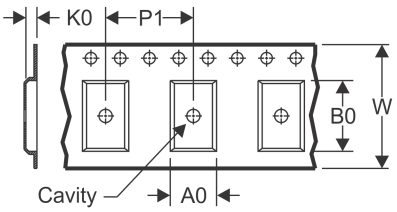
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

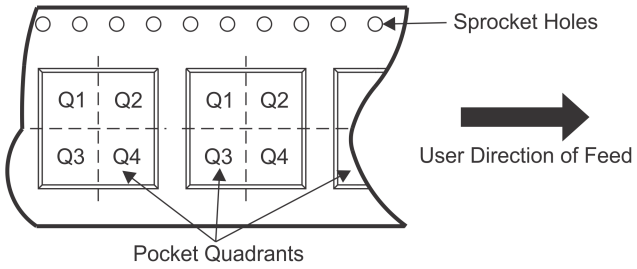


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

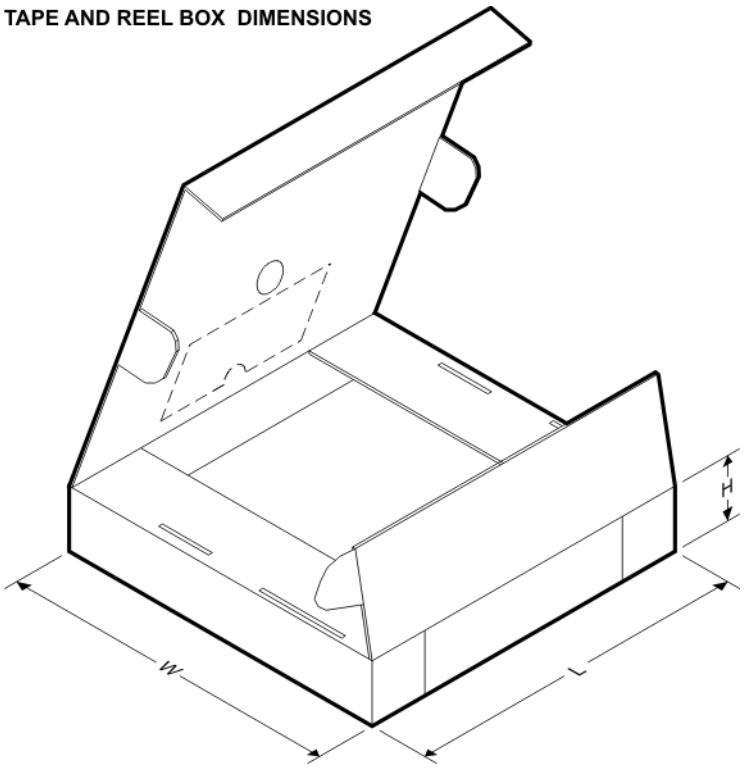
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157TDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

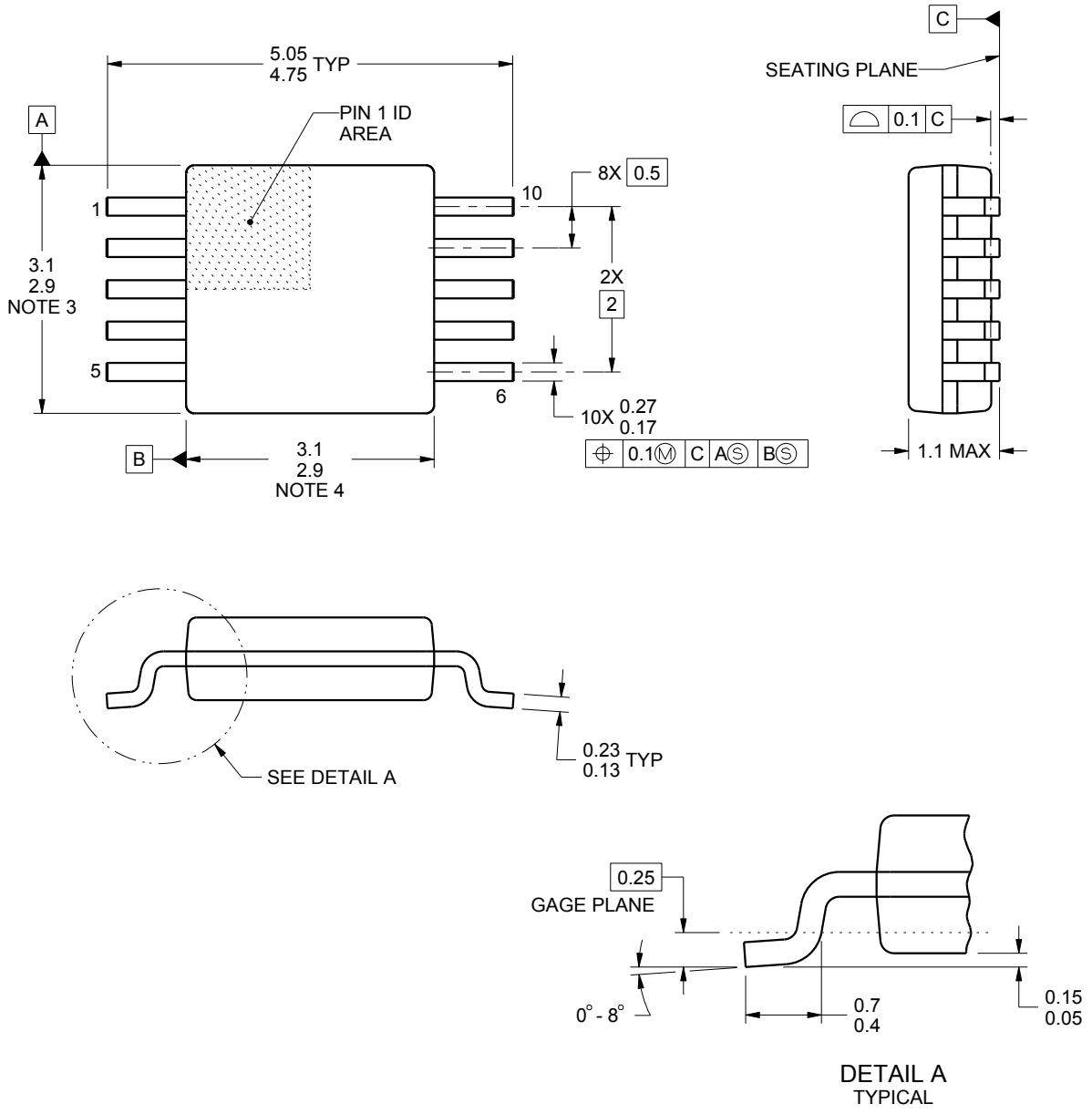
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157QDGSRQ1	VSSOP	DGS	10	2500	346.0	346.0	29.0
TS5A23157TDGSRQ1	VSSOP	DGS	10	2500	346.0	346.0	29.0

PACKAGE OUTLINE

DGS0010A

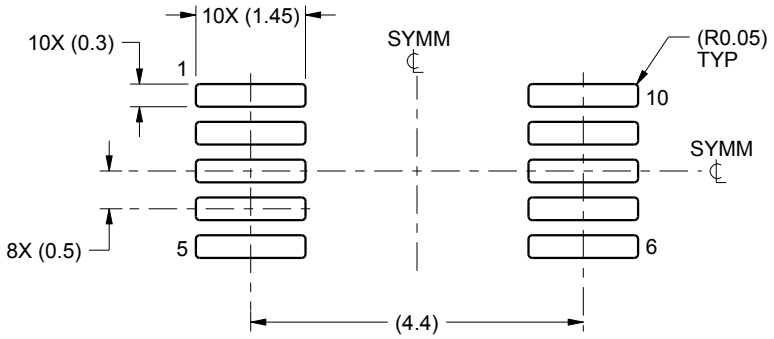
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

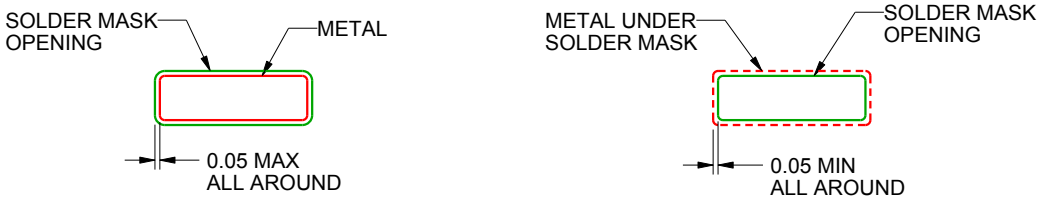


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

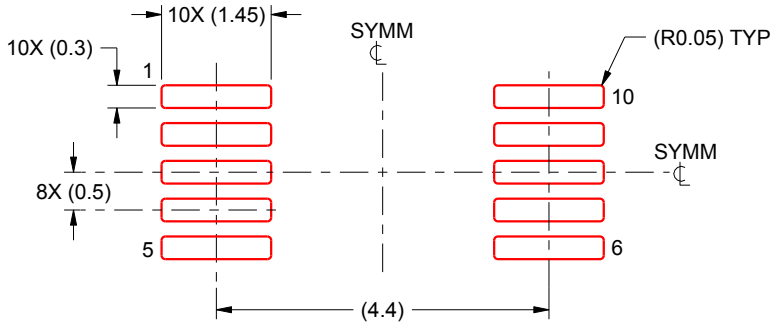


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月