TS3L501E 具有断电模式的 11 通道 SPDT/22 位至 11 位多路复用器和多路信号分离器以太网 LAN 开关

1 特性

- 集成断电模式
- 高带宽（BW = 600MHz，典型值）
- 低串扰（在 250MHz 下的典型值为 X_{TALK} = -37dB）
- 低位间偏差（$t_{sk(o)}$ = 100ps 最大值）
- 平缓的低导通状态电阻（r_{on} = 4Ω 典型值，$r_{on(flat)}$ = 0.5Ω 典型值）
- 低输入和输出电容（C_{ON} = 9pF 典型值）
- 支持在数据 I/O 端口上进行轨到轨开关（0V 至 3.6V）
- V_{CC} 工作电压范围：3V 至 3.6V
- 支持断电模式
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 性能（A、B、C 和 LED 引脚）
  - ±4kV IEC61000-4-2，接触放电
  - 符合 JESD22-A114E 标准的 6kV 人体放电模型（将 I/O 引脚切换到 GND）
- ESD 性能（所有引脚）
  - 符合 JESD22-A114E 的 2kV 人体放电模式

2 应用

- 10、100 和 1000 Base-T 信号开关
- 差分（LVDS 和 LVPECL）信号切换
- 音频和视频切换
- 集线器和路由器信号切换

3 说明

TS3L501E 是一款具有单选 (SEL) 输入和断电模式输入的 11 通道 SPDT 模拟开关或 22 位至 11 位多路复用器或多路信号分离器 LAN 开关。该器件提供用于切换状态指示 LED 信号的额外 I/O，并包含高 ESD 保护。SEL 输入控制多路复用器或多路信号分离器的数据路径。断电输入可将器件置于待机模式，从而更大限度地降低每种模式选择的电流消耗。

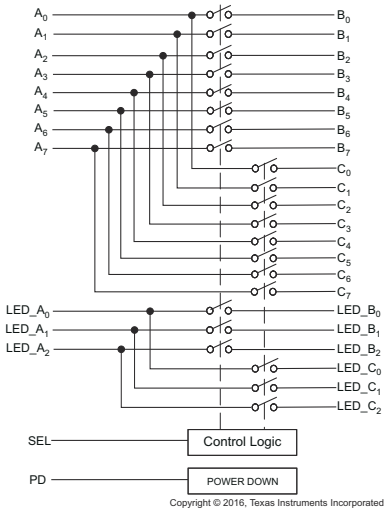
该器件提供平缓的低导通状态电阻（r_{on}）和出色的导通状态电阻匹配。该器件具有低输入或输出电容、高带宽、低偏斜和低通道间串扰，适用于各种 LAN 应用（例如 10/100/1000 Base-T），还可用于替代 LAN 应用中的机械继电器。它也可以用于将信号从 10/100 Base-T 以太网收发器路由至笔记本电脑或扩展坞中的 RJ-45 LAN 连接器。

其在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TS3L501E	RUA（WQFN，42）	9.00mm x 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

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4 Revision History

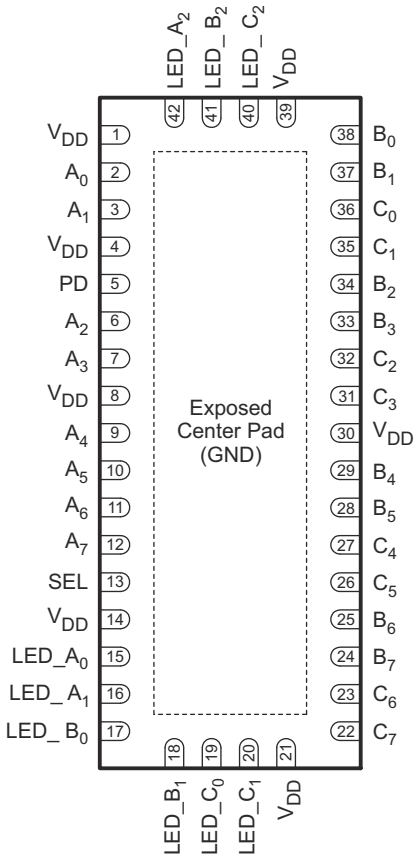
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (December 2017) to Revision D (October 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将整个数据表中的 *8 通道* 更改为 *11 通道*	1
• 将整个数据表中的 *16 位至 8 位* 更改为 *22 位至 11 位*	1

Changes from Revision B (May 2016) to Revision C (December 2017)	Page
• Added pin numbers 4, 8, 14, 21, 30, 39 to V_{DD} in the *Pin Functions* table	3

Changes from Revision A (September 2010) to Revision B (May 2016)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。	1
• 删除了*订购信息* 表	1

5 Pin Configuration and Functions



The exposed center pad must be connected to GND.

图 5-1. RUA Package, 42-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A_0	2	I/O	Port A Common I/O signal path
A_1	3	I/O	Port A Common I/O signal path
A_2	6	I/O	Port A Common I/O signal path
A_3	7	I/O	Port A Common I/O signal path
A_4	9	I/O	Port A Common I/O signal path
A_5	10	I/O	Port A Common I/O signal path
A_6	11	I/O	Port A Common I/O signal path
A_7	12	I/O	Port A Common I/O signal path
B_0	38	I/O	Port B I/O signal path
B_1	37	I/O	Port B I/O signal path
B_2	34	I/O	Port B I/O signal path
B_3	33	I/O	Port B I/O signal path
B_4	29	I/O	Port B I/O signal path
B_5	28	I/O	Port B I/O signal path
B_6	25	I/O	Port B I/O signal path
B_7	24	I/O	Port B I/O signal path

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
C_0	36	I/O	Port C I/O signal path
C_1	35	I/O	Port C I/O signal path
C_2	32	I/O	Port C I/O signal path
C_3	31	I/O	Port C I/O signal path
C_4	27	I/O	Port C I/O signal path
C_5	26	I/O	Port C I/O signal path
C_6	23	I/O	Port C I/O signal path
C_7	22	I/O	Port C I/O signal path
GND	Exposed Center Pad	—	Ground
LED_A_0	15	I/O	Port A LED I/O Common signal path, (may also be used as a general purpose signal path)
LED_A_1	16	I/O	Port A LED Common I/O signal path, (may also be used as a general purpose signal path)
LED_A_2	42	I/O	Port A LED Common I/O signal path, (may also be used as a general purpose signal path)
LED_B_0	17	I/O	Port B LED I/O signal path, (may also be used as a general purpose signal path)
LED_B_1	18	I/O	Port B LED I/O signal path, (may also be used as a general purpose signal path)
LED_B_2	41	I/O	Port B LED I/O signal path, (may also be used as a general purpose signal path)
LED_C_0	19	I/O	Port C LED I/O signal path, (may also be used as a general purpose signal path)
LED_C_1	20	I/O	Port C LED I/O signal path, (may also be used as a general purpose signal path)
LED_C_2	40	I/O	Port C LED I/O signal path, (may also be used as a general purpose signal path)
PD	5	I	Power down input, active high
SEL	13	I	Select input
V_{DD}	1, 4, 8, 14, 21, 30, 39	—	Power

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{DD} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1, 4, 5, 8, 13, 14, 21, 30, and 39	±6000	V
			Pins 1, 4, 5, 8, 13, 14, 21, 30, and 39	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
V_{IN}	Input voltage (SEL)	0	5.5	V
$V_{I/O}$	Input or output voltage	0	V_{DD}	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		TS3L501E RUA (WQFN) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	30.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics for 1000 Base-T Ethernet Switching

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
V_{IK}	SEL, PD	V_{DD} = 3.6 V, I_{IN} = – 18 mA		– 0.7	– 1.2	V
I_{IH}	SEL, PD	V_{DD} = 3.6 V, V_{IN} = V_{DD}			±2	µA
I_{IL}	SEL, PD	V_{DD} = 3.6 V, V_{IN} = GND			±1	µA
I_{OFF}	SEL, PD	V_{DD} = 0 V, V_{IN} = 0 to 3.6 V			±1	µA
I_{CC}		V_{DD} = 3.6 V, $I_{I/O}$ = 0, switch ON or OFF		250	600	µA
I_{CC_PD}		V_{DD} = 3.6 V, V_{IN} = 3.6 V, PD = high		1		
C_{IN}	SEL, PD	f = 1 MHz, V_{IN} = 0		2.6	3	pF
C_{OFF}	B or C port	V_I = 0,f = 1 MHz, outputs open, switch OFF		3	4	pF
C_{ON}		V_I = 0,f = 1 MHz, outputs open, switch ON		9	9.8	pF
r_{on}		V_{DD} = 3 V, 1.5 V ≤ V_I ≤ V_{DD}, I_O = – 40 mA		4	8	Ω
$r_{on(flat)}$ [3]		V_{DD} = 3 V, V_I = 1.5 V and V_{DD}, I_O = – 40 mA		0.7		Ω
Δr_{on} [4]		V_{DD} = 3 V, 1.5 V ≤ V_I ≤ V_{DD}, I_O = – 40 mA		0.8	1.5	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

6.6 Electrical Characteristics for 10/100 Base-T Ethernet Switching

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL, PD	V_{DD} = 3.6 V, I_{IN} = – 18 mA		– 0.7	– 1.2	V
I_{IH}	SEL, PD	V_{DD} = 3.6 V, V_{IN} = V_{DD}			±2	μA
I_{IL}	SEL, PD	V_{DD} = 3.6 V, V_{IN} = GND			±1	μA
I_{OFF}	SEL, PD	V_{DD} = 0 V, V_{IN} = 0 to 3.6 V			±1	μA
I_{CC}		V_{DD} = 3.6 V, $I_{I/O}$ = 0, switch ON or OFF		250	600	μA
I_{CC_PD}		V_{DD} = 3.6 V, V_{IN} = 3.6 V, PD = high		1		
C_{IN}	SEL, PD	f = 1 MHz, V_{IN} = 0		2.6	3.0	pF
C_{OFF}	B or C port	V_I = 0,f = 10 MHz, outputs open, switch OFF		3	4	pF
C_{ON}		V_I = 0,f = 10 MHz, outputs open, switch ON		9	9.8	pF
r_{on}		V_{DD} = 3 V, 1.25 V ≤ V_I ≤ V_{DD}, I_O = – 10 mA to – 30 mA		4	6	Ω
$r_{on(flat)}$ (3)		V_{DD} = 3 V, V_I = 1.25 V and V_{DD}, I_O = – 10 mA to – 30 mA		0.5		Ω
Δr_{on} (4)		V_{DD} = 3 V, 1.25 V ≤ V_I ≤ V_{DD}, I_O = – 10 mA to – 30 mA		0.8	1.5	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

6.7 Switching Characteristics

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd} (2)	A or B/C	B/C or A		0.3		ns
t_{PZH}, t_{PZL}	SEL	A or B/C	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	A or B/C	0.9		9	ns
$t_{sk(o)}$ (3)	A or B/C	B/C or A		50	100	ps
$t_{sk(p)}$ (4)	A or B/C	B/C or A		50	100	ps
t_{ON}/t_{OFF} (5)	PD	A or B/C			250	ns

(1) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_4 to A_5) to any other port
(4) Skew between opposite transitions of the same output in a given device |t_{PHL} – t_{PLH}|
(5) Device enable/disable time from PD

6.8 Dynamic Characteristics

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	R_L = 50 Ω, f = 250 MHz, see 图 7-4	– 37	dB
O_{IRR}	R_L = 50 Ω, f = 250 MHz, see 图 7-5	– 37	dB
BW	See 图 7-3	600	MHz

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

6.9 Typical Characteristics

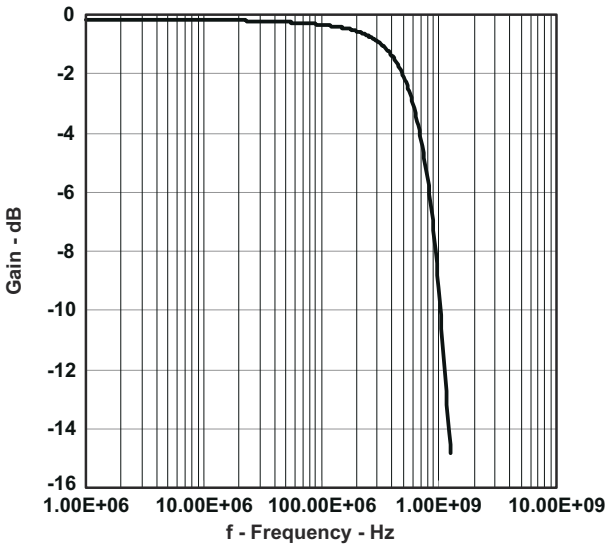


图 6-1. Gain vs Frequency

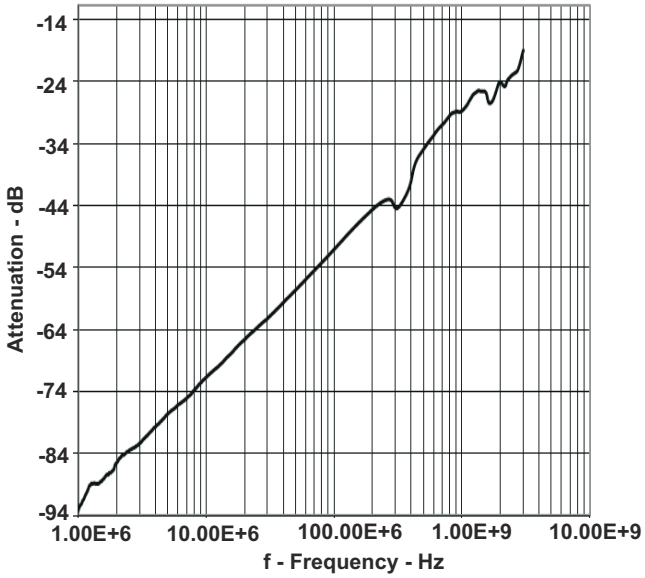


图 6-2. OFF Isolation vs Frequency

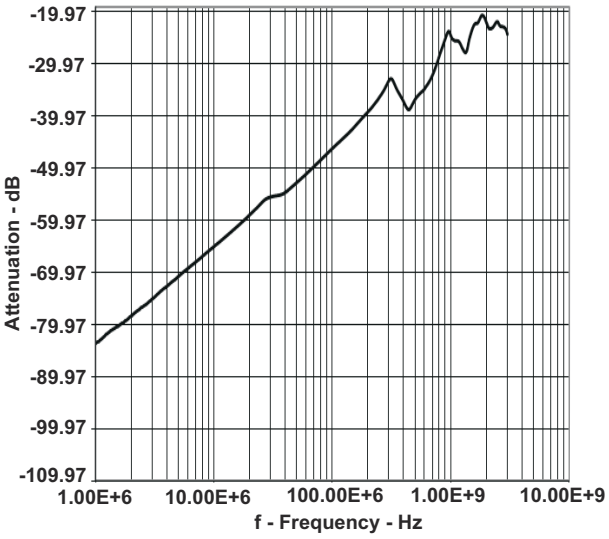


图 6-3. Crosstalk vs Frequency

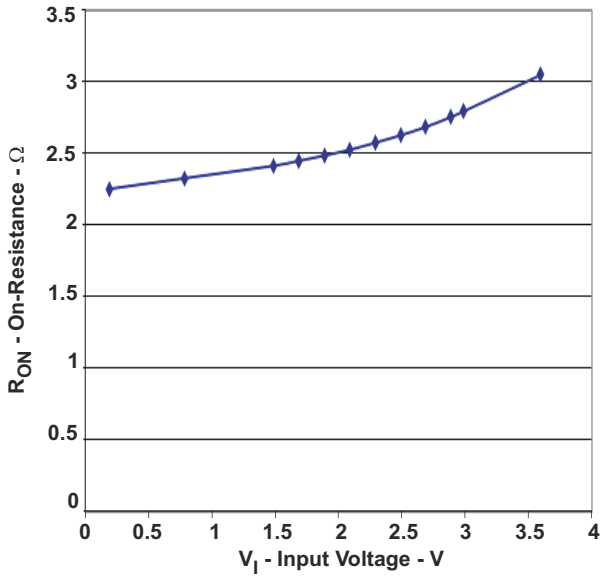
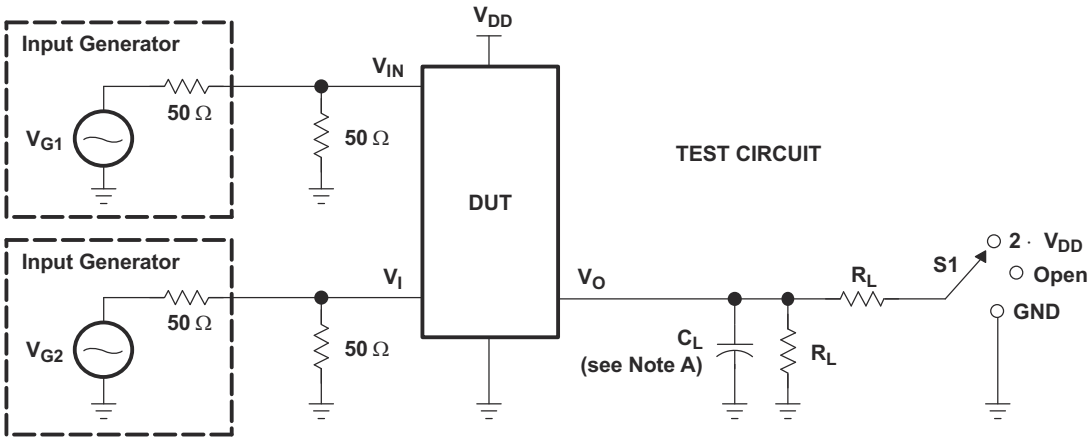


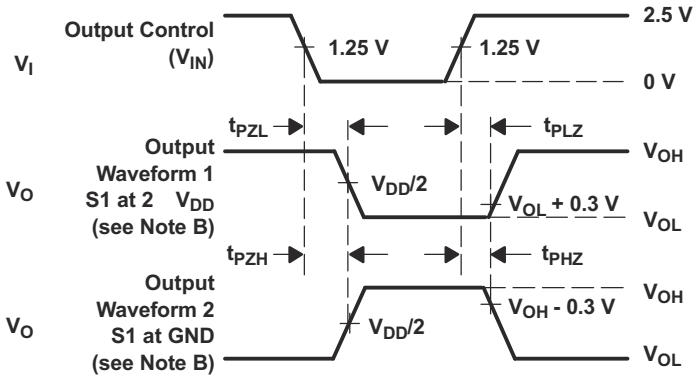
图 6-4. r_{on} (Ω) vs V_{com} (V)

7 Parameter Measurement Information

7.1 Enable and Disable Times



TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V	2 · V_{DD}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V

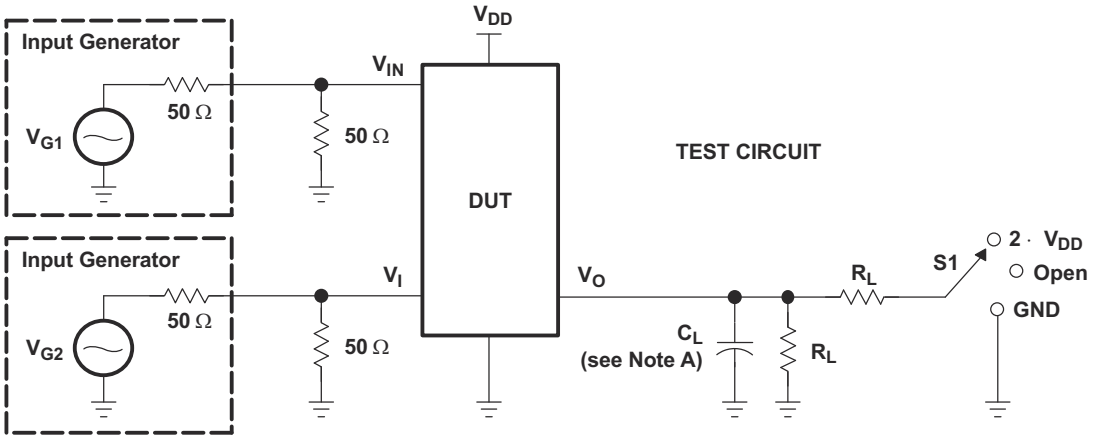


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

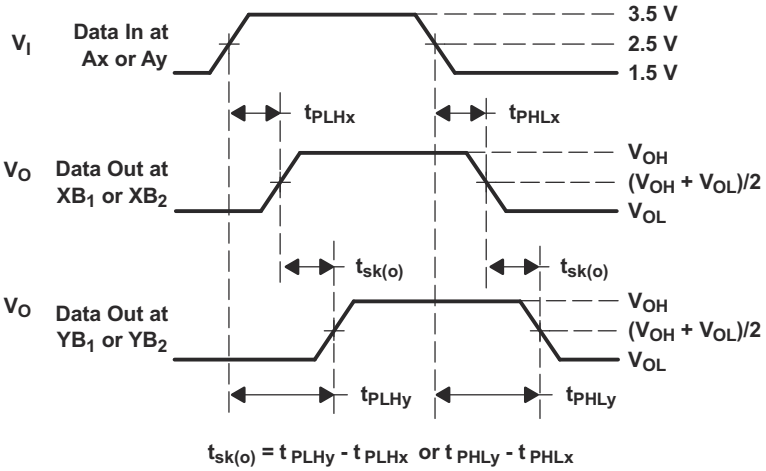
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

图 7-1. Test Circuit and Voltage Waveforms

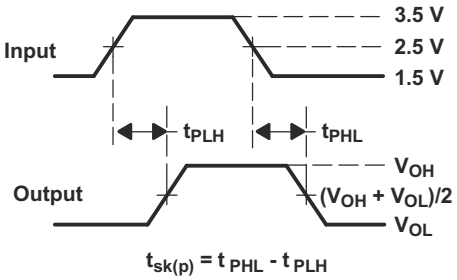
7.2 Skew



TEST	V_{DD}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF



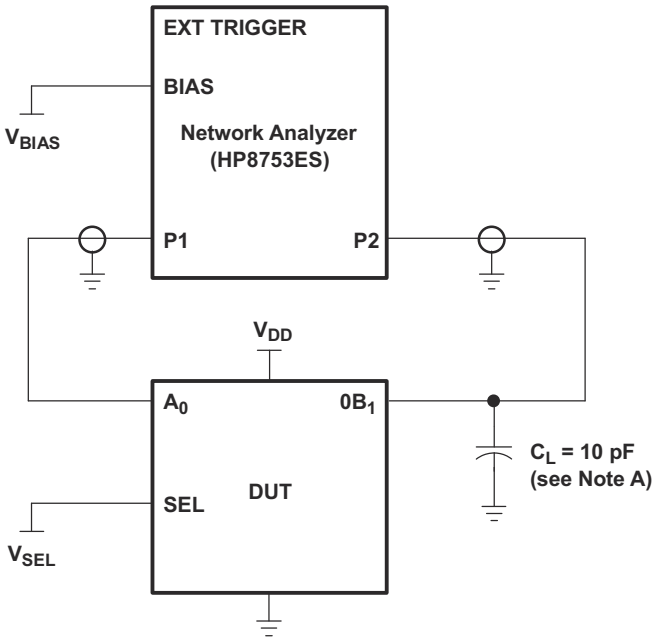
VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

图 7-2. Test Circuit and Voltage Waveforms



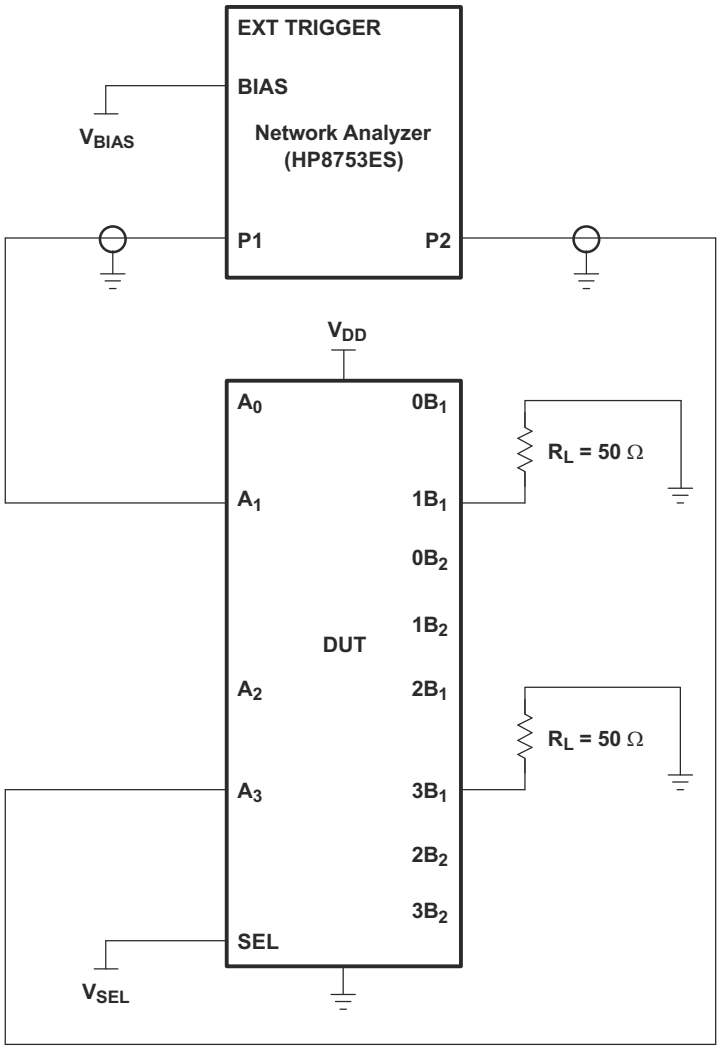
A. C_L includes probe and jig capacitance.

图 7-3. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

7.3 HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM



A. C_L includes probe and jig capacitance.

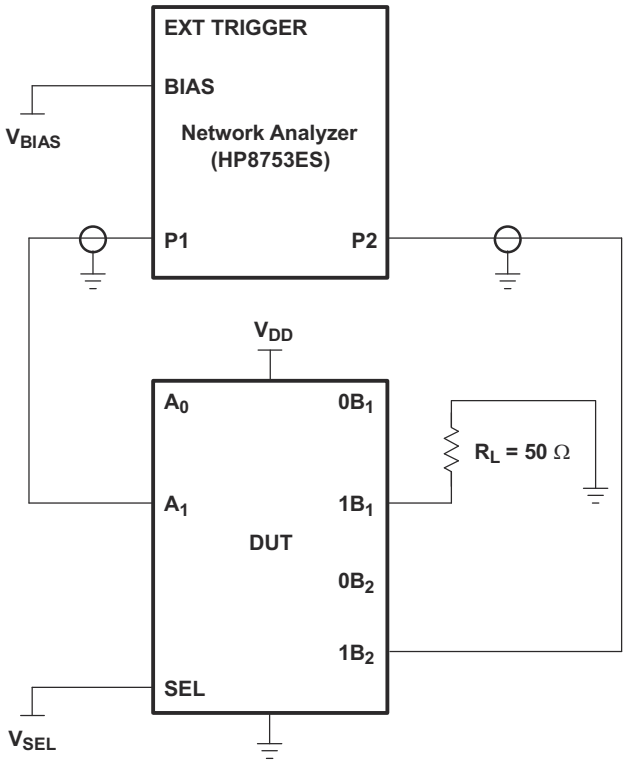
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

图 7-4. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

7.4 HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

图 7-5. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

7.5 HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

8 Detailed Description

8.1 Overview

The TS3L501E is a 11-channel SPDT analog switch or 22-bit to 11-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input and Power Down Mode input. The device provides additional I/Os for switching status indicating LED signals and includes high ESD protection. SEL input controls the data path of the multiplexer/demultiplexer. Power Down input can put the device into the standby mode for minimizing current consumption per mode selection.

The device provides a low and flat ON-state resistance (ron) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T. This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T Ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

8.2 Functional Block Diagram

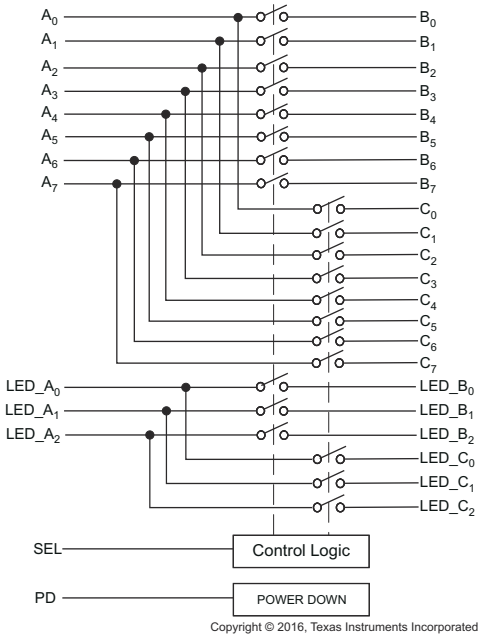


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The TS3L501E device switches and pin out are optimized for ethernet application but the device can used for many applications where a multi-channel, 1:2 SPDT, high bandwidth switch is needed.

8.4 Device Functional Modes

The TS3L501E supports a power down mode which reduces the current consumption of the device and places all the signal paths in a high impedance state. To place the TS3L501E in power down mode, set the PD pin with a logic high voltage as seen in 表 8-1.

表 8-1. Function Table

PD	SEL	FUNCTION
L	L	A_n to B_n, LED_A_n to LED_B_n
L	H	A_n to C_n, LED_A_n to LED_C_n
H	X	Hi-Z

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

There are many Local Area Network (LAN) applications in which the ethernet hubs or controllers have a limited number of I/Os or need to route signals from a single ethernet PHY to multiple ethernet jacks. The TS3L501E solution can effectively expand the limited I/Os by switching between multiple ethernet jacks to interface them to a single ethernet PHY.

The LED_A_n, LED_B_n,and LED_C_n pins are rated the same as the other signal path pins so you may use these pins as extra data paths if needed.

9.2 Typical Application

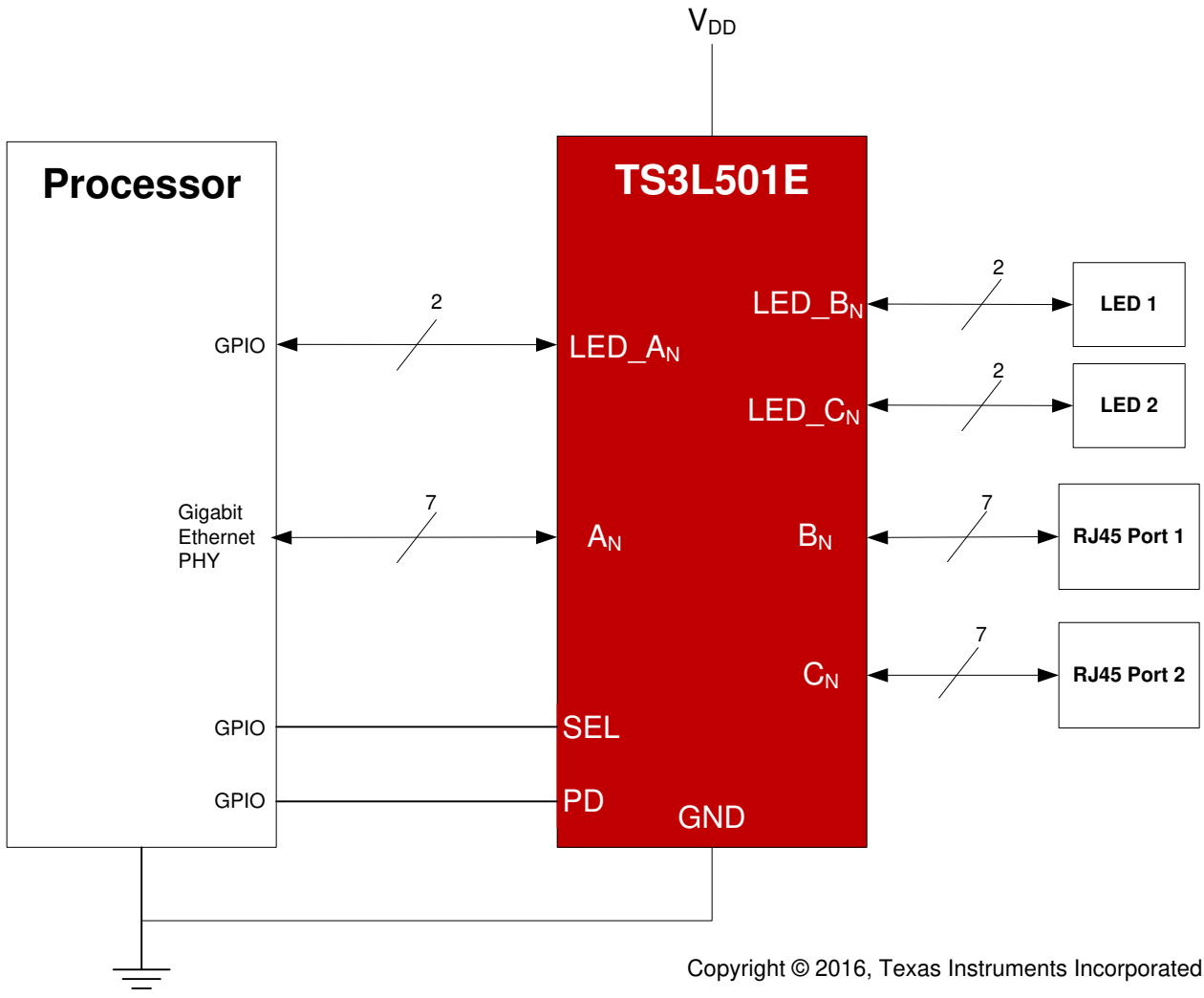


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the recommended operating ranges. To ensure proper performance, see *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

The TS3L501E can be properly operated without any external components.

TI recommends that the digital control pins SEL and PD be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

Connect the exposed thermal pad to ground.

9.2.3 Application Curves

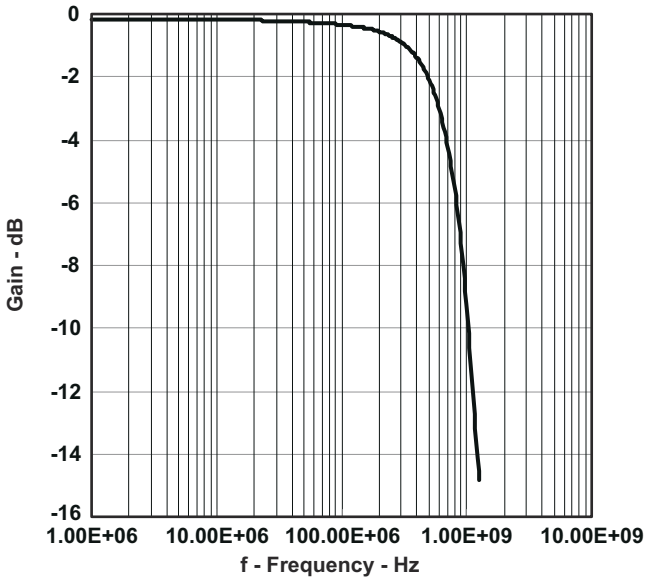


图 9-2. Gain vs Frequency

10 Power Supply Recommendations

Power to the device is supplied through the V_{DD} pins. TI recommends placing a bypass capacitor as close to the supply pin (VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

All V_{DD} pins are internally connected. One PCB layout option is to connect one of the V_{DD} to the power supply and leave the other V_{DD} pins open.

Supply the TS3L501E V_{DD} pins with the recommended voltage before appling a signal voltage to the I/O signal paths to avoid violating the recommended opperating condition I/O voltage 0-V_{DD}.

11 Layout

11.1 Layout Guidelines

- TI recommends keeping the high-speed signals as short as possible.
- Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
- Route all high-speed signal traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Due to high-frequency signals, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 11-1.
- The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

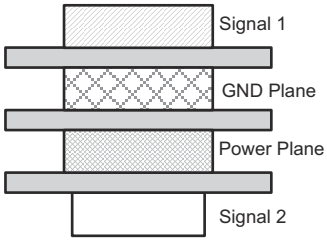


图 11-1. Four-Layer Board Stackup

11.2 Layout Example

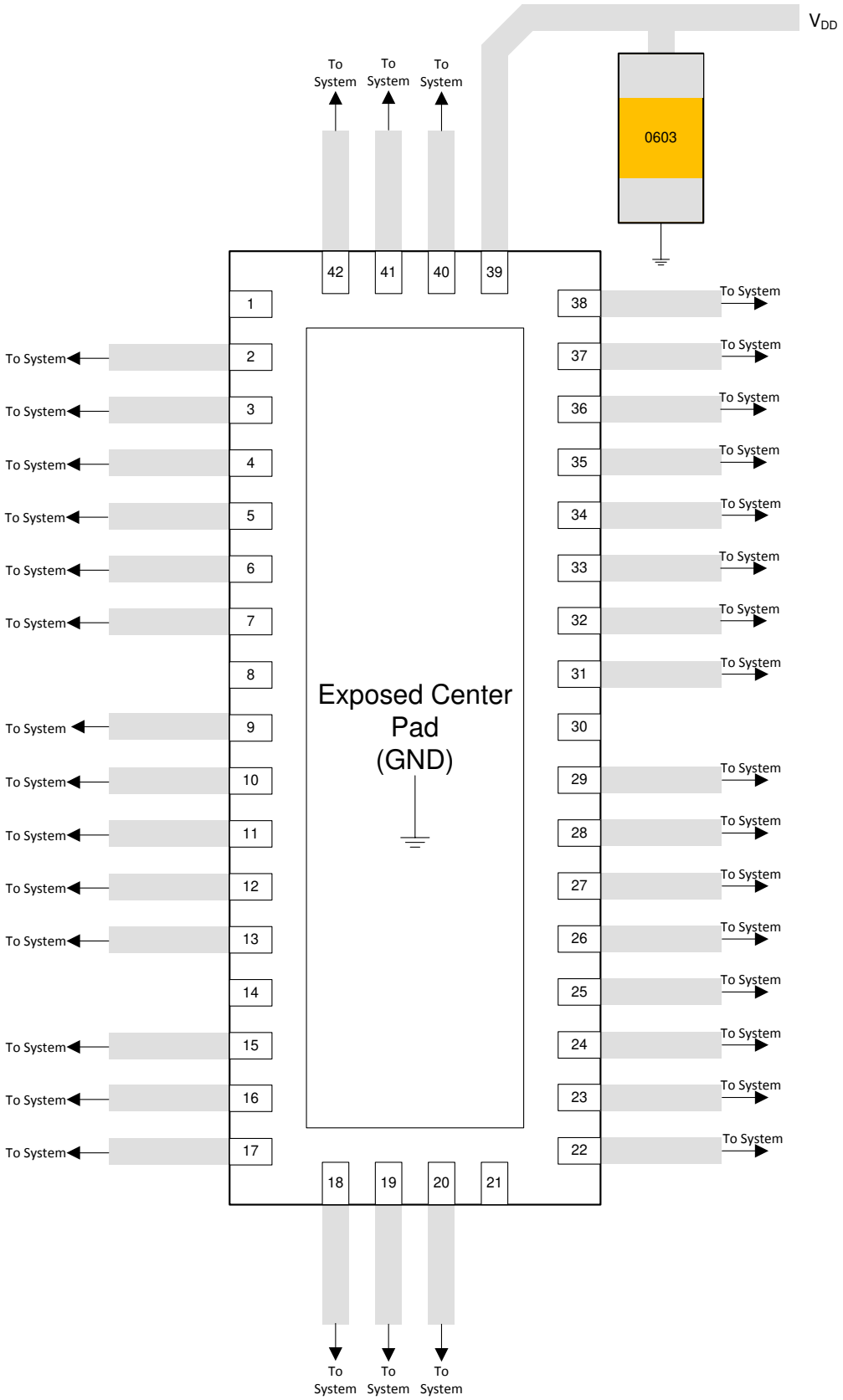


图 11-2. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

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所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3L501ERUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK501E
TS3L501ERUAR.B	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK501E
TS3L501ERUARG4	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK501E
TS3L501ERUARG4.B	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK501E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

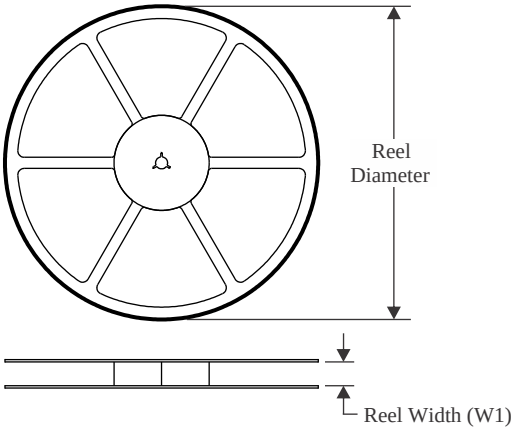
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

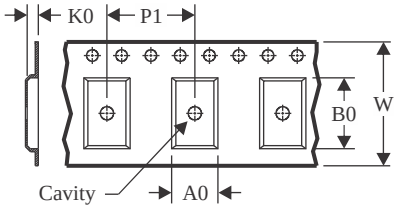
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

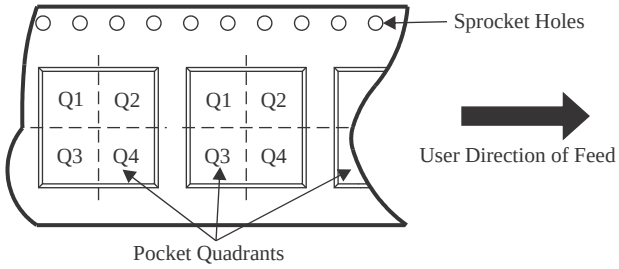


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

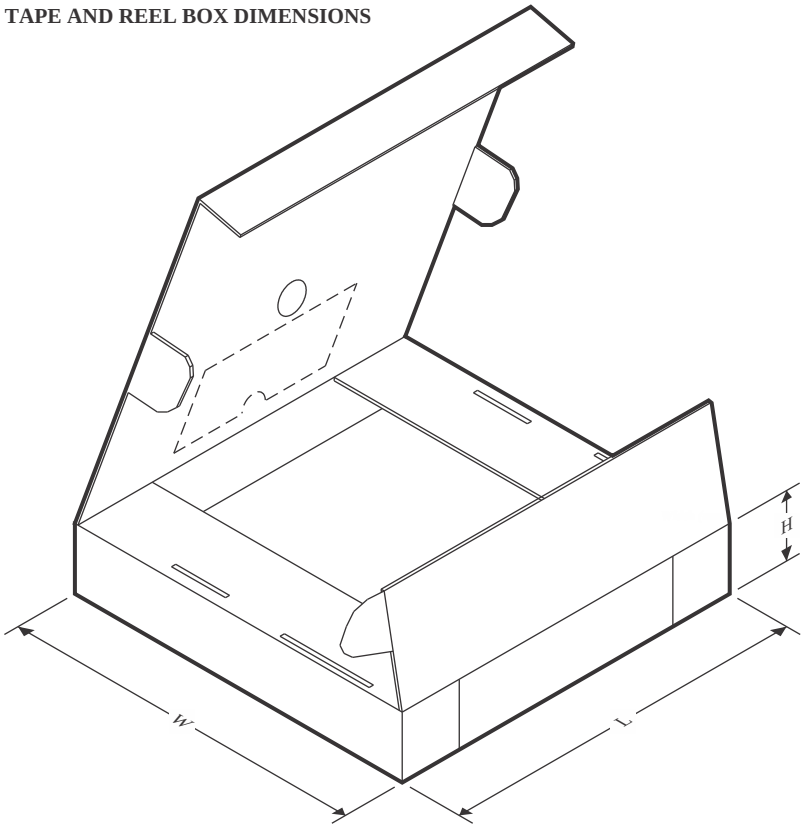
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L501ERUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3L501ERUARG4	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L501ERUAR	WQFN	RUA	42	3000	367.0	367.0	38.0
TS3L501ERUARG4	WQFN	RUA	42	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

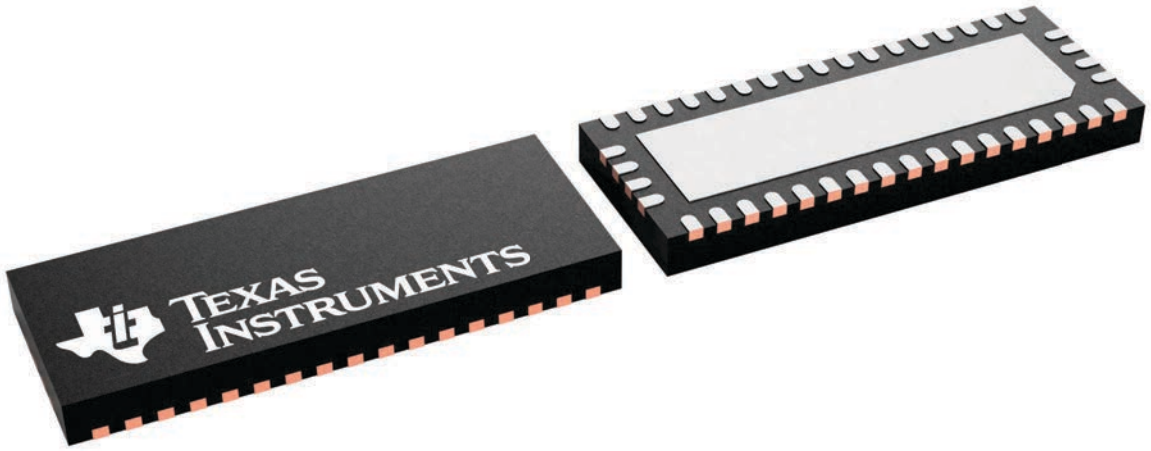
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

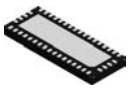
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



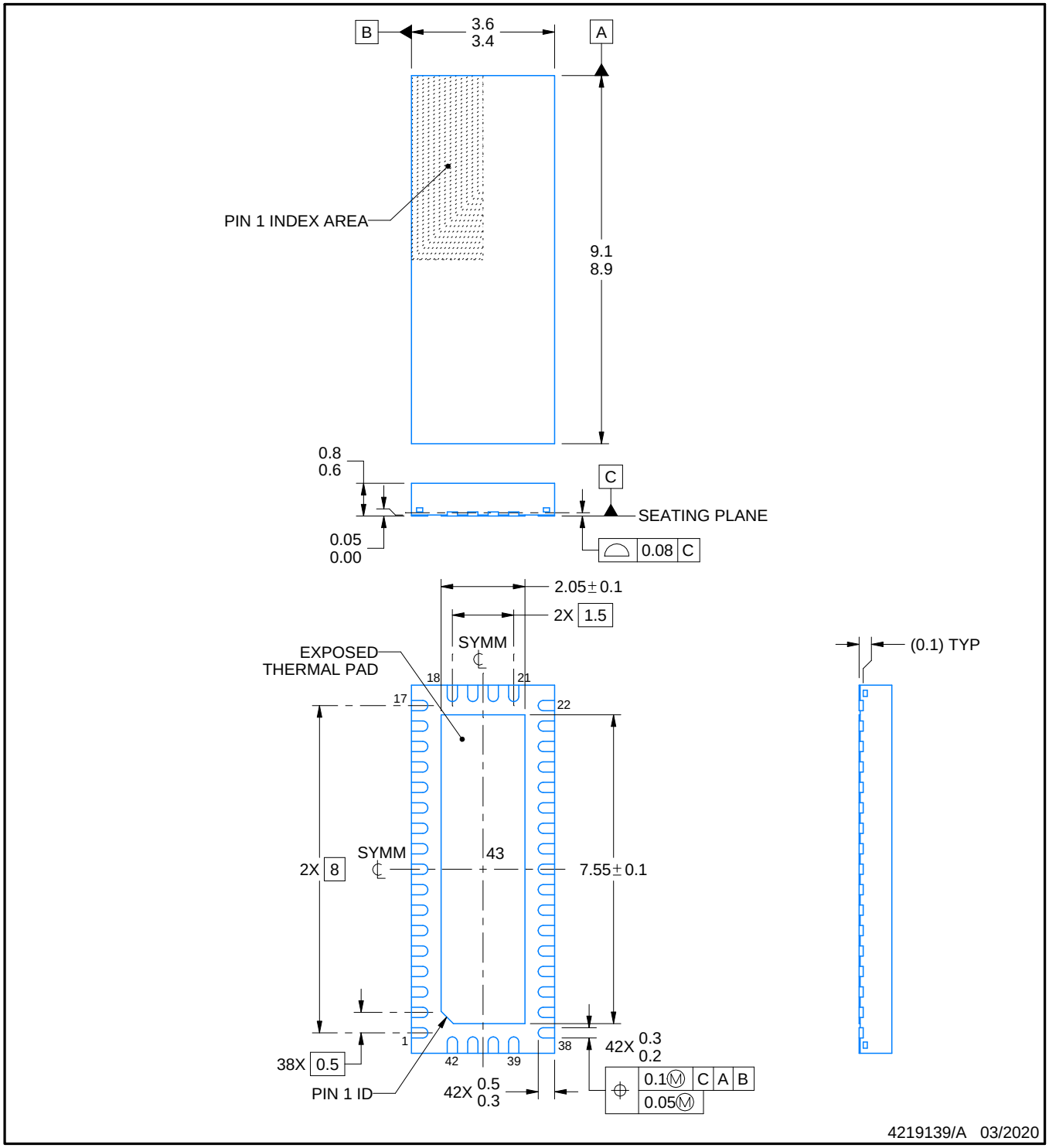
PACKAGE OUTLINE

RUA0042A



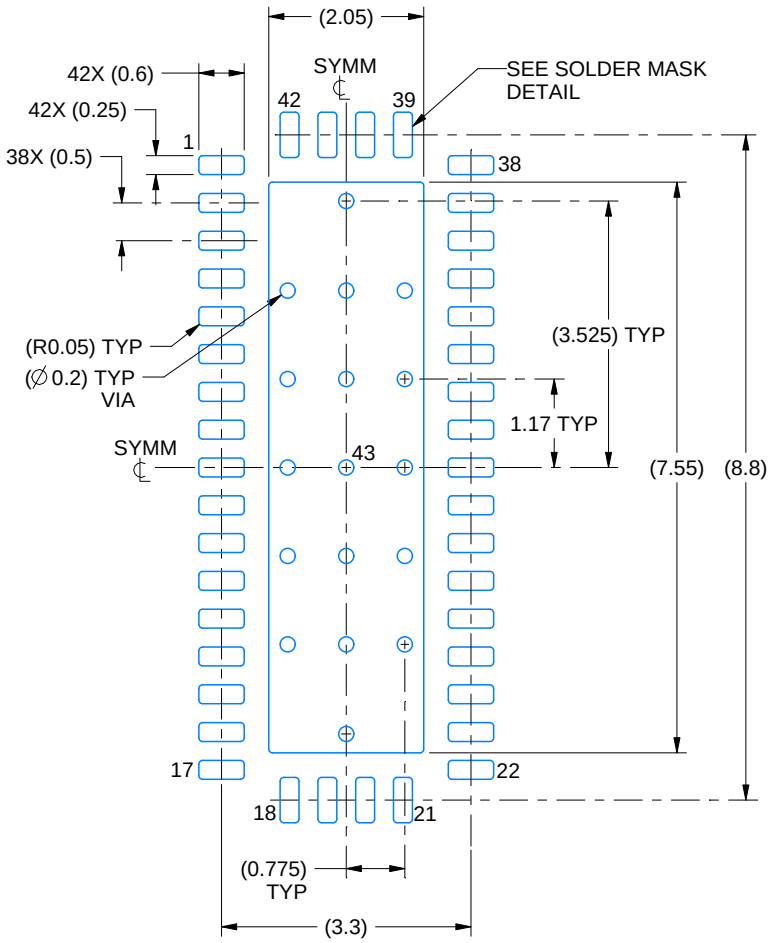
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

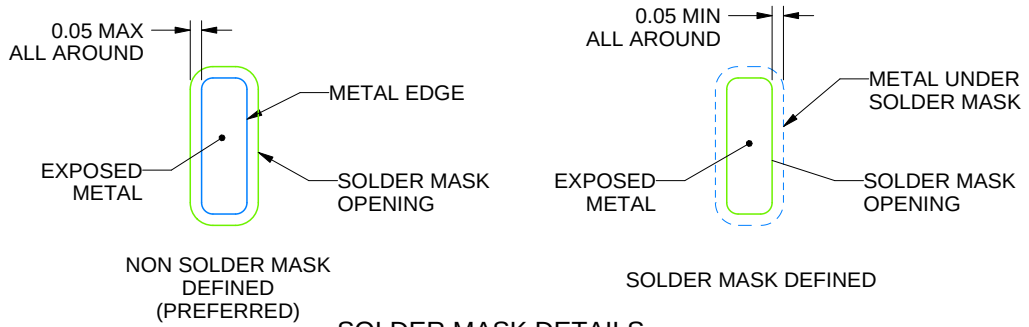


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

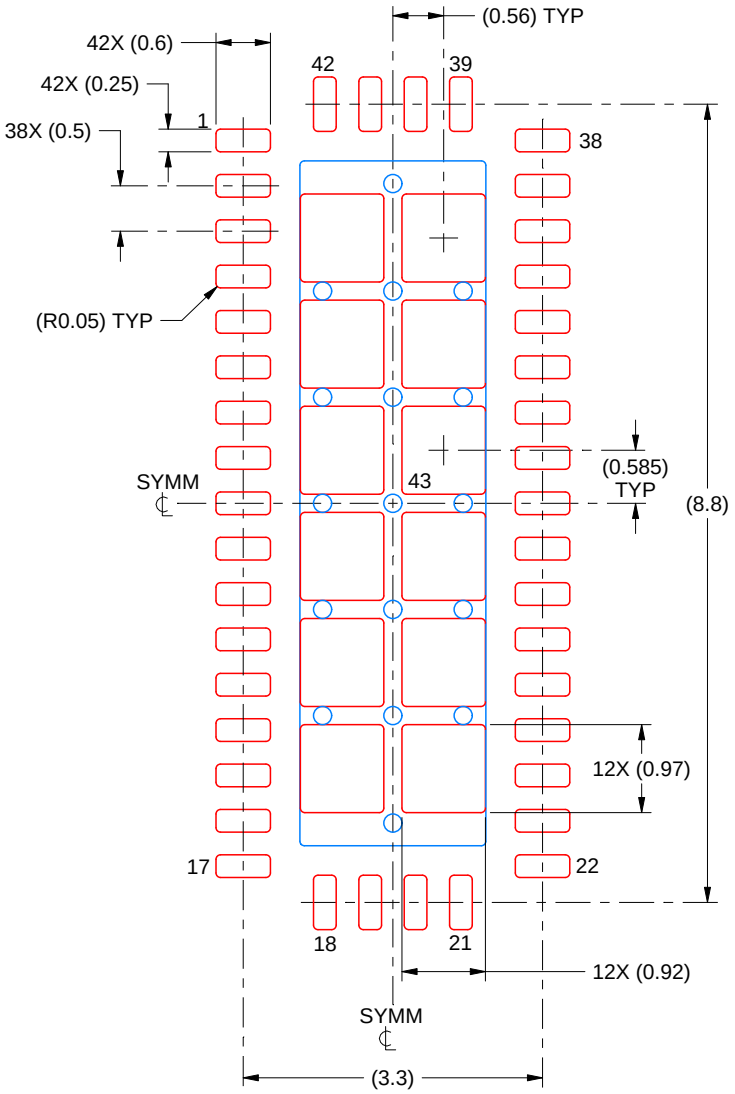
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月