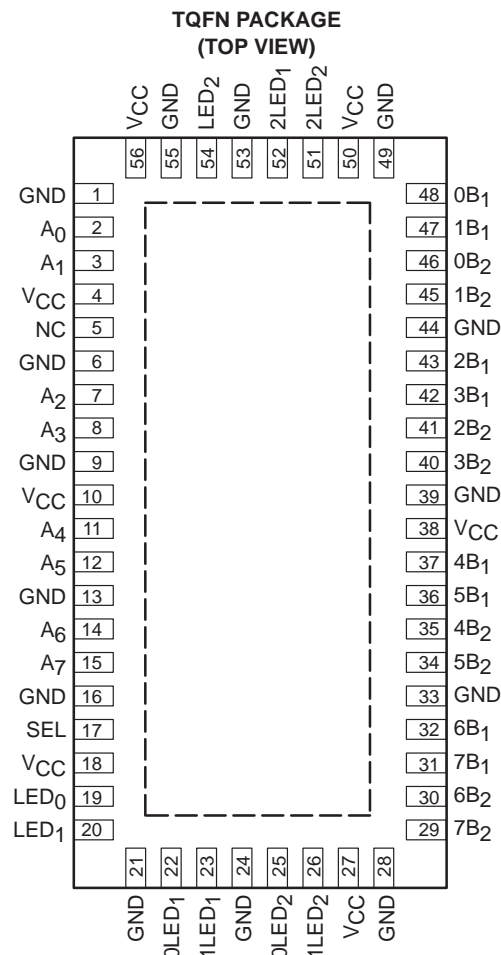


TS3L500

16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LED SWITCH

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- **Wide Bandwidth** (BW > 1100 MHz Typ)
- **Low Crosstalk** ($X_{TALK} = -37$ dB Typ)
- **Low Bit-to-Bit Skew** ($t_{sk(o)} = 100$ ps Max)
- **Low and Flat ON-State Resistance** ($r_{on} = 4 \Omega$ Typ, $r_{on(Flat)} = 0.5 \Omega$ Typ)
- **Low Input/Output Capacitance** ($C_{ON} = 8$ pF Typ)
- **Rail-to-Rail Switching on Data I/O Ports** (0 to 5 V)
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- **Applications**
 - 10/100/1000 Base-T Signal Switching
 - Differential (LVDS, LVPECL) Signal Switching
 - Audio/Video Switching
 - Hub and Router Signal Switching



description/ordering information

The TS3L500 is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides additional I/Os for switching status indicating LED signals.

The device provides a low and flat ON-state resistance (r_{on}) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TQFN	Tape and reel	TS3L500RHUR	TK500

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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WITH LED SWITCH

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FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT A_n	FUNCTION
L	nB_1	$A_n = nB_1, LED_x = XLED_1$
H	nB_2	$A_n = nB_2, LED_x = XLED_2$

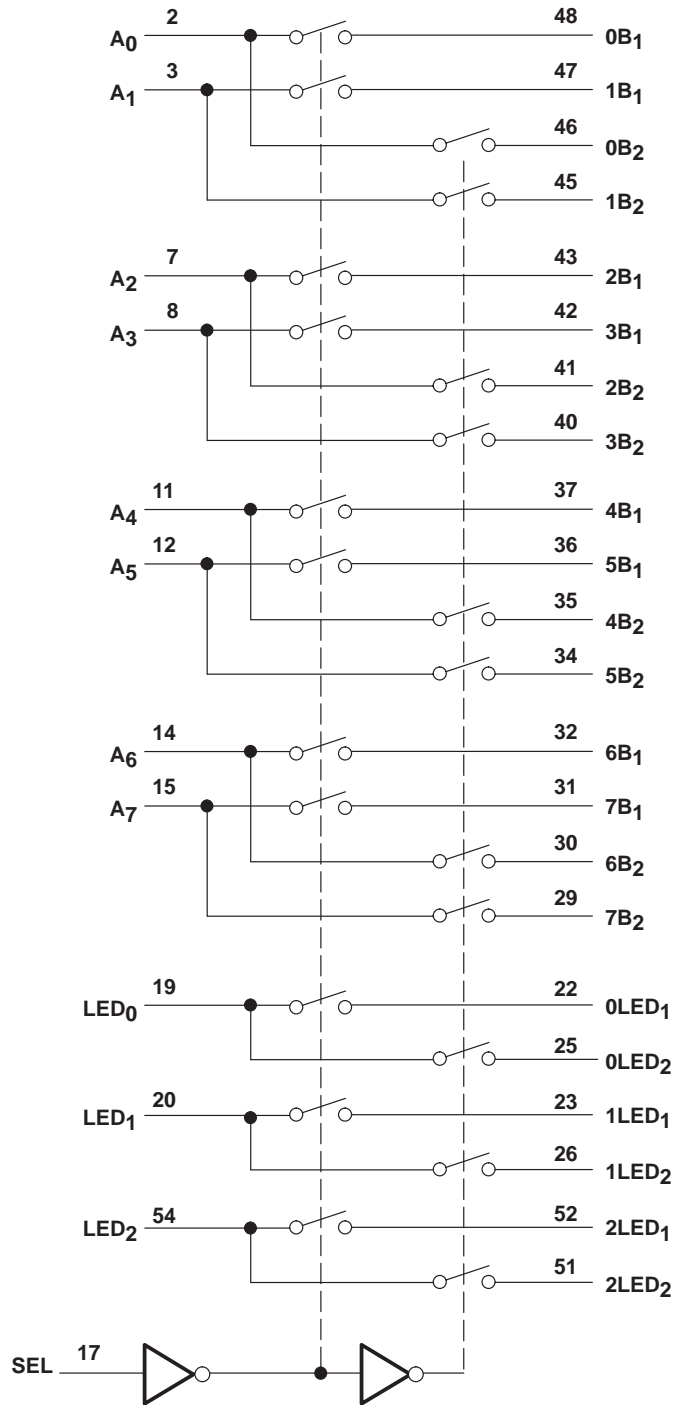
PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Data I/O
nB_m	Data I/O
SEL	Select input
LED_x	LED I/O port
$XLED_m$	LED I/O port

TS3L500 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LED SWITCH

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	-50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	± 128 mA
Continuous current through V_{CC} or GND terminals	± 100 mA
Package thermal impedance, θ_{JA} (see Note 5)	31.8°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics for 1000 Base-T ethernet switching over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)[†]

PARAMETER		TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IK}	SEL	$V_{CC} = 3.6\text{ V}$, $I_{IN} = -18\text{ mA}$	-0.7	-1.2		V
I_{IH}	SEL	$V_{CC} = 3.6\text{ V}$, $V_{IN} = V_{CC}$			± 1	μA
I_{IL}	SEL	$V_{CC} = 3.6\text{ V}$, $V_{IN} = \text{GND}$			± 1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF		250	500	μA
C_{IN}	SEL	$f = 1\text{ MHz}$, $V_{IN} = 0$		2	2.5	pF
C_{OFF}	B port	$V_I = 0$, $f = 1\text{ MHz}$, Outputs open, Switch OFF		2.5	4	pF
C_{ON}		$V_I = 0$, $f = 1\text{ MHz}$, Outputs open, Switch ON		8	9	pF
r_{on}		$V_{CC} = 3\text{ V}$, $1.5\text{ V} \leq V_I \leq V_{CC}$, $I_O = -40\text{ mA}$		4	6	Ω
$r_{on(\text{flat})}$ [§]		$V_{CC} = 3\text{ V}$, $V_I = 1.5\text{ V}$ and V_{CC} , $I_O = -40\text{ mA}$		0.5		Ω
Δr_{on} [¶]		$V_{CC} = 3\text{ V}$, $1.5\text{ V} \leq V_I \leq V_{CC}$, $I_O = -40\text{ mA}$		0.4	1	Ω

[†] V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[§] $r_{on(\text{flat})}$ is the difference of r_{on} in a given channel at specified voltages.

[¶] Δr_{on} is the difference of r_{on} from center (A4, A5) ports to any other port.

electrical characteristics for 10/100 Base-T ethernet switching over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)[†]

PARAMETER		TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IK}	SEL	$V_{CC} = 3.6\text{ V}$, $I_{IN} = -18\text{ mA}$	-0.7	-1.2		V
I_{IH}	SEL	$V_{CC} = 3.6\text{ V}$, $V_{IN} = V_{CC}$			± 1	μA
I_{IL}	SEL	$V_{CC} = 3.6\text{ V}$, $V_{IN} = \text{GND}$			± 1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF		250	500	μA
C_{IN}	SEL	$f = 1\text{ MHz}$, $V_{IN} = 0$		2	2.5	pF
C_{OFF}	B port	$V_I = 0$, $f = 1\text{ MHz}$, Outputs open, Switch OFF		2.5	4	pF
C_{ON}		$V_I = 0$, $f = 1\text{ MHz}$, Outputs open, Switch ON		8		pF
r_{on}		$V_{CC} = 3\text{ V}$, $1.25\text{ V} \leq V_I \leq V_{CC}$, $I_O = -10\text{ mA}$ to -30 mA		4	6	Ω
$r_{on(\text{flat})}$ [§]		$V_{CC} = 3\text{ V}$, $V_I = 1.25\text{ V}$ and V_{CC} , $I_O = -10\text{ mA}$ to -30 mA		0.5		Ω
Δr_{on} [¶]		$V_{CC} = 3\text{ V}$, $1.25\text{ V} \leq V_I \leq V_{CC}$, $I_O = -10\text{ mA}$ to -30 mA		0.4	1	Ω

[†] V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[§] $r_{on(\text{flat})}$ is the difference of r_{on} in a given channel at specified voltages.

[¶] Δr_{on} is the difference of r_{on} from center (A4, A5) ports to any other port.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $R_L = 200\ \Omega$, $C_L = 10\text{ pF}$ (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{pd}‡$	A or B	B or A		0.25		ns
t_{PZH} , t_{PZL}	SEL	A or B	0.5		15	ns
t_{PHZ} , t_{PLZ}	SEL	A or B	0.9		9	ns
$t_{sk(o)}§$	A or B	B or A		50	100	ps
$t_{sk(p)}¶$				50	150	ps

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

§ Output skew between center port (A₄ to A₅) to any other port

¶ Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

dynamic characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP†	UNIT
X _{TALK}	$R_L = 100\ \Omega$, $f = 250\text{ MHz}$, See Figure 8	-37	dB
O _{IRR}	$R_L = 100\ \Omega$, $f = 250\text{ MHz}$, See Figure 9	-37	dB
BW	$R_L = 100\ \Omega$, See Figure 7	1100	MHz

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.



OPERATING CHARACTERISTICS

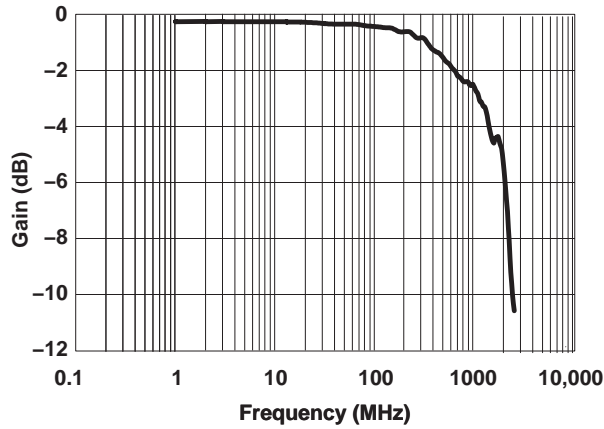


Figure 1. Gain vs Frequency

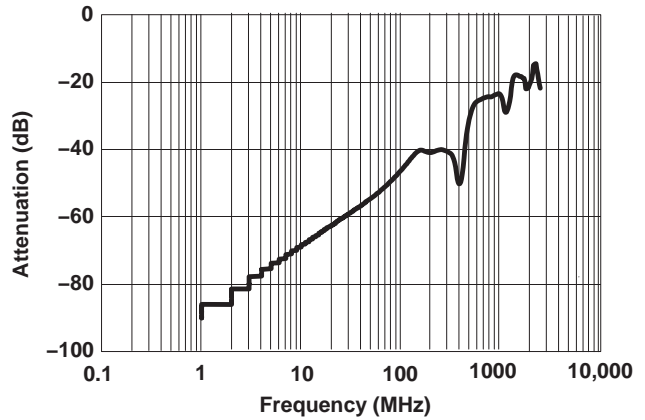


Figure 2. OFF Isolation vs Frequency

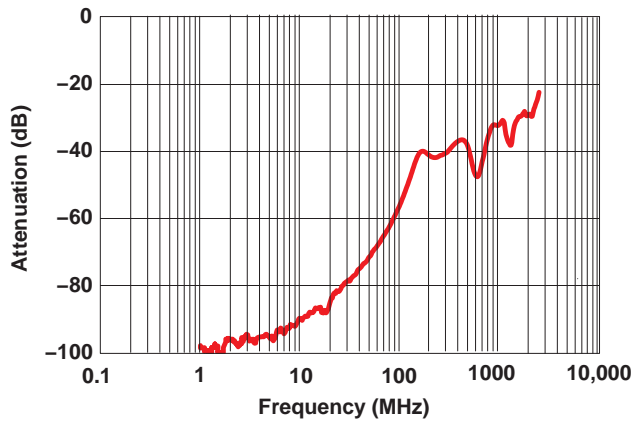


Figure 3. Crosstalk vs Frequency

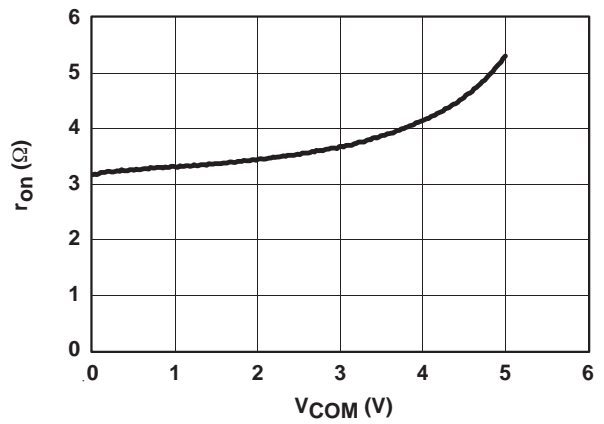
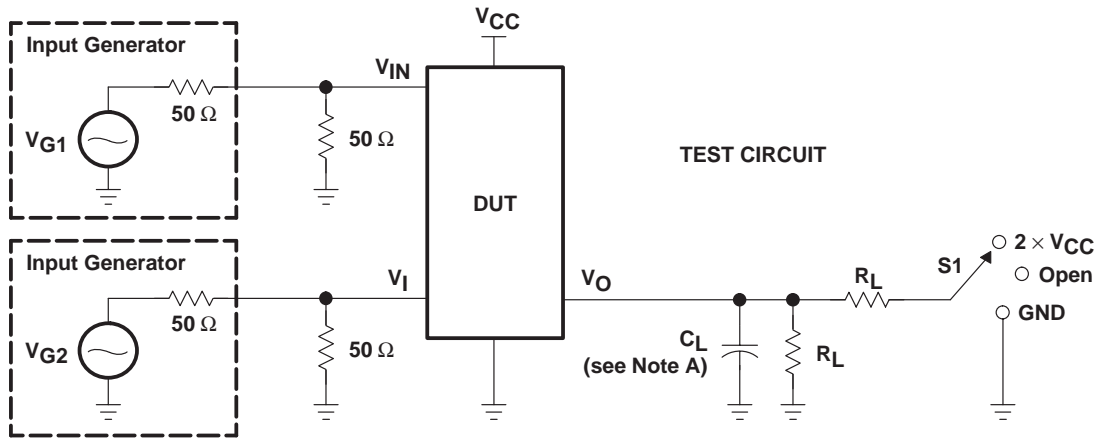


Figure 4. r_{on} (Ω) vs V_{com} (V)

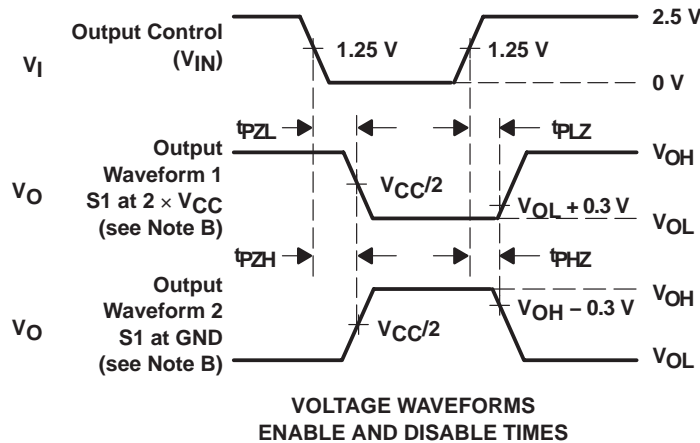
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16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH
WITH LED SWITCH

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PARAMETER MEASUREMENT INFORMATION
Enable and Disable Times



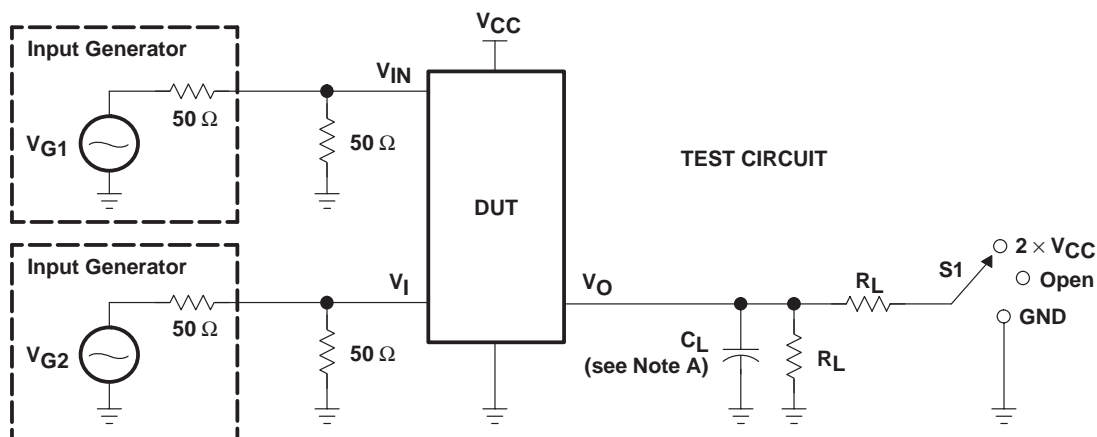
TEST	V _{CC}	S1	R _L	V _{in}	C _L	V _Δ
t _{PLZ} /t _{PZL}	3.3 V ± 0.3 V	2 × V _{CC}	200 Ω	GND	10 pF	0.3 V
t _{PHZ} /t _{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V _{CC}	10 pF	0.3 V



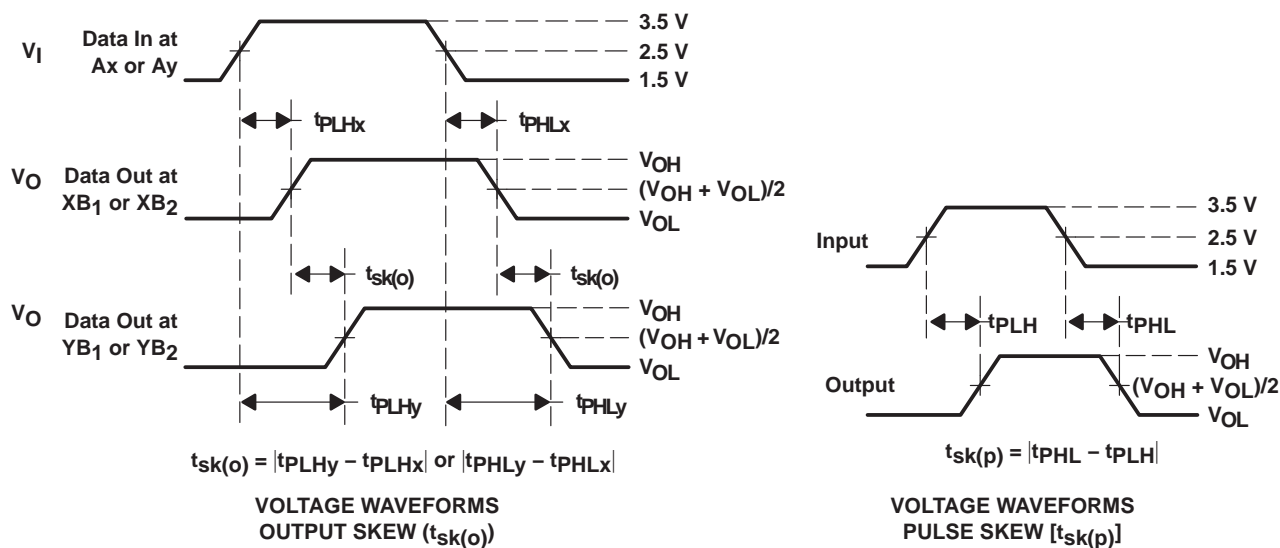
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
Skew



TEST	VCC	S1	RL	Vin	CL
t _{sk(o)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF
t _{sk(p)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF



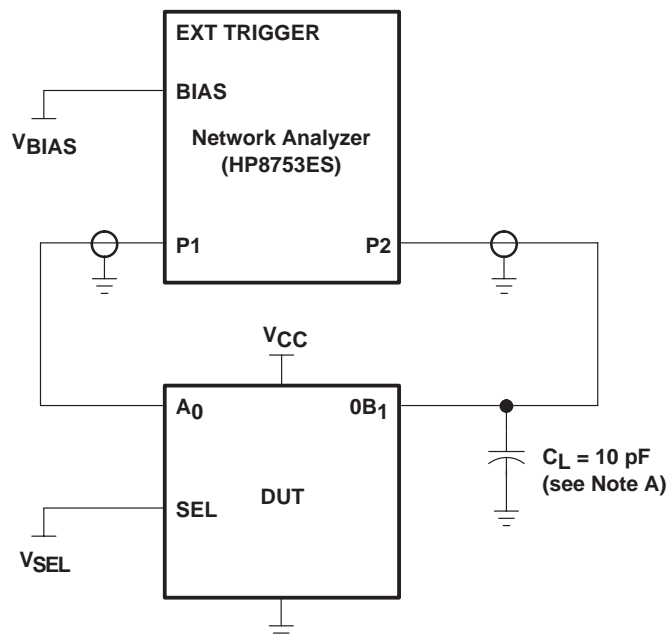
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

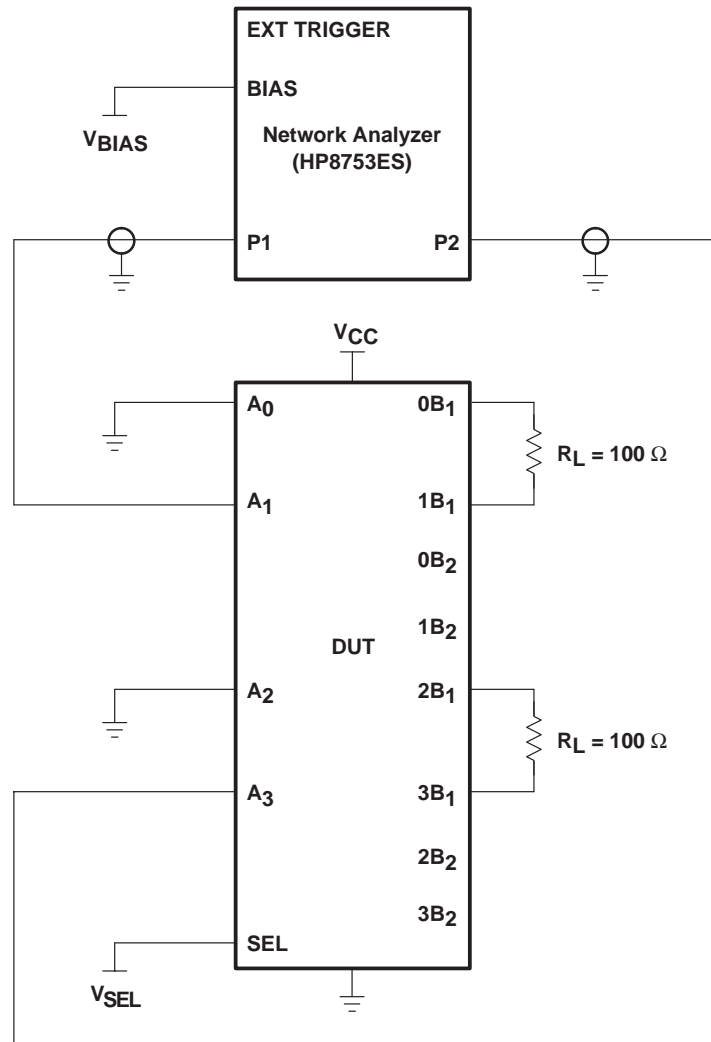
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at OB_1 . All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50- Ω pulldown resistors.

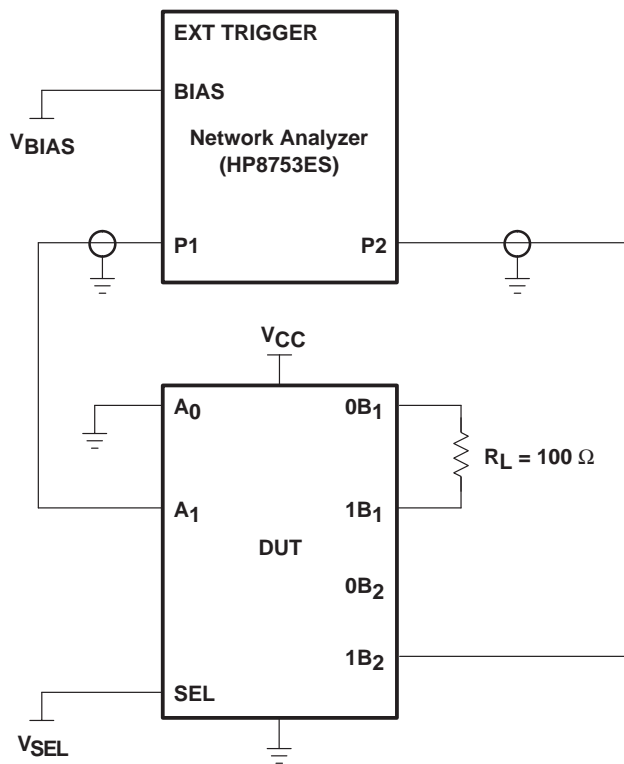
HP8753ES setup

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35$ V
- ST = 2 s
- P1 = 0 dBm

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = V_{CC}$ and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50- Ω pull-down resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3L500RHUR	Active	Production	WQFN (RHU) 56	2000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK500
TS3L500RHUR.B	Active	Production	WQFN (RHU) 56	2000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK500

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L500RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

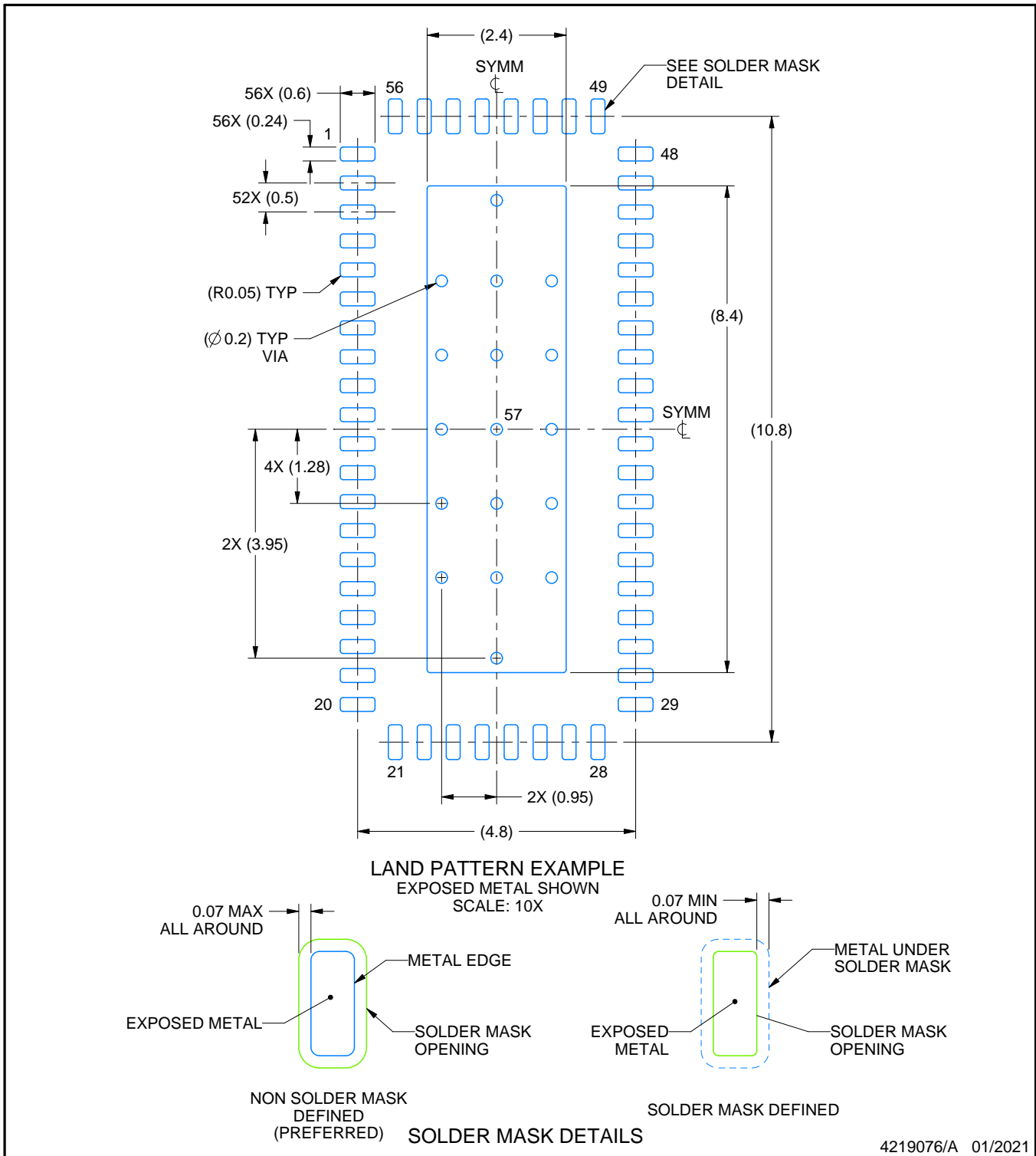
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L500RHUR	WQFN	RHU	56	2000	346.0	346.0	35.0

EXAMPLE BOARD LAYOUT

RHU0056A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

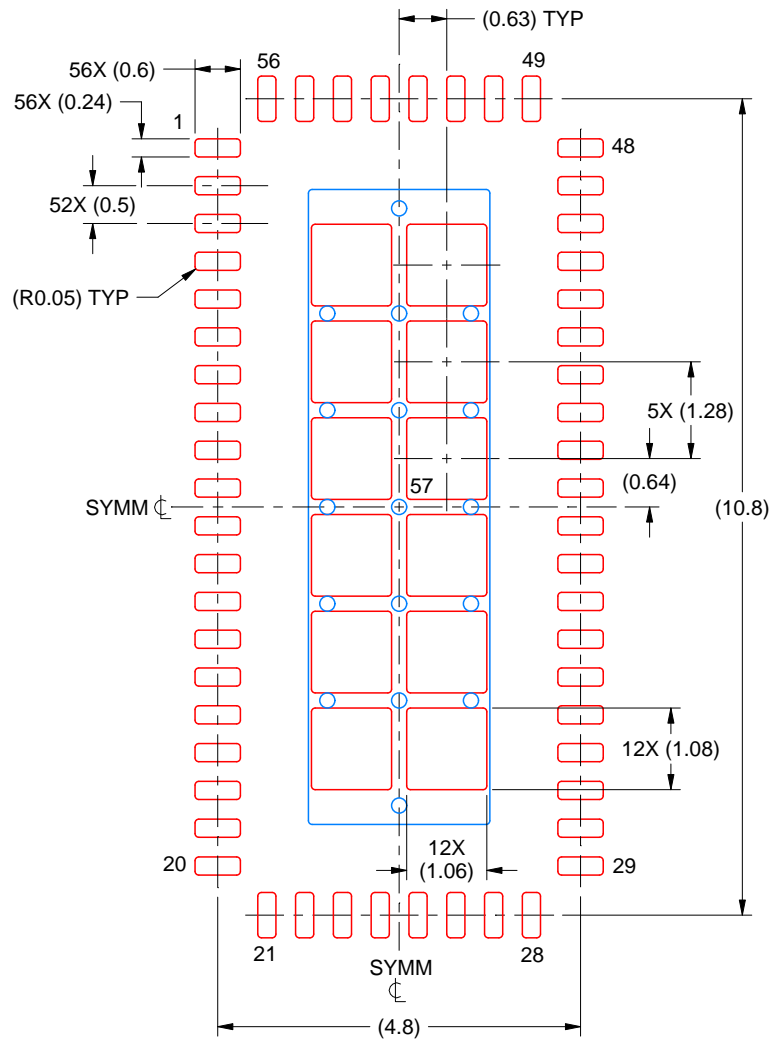
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHU0056A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 10X

EXPOSED PAD 57
 68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219076/A 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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