

## TS3A5223 0.45Ω 双通道 SPDT 双向模拟开关

### 1 特性

- 低导通电阻开关
  - 电压为 3.6V 时为 0.45Ω（典型值）
  - 电压为 1.8V 时为 0.85Ω（典型值）
- 宽电源电压：1.65V 至 3.6V
- 1.0V 兼容逻辑接口
- 高切换带宽 80MHz
- 在整个波段上，总谐波失真 (THD) 为 0.01%
- 额定最小先开后合
- 双向切换
- 75dB 通道至通道串扰
- 具有极低功率耗散和泄漏电流的 -70dB 通道至通道关闭隔离
- 极小型 QFN-10 封装：1.8mm x 1.4mm
- 针对所有引脚的 ESD 保护
  - 2kV HBM, 500V CDM

### 2 应用

- 便携式电子产品
- 智能手机、平板电脑
- 家用电器
- 有线通信

### 3 说明

TS3A5223 是一款高速双通道模拟开关，此开关具有先断后通以及双向信号切换功能。TS3A5223 可被用作一个双路 2:1 复用器或者一个 1:2 双路去复用器。

TS3A5223 提供极低的导通电阻、很低的 THD 和通道间串扰以及很高的关闭隔离。这些特性使得 TS3A5223 适用于音频信号传输和切换应用。

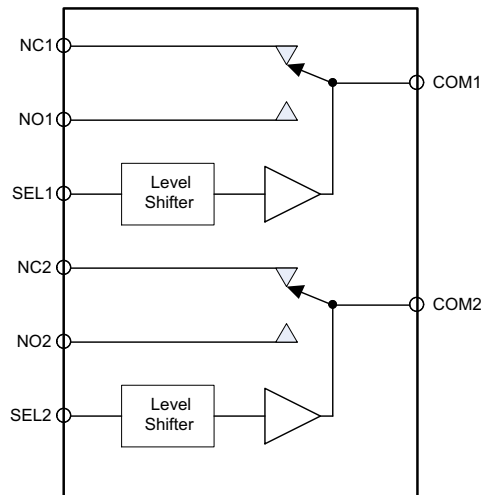
TS3A5223 控制逻辑支持 1V - 3.6V CMOS 逻辑电平。此逻辑接口可在不增加电源输出电流 ( $I_{CC}$ ) 的前提下实现与各种 CPU 和微控制器的直接对接，从而降低了功耗。

器件信息<sup>(1)</sup>

| 器件型号     | 封装        | 封装尺寸（标称值）       |
|----------|-----------|-----------------|
| TS3A5223 | μQFN (10) | 1.80mm x 1.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能图



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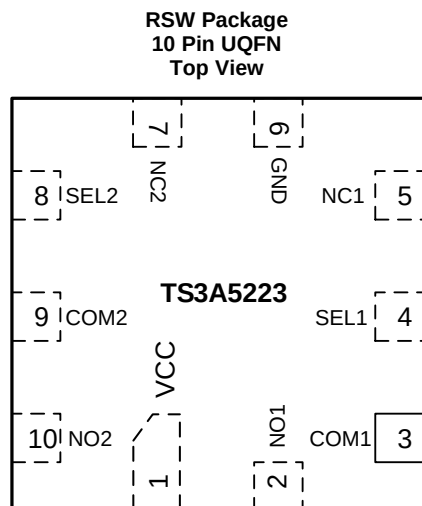
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| <b>Changes from Revision A (February 2013) to Revision B</b>                                                           | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------|-------------|
| • 添加了器件信息表、ESD 额定值表、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....                            | <b>1</b>    |
| • Changed the $V_{MAX}$ MAX value From: 3.6 V To: $V_{CC}$ in the <i>Recommended Operating Conditions</i> table .....  | <b>4</b>    |
| • Deleted: "dt/dv, SEL pin Input rise and fall time limit" from the <i>Recommended Operating Conditions</i> table..... | <b>4</b>    |
| • Deleted the Dissipation Ratings table.....                                                                           | <b>4</b>    |

| <b>Changes from Original (January 2013) to Revision A</b> | <b>Page</b> |
|-----------------------------------------------------------|-------------|
| • 将器件状态从“预览”更改为“生产” .....                                 | <b>1</b>    |

## 5 Pin Configuration and Functions



**Pin Functions**

| NAME       | PIN NUMBER | DESCRIPTION                                                                           |
|------------|------------|---------------------------------------------------------------------------------------|
| VCC        | 1          | Positive supply Input – Connect 1.65 V to 3.6 V supply voltage                        |
| NC1        | 5          | Signal path Input/Output signal pins                                                  |
| NO1        | 2          |                                                                                       |
| NC2        | 7          |                                                                                       |
| NO2        | 10         |                                                                                       |
| COM1, COM2 | 3, 9       | Common signal path Input/Output signal pins                                           |
| GND        | 6          | Ground reference pin                                                                  |
| SEL1, SEL2 | 4, 8       | Select digital logic pin. Logic low connects COM to NC, Logic high connects COM to NO |

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

Specified at  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise noted.

|                                                        |                                                            |             | VALUE |                    | UNIT |
|--------------------------------------------------------|------------------------------------------------------------|-------------|-------|--------------------|------|
|                                                        |                                                            |             | MIN   | MAX                |      |
| V <sub>CC</sub>                                        | Positive DC supply voltage                                 |             | −0.3  | 4.3 <sup>(2)</sup> | V    |
| V <sub>COM</sub><br>V <sub>NO</sub><br>V <sub>NC</sub> | Analog voltage                                             |             | −0.3  | 4.3 <sup>(2)</sup> | V    |
| I <sub>COM</sub><br>I <sub>NO</sub><br>I <sub>NC</sub> | On-state switch continuous current                         |             |       | ±300               | mA   |
| I <sub>COM</sub><br>I <sub>NO</sub><br>I <sub>NC</sub> | On-state switch peak current (1ms pulse at 10% duty cycle) |             |       | ±500               | mA   |
| P <sub>D</sub>                                         | Total device power dissipation at<br>T <sub>A</sub> = 85°C | 10-μQFN RSW |       | 430                | mW   |
| T <sub>A</sub>                                         | Operating free-air ambient temperature range               |             | −40   | 85                 | °C   |
| T <sub>J</sub>                                         | Junction temperature range                                 |             | −55   | 150                | °C   |
| T <sub>stg</sub>                                       | Storage temperature range                                  |             | −55   | 150                | °C   |

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Not rated for continuous operation, 0.5% duty cycle at 1 kHz recommended

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                         |                                              | MIN  | MAX             | UNIT |
|---------------------------------------------------------|----------------------------------------------|------|-----------------|------|
| V <sub>CC</sub>                                         | Positive DC supply voltage                   | 1.65 | 3.6             | V    |
| V <sub>COM</sub> , V <sub>NO</sub> ,<br>V <sub>NC</sub> | Analog voltage range                         | 0    | V <sub>CC</sub> | V    |
| V <sub>SEL1</sub><br>V <sub>SEL2</sub>                  | Digital logic voltage                        | 0    | V <sub>CC</sub> | V    |
| T <sub>A</sub>                                          | Operating free-air ambient temperature range | −40  | 85              | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TS3A5223   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RSW (UQFN) |      |
|                               |                                              | 10 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 92.5       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 46.0       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 44.5       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 1.5        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 44.5       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 31.2       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

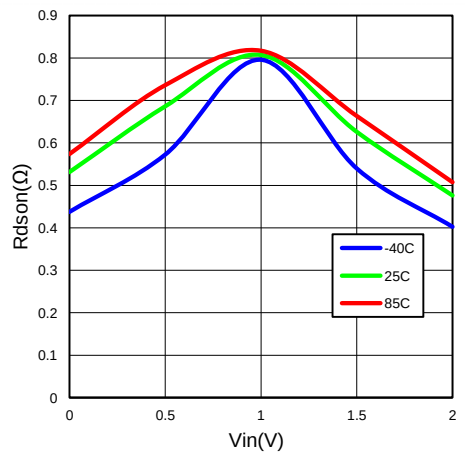
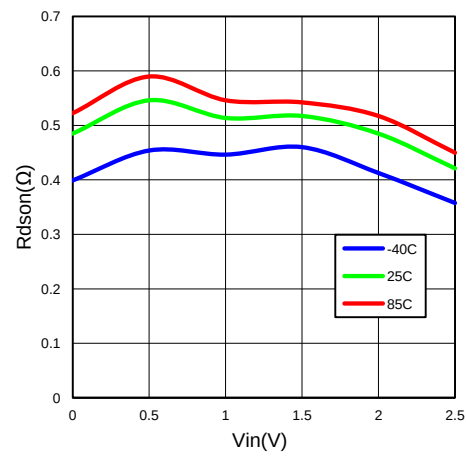
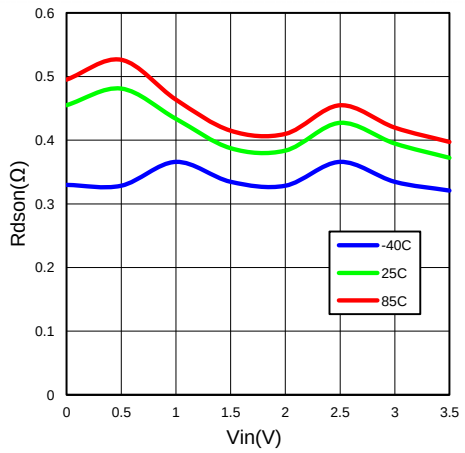
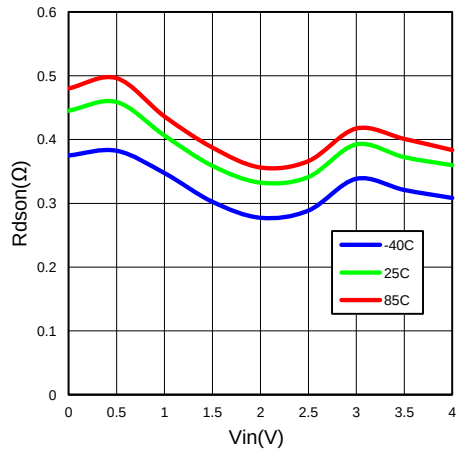
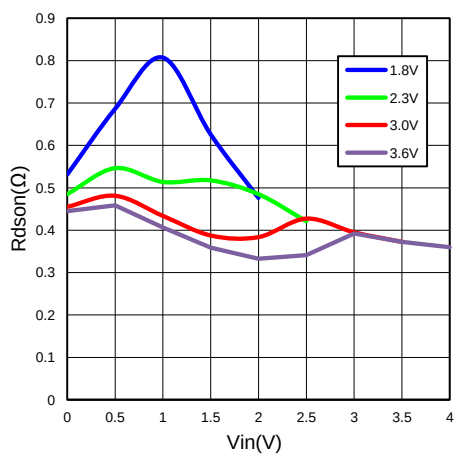
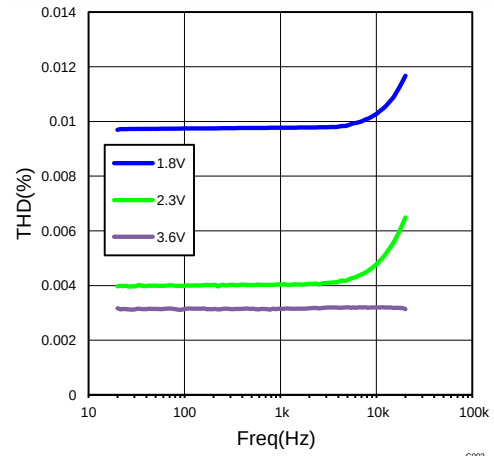
## 6.5 Electrical Characteristics

Specified over the recommended junction temperature range  $T_A = T_J = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Typical values are at  $T_A = T_J = 25^{\circ}\text{C}$  (unless otherwise noted).

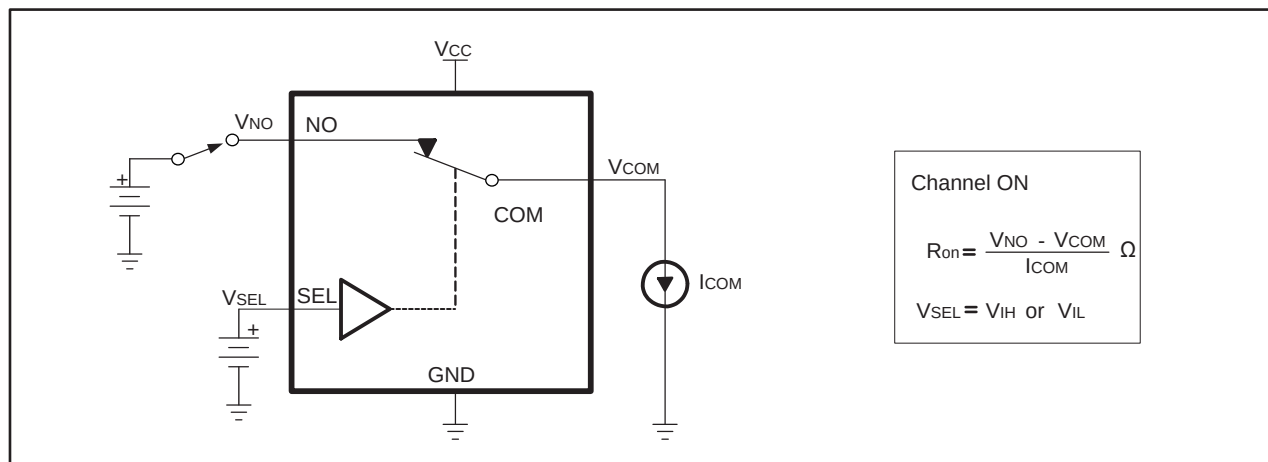
| PARAMETER                                     |                                                      | $V_{CC}$ (V) | TEST CONDITIONS                                                         | MIN | TYP   | MAX  | UNIT     |
|-----------------------------------------------|------------------------------------------------------|--------------|-------------------------------------------------------------------------|-----|-------|------|----------|
| <b>DC CHARACTERISTICS</b>                     |                                                      |              |                                                                         |     |       |      |          |
| $V_{IH}$                                      | High-level Input voltage SEL1, SEL2 inputs           | 3.6          |                                                                         | 0.8 |       |      | V        |
|                                               |                                                      | 2.3          |                                                                         | 0.8 |       |      |          |
|                                               |                                                      | 1.8          |                                                                         | 0.8 |       |      |          |
| $V_{IL}$                                      | Low-level Input voltage SEL1, SEL2 inputs            | 3.6          |                                                                         |     |       | 0.3  | V        |
|                                               |                                                      | 2.3          |                                                                         |     |       | 0.3  |          |
|                                               |                                                      | 1.8          |                                                                         |     |       | 0.3  |          |
| $R_{ON}$                                      | Switch ON Resistance                                 | 3.6          | $V_S = 0$ to $V_{CC}$ , $I_S = 100$ mA,<br>$V_{SEL} = 1$ V, $0$ V       |     | 0.45  | 0.6  | $\Omega$ |
|                                               |                                                      | 2.3          |                                                                         |     | 0.6   | 0.8  |          |
|                                               |                                                      | 1.8          |                                                                         |     | 0.85  | 1.2  |          |
| $\Delta R_{ON}$                               | Difference of on-state resistance between switches   | 3.6          | $V_S = 2$ V, $0.8$ V, $I_S = 100$ mA,<br>$V_{SEL} = 1$ V, $0$ V         |     | 0.05  |      | $\Omega$ |
| $R_{ON-FLAT}$                                 | ON resistance flatness                               | 3.6          | $V_S = 0$ to $V_{CC}$ , $I_S = 100$ mA,<br>$V_{SEL} = 1$ V, $0$ V       |     | 0.1   | 0.2  | $\Omega$ |
|                                               |                                                      | 2.3          |                                                                         |     | 0.15  | 0.35 |          |
|                                               |                                                      | 1.8          |                                                                         |     | 0.4   | 0.65 |          |
| $I_{OFF}$                                     | NC, NO pin leakage current when switch is off        | 3.6          | $V_S = 0.3$ or $3.0$ V, $V_{COM} = 3$ or $0.3$ V                        |     | 5     | 90   | nA       |
| $I_{S(ON)}$                                   | NC, NO pin leakage current when switch is on         | 3.6          | $V_S = 0.3$ or $3.0$ V, $V_{COM} = \text{No Load}$                      |     | 4     | 60   | nA       |
| $I_{SEL}$                                     | Select pin input leakage current                     | $V_S$        | $V_S = 0$ or $3.6$ V                                                    |     |       | 100  | nA       |
| $I_{CC}$                                      | Quiescent supply current                             | 3.6          | $V_{SEL} = 0$ or $V_{CC}$                                               |     | 700   | 2000 | nA       |
| $I_{CCLV}$                                    | Supply current change                                | 3.6          | $V_{SEL} = 1$ V to $V_{SEL} = V_{CC}$                                   |     |       | 200  | nA       |
| <b>SWITCHING PARAMETERS <sup>(1)(2)</sup></b> |                                                      |              |                                                                         |     |       |      |          |
| $t_{PHL}$                                     | Logic high to low propagation delay                  | 3.6          | $R_L = 50$ $\Omega$ , $C_L = 35$ pF                                     |     | 0.1   |      | ns       |
|                                               |                                                      | 2.5          |                                                                         |     | 0.2   |      |          |
|                                               |                                                      | 1.8          |                                                                         |     | 0.2   |      |          |
| $t_{PLH}$                                     | Logic low to high propagation delay                  | 3.6          | $R_L = 50$ $\Omega$ , $C_L = 35$ pF                                     |     | 0.1   |      | ns       |
|                                               |                                                      | 2.5          |                                                                         |     | 0.2   |      |          |
|                                               |                                                      | 1.8          |                                                                         |     | 0.2   |      |          |
| $t_{ON}$                                      | Turn-ON time                                         | 2.3 - 3.6    | $R_L = 50$ $\Omega$ , $C_L = 35$ pF, $V_S = 1.5$ V                      |     |       | 70   | ns       |
| $t_{OFF}$                                     | Turn-OFF time                                        | 2.3 - 3.6    | $R_L = 50$ $\Omega$ , $C_L = 35$ pF, $V_S = 1.5$ V                      |     |       | 75   | ns       |
| $t_{BBM}$                                     | Break-before-make time delay                         | 3.6          | $R_L = 50$ $\Omega$ , $C_L = 35$ pF, $V_S = 1.5$ V                      | 2   | 8     |      | ns       |
| $Q_{INJ}$                                     | Charge Injection                                     | 3.6          | $C_L = 1$ nF, $V_S = 0$ V                                               |     | 40    |      | pC       |
| <b>AC CHARACTERISTICS</b>                     |                                                      |              |                                                                         |     |       |      |          |
| BW                                            | -3 dB Bandwidth                                      | 1.65 - 3.6   | $R_L = 50$ $\Omega$ , $C_L = 35$ pF                                     |     | 80    |      | MHz      |
| $V_{ISO}$                                     | Channel OFF isolation                                | 1.65 - 3.6   | $V_S = 1$ Vrms, $f = 100$ kHz                                           |     | -70   |      | dB       |
| $V_{XTalk}$                                   | Channel-to-Channel Crosstalk                         | 1.65 - 3.6   | $V_S = 1$ Vrms, $f = 100$ kHz                                           |     | -75   |      | dB       |
| THD                                           | Total harmonic distortion                            | 1.65 - 3.6   | $R_L = 600$ $\Omega$ , $V_{SEL} = 2$ Vpk-pk,<br>$f = 20$ Hz to $20$ kHz |     | 0.01% |      |          |
| $C_{SEL}$                                     | Select pin input capacitance                         | 3.3          | $f = 1$ MHz                                                             |     | 3     |      | pF       |
| $C_{ON}$                                      | NC, NO, and COM input capacitance when switch is on  | 3.3          | $f = 1$ MHz                                                             |     | 115   |      | pF       |
| $C_{OFF}$                                     | NC, NO, and COM input capacitance when switch is off | 3.3          | $f = 1$ MHz                                                             |     | 50    |      | pF       |

- (1) Rise and Fall propagation delays,  $t_{PHL}$  and  $t_{PLH}$ , are measured between 50% values of the input and the corresponding output signal amplitude transition.
- (2) Specified by characterization only. Validated during qualification. Not measured in production testing.

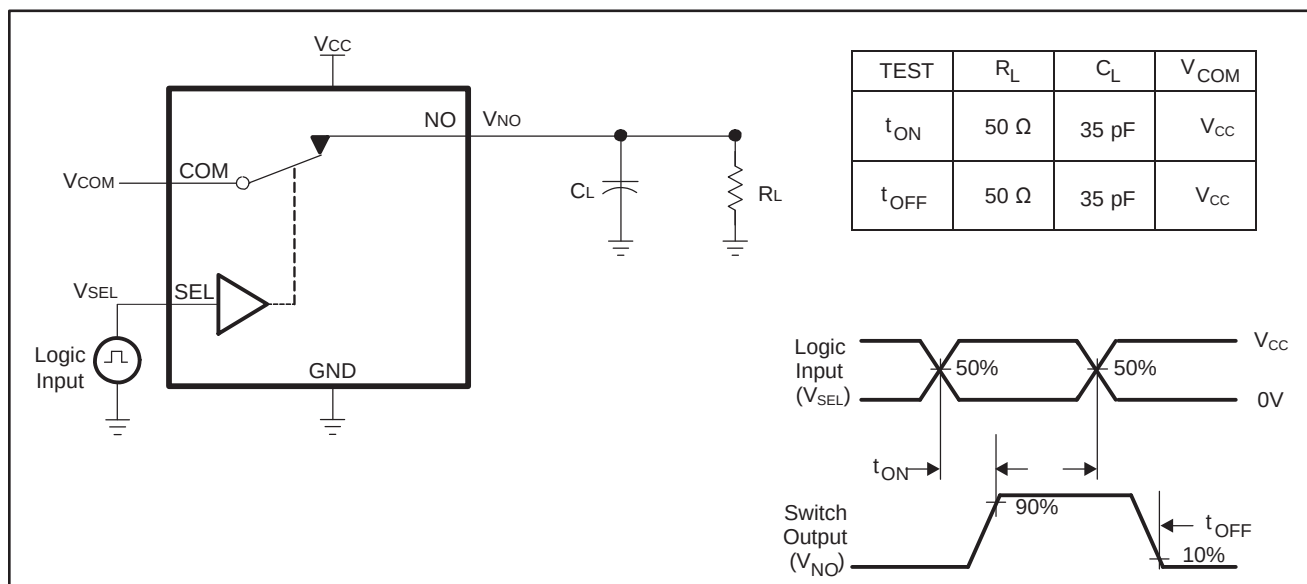
## 6.6 Typical Characteristics


 $V_{CC} = 1.8 \text{ V}$ 
**Figure 1. On-Resistance vs Switch Input Voltage**

 $V_{CC} = 2.3 \text{ V}$ 
**Figure 2. On-Resistance vs Switch Input Voltage**

 $V_{CC} = 3 \text{ V}$ 
**Figure 3. On-Resistance vs Switch Input Voltage**

 $V_{CC} = 3.6 \text{ V}$ 
**Figure 4. On-Resistance vs. Switch Input Voltage**

 $T_A = 25^\circ\text{C}$ 
**Figure 5. On-Resistance vs. Switch Input Voltage**

**Figure 6. Total Harmonic Distortion**

## 7 Parameter Measurement Information

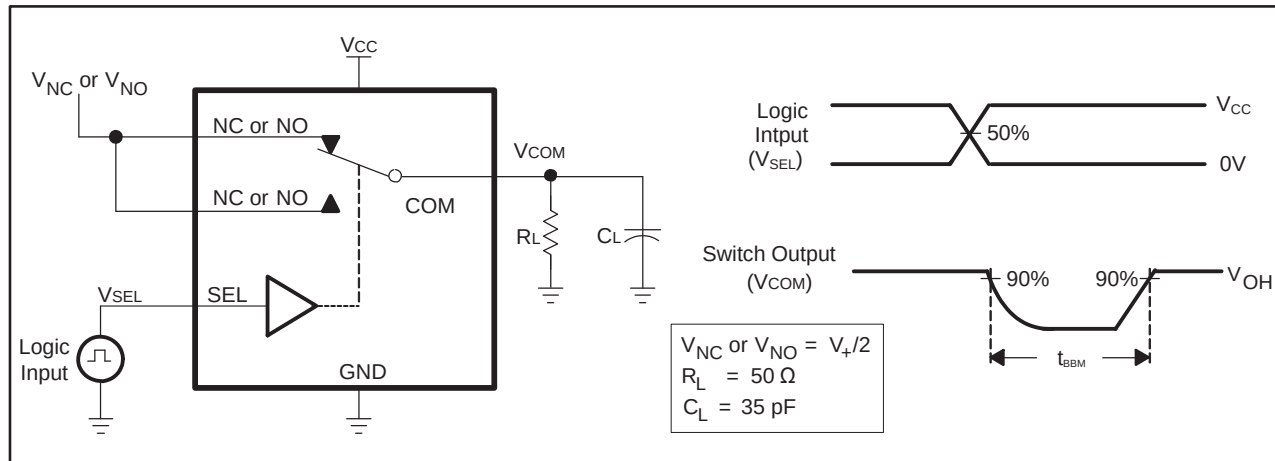


**Figure 7. ON-State Resistance ( $R_{ON}$ )**

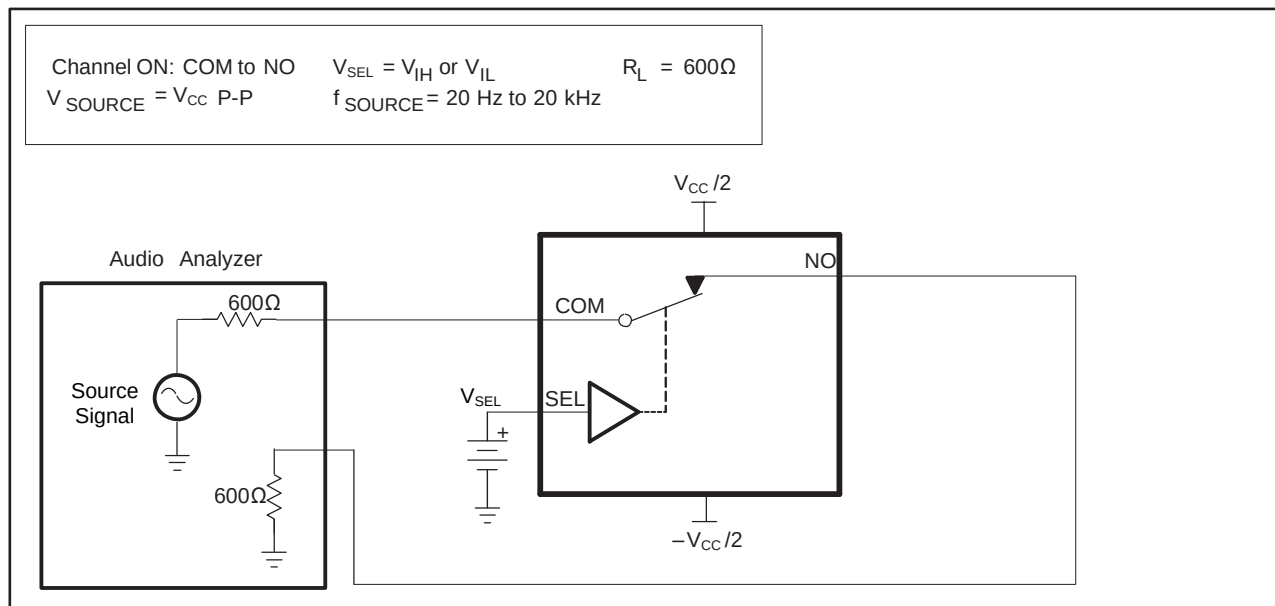


**Figure 8. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )**

### Parameter Measurement Information (continued)



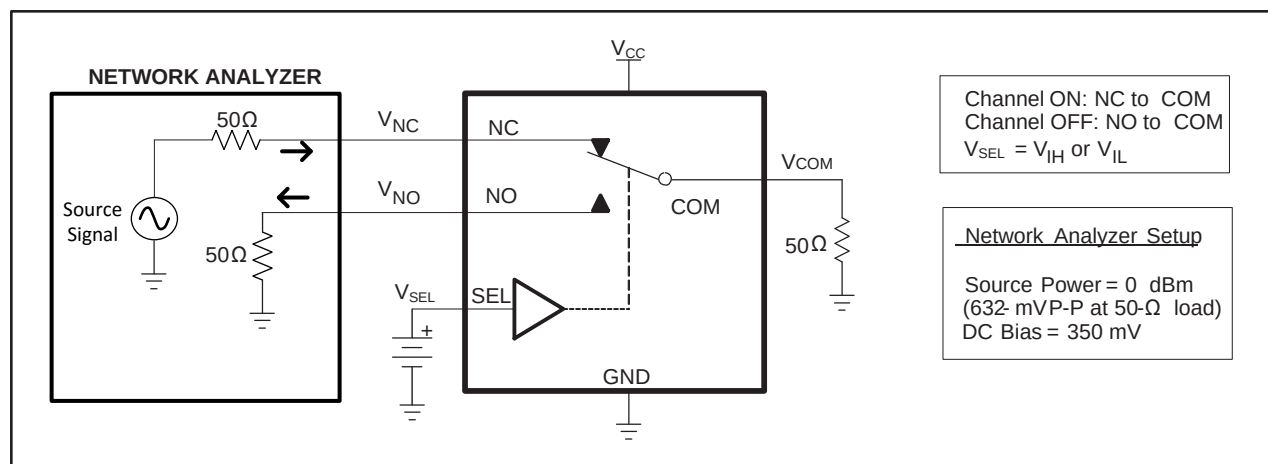
**Figure 9. Break-Before-Make Time (t<sub>BBM</sub>)**



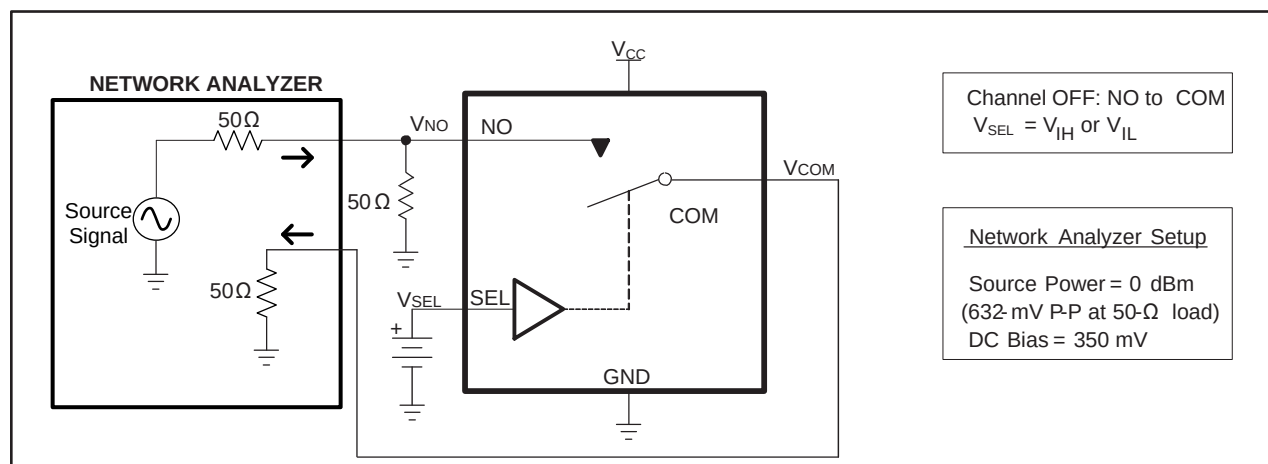
**Figure 10. TOTAL HARMONIC DISTORTION (THD)**



## Parameter Measurement Information (continued)



**Figure 11. Crosstalk ( $X_{TALK}$ )**



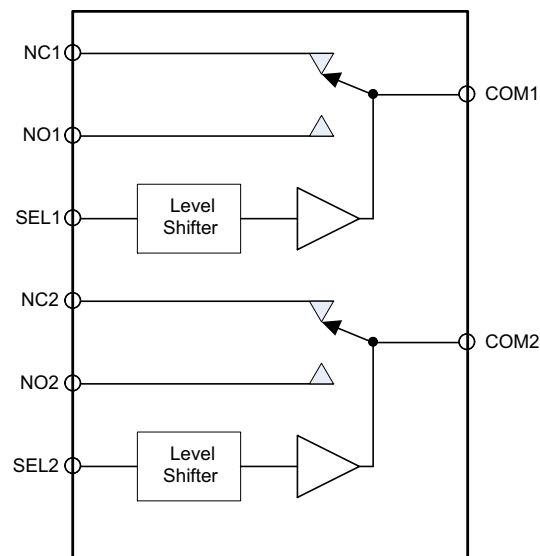
**Figure 12. OFF Isolation ( $O_{ISO}$ )**

## 8 Detailed Description

### 8.1 Overview

The TS3A5223 is a bidirectional, 2-channel, single-pole double-throw (2:1 SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. This switch solution comes in a small 1.4mm x 1.8 mm QFN package while maintaining excellent signal integrity, which makes the TS3A5223 suitable for a wide range of applications in personal electronics, portable instrumentation, and test and home electronics. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS3A5223 device also has a specified break-before-make feature.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

#### 8.3.1 Digital Logic Translation

The TS3A5223 device supports down to 1-V logic signals irrespective of the supply voltage. The device accomplishes this with integrated level shifters on the digital input SEL1 and SEL2 pins.

#### 8.3.2 Break-Before-Make

The TS3A5223 device prevents signal distortions when switching signals between the NO and NC pins by completely turning off one signal path before turning on the other signal path. The break-before-make timing specifications are found in the [Electrical Characteristics](#) table.

## 8.4 Device Functional Modes

Logic low voltage on SEL1 or SEL2 pins connect the COM pin to NC pin.

Logic high voltage on SEL1 or SEL2 pins connect the COM pin to NO pin.

**Table 1. TS3A5223 Function Table**

| SEL1 | SEL2 | COM1 | COM2 |
|------|------|------|------|
| 0    | 0    | NC1  | NC2  |
| 1    | 1    | NO1  | NO2  |
| 1    | 0    | NO1  | NC2  |
| 0    | 1    | NC1  | NO2  |

## 9 Application and Implementation

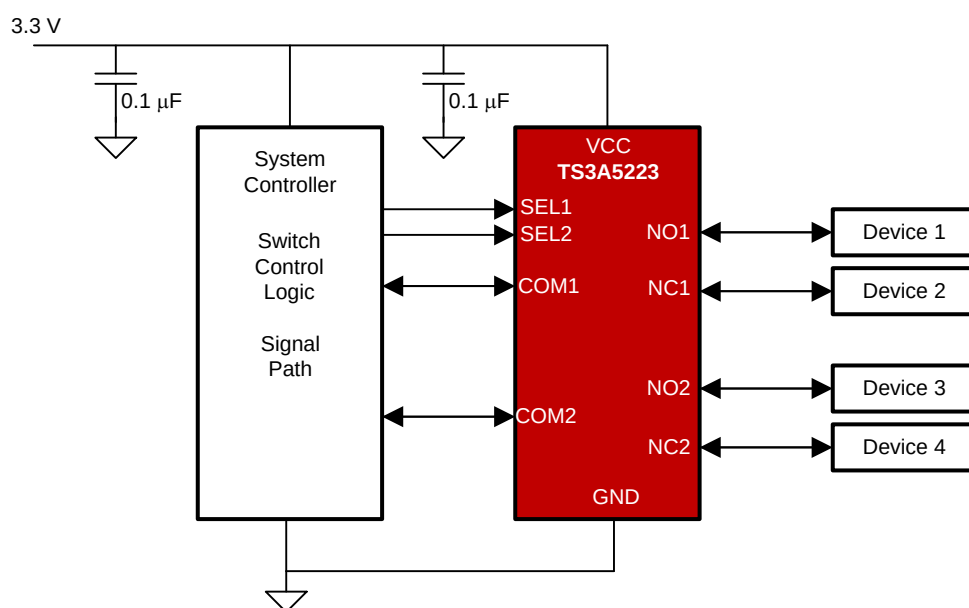
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS3A5223 switch is bidirectional, so the NO, NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 2 different signal paths.

### 9.2 Typical Application



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**Figure 13. Typical Application**

#### 9.2.1 Design Requirements

The TS3A5223 can be properly operated without any external components.

Unused, pins COM, NC, and NO may be left floating or grounded.

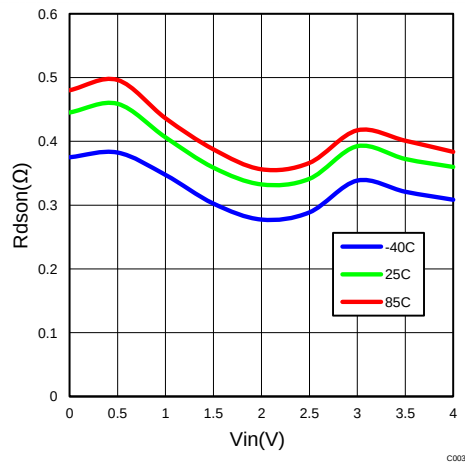
Digital control pins IN must be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin and cause excess current consumption. For more information, refer to the application note [Implications of Slow or Floating CMOS Inputs \(SCBA002\)](#).

#### 9.2.2 Detailed Design Procedure

Ensure that all of the signals passing through the switch are within the ranges specified in [Recommended Operating Conditions](#) to ensure proper performance.

## Typical Application (continued)

### 9.2.3 Application Curves



$$V_{CC} = 3.6 \text{ V}$$

**Figure 14. On-Resistance vs. Switch Input Voltage**

## 10 Power Supply Recommendations

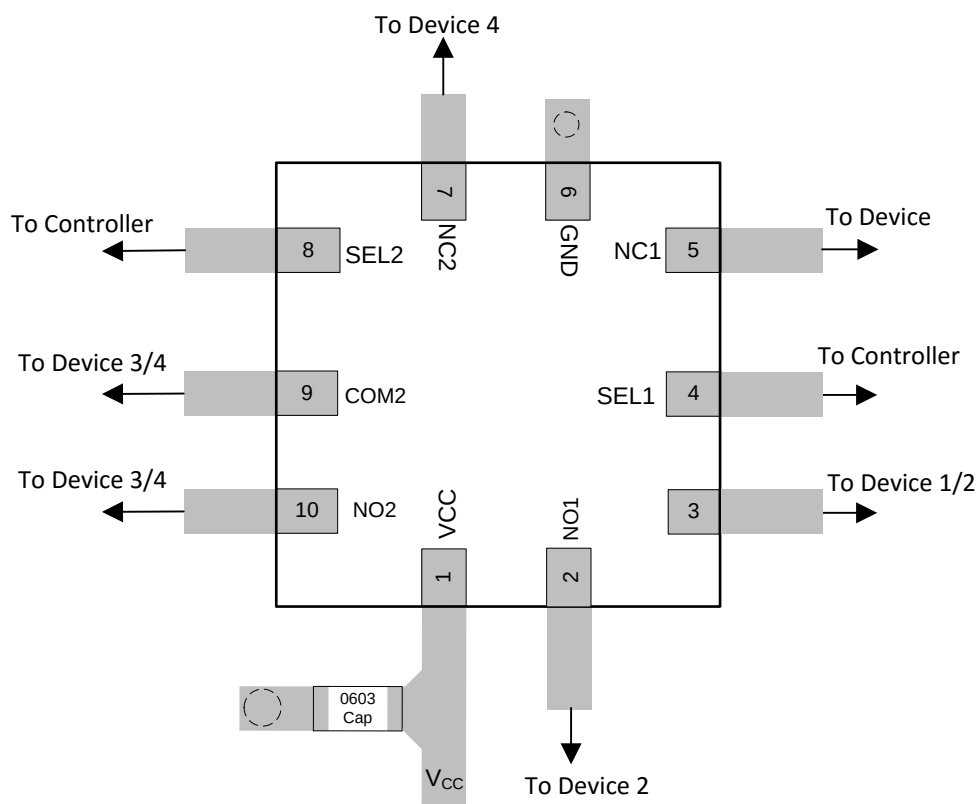
TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute-maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

## 11 Layout

### 11.1 Layout Guidelines

- TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.
- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

### 11.2 Layout Example



**Figure 15. Layout Example**

## 12 器件和文档支持

### 12.1 文档支持

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 12.3 社区资源

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

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### 12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TS3A5223RSWR</a> | Active        | Production           | UQFN (RSW)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | B2A                 |
| TS3A5223RSWR.B               | Active        | Production           | UQFN (RSW)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | B2A                 |
| TS3A5223RSWRG4               | Active        | Production           | UQFN (RSW)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | B2A                 |
| TS3A5223RSWRG4.B             | Active        | Production           | UQFN (RSW)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | B2A                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS3A5223RSWR   | UQFN         | RSW             | 10   | 3000 | 180.0              | 8.4                | 1.7     | 2.1     | 0.7     | 4.0     | 8.0    | Q1            |
| TS3A5223RSWRG4 | UQFN         | RSW             | 10   | 3000 | 180.0              | 8.4                | 1.7     | 2.1     | 0.7     | 4.0     | 8.0    | Q1            |

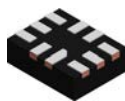
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS3A5223RSWR   | UQFN         | RSW             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TS3A5223RSWRG4 | UQFN         | RSW             | 10   | 3000 | 210.0       | 185.0      | 35.0        |

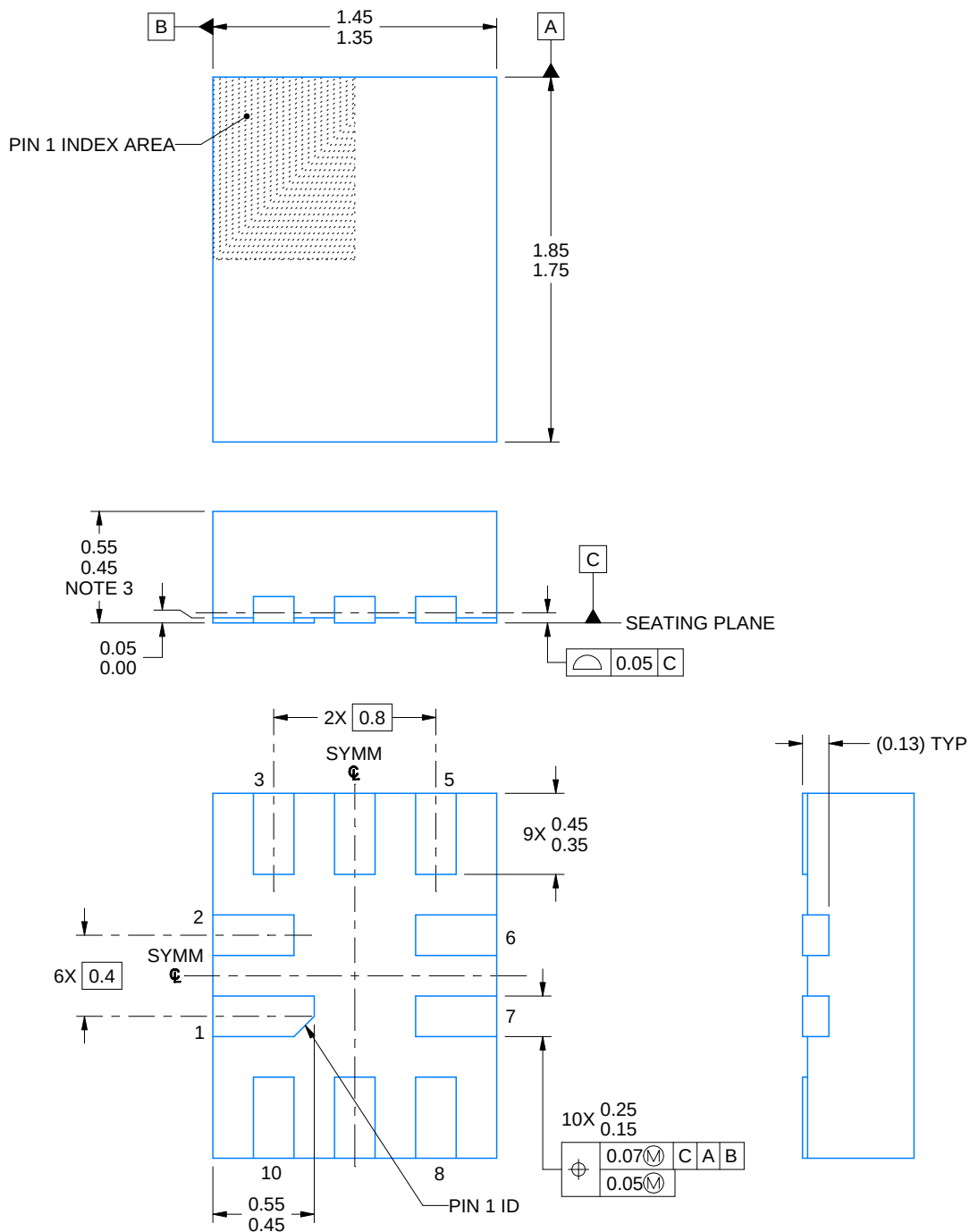
RSW0010A



# PACKAGE OUTLINE

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4224897/A 03/2019

## NOTES:

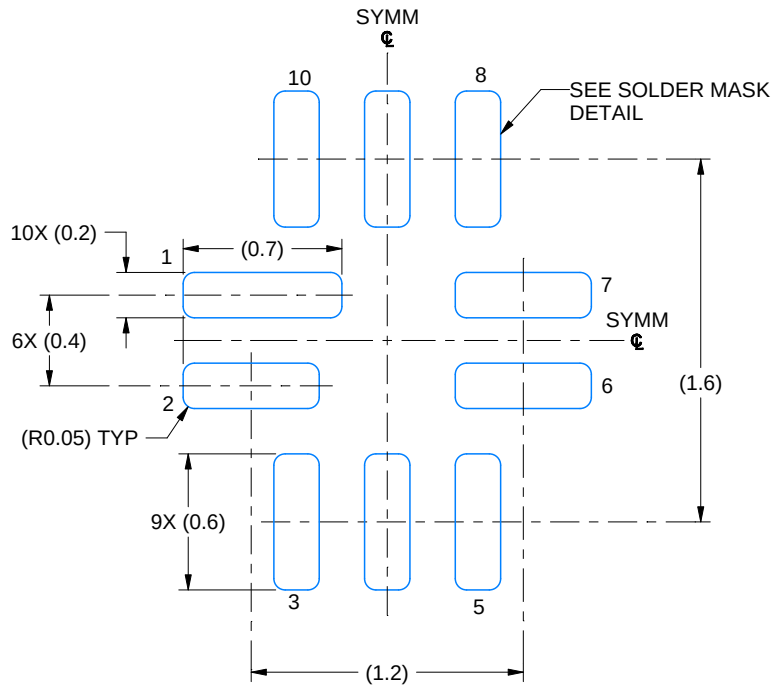
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

# EXAMPLE BOARD LAYOUT

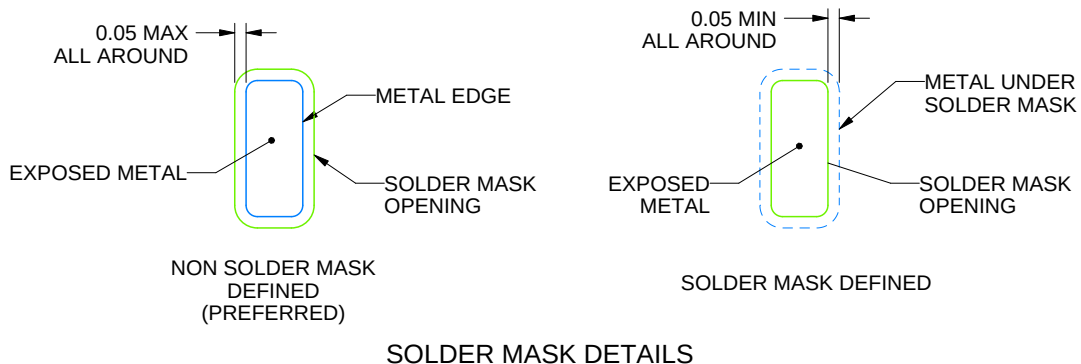
RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



SOLDER MASK DETAILS

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NOTES: (continued)

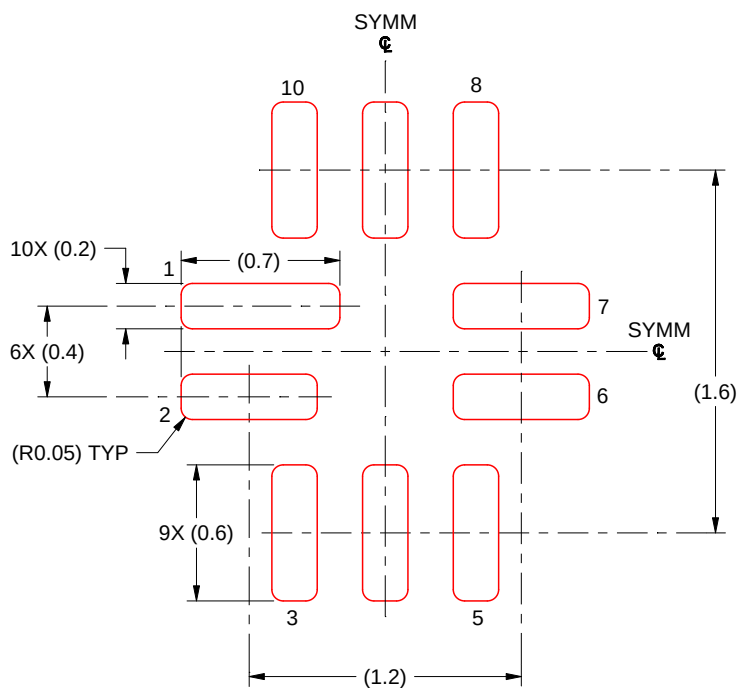
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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