

TRS208 具有 $\pm 15\text{kV}$ ESD 保护的 5V 多通道 RS-232 线路驱动器和接收器

1 特性

- 为 RS-232 I/O 引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模式 (HBM)
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 $5\text{V } V_{\text{CC}}$ 电源供电
- 四个驱动器和四个接收器
- 速率高达 120 kbit/s
- 外部电容器： $4 \times 0.1 \mu\text{F}$
- 闩锁性能超过 100 mA ，符合 JESD 78 II 类规范的要求

2 应用

- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

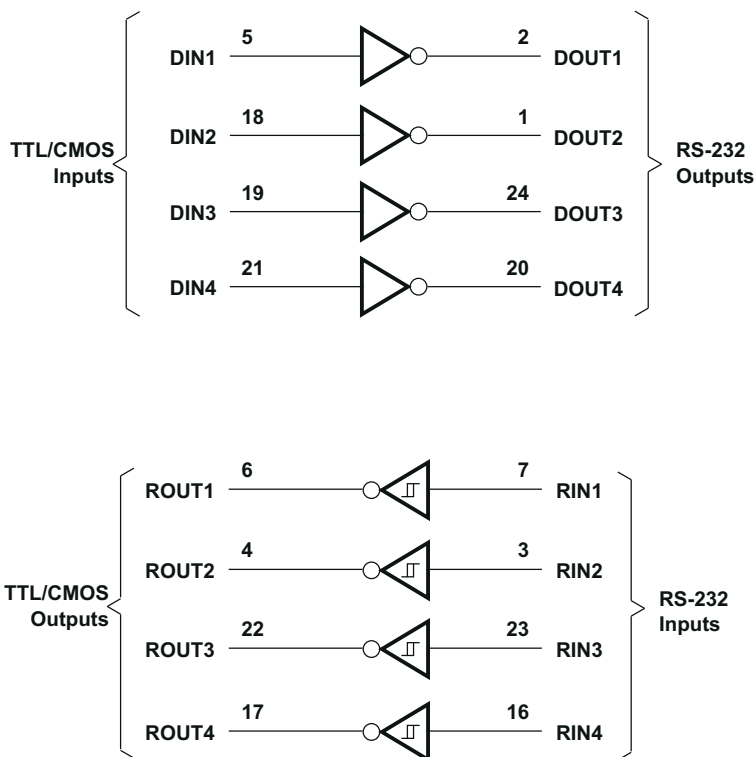
TRS208 器件由四个线路驱动器、四个线路接收器和一个双电荷泵电路组成，具有引脚对引脚（串行端口连接引脚，包括 GND） $\pm 15\text{kV}$ HBM ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由单个 5V 电源供电。这些器件以高达 120 kbit/s 的数据信号传输速率和最高 $30\text{V}/\mu\text{s}$ 的驱动器输出压摆率运行。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TRS208	DB (SSOP)	8.2 mm x 7.8mm
	DW (SOIC)	15.5mm x 10.3mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）



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4 Pin Configuration and Functions

**DB, DW, OR NT PACKAGE
(TOP VIEW)**

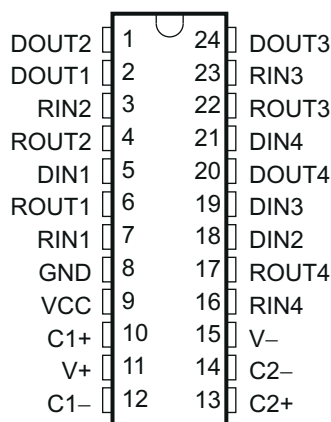


表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DB or DW		
DOUT2	1	O	RS232 line data output (to remote RS232 system)
DOUT1	2	O	RS232 line data output (to remote RS232 system)
RIN2	3	I	RS232 line data input (from remote RS232 system)
ROUT2	4	O	Logic data output (to UART)
DIN1	5	I	Logic data input (from UART)
ROUT1	6	O	Logic data output (to UART)
RIN1	7	I	RS232 line data input (from remote RS232 system)
GRD	8	-	Ground
V _{CC}	9	-	Supply Voltage, Connect to external 3V to 5.5V power supply
C1+	10	-	Positive lead of C1 capacitor
V+	11	O	Positive charge pump output for storage capacitor only
C1-	12	-	Negative lead of C1 capacitor
C2+	13	-	Positive lead of C2 capacitor
C2-	14	-	Negative lead of C2 capacitor
V-	15	O	Negative charge pump output for storage capacitor only
RIN4	16	I	RS232 line data input (from remote RS232 system)
ROUT4	17	O	Logic data output (to UART)
DIN2	18	I	Logic data input (from UART)
DIN3	19	I	Logic data input (from UART)
DOUT4	20	O	RS232 line data output (to remote RS232 system)
DIN4	21	I	Logic data input (from UART)
ROUT3	22	O	Logic data output (to UART)
RIN3	23	I	RS232 line data input (from remote RS232 system)
DOUT3	24	O	RS232 line data output (to remote RS232 system)
Thermal Pad	-	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted), see ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	- 0.3	6	V
V+	Positive charge pump voltage range ⁽²⁾	V _{CC} - 0.3	14	V
V-	Negative charge pump voltage range ⁽²⁾	- 14	0.3	V
V _I	Input voltage range	Drivers	V+ + 0.3	V
		Receivers (DB package)	±25	
		Receivers (DW package)	±30	V
V _O	Output voltage range	Drivers	V- - 0.3	V
		Receivers	- 0.3	
	Short-circuit duration	DOUT	Continuous	
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	- 65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ DOUT and RIN pins	±15	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See 图 8-3 and ⁽¹⁾

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V _{IH}	Driver high-level input voltage	DIN	2			V
V _{IL}	Driver low-level input voltage	DIN			0.8	V
V _I	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage (DB package)		- 25		25	
	Receiver input voltage (DW package)		-30		30	V
T _A	Operating free-air temperature	TRS208C	0		70	°C
		TRS208I	- 40		85	

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 5V ± 0.5V.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SSOP)	DW (SOIC)	UNIT
		24-Pins	24-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.0	46	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.8	54.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [图 8-3](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
I_{CC} Supply current	No load, $V_{CC} = 5V$, $T_A = 25^\circ C$		11	20	mA

- (1) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 5V \pm 0.5V$.

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 8-3](#))

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH} High-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND, DIN = GND	5	9		V
V_{OL} Low-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND, DIN = V_{CC}	- 5	- 9		V
I_{IH} High-level input current	$V_I = V_{CC}$		15	200	μA
I_{IL} Low-level input current	V_I at 0V		- 15	- 200	μA
I_{OS} ⁽²⁾ Short-circuit output current	$V_{CC} = 5.5V$, $V_O = 0V$		± 10	± 60	mA
r_o Output resistance	V_{CC} , V_+ , and $V_- = 0V$, $V_O = \pm 2V$	300			Ω

- (1) All typical values are at $V_{CC} = 5V$, and $T_A = 25^\circ C$
 (2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
 (3) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 5V \pm 0.5V$.

5.7 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 图 8-3)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -1mA	3.5			V
V _{OL} Low-level output voltage	I _{OL} = 1.6mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 5V, T _A = 25°C		1.7	2.4	V
V _{IT-} Negative-going input threshold voltage	V _{CC} = 5V, T _A = 25°C	0.8	1.2		V
V _{hys} Input hysteresis (V _{IT+} - V _{IT-})	V _{CC} = 5V	0.2	0.5	1	V
r _i Input resistance	V _I = ±3V to ±25V, V _{CC} = 5V, T _A = 25°C	3	5	7	kΩ

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 5V ± 0.5V.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 图 8-3)

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate	C _L = 50pF to 1000pF, R _L = 3kΩ to 7kΩ, One DOUT switching, See 图 6-1	120			kbit/s
t _{PLH(D)} Propagation delay time, low- to high-level output	C _L = 2500pF, R _L = 3kΩ, All drivers loaded, See 图 6-1		2		μs
t _{PHL(D)} Propagation delay time, high- to low-level output	C _L = 2500pF, R _L = 3kΩ, All drivers loaded, See 图 6-1		2		μs
t _{sk(p)} Pulse skew ⁽²⁾	C _L = 150pF to 2500pF, R _L = 3kΩ to 7kΩ, See 图 6-2		300		ns
SR(tr) Slew rate, transition region (see 图 6-1)	C _L = 50pF to 1000pF, R _L = 3kΩ to 7kΩ, V _{CC} = 5V	3	6	30	V/μs

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 5V ± 0.5V.

5.9 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 图 6-3)

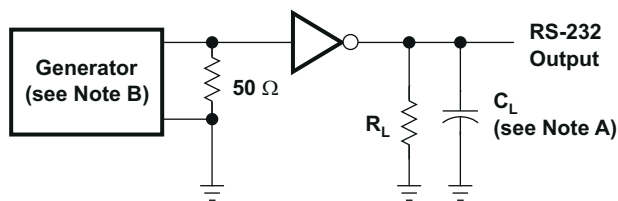
PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH(R)} Propagation delay time, low- to high-level output	C _L = 150pF		0.5	10	μs
t _{PHL(R)} Propagation delay time, high- to low-level output	C _L = 150pF		0.5	10	μs
t _{sk(p)} Pulse skew ⁽²⁾			300		ns

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

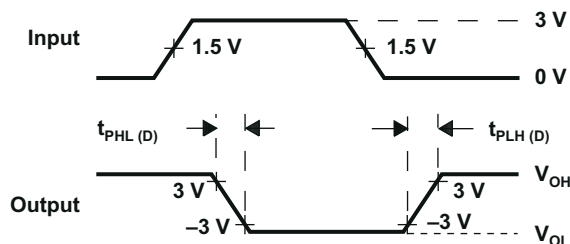
(3) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 5V ± 0.5V.

6 Parameter Measurement Information



TEST CIRCUIT

$$SR(tf) = \frac{6\text{ V}}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$

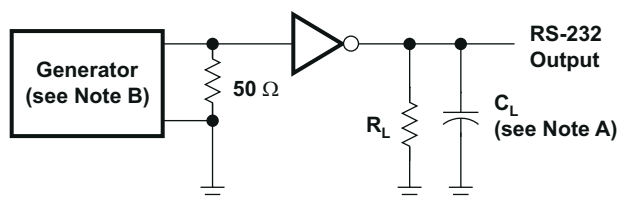


VOLTAGE WAVEFORMS

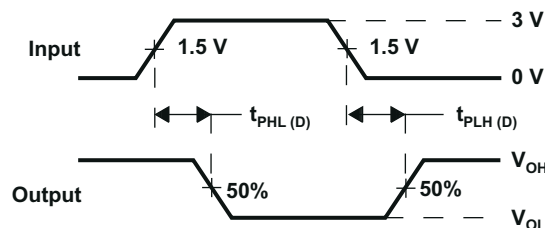
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-1. Driver Slew Rate



TEST CIRCUIT

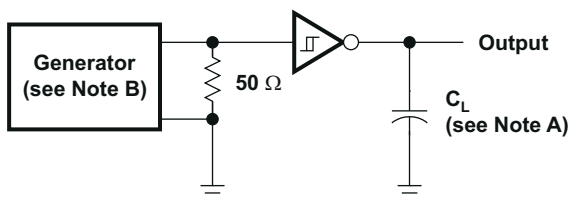


VOLTAGE WAVEFORMS

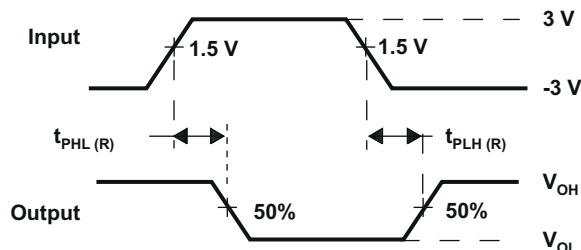
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-2. Driver Pulse Skew



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-3. Receiver Propagation Delay Times

7 Device Functional Modes

**Function Table
Each Driver ⁽¹⁾**

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

**Function Table
Each Receiver ⁽¹⁾**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Capacitor Selection

The capacitor type used for C1 – C4 is not critical for proper operation. The TRS208 requires 0.1 μ F capacitors, although capacitors up to 10 μ F can be used without harm. Ceramic dielectrics are suggested for the 0.1 μ F capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (2 $\times$) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V –.

Use larger capacitors (up to 10 μ F) to reduce the output impedance at V+ and V –.

Bypass V_{CC} to ground with at least 0.1 μ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 – C4).

8.1.2 Electrostatic Discharge (ESD) Protection

TI TRS208 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ± 15 kV when powered down.

8.1.3 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

8.1.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in 图 8-1, while 图 8-2 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100pF capacitor, charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5k Ω resistor.

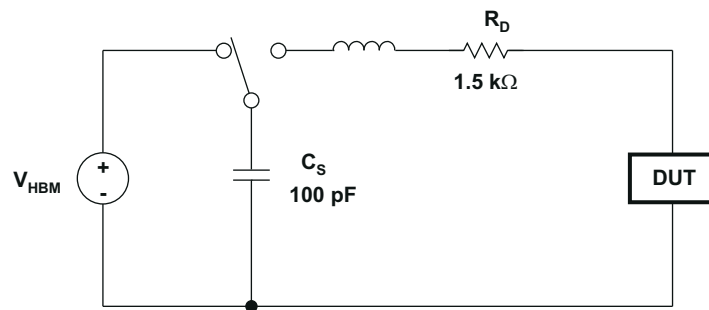


图 8-1. HBM ESD Test Circuit

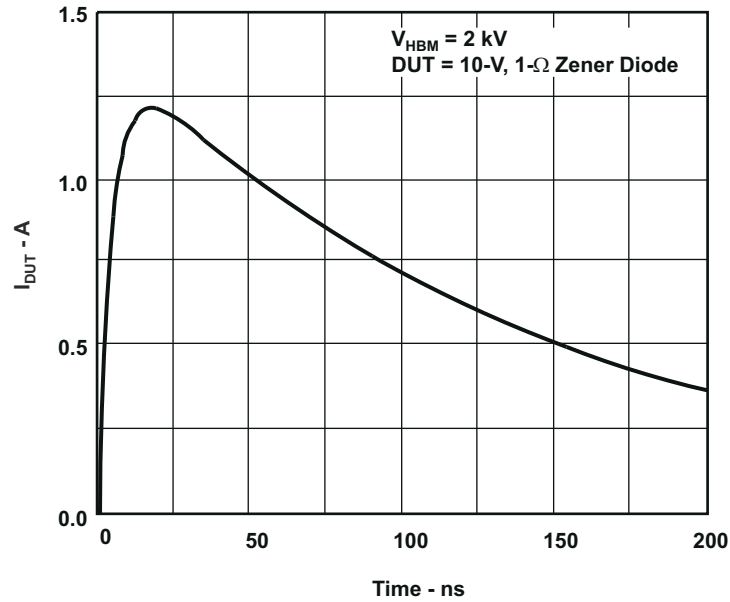
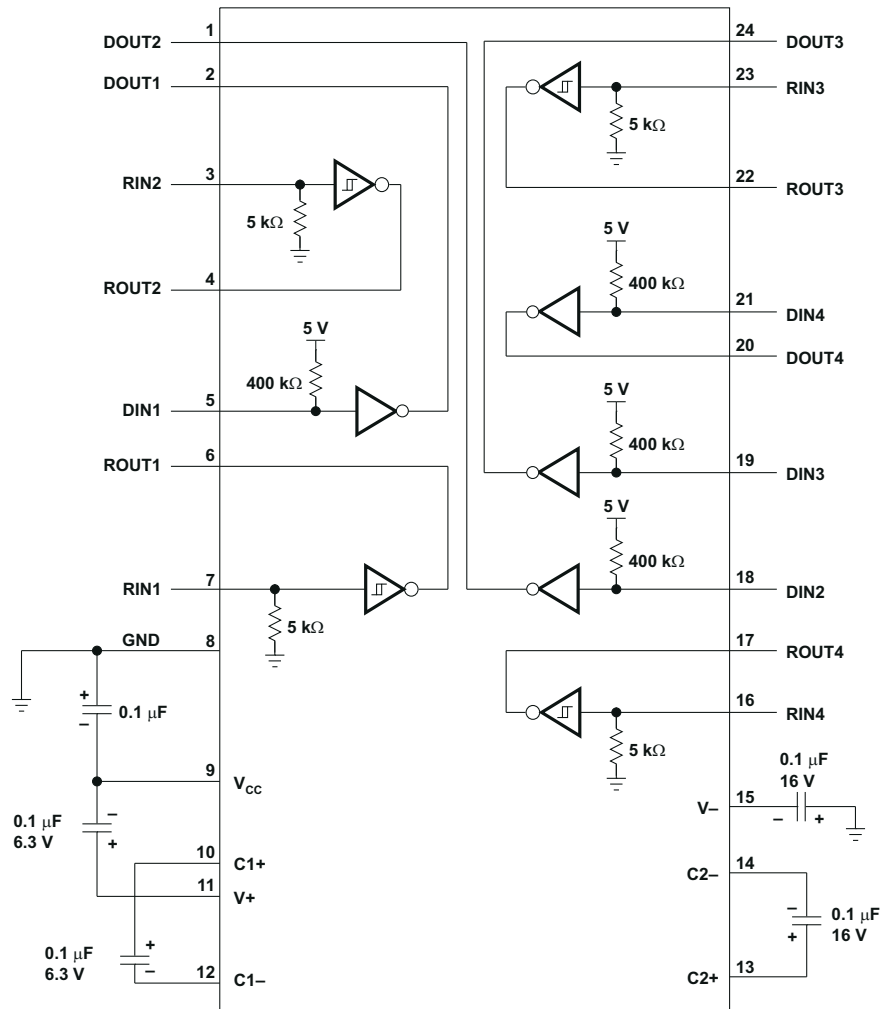


图 8-2. Typical HBM Current Waveform

8.1.5 Machine Model (MM)

The MM ESD test applies to all pins using a 200pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

8.1.6 Typical Application



- NOTES: A. Resistor values shown are nominal.
B. Non-polarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

图 8-3. Typical Operating Circuit and Capacitor Values

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2007) to Revision A (July 2024)	Page
• 通篇更改了表格、图和交叉参考的编号格式.....	1
• Changed the DB package Input voltage range for Receivers from $\pm 30V$ to $\pm 25V$ in the <i>Absolute Maximum Ratings</i> and the <i>Recommended Operating Conditions</i>	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS208CDBR	Obsolete	Production	SSOP (DB) 24	-	-	Call TI	Call TI	0 to 70	RU08C
TRS208CDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS208C
TRS208CDWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS208C
TRS208IDB	Obsolete	Production	SSOP (DB) 24	-	-	Call TI	Call TI	-40 to 85	RU08I
TRS208IDBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU08I
TRS208IDBR.A	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU08I
TRS208IDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS208I
TRS208IDWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS208I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

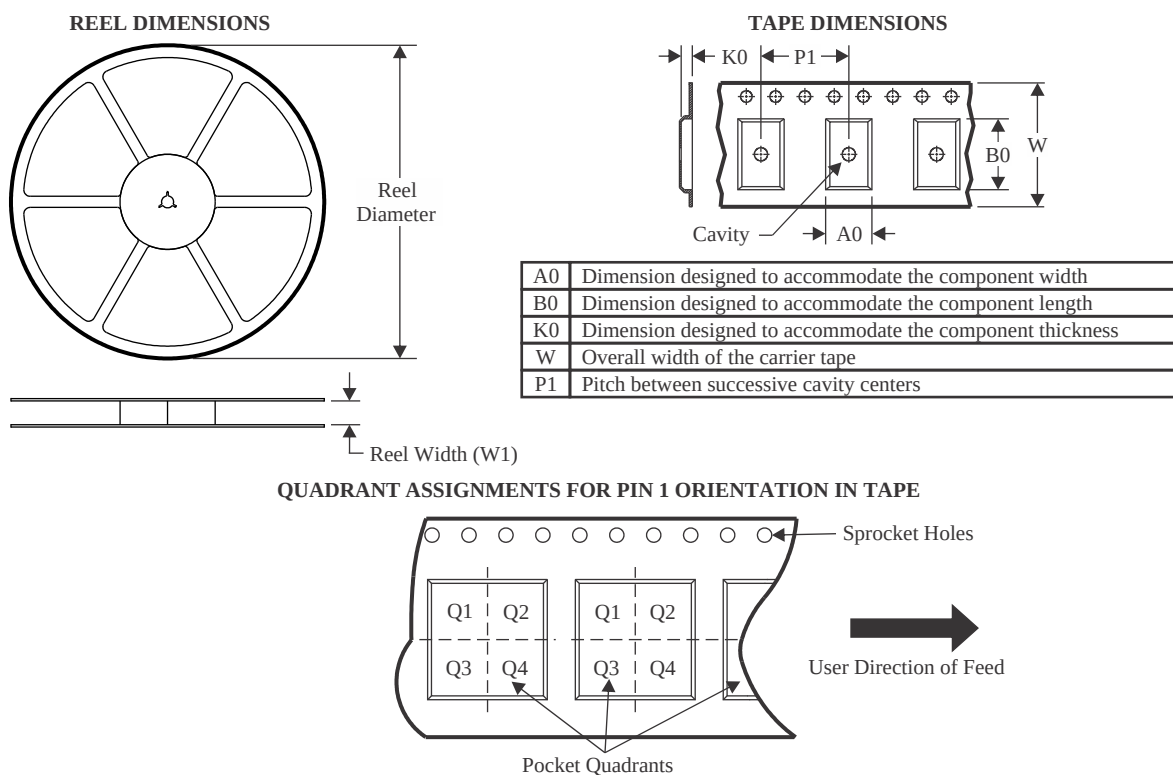
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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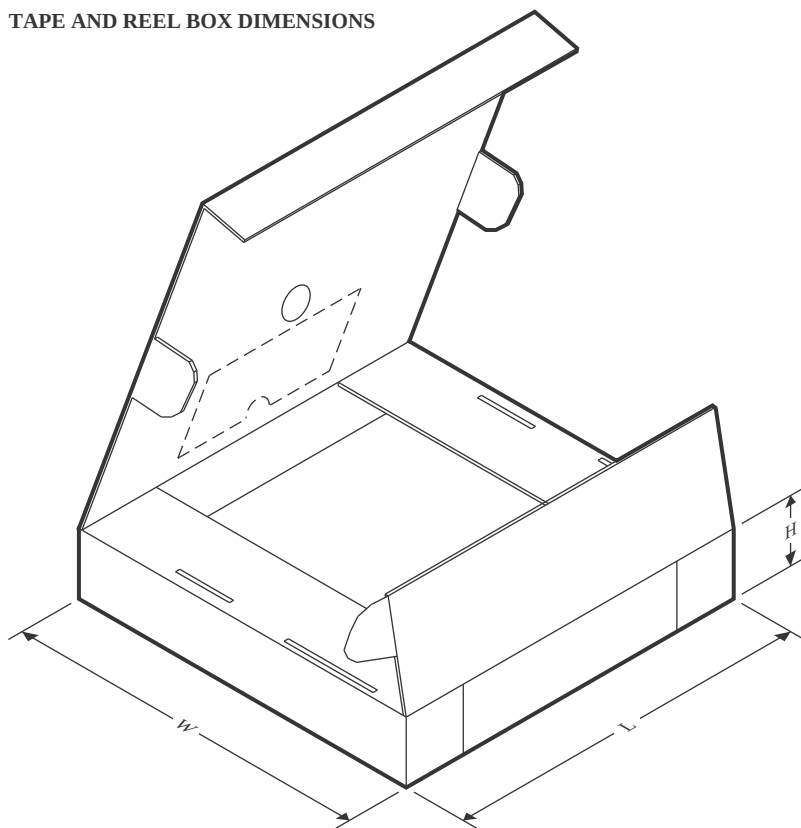
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS208CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TRS208IDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TRS208IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

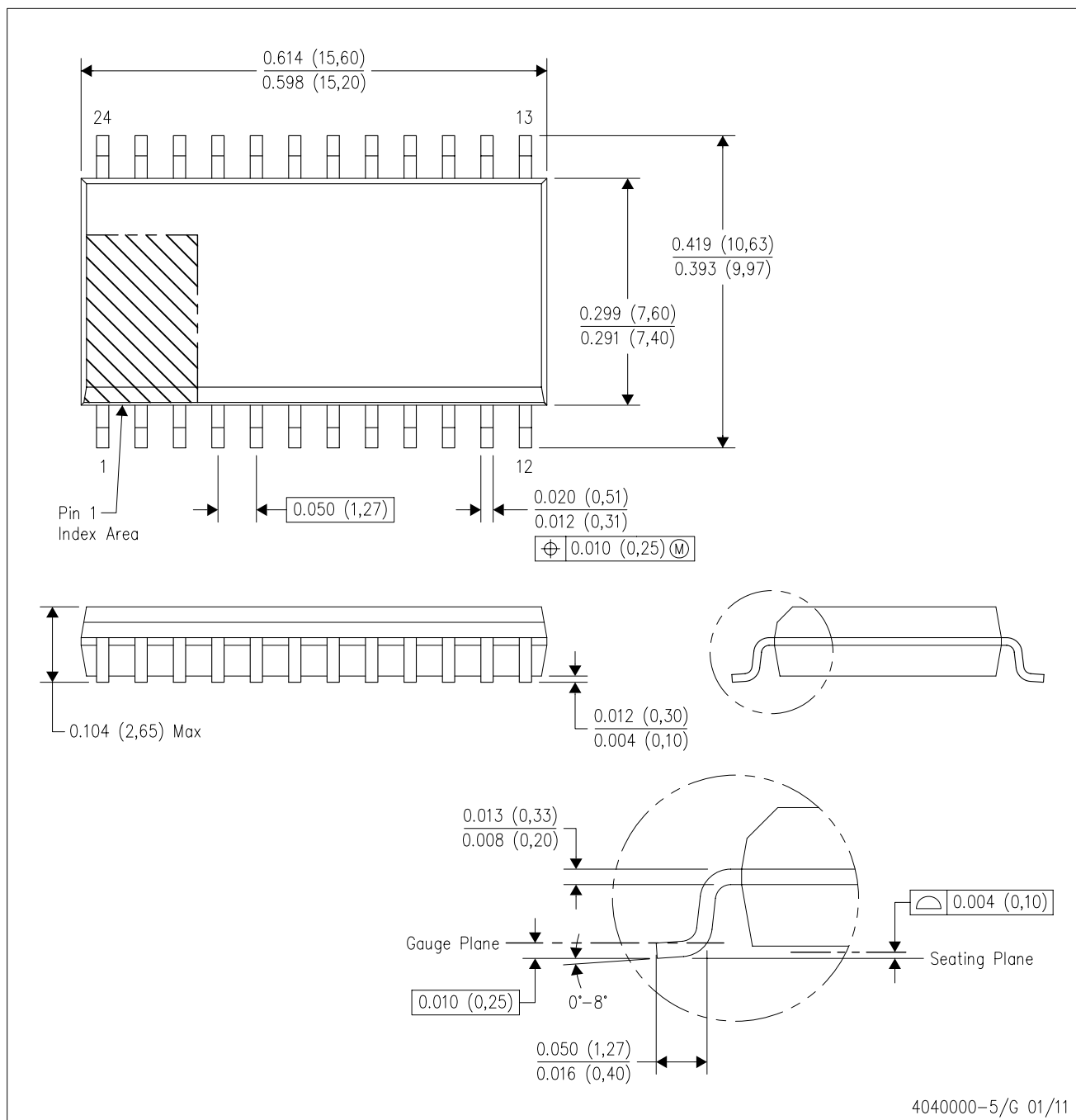


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS208CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TRS208IDBR	SSOP	DB	24	2000	353.0	353.0	32.0
TRS208IDWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

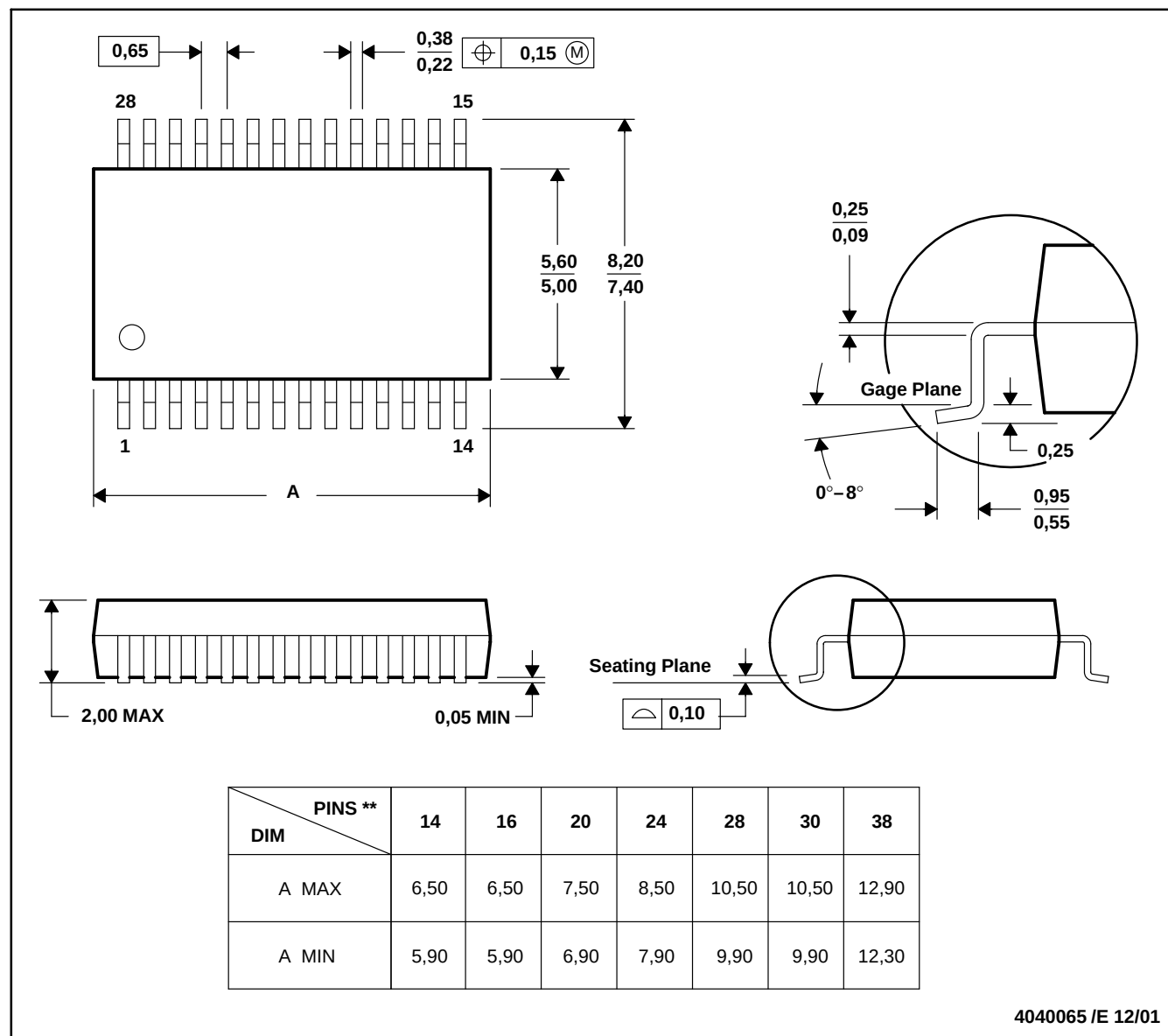


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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最后更新日期：2025 年 10 月