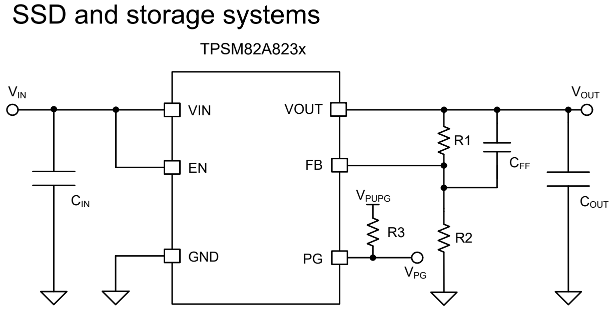
TPSM82A823x, TPSM82A824x 3A and 4A, High-Efficiency, Step-Down Converter MicroSiP™ Power Modules With Integrated Inductor

1 Features

- High efficiency
  - > 92% at V_{IN} = 3.3V and V_{OUT} = 1.2V
  - > 97% at V_{IN} = 5V and V_{OUT} = 3.3V
- 2.5V to 5.5V input voltage range
- 0.6V to V_{IN} adjustable output voltage
- 26µA operating quiescent current at V_{IN} = 5V (non-switching)
- Forced-PWM (pulse-width modulation) (TPSM82A823A, TPSM82A824A) and PSM (automatic power save mode) versions
- 100% duty cycle enables low-dropout operation (VIN – VOUT minimum drop)
- Output discharge
- Power-good output
- Integrated soft start-up with prebiased output start-up capability
- Overtemperature and hiccup short-circuit protection with automatic recovery
- 2.2MHz fixed switching frequency
- Peak current-mode control
- Pin and footprint-compatible with TPSM82821, TPSM82822, and TPSM82823
- 2.5mm × 2mm design size, 10-pin µSiP with 1.2mm maximum height

2 Applications

- Optical modules
- Machine vision
- Industrial PCs
- PLCs
- Wired networking
- Point-of load (POL) power conversion
- FPGA and DSP core supply
- SSD and storage systems



Application Example TPSM82A823x

3 Description

The TPSM82A823x and TPSM82A824x are 3A and 4A synchronous step-down converter modules in MicroSiP™ package with integrated inductor for compact design. Peak efficiency occurs between 1A and 2A output current.

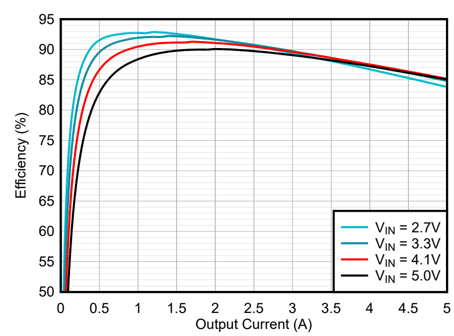
The integrated inductor simplifies the design, reduces external components, and saves PCB area. The TPSM82A823A and TPSM82A824A operate in PWM; the TPSM82A823 and TPSM82A824 support automatic PSM at light loads. All variants operate at 2.2MHz fixed frequency with peak current-mode control for stable regulation across load and input voltage variations.

EN and PG pins enable flexible sequencing. Integrated soft start-up reduces the inrush current required from the input supply. Overtemperature and overcurrent short-circuit protection deliver a robust and reliable design.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSM82A823	SIH (µSiP, 10)	2.5mm × 2mm
TPSM82A823A		
TPSM82A824		
TPSM82A824A		

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPSM82A823A, TPSM82A824A Efficiency 1.2V Output

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4 Device Comparison Table

ORDERABLE PART NUMBER[(1)]	OUTPUT VOLTAGE	MODE OF OPERATION	PEAK EFFICIENCY (V_{IN} = 3.3V, V_{OUT} = 1.2V)		OUTPUT CURRENT
			I_{OUT} RANGE	EFFICIENCY	
TPSM82A823ASIHR	Adjustable	Forced PWM	1A – 2A	91% – 92%	3A
TPSM82A823SIHR	Adjustable	Auto PSM	1A – 2A	91% – 92%	3A
TPSM82A824ASIHR	Adjustable	Forced PWM	1A – 2A	91% – 92%	4A
TPSM82A824SIHR	Adjustable	Auto PSM	1A – 2A	91% – 92%	4A

(1) For all available packages, see the orderable addendum at the end of the datasheet.

5 Pin Configuration and Functions

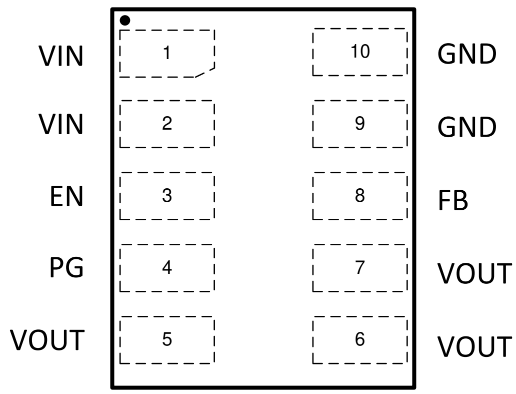


Figure 5-1. SIH Package, µSiP 10-Pin (Top View)

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
VIN	1, 2	PWR	Input voltage pin
EN	3	I	Device enable pin. Drive this pin high to turn the device on. Drive this pin low to turn off the device. Do not leave floating.
PG	4	O	Power-good open-drain output pin with window comparator. The pullup resistor can be connected to voltages up to 5.5V. If unused, connect to GND or leave open.
VOUT	5, 6, 7	PWR	Output voltage pin
FB	8	I	Feedback pin. Connect this pin to the center of the output voltage resistor divider.
GND	9, 10	PWR	Ground pin

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Pin voltage[2]	VIN, EN, PG	–0.3	6	V
Pin voltage[2]	VOUT	–0.3	V_{IN} + 0.3	V
Pin voltage[2]	FB	–0.3	3	V
Operating junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
C_{OUT}	Effective output capacitance	V_{OUT} < 1.2V		120		µF
C_{OUT}	Effective output capacitance	1.2V ≤ V_{OUT} < 1.8V		45		µF
C_{OUT}	Effective output capacitance	V_{OUT} ≥ 1.8V		45		µF
I_{OUT}	Output current range	TPSM82A823x	0		3	A
I_{PG}	Power-Good input current capability		0		1	mA
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPSM82A823x, TPSM82A824x		UNIT
		SIH (JEDEC)[2]	SIH (EVM)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.2	72.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.2	11.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.5	28.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) JEDEC standard PCB with 4 layers, no thermal vias.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610mV		26		µA
$I_{SD(VIN)}$	VIN shutdown supply current	T_J = –40°C to 85°C, V_{EN} = Low		0.01	4	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.2			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5V			100	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 125°C, PWM mode	594	600	606	mV
V_{FB}	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5V, V_{OUT} = 1.8V		2200		kHz
STARTUP						
	Internal fixed soft-start time	From EN = high to V_{FB} = 0.56V		0.5	1	ms
POWER STAGE						
R_{DP}	Dropout resistance	V_{IN} = 5V		50		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	V_{IN} = 5V	8.2	10		A
$I_{LS(OC)}$	Low-side valley current limit	V_{IN} = 5V		9.1		A
POWER GOOD						
V_{PGTH}	Power-Good threshold	PG low, FB falling		93.5		%
V_{PGTH}	Power-Good threshold	PG high, FB rising		96		%
	PG delay falling			30		µs
	PG delay rising			10		µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5V			100	nA
	PG pin output low-level voltage	I_{PG} = 1mA			200	mV
OUTPUT DISCHARGE						
	Output discharge current on V_{OUT} pin	V_{IN} = 3V, V_{OUT} = 2.0V		150		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

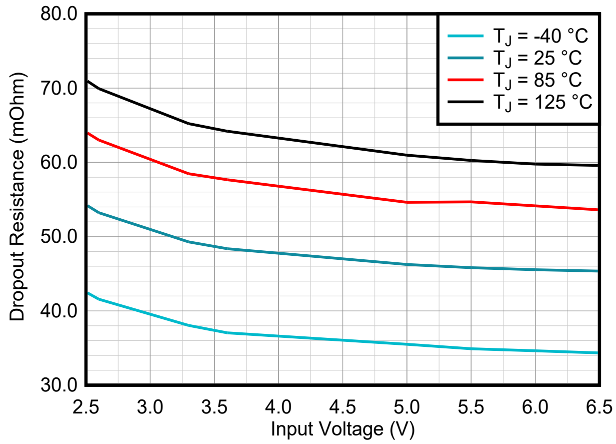


Figure 6-1. TPSM82A823/TPSM82A823A Dropout Resistance

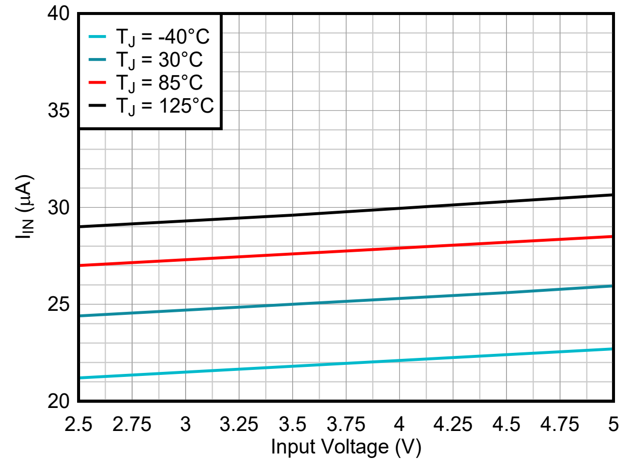


Figure 6-2. Quiescent Current

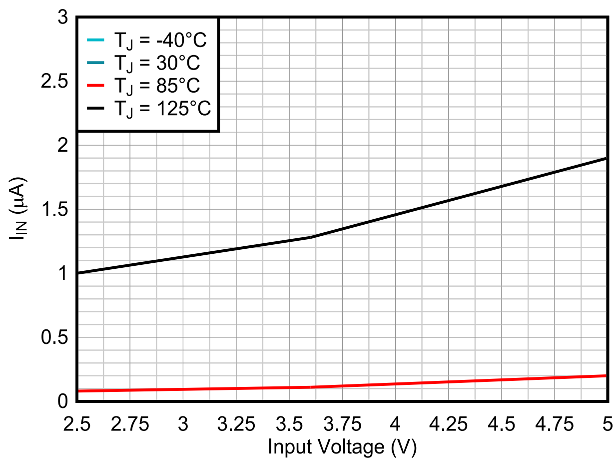


Figure 6-3. Shutdown Current

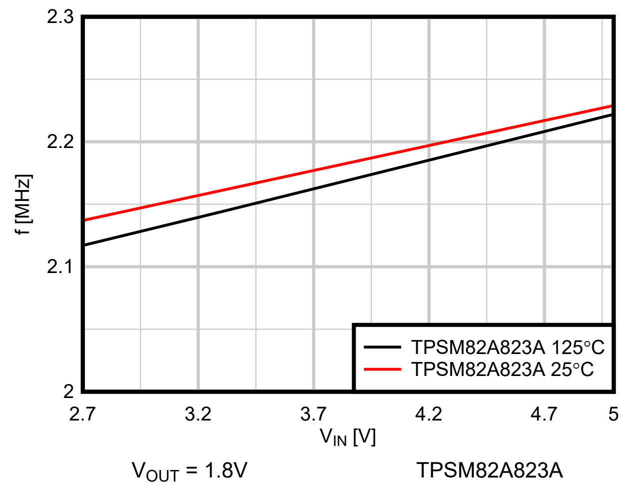


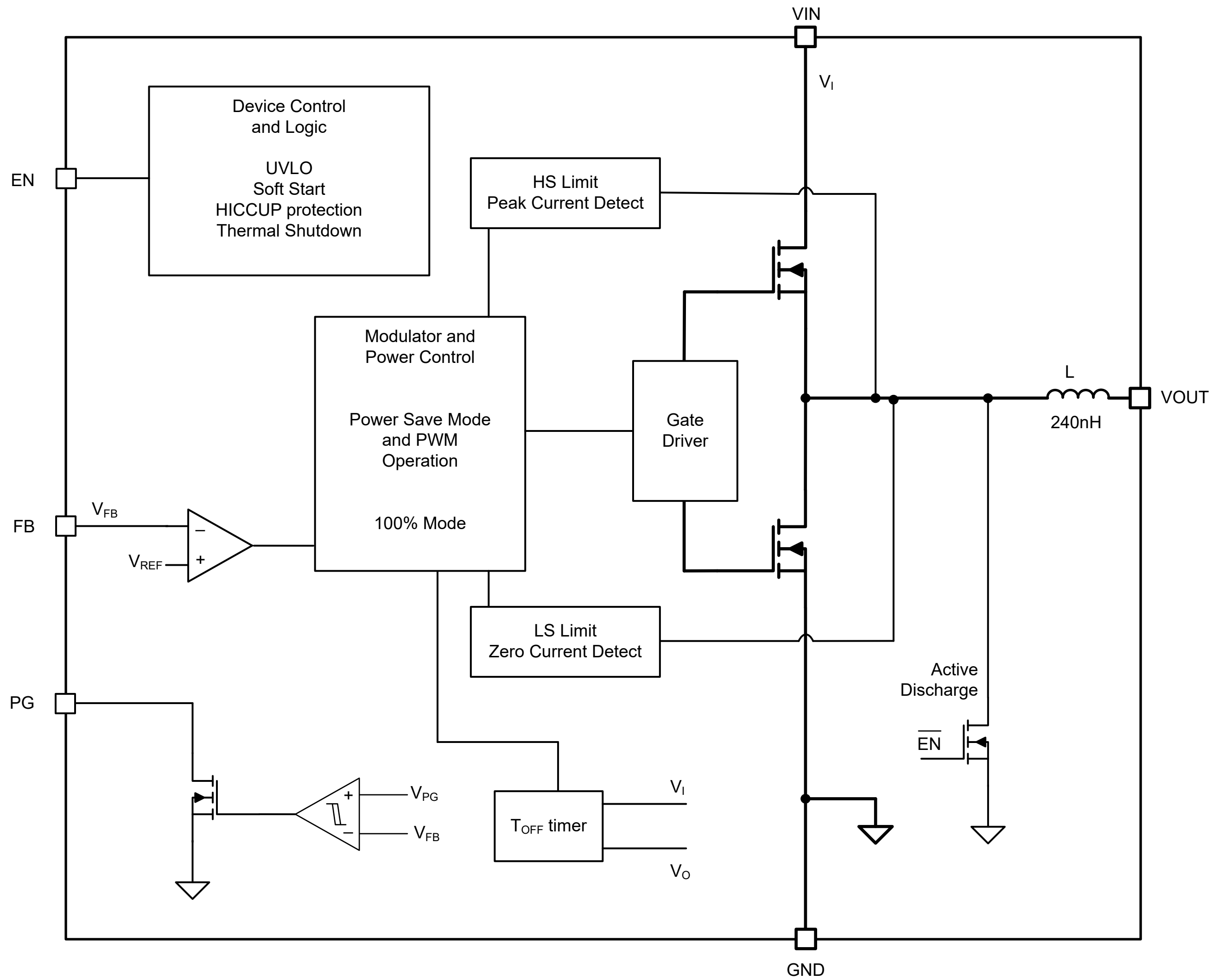
Figure 6-4. fSW over VIN

7 Detailed Description

7.1 Overview

The TPSM82A823x and TPSM82A824x devices are high-efficiency, synchronous step-down converter modules with an integrated inductor. The devices use an adaptive off-time, peak current-mode control scheme. The devices operate at a nominal 2.2MHz switching frequency at moderate to heavy load currents. An off-time control circuit adjusts the low-side MOSFET off time based on the V_{IN}/V_{OUT} ratio, keeping the switching frequency stable across varying input voltage, output voltage, and load current conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

The TPSM82A823A and TPSM82A824A operate in forced PWM mode where the power save mode is permanently deactivated. The device is designed to maintain a constant switching frequency independent of load current, temperature and within limits also input voltage (see graph f_{SW} versus V_{IN}). Unlike the TPSM82A823A and TPSM82A824A, the TPSM82A823 and TPSM82A824 devices automatically enter power save mode (PSM) at light loads when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

All device family members offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times R_{DS(ON)} + R_{DCR} \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_{DCR} = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

After turning the device on, an internal soft start-up circuitry ramps up the output voltage to the set point within the specified time (see Section 6.5). This action minimizes inrush current and provides a defined V_{OUT} ramp. Soft start-up circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPSM82A823x and TPSM82A824x family supports start-up into a prebiased output capacitor. The converter begins switching from the applied prebias voltage and ramps the output voltage to the nominal set point.

7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device reduces the current limit for an additional 32 cycles and then stops switching to protect the output. The device then automatically starts a new start-up ramp after a typical delay time of 150µs has passed. This behavior is called hiccup-mode short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also active during the start-up.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 100mV.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds $T_{J(SD)}$. When the device temperature falls below the threshold by $T_{J(HYS)}$, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Activate and Deactivate

The device is activated by driving the EN input high. Accordingly, a logic low deactivates the device and the device enters the shutdown mode with a supply current reduced to $I_{SD(VIN)}$. If the device is active, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and must not be left floating.

7.4.2 Power Good

The TPSM82A823x and TPSM82A824x family has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low.

If the power-good output is not used, tie the PG pin to GND or leave the pin open.

Table 7-1. Power-Good indicator Functional Table

LOGIC SIGNALS				PG STATUS
V_{IN}	EN	THERMAL SHUTDOWN	V_{OUT}	
V_{IN} > UVLOx	HIGH	NO	V_{OUT} on target	High Impedance
			V_{OUT} < target	LOW
	LOW	x	x	LOW
	x	YES	x	LOW
1.8V < V_{IN} < UVLO	x	x	x	LOW
V_{IN} < 1.8V	x	x	x	Not specified(1)

(1) The 1.8V threshold represents the minimum V_{IN} level at which the PG pin output transistor maintains a defined low-level output. Below this level, PG pin behavior is not specified.

7.4.3 Output Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is turned off and to keep the output voltage close to 0V. The output discharge is active when the EN pin is set to a logic low and during thermal shutdown. The discharge is not active in UVLO.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

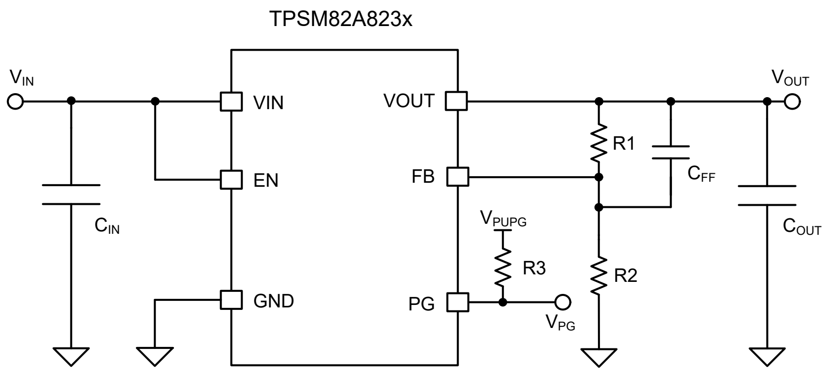


Figure 8-1. TPSM82A823x and TPSM82A824x Typical Application Circuit (With TPSM82A823x as Example)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5V to 5.5V
Output voltage	1.2V
Maximum output current	3.0A

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER[(1)]
C_{IN}	22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
C_{OUT}	3 × 22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
R1, R2	Chip resistor, 1%, size 0603	Std.
C_{FF}	Optional, 120pF (R2 = 100kΩ) if needed for transient improvement or for PSM ripple reduction	Std.

(1) See the *Third-Party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

Select resistors R1 and R2 to set the output voltage within a range of 0.6V to V_{IN} according to Equation 2. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 6μA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (2)$$

8.2.2.2 Feedforward Capacitor

A feedforward capacitor (C_{FF}) in parallel with R1 improves transient response. In TPSM82A823, a feedforward capacitor also improves the PSM ripple. Use the following equation to calculate the C_{FF} value. For the recommended 100kΩ value for R2, the calculated value for C_{FF} is 120pF.

$$C_{FF} = \frac{12\mu s}{R2} \quad (3)$$

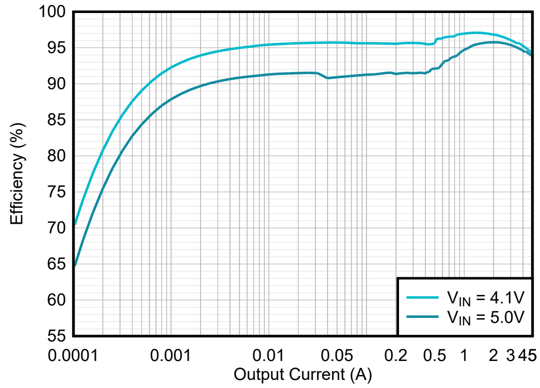
8.2.2.3 Input and Output Capacitor Selection

For the best output and input voltage filtering, ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. The capacitor value must be large enough that the device does not experience input voltage drop below the undervoltage lockout level. A 10μF (5μF effective) input capacitor is a good calculation starting point for 1.5A inductor ripple current and 3.3V input voltage out of 200mΩ source impedance (V_{OUT} = 1.2V). The input ripple is approximately 50mV under these conditions. The output capacitor value can range from 44μF up to 100μF. The recommended typical output capacitor value is 2 × 22μF or 3 × 22μF with an X5R or X7R dielectric. With the devices peak current mode control scheme, output capacitor values over 100μF for ripple-sensitive applications are possible but the designer must perform loop stability analysis (Bode plot). A feedforward capacitor improves transient performance.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Select the right capacitor carefully in combination with considering the package size and voltage rating. Verify that the effective input capacitance is at least 5μF and the effective output capacitance is at least 28μF.

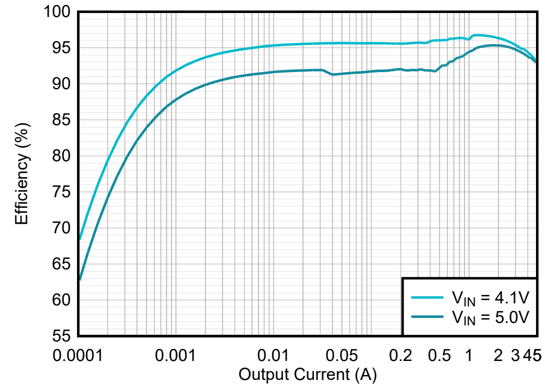
8.2.3 TPSM82A823x and TPSM82A824x Performance Curves

8.2.3.1 PSM Performance Curves



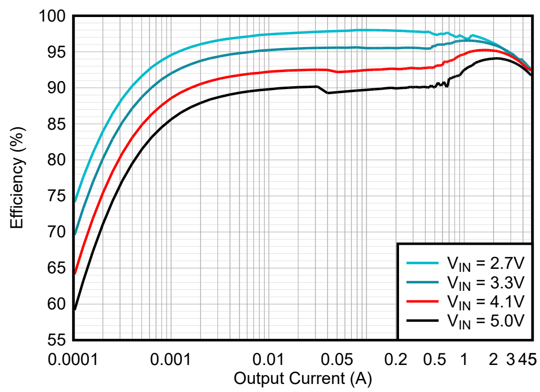
V_{OUT} = 3.3V T_A = 25°C   TPSM82A823, TPSM82A824

Figure 8-2. Efficiency



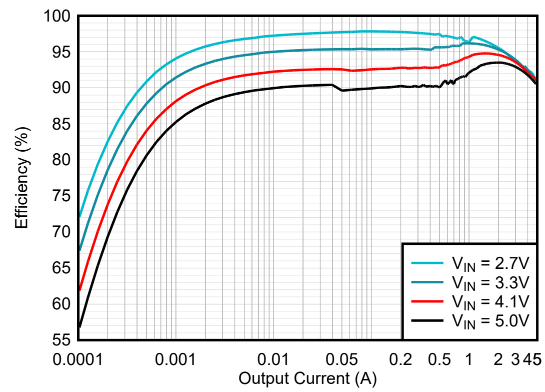
V_{OUT} = 3.3V T_A = 85°C   TPSM82A823, TPSM82A824

Figure 8-3. Efficiency



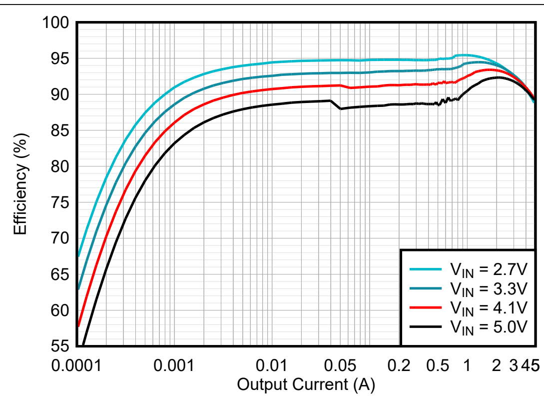
V_{OUT} = 2.5V T_A = 25°C   TPSM82A823, TPSM82A824

Figure 8-4. Efficiency



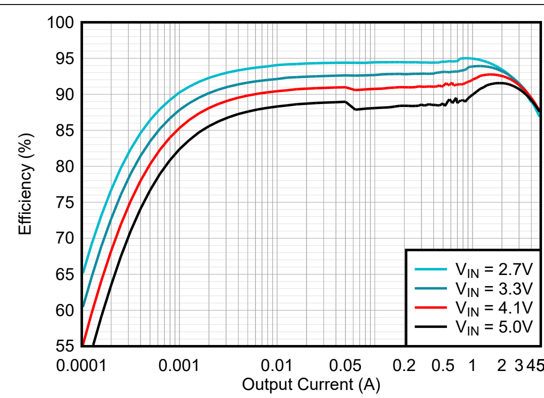
V_{OUT} = 2.5V T_A = 85°C   TPSM82A823, TPSM82A824

Figure 8-5. Efficiency



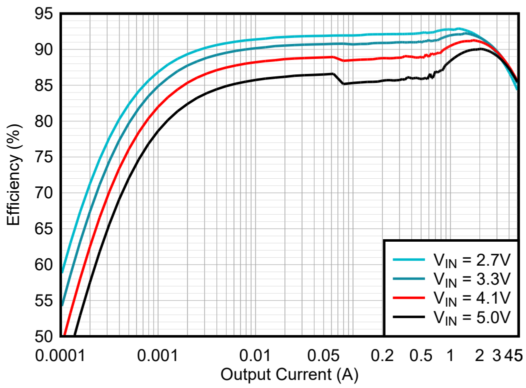
V_{OUT} = 1.8V T_A = 25°C   TPSM82A823, TPSM82A824

Figure 8-6. Efficiency



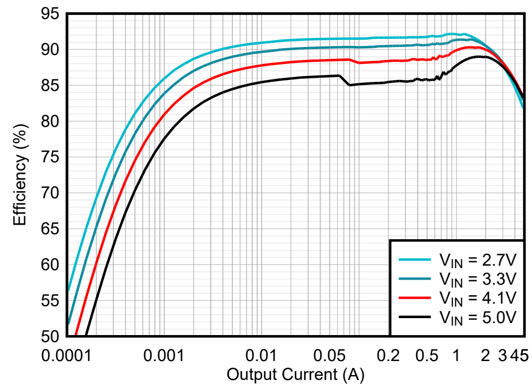
V_{OUT} = 1.8V T_A = 85°C   TPSM82A823, TPSM82A824

Figure 8-7. Efficiency



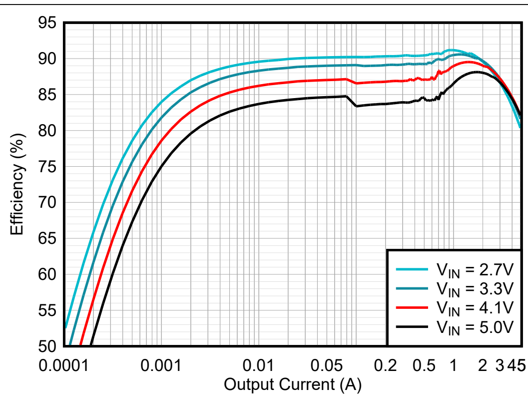
V_{OUT} = 1.2V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-8. Efficiency



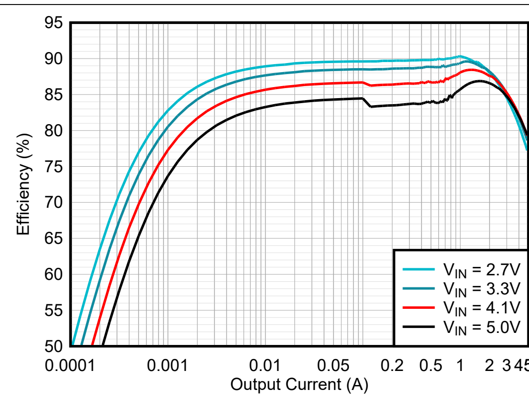
V_{OUT} = 1.2V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-9. Efficiency



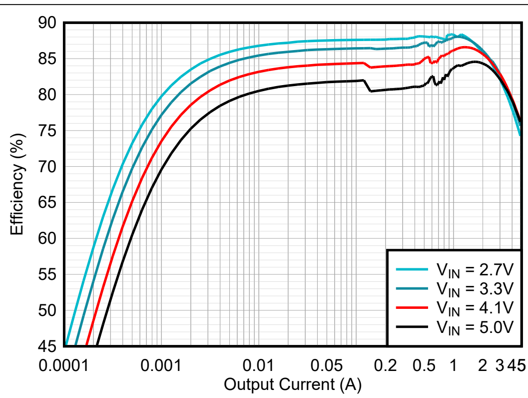
V_{OUT} = 0.9V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-10. Efficiency



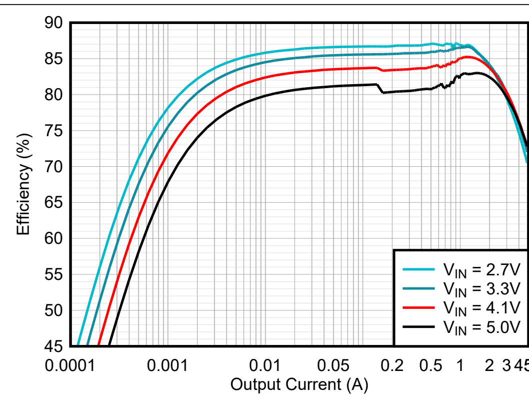
V_{OUT} = 0.9V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-11. Efficiency



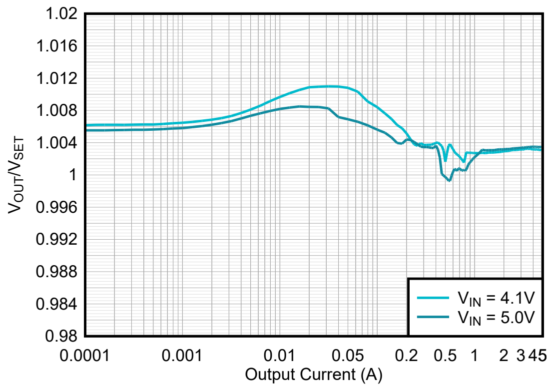
V_{OUT} = 0.6V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-12. Efficiency



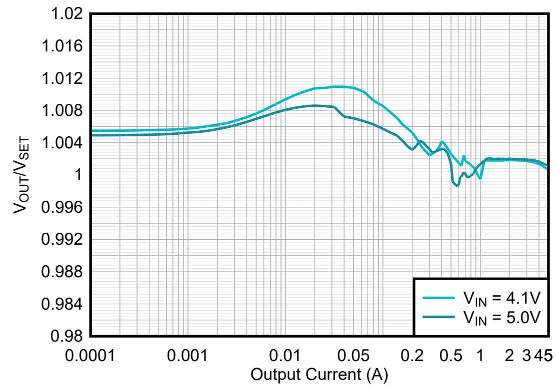
V_{OUT} = 0.6V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-13. Efficiency



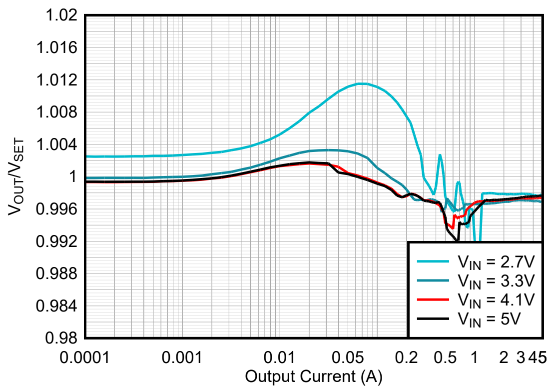
V_{OUT} = 3.3V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-14. VOUT Accuracy



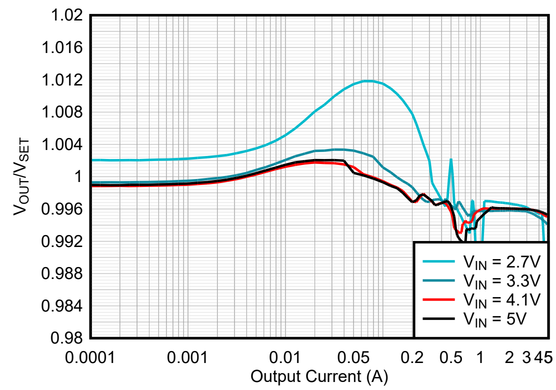
V_{OUT} = 3.3V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-15. VOUT Accuracy



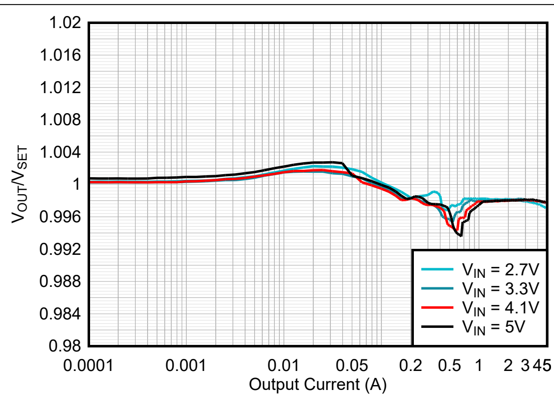
V_{OUT} = 2.5V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-16. VOUT Accuracy



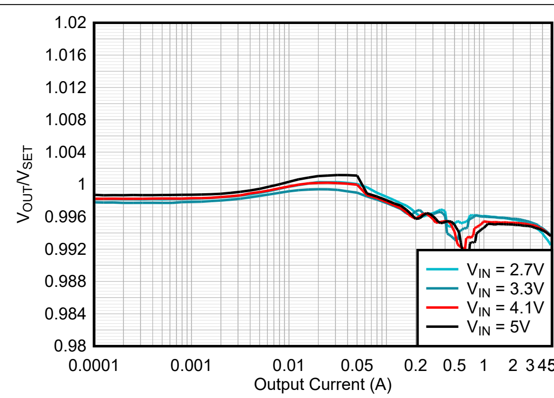
V_{OUT} = 2.5V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-17. VOUT Accuracy



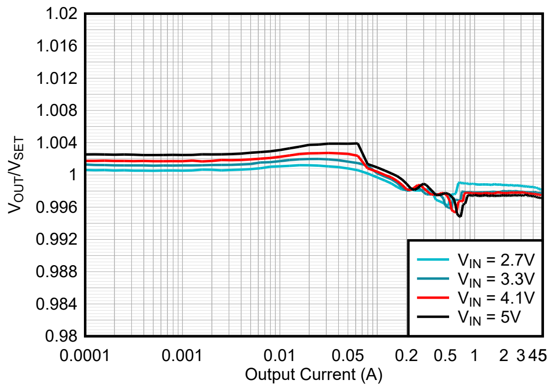
V_{OUT} = 1.8V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-18. VOUT Accuracy



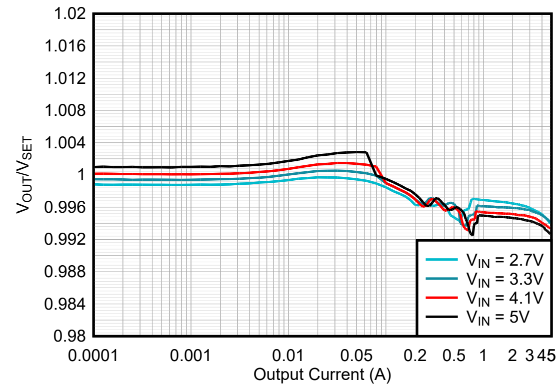
V_{OUT} = 1.8V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-19. VOUT Accuracy



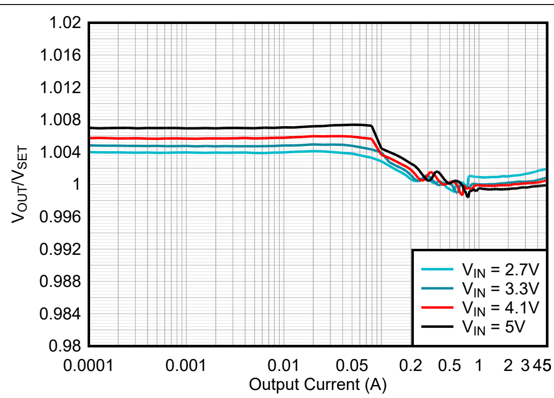
V_{OUT} = 1.2V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-20. VOUT Accuracy



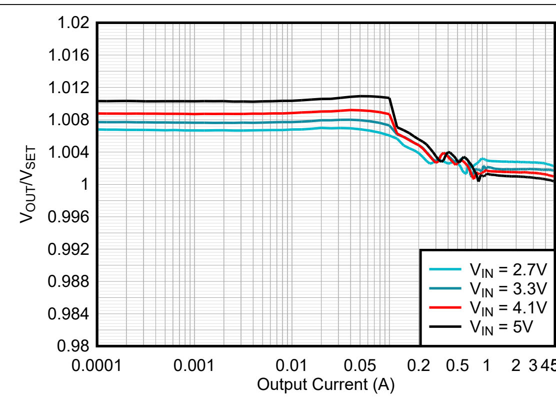
V_{OUT} = 1.2V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-21. VOUT Accuracy



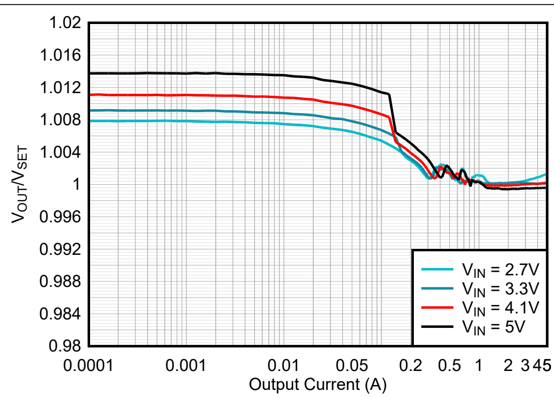
V_{OUT} = 0.9V T_A = 25°C TPSM82A823, TPSM82A824

Figure 8-22. VOUT Accuracy



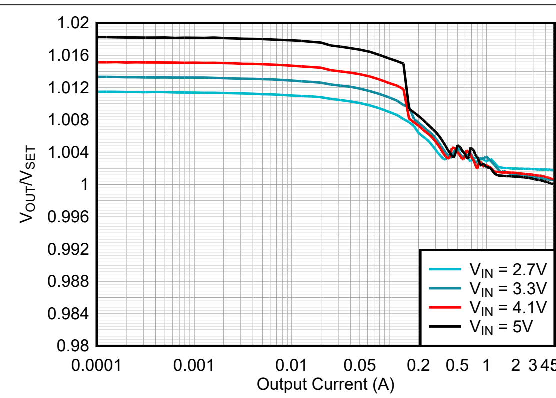
V_{OUT} = 0.9V T_A = 85°C TPSM82A823, TPSM82A824

Figure 8-23. VOUT Accuracy



V_{OUT} = 0.6V T_A = 25°C TPSM82A823, TPSM82A824

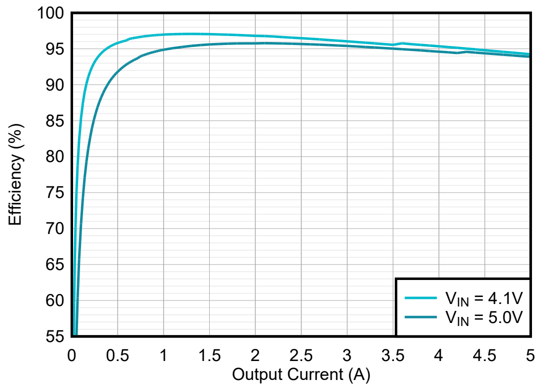
Figure 8-24. VOUT Accuracy



V_{OUT} = 0.6V T_A = 85°C TPSM82A823, TPSM82A824

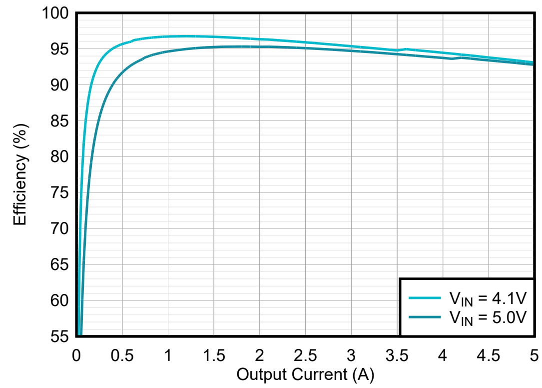
Figure 8-25. VOUT Accuracy

8.2.3.2 PWM Performance Curves



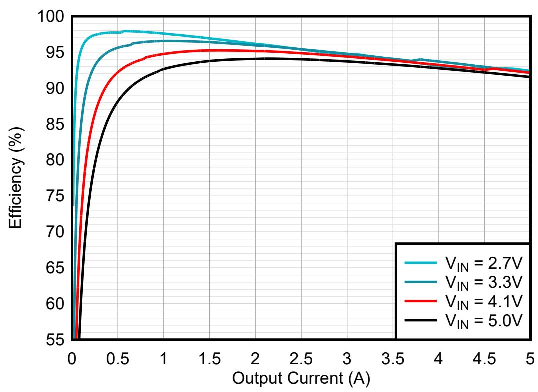
V_{OUT} = 3.3V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-26. Efficiency



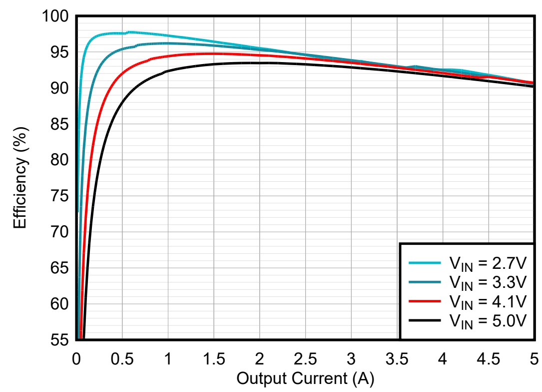
V_{OUT} = 3.3V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-27. Efficiency



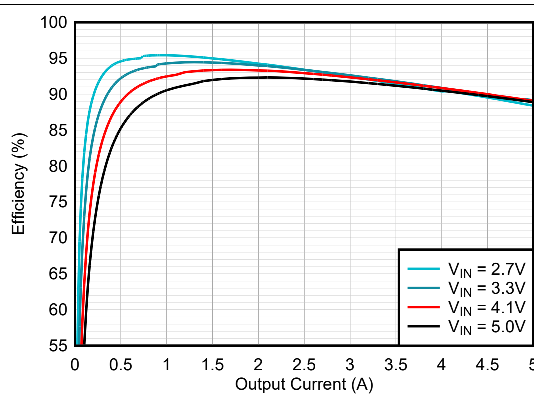
V_{OUT} = 2.5V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-28. Efficiency



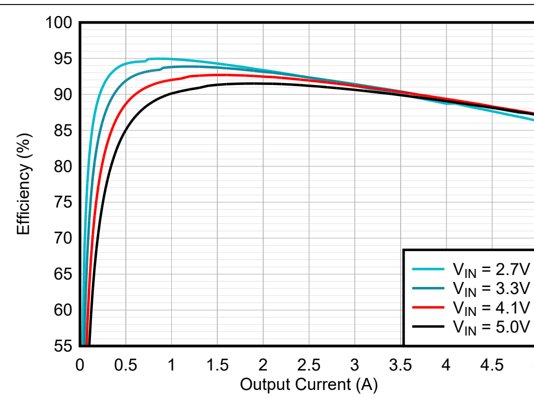
V_{OUT} = 2.5V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-29. Efficiency



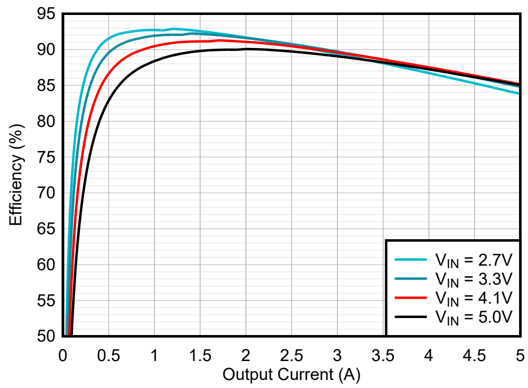
V_{OUT} = 1.8V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-30. Efficiency



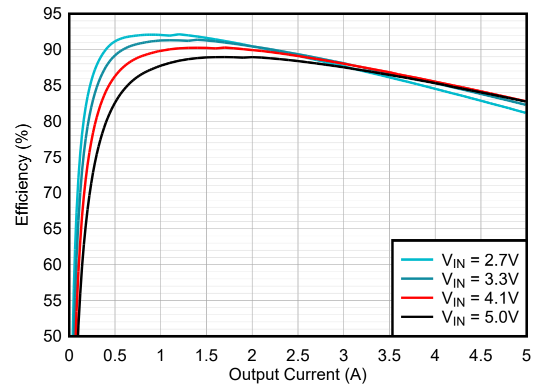
V_{OUT} = 1.8V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-31. Efficiency



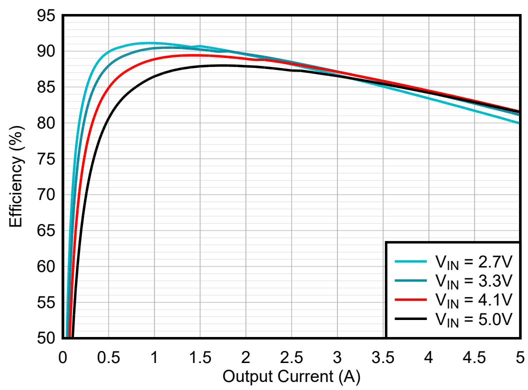
V_{OUT} = 1.2V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-32. Efficiency



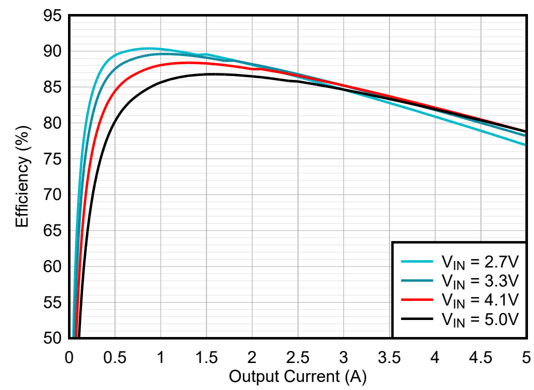
V_{OUT} = 1.2V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-33. Efficiency



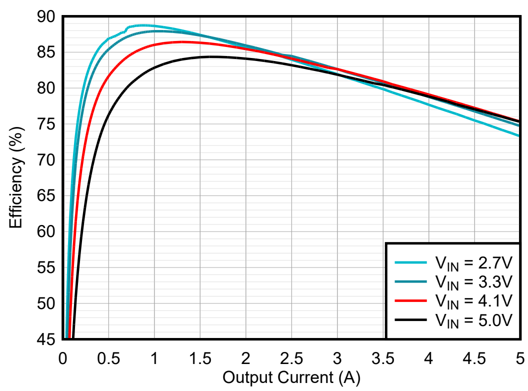
V_{OUT} = 0.9V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-34. Efficiency



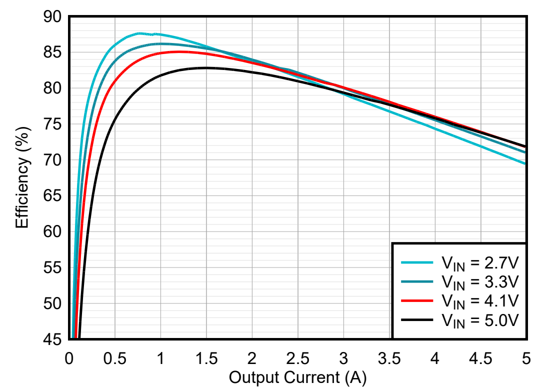
V_{OUT} = 0.9V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-35. Efficiency



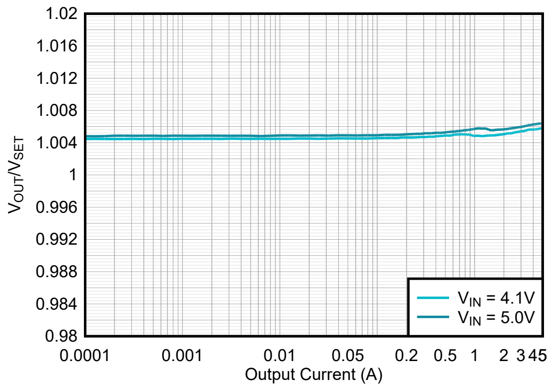
V_{OUT} = 0.6V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-36. Efficiency



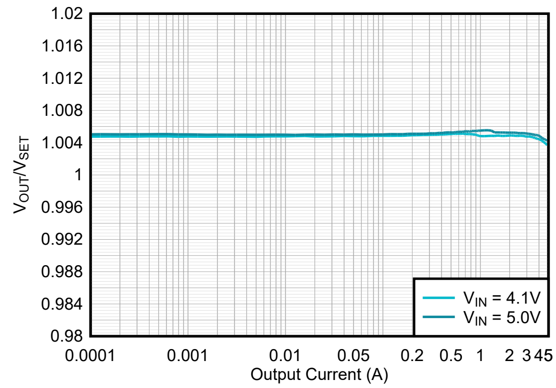
V_{OUT} = 0.6V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-37. Efficiency



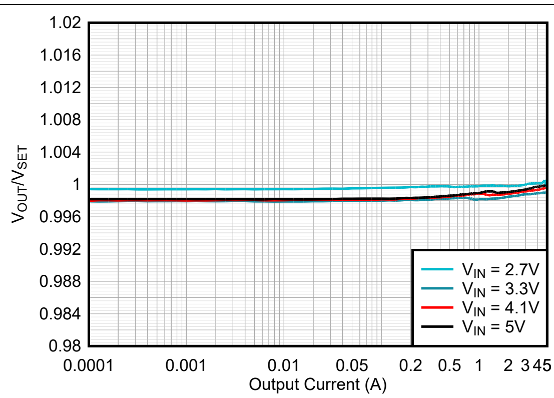
V_{OUT} = 3.3V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-38. VOUT Accuracy



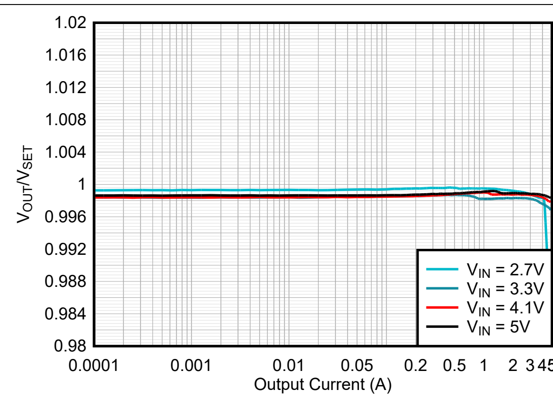
V_{OUT} = 3.3V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-39. VOUT Accuracy



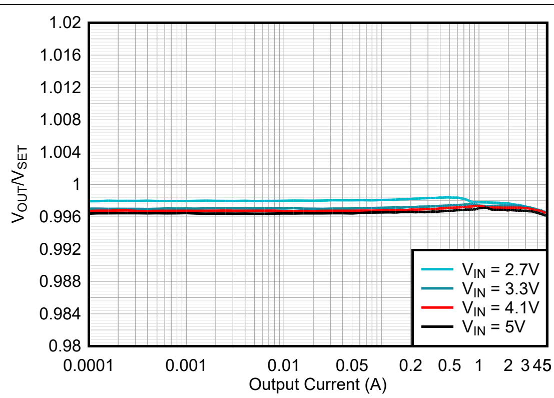
V_{OUT} = 2.5V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-40. VOUT Accuracy



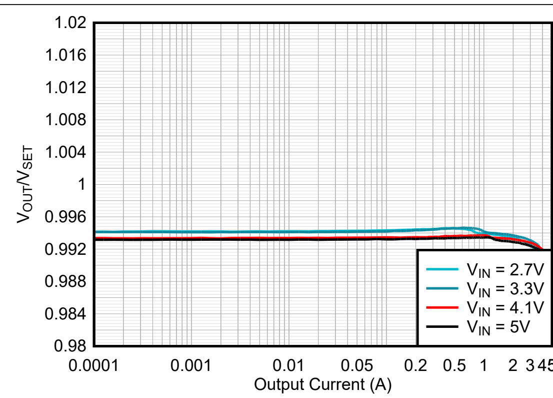
V_{OUT} = 2.5V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-41. VOUT Accuracy



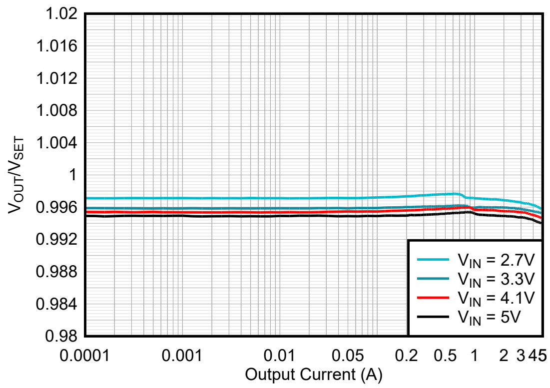
V_{OUT} = 1.8V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-42. VOUT Accuracy



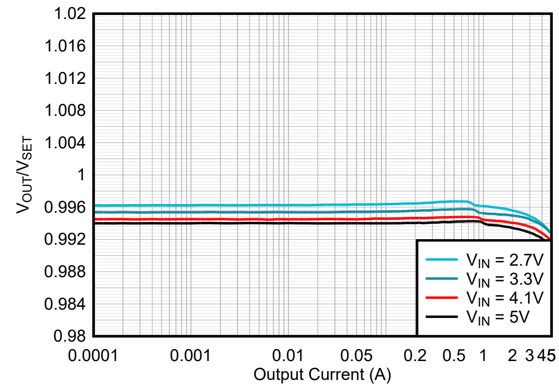
V_{OUT} = 1.8V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-43. VOUT Accuracy



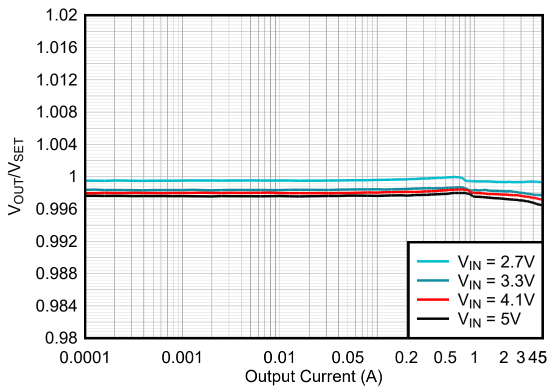
V_{OUT} = 1.2V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-44. VOUT Accuracy



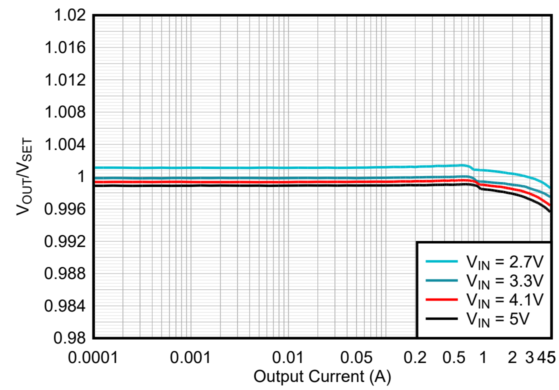
V_{OUT} = 1.2V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-45. VOUT Accuracy



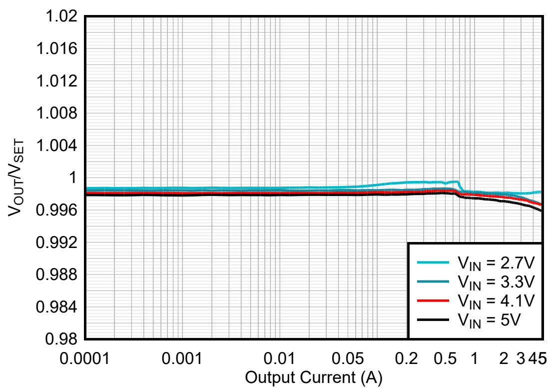
V_{OUT} = 0.9V T_A = 25°C TPSM82A823A, TPSM82A824A

Figure 8-46. VOUT Accuracy



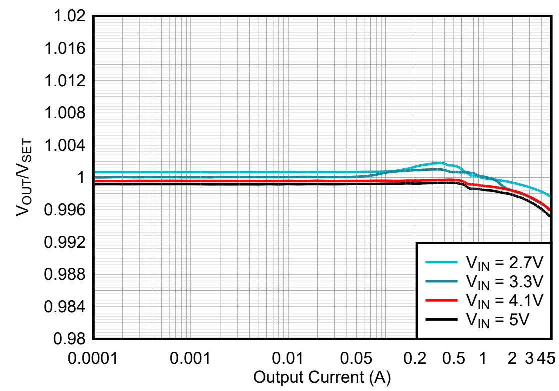
V_{OUT} = 0.9V T_A = 85°C TPSM82A823A, TPSM82A824A

Figure 8-47. VOUT Accuracy



V_{OUT} = 0.6V T_A = 25°C TPSM82A823A, TPSM82A824A

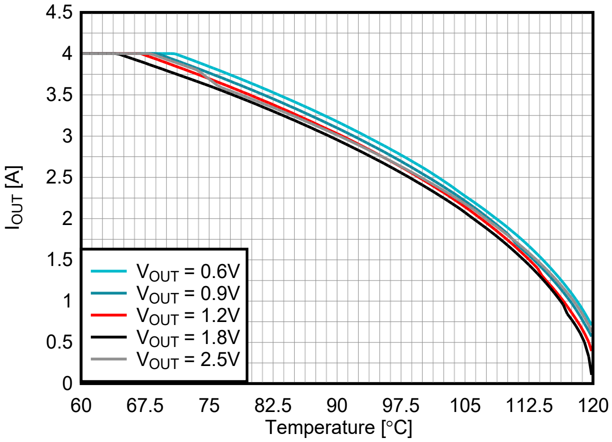
Figure 8-48. VOUT Accuracy



V_{OUT} = 0.6V T_A = 85°C TPSM82A823A, TPSM82A824A

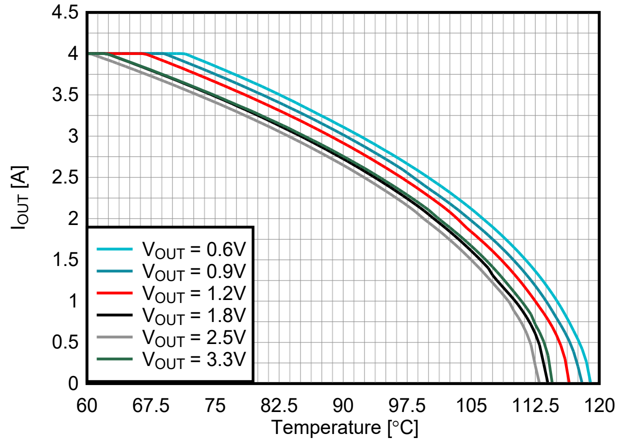
Figure 8-49. VOUT Accuracy

8.2.3.3 Application Curves



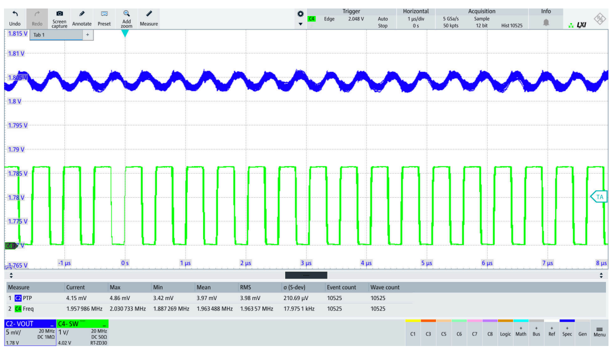
V_{IN} = 3.3V TPSM82A823A, TPSM82A824A

Figure 8-50. Safe Operating Area



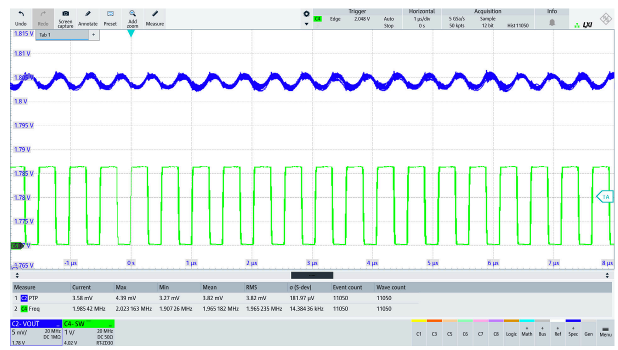
V_{OUT} = 5.0V TPSM82A823A, TPSM82A824A

Figure 8-51. Safe Operating Area



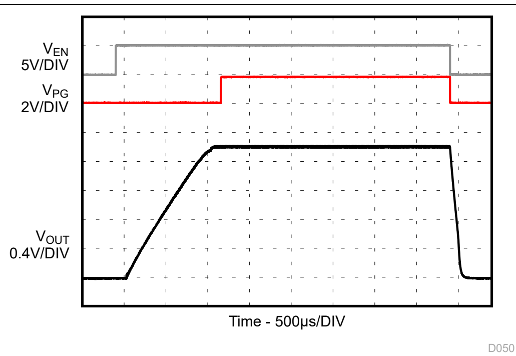
I_{OUT} = 3A 2 × 22µF TPSM82A823A, TPSM82A824A

Figure 8-52. Output Ripple in PWM Mode



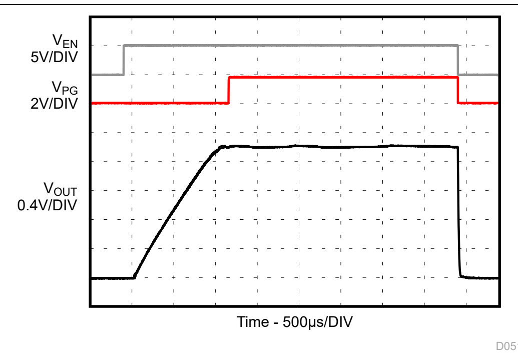
I_{OUT} = 3A 3 × 22µF TPSM82A823A, TPSM82A824A

Figure 8-53. Output Ripple in PWM Mode



I_{OUT} = no load TPSM82A823A, TPSM82A824A

Figure 8-54. Start-Up / Shutdown Without Load



I_{OUT} = 3A TPSM82A823A, TPSM82A824A

Figure 8-55. Start-Up / Shutdown With Resistive Load

8.3 Power Supply Recommendations

The devices are designed to operate from an input supply voltage range between 2.5V and 5.5V. Use the following equation to calculate the average input current of the TPSM82A823x and TPSM82A824x:

$$I_{\mathrm{IN}} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{4}$$

Verify that the power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM82A823x and TPSM82A824x demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. See also the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin to minimize noise pickup.
- The recommended layout is implemented on the EVM and shown in the *TPSM8282xEVM-080 and TPSM8282xAEVM-127 Evaluation Modules* user's guide.
- The recommended land pattern for the TPSM82A823x and TPSM82A824x is shown at the end of this datasheet. For best manufacturing results, make sure to create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

8.4.2 Layout Example

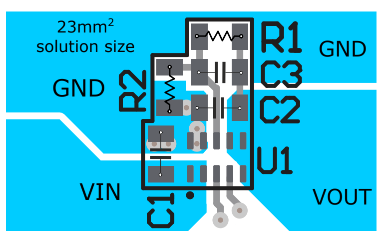


Figure 8-56. TPSM82A823x PCB Layout for the Adjustable Devices (BOM as per List of Components With 2 × 22uF for C2)

This example is preliminary to show the principle. The final layout includes additional 2 × 22µF added to C2.

8.4.2.1 Thermal Consideration

The TPSM82A823x module temperature must be kept below the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM82A823x, apply the typical efficiency stated in this datasheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrate the required derating in maximum output current at high ambient temperatures. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Development Support

9.1.2.1 Models and Simulators

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM82822EVM-080 Evaluation Module* EVM user's guide
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*
- Texas Instruments, *TPSM8282xEVM-080 and TPSM8282xAEVM-127 Evaluation Modules* user's guide
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

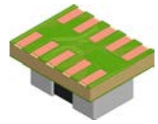
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

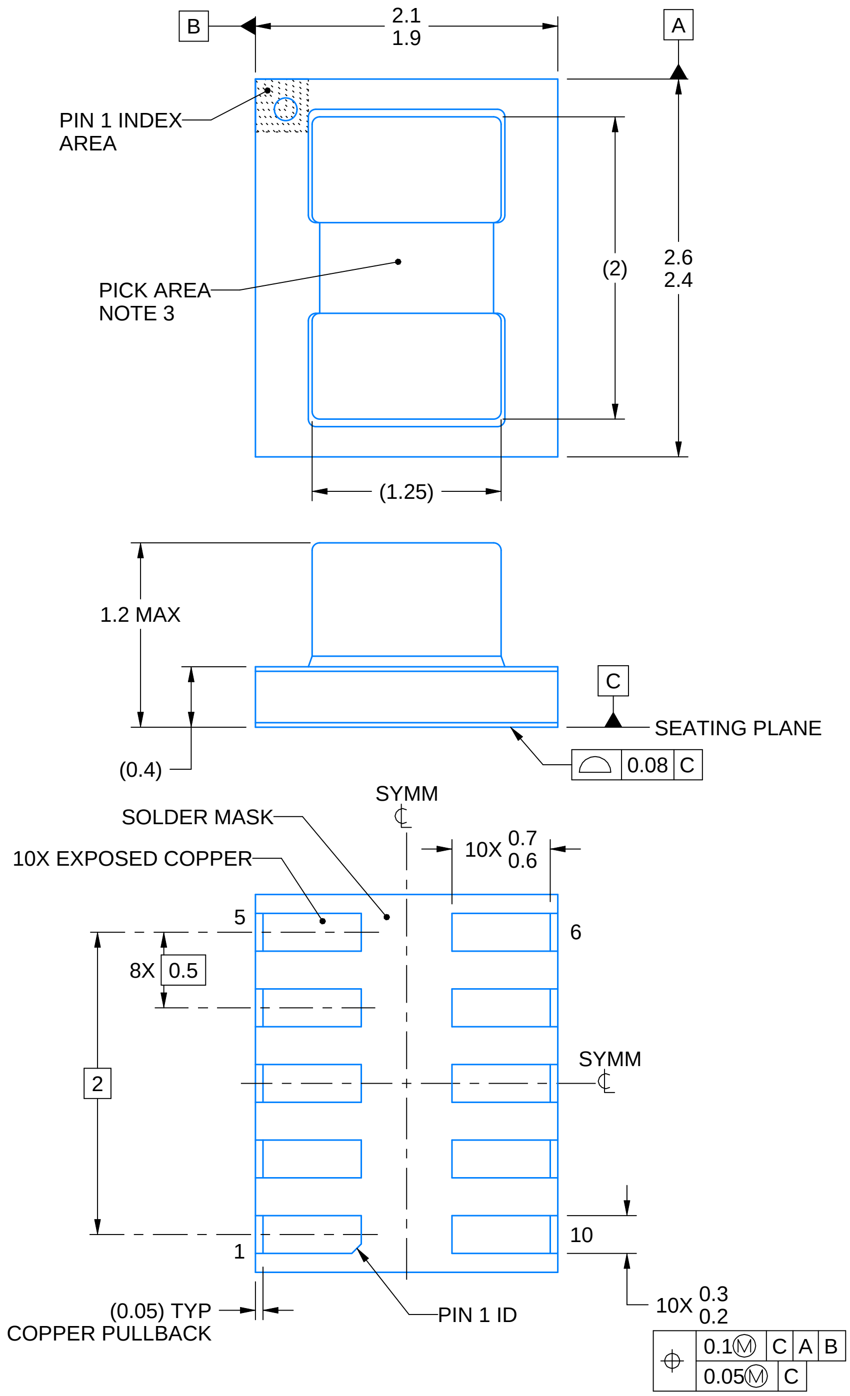
10 Revision History

DATE	REVISION	NOTES
July 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





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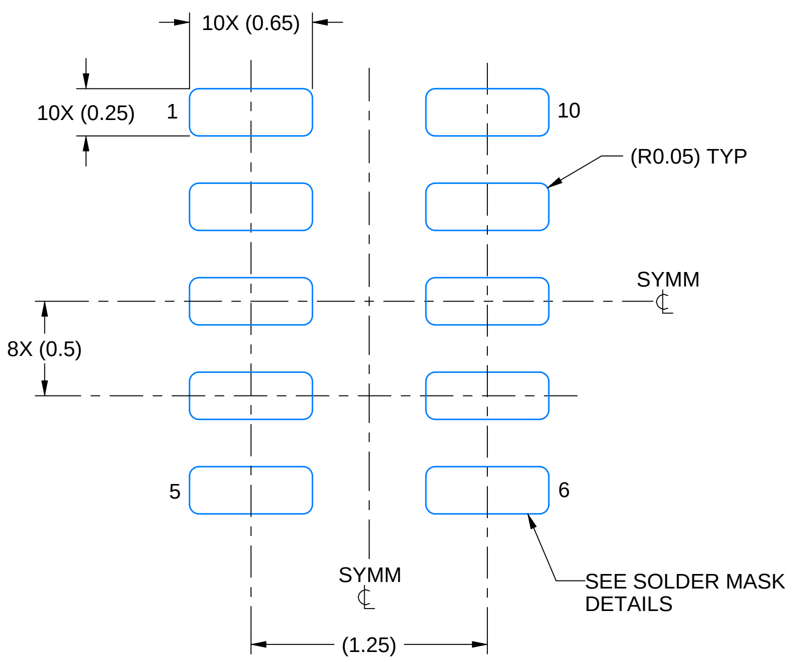
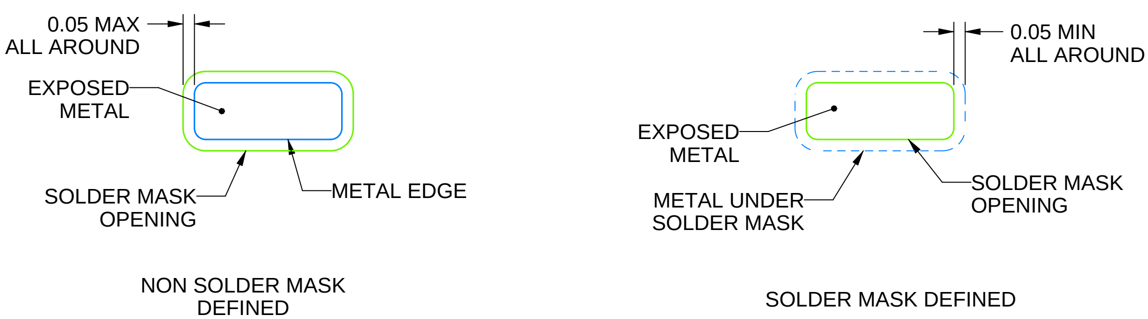
NOTES:

MicroSiP is a trademark of Texas Instruments

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 0.33 mm or smaller recommended.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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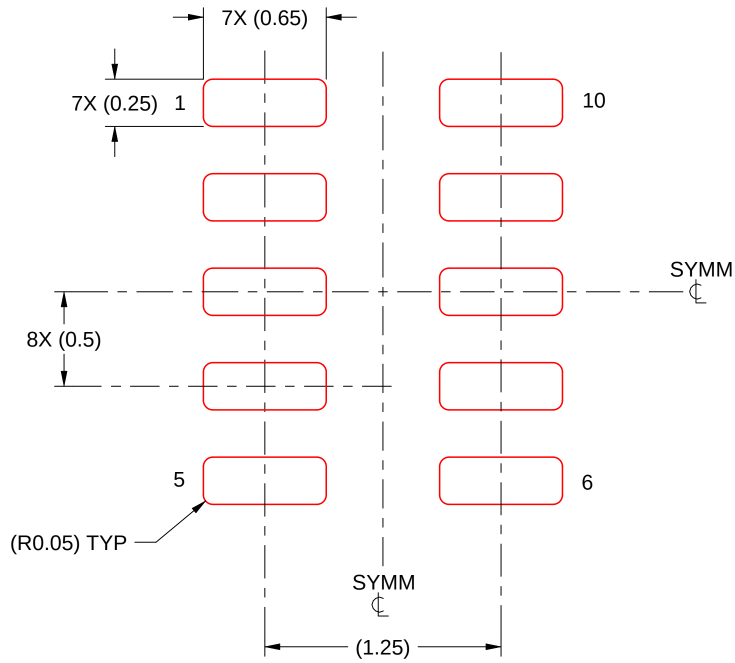
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.