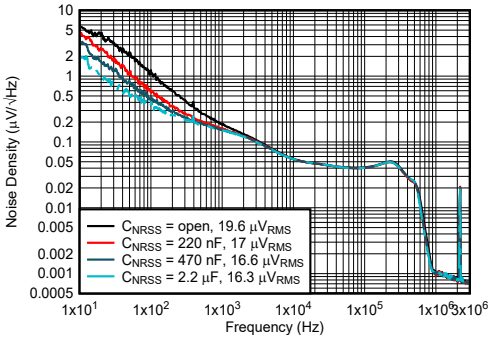
TPSM8291x 具有集成式铁氧体磁珠滤波器补偿的 3V 至 17V、2A/3A 低噪声和低纹波降压电源模块

1 特性

- 低输出噪声 < 20μV_{RMS}（100Hz 至 100kHz）
- 采用铁氧体磁珠后，低输出电压纹波 < 10μV_{RMS}
- 大于 65dB 的高 PSRR（高达 100kHz）
- 2.2MHz 或 1MHz 定频峰值电流模式控制
- 可与外部时钟同步（可选）
- 集成环路补偿支持铁氧体磁珠，适用于具有 30dB 衰减的二阶 L-C 滤波器（可选）
- 展频调制（可选）
- 3.0V 至 17V 输入电压范围
- 0.8V 至 5.5V 输出电压范围
- 57mΩ/20mΩ R_{DSon}
- 输出电压精度为 ±1%
- 精密使能输入可实现
  - 用户定义的欠压锁定
  - 准确排序
- 可调节软启动
- 电源正常状态输出
- 输出放电（可选）
- -40°C 至 125°C 的结温范围
  - -ET 版本为 –55°C 至 125°C
- 使用 TPSM8291x 并借助 WEBENCH® Power Designer 创建定制设计

2 应用

- 电信基础设施
- 测试和测量
- 航天和国防（雷达、航空电子设备）
- 医疗



输出噪声与频率间的关系

3 说明

TPSM8291x 器件是一系列高效、低噪声和低纹波电流模式同步降压电源模块。这些器件非常适合通常使用 LDO 实现后置稳压的噪声敏感型应用，例如高速 ADC、时钟和抖动清除器、串行器、解串器和雷达应用。

这些器件在 2.2MHz 或 1MHz 的固定开关频率下工作，并可与外部时钟同步。

为了进一步减小输出电压纹波，器件集成了环路补偿，可与可选的第二级铁氧体磁珠 L-C 滤波器一起工作。该功能可将输出电压纹波降至 10μV_{RMS} 以下。

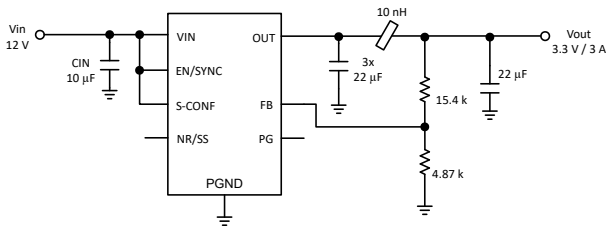
通过使用 NR/SS 引脚上的集成电容器对内部电压基准进行滤波来实现类似于低噪声 LDO 的低频噪声水平。可以在模块中添加一个外部电容器以进行额外的滤波。

可选展频调制方案扩展了更宽范围内的直流/直流开关频率，从而降低了混合毛刺。

器件信息

器件名称	输出电流	封装(1)	封装尺寸（标称值）
TPSM82912	2A	RDU（QFN，28）	4.50 mm × 5.50 mm × 1.80 mm
TPSM82913、TPSM82913E	3A		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 2023) to Revision C (July 2023) — **Page**

- 删除了 *器件信息* 表中的 TPSM82912 预发布状态 1

Changes from Revision A (December 2022) to Revision B (May 2023) — **Page**

- 从 *器件信息* 表中删除了 TPSM82912-ET 1
- 在 *器件信息* 表中将 TPSM82913-ET 更新为 TPSM82913E 并删除了预发布状态 1
- Added -ET temp range in the *Electrical Characteristics* table 4

Changes from Revision * (October 2022) to Revision A (December 2022) — **Page**

- 将数据表状态从“预告信息”更改为“混合量产” 1

5 Pin Configuration and Functions

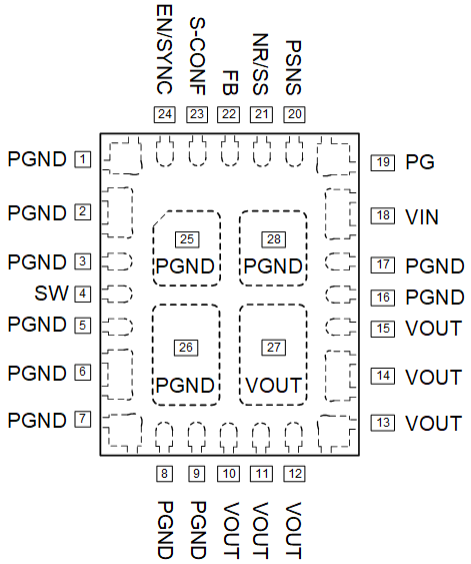


图 5-1. 28-Pin QFN RDU Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
18	VIN	I	Power supply input voltage pin
1, 2, 3, 5, 6, 7, 8, 9, 16, 17, 25, 26, 28	PGND		Power ground connection
10, 11, 12, 13, 14, 15, 27	VOUT	O	Output connection. Connect recommended output capacitance from VOUT to PGND.
4	SW	NC	Switch pin of the power stage. Do not connect, leave floating.
19	PG	O	Open-drain power-good output. This pin is pulled to GND when V_{OUT} is below the power-good threshold. It requires a pull-up resistor to output a logic high. It can be left open or tied to GND if not used.
20	PSNS	I	Power sense ground. Connect directly to the ground plane.
21	NR/SS	O	A capacitor connected to this pin sets the soft-start time and low frequency noise level of the device.
22	FB	I	Feedback pin of the device
23	S-CONF	O	Smart Configuration pin. This pin configures the operation modes of the device. See 表 7-1.
24	EN/SYNC	I	Enable/Disable pin including threshold-comparator. Connect to logic low to disable the device. Pull high to enable the device. This pin has an internal pull-down resistor of typically 500 kΩ when the device is disabled. Apply a clock to this pin to synchronize the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN/SYNC, PG, S-CONF	–0.3	18	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC, less than 10ns)(3)	–2.5	21	V
	VOUT, FB, NR/SS	–0.3	6	V
	PSNS	–0.3	0.3	V
Sink Current	PG		10	mA
T_J	Junction temperature, -ET versions only	–55	125	°C
T_{stg}	Storage temperature	–65	125	°C
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.0		17	V
V_{OUT}	Output voltage	0.8		5.5	V
C_{IN}	Effective input capacitance	5	10		µF
C_{OUT}	Effective output capacitance	40	47	80	µF
L_f	Effective filter inductance	0	10	50	nH
C_f	Effective filter capacitance	20	40	160	µF
C_{OUT} + C_f	Effective total output capacitance, including first and second L-C filter	40		200	µF
I_{OUT}	Output current for TPSM82913	0		3	A
I_{OUT}	Output current for TPSM82912	0		2	A
T_J (1)	Junction temperature	–40		125	°C
T_J (1)	Junction temperature, -ET versions only	–55		125	°C

(1) Operating lifetime is derated at junction temperatures above 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		TPSM8291x		UNIT
		RDU 30-pin QFN		
		JEDEC 51-7 PCB	TPSM8291xEVM-213	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.4	n/a [2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	n/a [2]	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	-4.9 [3]	-3.0 [3]	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.1	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM
(3) This is a negative value because the case temperature is higher than the die junction temperature due to the integrated inductor having the highest power dissipation in the module.

6.5 Electrical Characteristics

Over recommended input voltage range, T_J = -40 ℃ to 125 ℃, (T_J = -55 ℃ to 125 ℃ for -ET parts). Typical values are at Vin = 12 V andT_J = 25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device switching, fsw = 1 MHz		5		mA
I_{SD}	Shutdown current	EN = GND		0.3	70	µA
V_{UVLO}	Under voltage lockout	V_{IN} rising	2.85	2.92	3.0	V
V_{UVLO}	Under voltage lockout	V_{IN} rising			3.04	V
V_{HYS}	Under voltage lockout hysteresis			200		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
CONTROL and INTERFACE						
V_{H_EN}	High-level input-threshold voltage at EN/SYNC		0.97	1.01	1.04	V
V_{L_EN}	Low-level input-threshold voltage at EN/SYNC		0.87	0.9	0.93	V
V_{H_SYNC}	High-level input-threshold clock signal on EN/SYNC	EN/SYNC = clock	1.1			V
V_{L_SYNC}	Low-level input-threshold clock signal on EN/SYNC	EN/SYNC = clock			0.4	V
$I_{EN,LKG}$	Input leakage current into EN/SYNC	EN/SYNC = GND or VIN		5	160	nA
R_{PD}	Pull-down resistor on EN/SYNC	EN/SYNC = Low	330	500		kΩ
t_{delay}	Enable delay time	Time from EN/SYNC high to device starts switching, R_{S-CONF} = 80.6 kΩ		1		ms
$I_{NR/SS}$	NR/SS source current		67.5	75	82.5	µA
R_{S-CONF}	S-CONF resistor step range accuracy	R_{S-CONF} tolerance for all settings according to 表 7-1	-4		+4	%
C_{S-CONF}	Maximum capacitance connected to S-CONF pin				30	pF
V_{PG}	Power good threshold	V_{FB} rising, referenced to V_{FB} nominal	93	95	98	%
V_{PG}	Power good threshold	V_{FB} falling, referenced to V_{FB} nominal	88	90	93	%
$V_{PG,OL}$	Low-level output voltage at PG pin	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5 V		5	500	nA

6.5 Electrical Characteristics (continued)

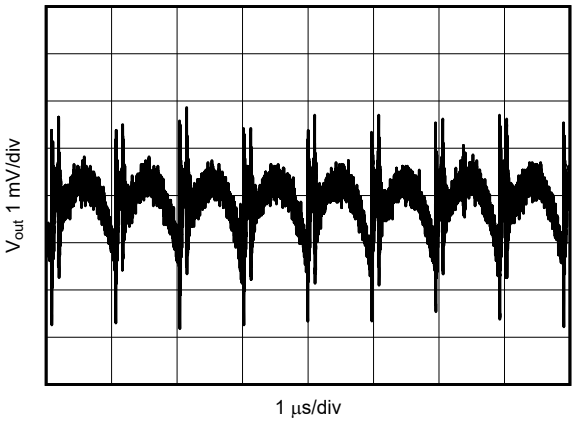
Over recommended input voltage range, T_J = -40 ℃ to 125 ℃, (T_J = -55 ℃ to 125 ℃ for -ET parts). Typical values are at Vin = 12 V andT_J = 25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PG,DLY}$	Power good delay time	V_{FB} falling		8		µs
OUTPUT						
t_{on}	Minimum on-time	$V_{IN} \geqslant$ 5 V, I_{out} = 1 A		35	70	ns
t_{off}	Minimum off-time	$V_{IN} \geqslant$ 5 V, I_{out} = 1 A		50	60	ns
V_{FB}	Feedback regulation accuracy	–40℃ ⩽ T_J ⩽ 125℃	0.792	0.8	0.808	V
$I_{FB,LKG}$	Input leakage current into FB	V_{FB} = 0.8 V		1	70	nA
PSRR	Power supply rejection ratio	V_{IN} = 12 V, 1.2 V_{OUT}, 1 A, $C_{NR/SS}$ = 220 nF, f_{sw} = 1 MHz, C_{FF} = open, C_{OUT} = 3 x 22 µF, f ⩽ 100 kHz		65		dB
V_{NRMS}	Output voltage RMS noise	V_{IN} = 12 V, BW = 100 Hz to 100 kHz, $C_{NR/SS}$ = 220 nF, f_{SW} = 1 MHz, V_{OUT} = 1.2 V, C_{FF} = open, C_{OUT} = 3 x 22 µF		27.4		μV_{RMS}
V_{NRMS}	Output voltage RMS noise	V_{IN} = 5 V, BW = 100 Hz to 100 kHz, $C_{NR/SS}$ = 220 nF, f_{SW} = 2.2 MHz, V_{OUT} = 1.2 V, C_{FF} = open, C_{OUT} = 3 x 22 µF		13.3		μV_{RMS}
V_{opp}	Output ripple voltage at f_{SW}	V_{IN} = 12 V, f_{SW} = 1 MHz, V_{OUT} = 1.2 V, C_{OUT} = 3 x 22 µF, L_f = 10 nH, C_f = 2 x 22 µF		9		μV_{RMS}
V_{opp}	Output ripple voltage at f_{SW}	V_{IN} = 5 V, f_{SW} = 2.2 MHz, V_{OUT} = 1.2V, C_{OUT} = 3 x 22 µF, L_f = 10 nH, C_f = 2 x 22 uF		< 3		μV_{RMS}
R_{DIS}	Output discharge resistance	EN/SYNC = GND, V_{OUT} = 1.2 V, $V_{IN} \geqslant$ 5 V. See 节 6.6 for plot.		7		Ω
R_{DIS}	Output discharge resistance	EN/SYNC = GND, V_{OUT} = 5 V, $V_{IN} \geqslant$ 5 V. See 节 6.6 for plot.		32		Ω
f_{SW}	Switching frequency	2.2-MHz setting	1.98	2.2	2.42	MHz
f_{SW}	Synchronization range	2.2-MHz setting	1.9	2.2	2.42	MHz
f_{SW}	Switching frequency	1-MHz setting	0.9	1	1.18	MHz
f_{SW}	Synchronization range	1-MHz setting	0.86	1	1.2	MHz
D_{SYNC}	Synchronization duty cycle		45		55	%
t_{sync_delay}	Synchronization phase delay	Phase delay from EN/SYNC rising edge to SW rising edge		90		ns
I_{SWpeak}	Peak switch current limit	TPSM82912(1)	2.9	3.5	4.0	A
I_{SWpeak}	Peak switch current limit	TPSM82913	3.7	4.3	5.1	A
$I_{SWvalley}$	Valley switch current limit	TPSM82912(1)		3.4		A
$I_{SWvalley}$	Valley switch current limit	TPSM82913		4.2		A
$Ineg_{valley}$	Negative valley current limit			-1.39	-0.96	A
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geqslant$ 5 V		57	95	mΩ
	Low-side FET on-resistance	$V_{IN} \geqslant$ 5 V		20	39	mΩ

(1) Preview information

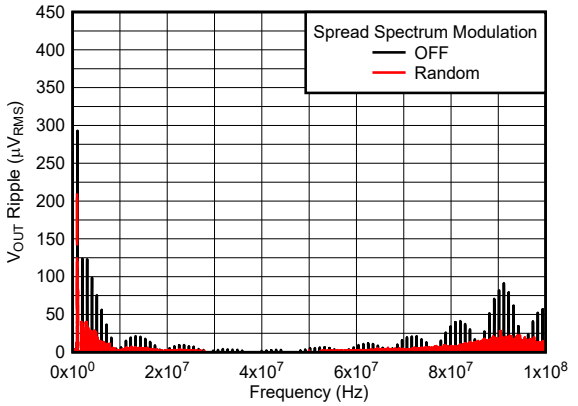
6.6 Typical Characteristics

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



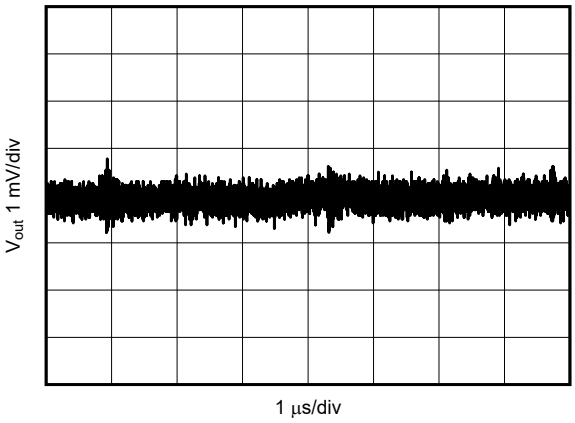
12 V to 1.2 V, 1 A 2.2 µH, 1 MHz First L-C Only

图 6-1. V_{OUT} Ripple After the First L-C Filter



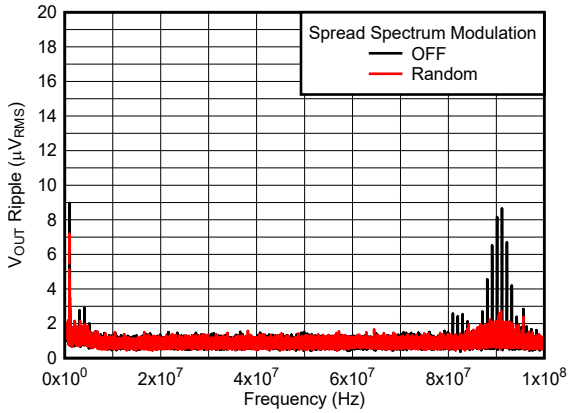
12 V to 1.2 V, 1 A 2.2 µH, 1 MHz First L-C Only

图 6-2. V_{OUT} Ripple FFT After the First L-C Filter



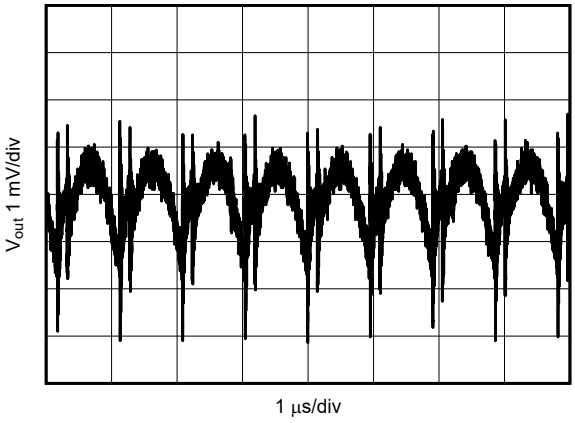
12 V to 1.2 V, 1 A 2.2 µH, 1 MHz First and second L-C

图 6-3. V_{OUT} Ripple After the Second L-C Filter



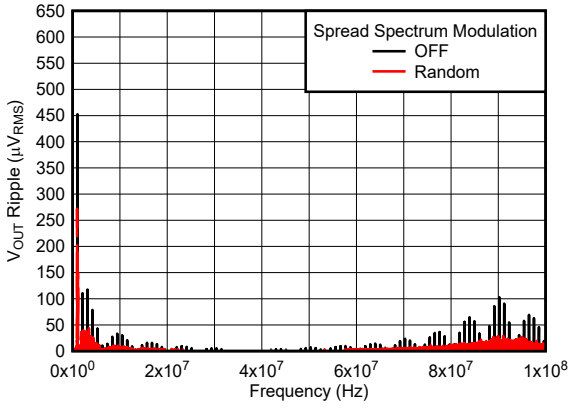
12 V to 1.2 V, 1 A 2.2 µH, 1 MHz First and second L-C

图 6-4. V_{OUT} Ripple FFT After the Second L-C Filter



12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First L-C Only

图 6-5. V_{OUT} Ripple After the First L-C Filter

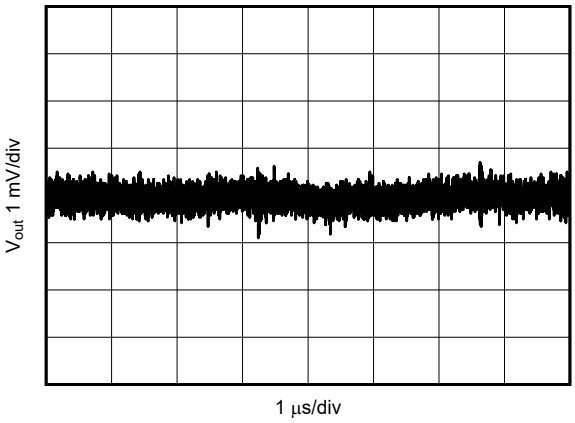


12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First L-C Only

图 6-6. V_{OUT} Ripple FFT After the First L-C Filter

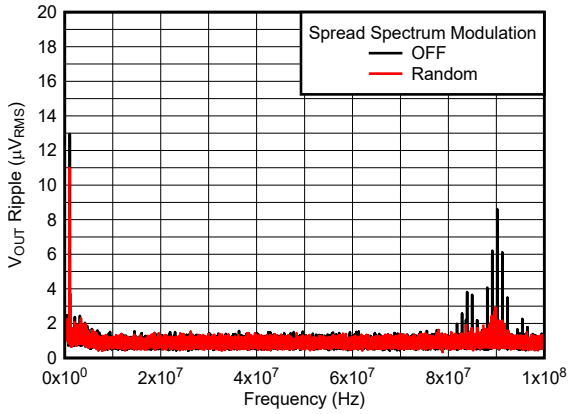
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First and second L-C

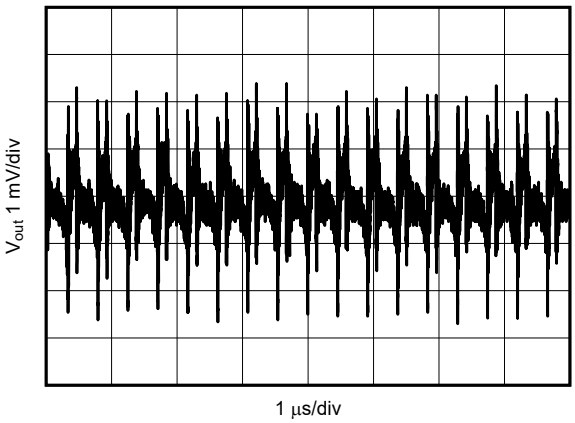
图 6-7. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

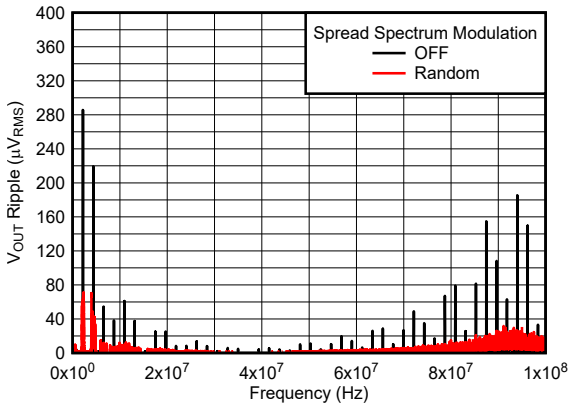
12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First and second L-C

图 6-8. V_{OUT} Ripple FFT After the Second L-C Filter



12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

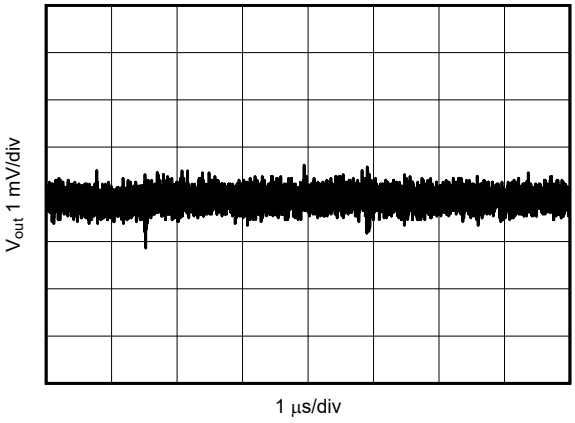
图 6-9. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

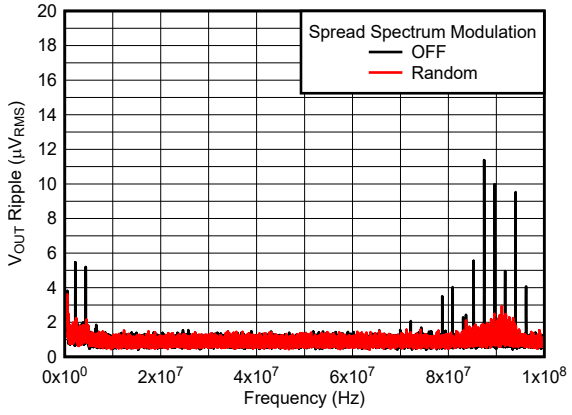
12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

图 6-10. V_{OUT} Ripple FFT After the First L-C Filter



12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-11. V_{OUT} Ripple After the Second L-C Filter



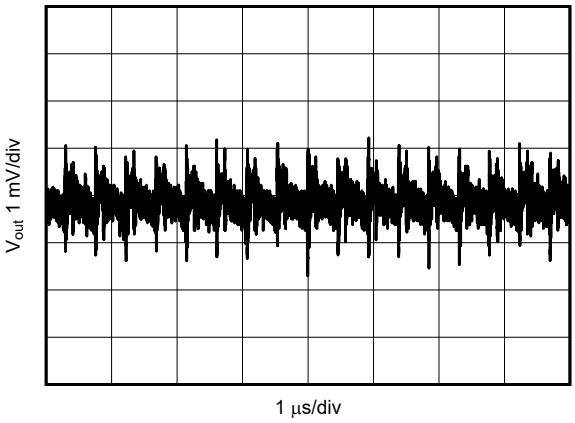
BW = 10 kHz

12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-12. V_{OUT} Ripple FFT After the Second L-C Filter

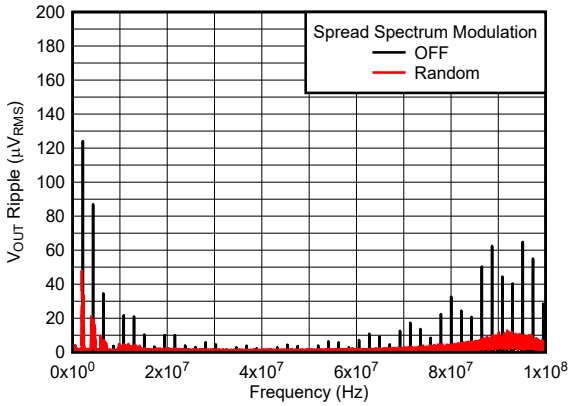
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



5 V to 1.2 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

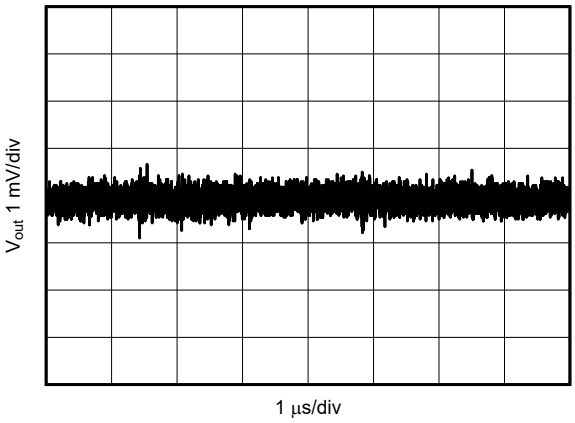
图 6-13. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

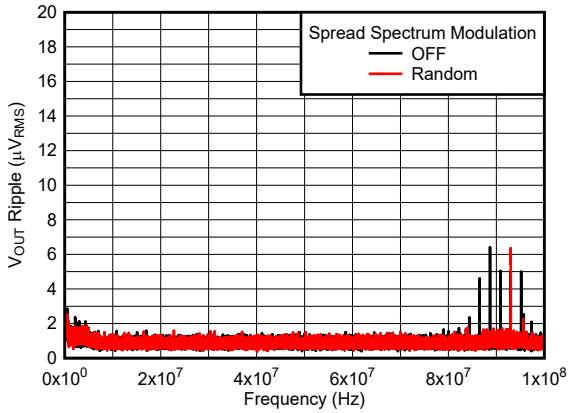
5 V to 1.2 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

图 6-14. V_{OUT} Ripple FFT After the First L-C Filter



5 V to 1.2 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

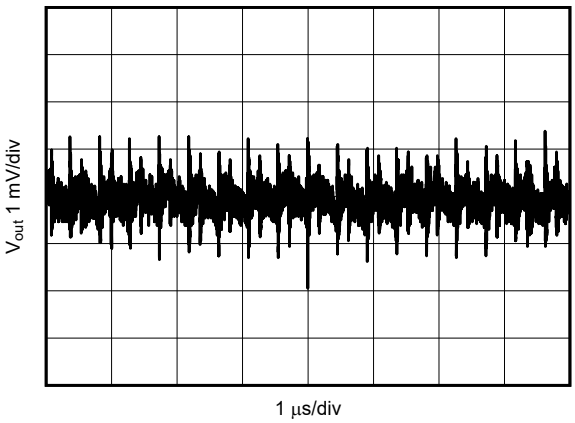
图 6-15. V_{OUT} Ripple after the Second L-C Filter



BW = 10 kHz

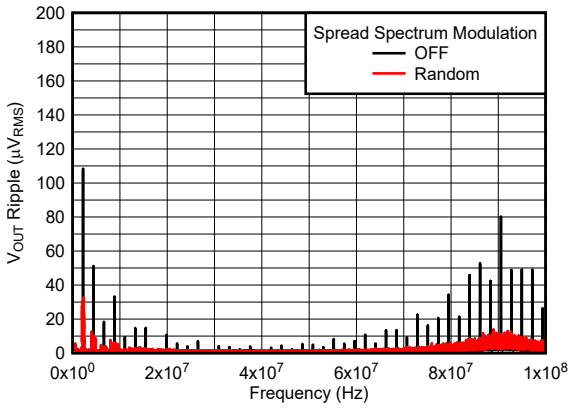
5 V to 1.2 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-16. V_{OUT} Ripple FFT After the Second L-C Filter



5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

图 6-17. V_{OUT} Ripple After the First L-C Filter



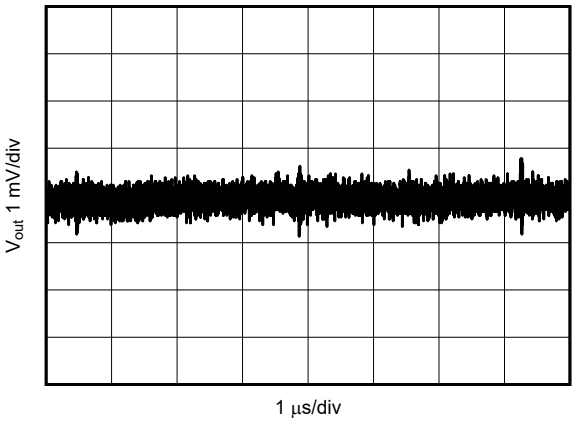
BW = 10 kHz

5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

图 6-18. V_{OUT} Ripple FFT After the First L-C Filter

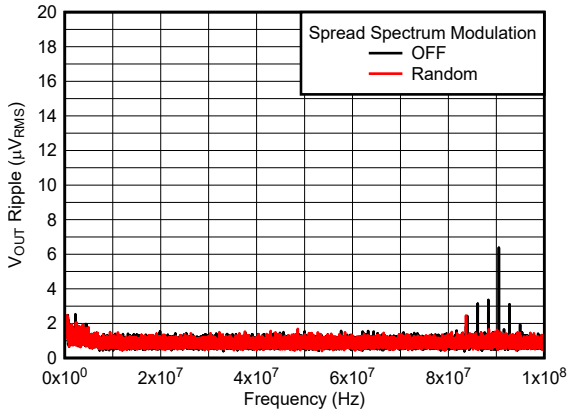
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

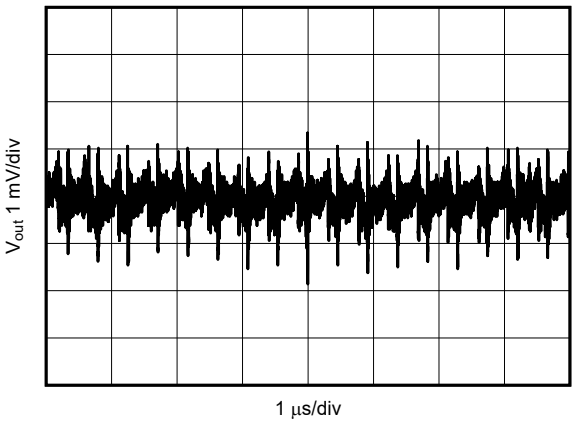
图 6-19. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

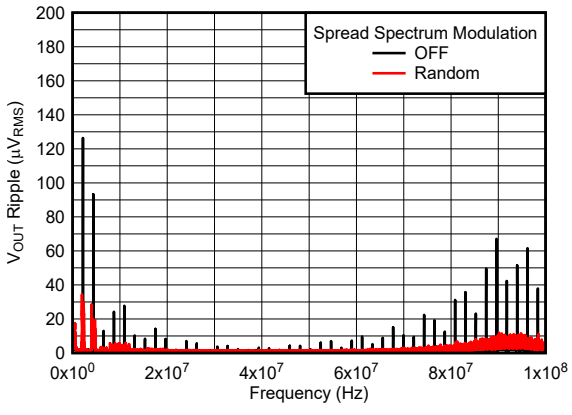
5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-20. V_{OUT} Ripple FFT After the Second L-C Filter



5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

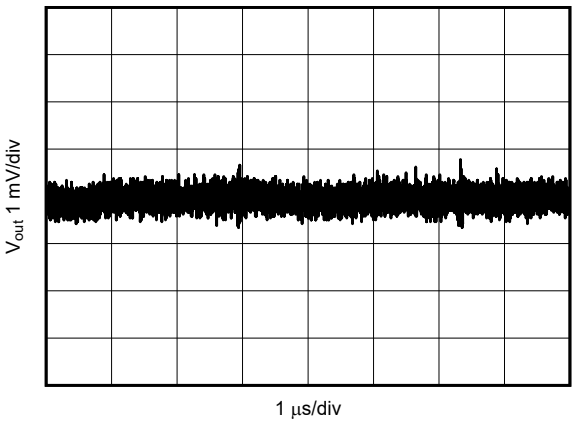
图 6-21. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

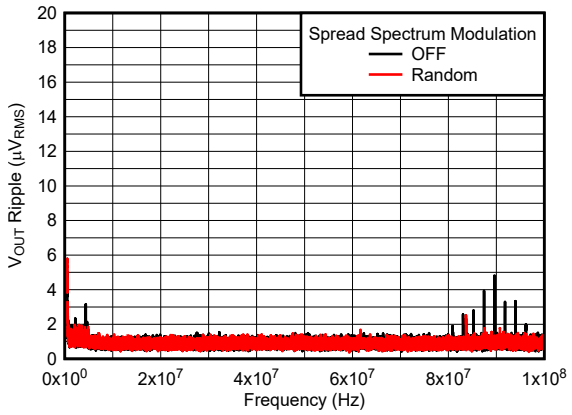
5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

图 6-22. V_{OUT} Ripple FFT After the First L-C Filter



5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-23. V_{OUT} Ripple After the Second L-C Filter



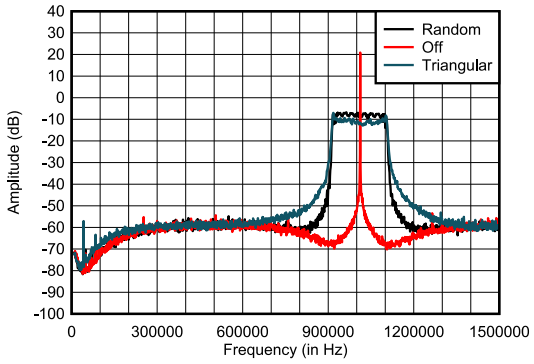
BW = 10 kHz

5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

图 6-24. V_{OUT} Ripple FFT After the Second L-C Filter

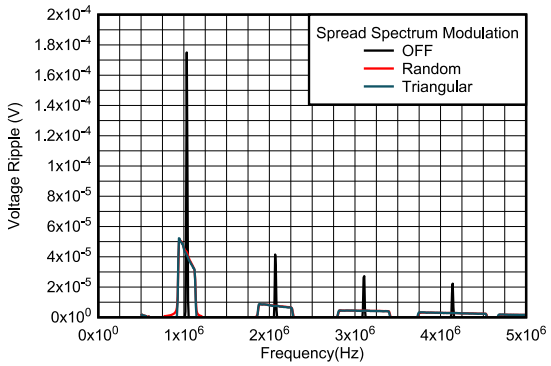
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



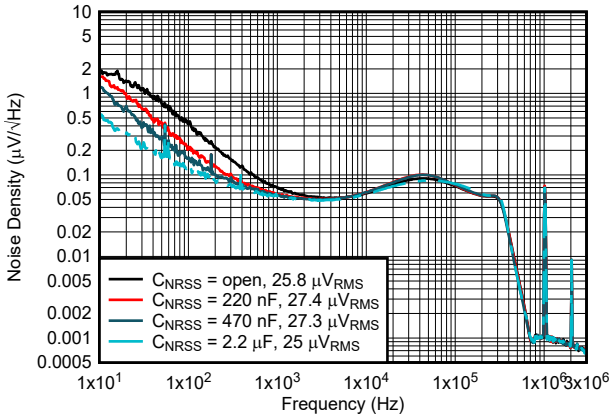
6 V to 1.2 V, 1 A 2.2 µH, 1 MHz BW = 50 Hz
S-CONF = OFF, Triangular, Random

图 6-25. Spread Spectrum FFT - 50-Hz BW



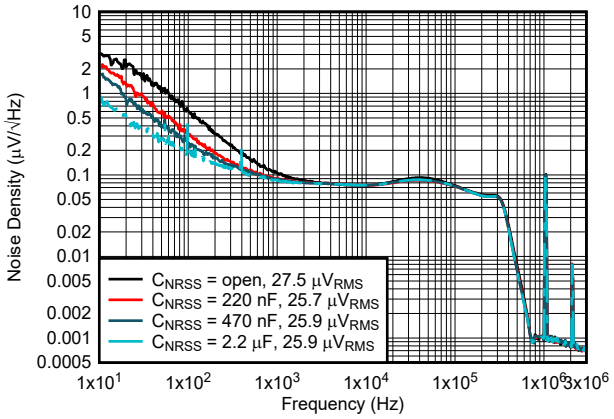
12 V to 1.2 V, 2 A 2.2 µH, 1 MHz BW = 10 kHz
S-CONF = OFF, Triangular, Random

图 6-26. Spread Spectrum FFT - 10-kH BW



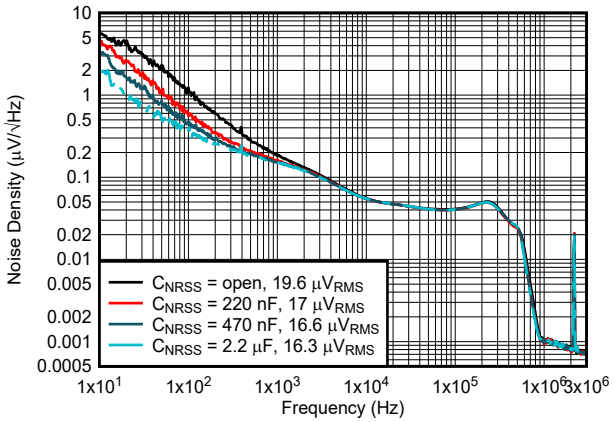
12 V to 1.2 V 1 MHz After ferrite bead filter
NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

图 6-27. Output Noise Density vs Frequency



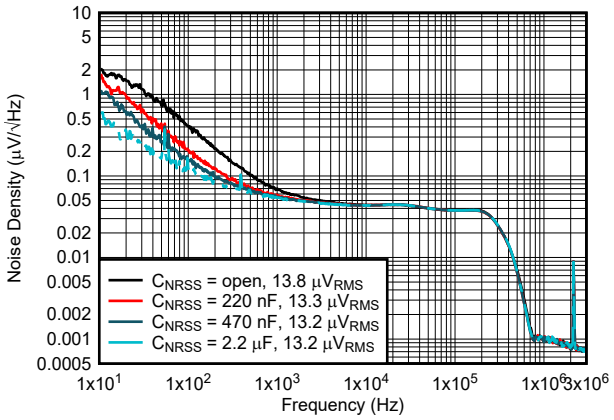
12 V to 1.8 V 1 MHz After ferrite bead filter
NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

图 6-28. Output Noise Density vs Frequency



12 V to 3.3 V 2.2 MHz After ferrite bead filter
NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

图 6-29. Output Noise Density vs Frequency

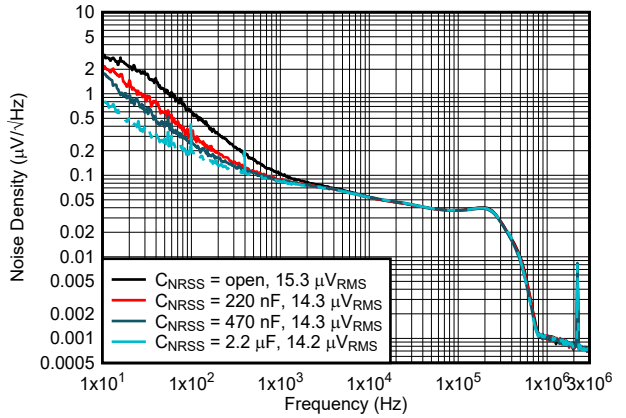


5 V to 1.2 V 2.2 MHz After ferrite bead filter
NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

图 6-30. Output Noise Density vs Frequency

6.6 Typical Characteristics (continued)

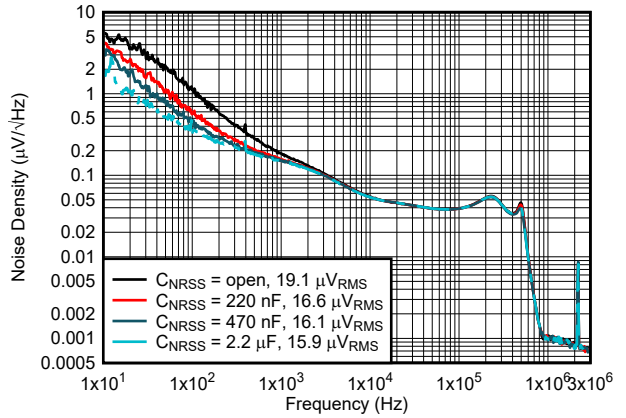
V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



5 V to 1.8 V 2.2 MHz After ferrite bead filter

NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

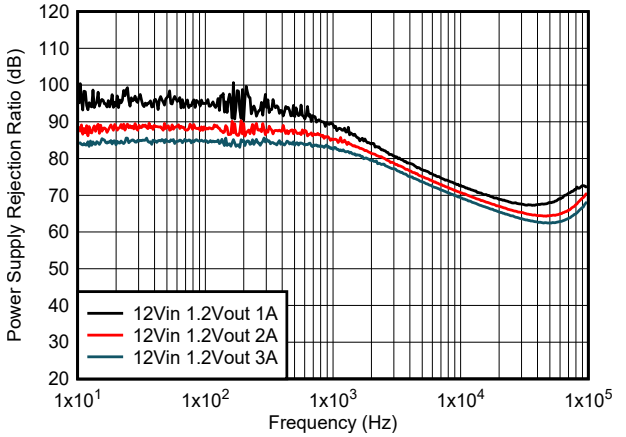
图 6-31. Output Noise Density vs Frequency



5 V to 3.3 V 2.2 MHz After ferrite bead filter

NR/SS = Open, 220 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

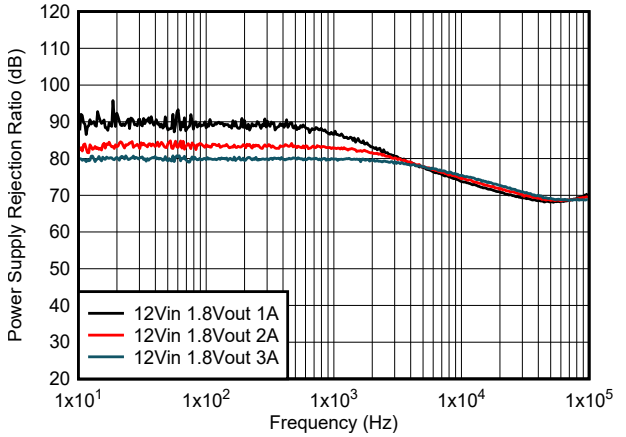
图 6-32. Output Noise Density vs Frequency



12 V to 1.2 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

After ferrite bead filter

图 6-33. PSRR vs Frequency



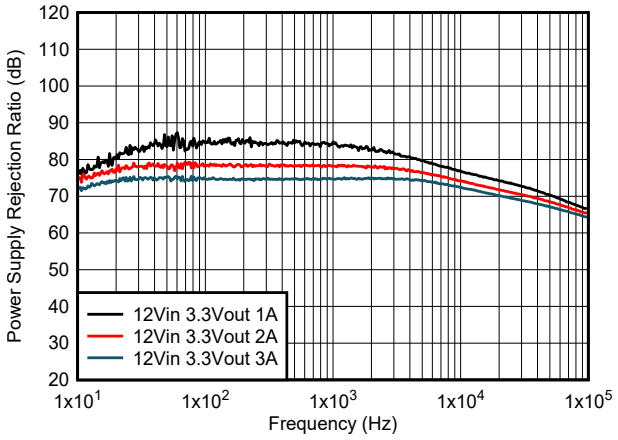
12 V to 1.8 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

After ferrite bead filter

图 6-34. PSRR vs Frequency

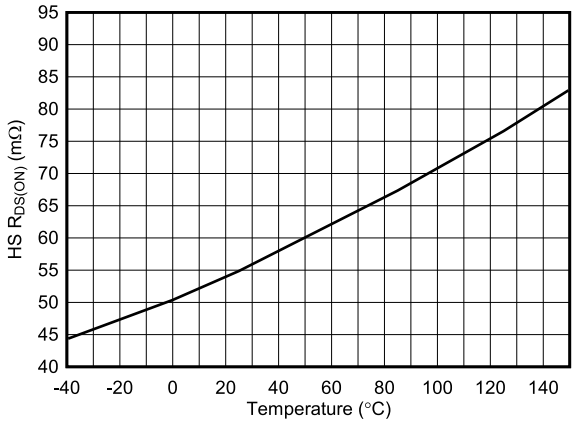
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



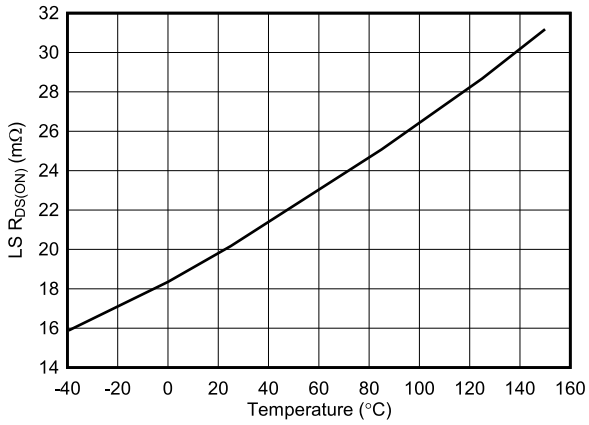
12 V to 3.3 V　2.2 μH, 2.2 MHz After ferrite bead filter　1 A, 2 A, 3 A

图 6-35. PSRR vs Frequency



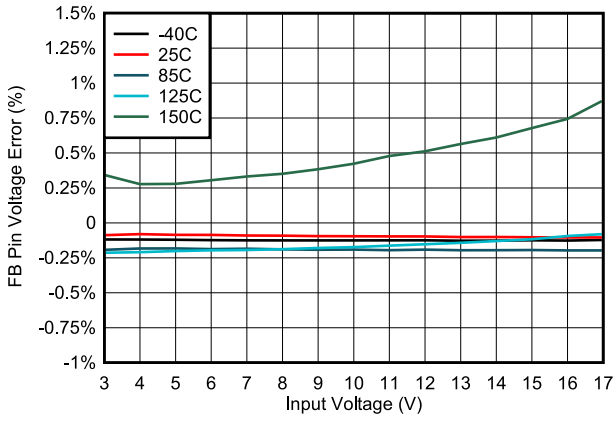
VIN = 5 V

图 6-36. High-Side $R_{DS(ON)}$ vs Junction Temperature



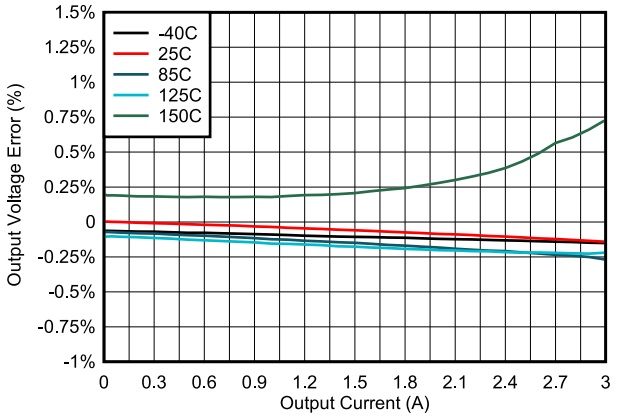
VIN = 5 V

图 6-37. Low-Side $R_{DS(ON)}$ vs Junction Temperature



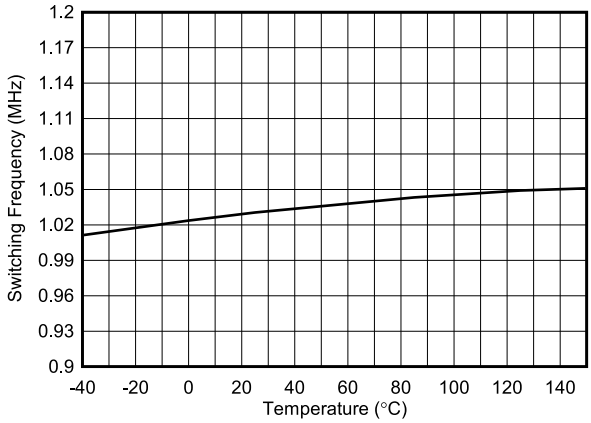
1 MHz, 2 A

图 6-38. FB Pin Voltage Error vs Input Voltage



5 V_{IN} to 0.8 V_{OUT}　1 MHz

图 6-39. Output Voltage Error vs Load

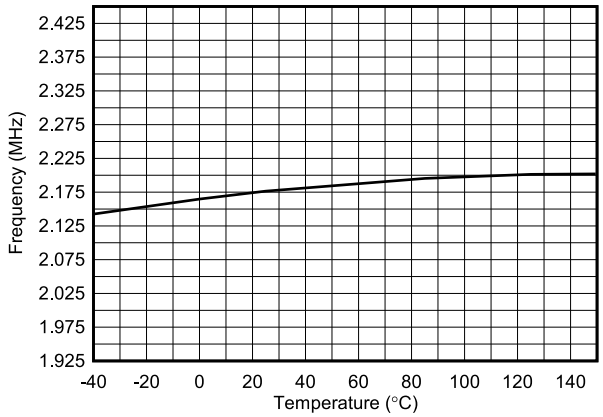


12 V_{IN}　1 MHz

图 6-40. Oscillator Frequency vs Temperature

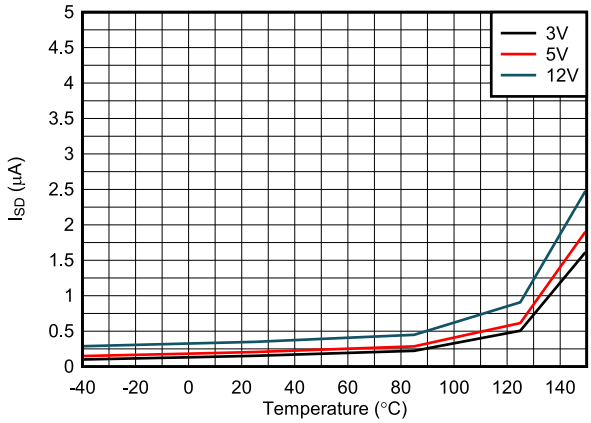
6.6 Typical Characteristics (continued)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



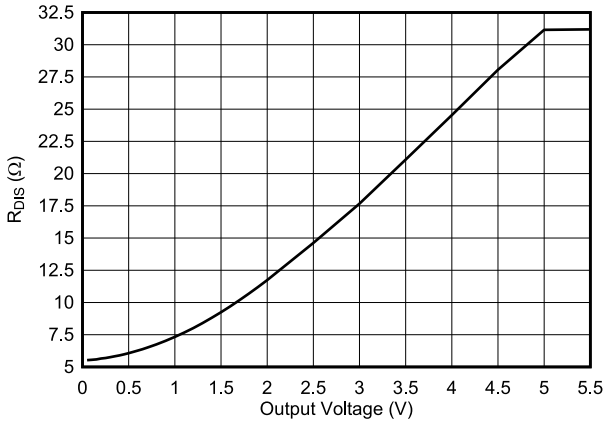
12 V_{IN} 2.2 MHz

图 6-41. Oscillator Frequency vs Temperature



V_{IN}: 3 V, 5 V, 12 V

图 6-42. Shutdown Current vs Temperature



V_{IN}: 12 V 25°C

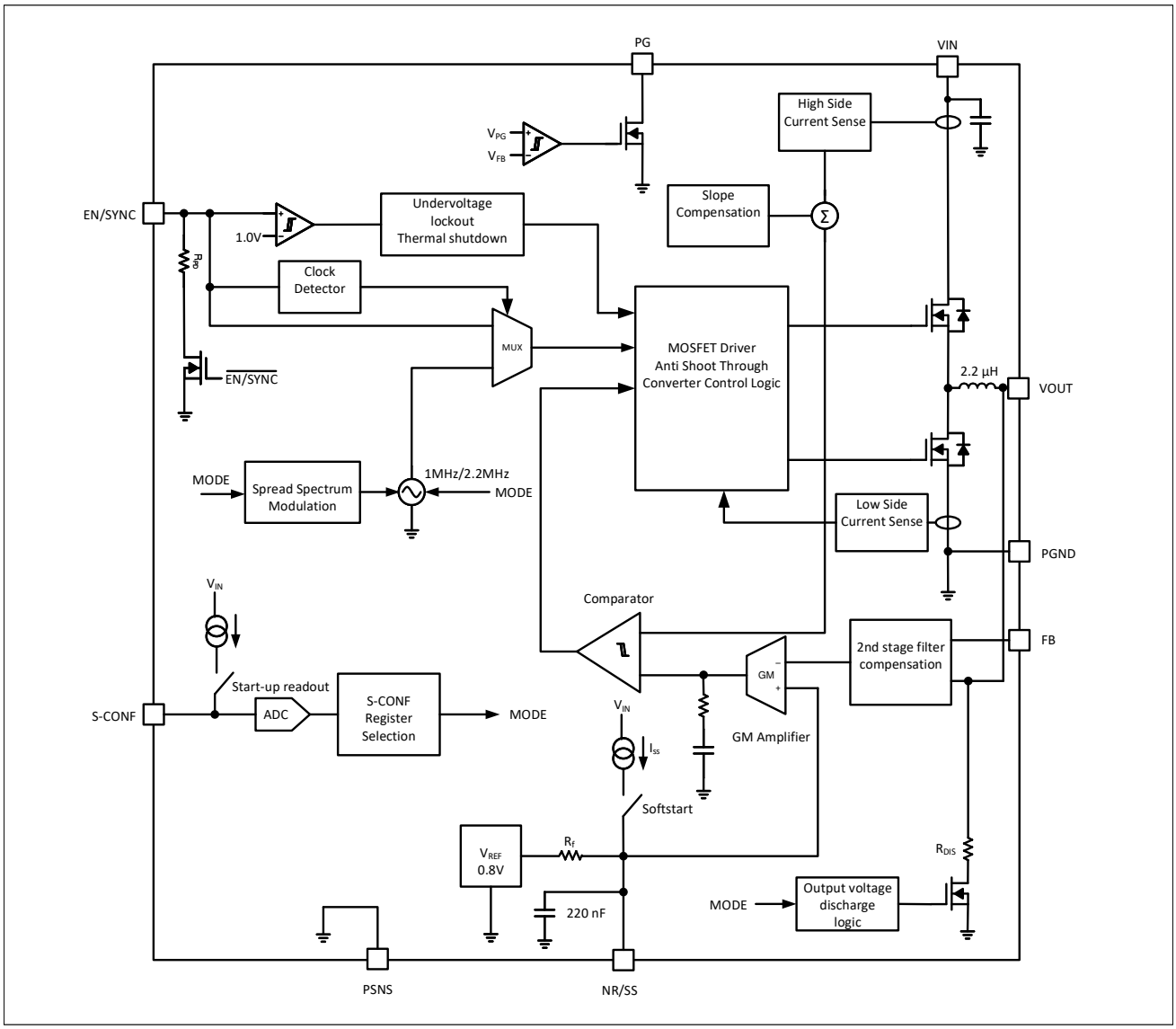
图 6-43. Output Discharge Resistance vs Output Voltage

7 Detailed Description

7.1 Overview

The TPSM8291x low-noise, low-ripple synchronous buck converter module is a fixed frequency current mode converter module. The converter module has a filtered internal reference to achieve a low-noise output similar to low-noise LDOs. The converter module achieves lower output voltage ripple by using a switching frequency of either 2.2 MHz or 1 MHz and an integrated 2.2- µ H inductor. The output voltage ripple can be further reduced by adding a small second stage L-C filter to the output. This can be a ferrite bead or a small inductor, followed by an output capacitor. Internal compensation maintains stability with an external filter inductor up to 50 nH. To avoid voltage drops across this second stage filter, the device regulates the output voltage after the filter. The TPSM8291x family supports an optional spread spectrum modulation. For example, when powering ADCs, spread spectrum modulation reduces the mixing spurs. Switching frequency, spread spectrum modulation, and output discharge are set using the S-CONF pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Config (S-CONF)

This S-CONF pin configures the device based on the resistor value. This pin is read after EN/SYNC goes high. The device configuration cannot be changed during operation. The S-CONF value is re-read if EN is pulled below 200 mV or if VIN falls below UVLO. 表 7-1 shows the configuration options of the following:

- Switching frequency
- Spread spectrum modulation
- Output discharge
- Synchronization

表 7-1. S-CONF Device Configuration Modes

S-CONF	SWITCHING FREQUENCY	SPREAD SPECTRUM	OUTPUT DISCHARGE	SYNCHRONIZATION
VIN	2.2 MHz	OFF	OFF	No
GND	1 MHz	OFF	OFF	No
4.87 kΩ	2.2 MHz	OFF	OFF	1.9 MHz to 2.42 MHz
6.04kΩ	2.2MHz	Triangle	OFF	No
7.5 kΩ	2.2 MHz	Random	OFF	No
9.31 kΩ	1 MHz	OFF	OFF	0.9 MHz to 1.2 MHz
11.5kΩ	1 MHz	Triangle	OFF	No
14.3 kΩ	1 MHz	Random	OFF	No
			Discharge On	
18.2 kΩ	2.2 MHz	OFF	ON	No
22.1 kΩ	1 MHz	OFF	ON	No
27.4 kΩ	2.2 MHz	OFF	ON	1.9 MHz to 2.42 MHz
34 kΩ	2.2 MHz	Triangle	ON	No
42.2 kΩ	2.2 MHz	Random	ON	No
52.3 kΩ	1 MHz	OFF	ON	0.9 MHz to 1.2 MHz
64.9kΩ	1 MHz	Triangle	ON	No
80.6 kΩ	1 MHz	Random	ON	No

7.3.2 Device Enable (EN/SYNC)

The device is enabled by pulling the EN/SYNC pin high and has an accurate rising threshold voltage of typically 1.01 V. After the device is enabled, the operation mode is set by the configuration of the S-CONF pin. This occurs during the device start-up delay time t_{delay}. After t_{delay} expires, the internal soft-start circuitry ramps up the output voltage over the soft-start time set by the $C_{NR/SS}$ capacitor. The start-up delay time t_{delay} varies depending on the selected S-CONF value. the time is shortest with smaller S-CONF resistors.

The EN/SYNC pin has an active pulldown resistor R_{PD}. This resistor prevents an uncontrolled start-up of the device, in case the EN/SYNC pin cannot be driven to a low level. The pulldown resistor is disconnected after start-up. With EN set to a low level, the device enters shutdown and the pulldown resistor is activated again.

7.3.3 Device Synchronization (EN/SYNC)

The EN/SYNC pin is also used for device synchronization. After a clock signal is applied to this pin, the device is enabled and reads the configuration of the S-CONF pin. The external clock frequency must be within the clock synchronization frequency range set by the S-CONF pin. When the clock signal changes from a clock to a static high, then the device switches from external clock to internal clock. To shutdown the device when using an external clock, EN/SYNC must go low for at least 10 µs.

The clock signal can be a logic signal with a logic level as specified in the electrical table, and can be applied directly to the EN/SYNC pin. External logic, such as an AND gate, can be used to combine separate enable and clock inputs, as shown in 图 7-1.

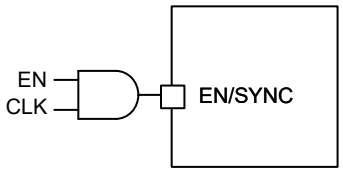


图 7-1. Synchronization with Separate Enable Signal (Optional)

7.3.4 Spread Spectrum Modulation

Using the S-CONF pin enables or disables spread spectrum modulation. DC/DC converters generate an output voltage ripple at the switching frequency. When powering ADCs or an analog front end (AFE), the switching frequency generates high frequency mixing spurs as well as a low frequency spur in the output frequency spectrum. Using the optional second stage L-C filter reduces the ripple of the converter and spurs by up to 30 dB.

The device has integrated two different spread spectrum modulation (SSM) schemes that are selected by the resistor connected to the S-CONF pin according to 表 7-1. It is possible to select random or triangle modulation to spread the switching frequency over a larger frequency range. The triangular SSM is modulated based on the switching frequency, and results in 1.9-kHz for 1-MHz switching frequency and 4.3-kHz for 2.2-MHz switching frequency. The modulation spread is ±10% of the device switching frequency. This SSM provides high attenuation when the receiver bandwidth is less than the modulation frequency, typically the case for systems using Fast Fourier Transforms (FFT) post processing as in high speed ADC applications. For applications sensitive to noise at the modulation frequency, random SSM is used. Using a random spread spectrum modulation also reduces the spurs in the output spectrum as shown in 图 6-2. The random SSM operates with the same frequency spread and modulation period as the triangular SSM. The randomized modulation uses a Fibonacci Linear-Feedback Shift Register (LFSR) so that every tone is generated once during the pseudo-random generation period. The frequency spreading is shown in 图 7-2.The attenuation using random or triangle SSM is shown in 图 6-26.

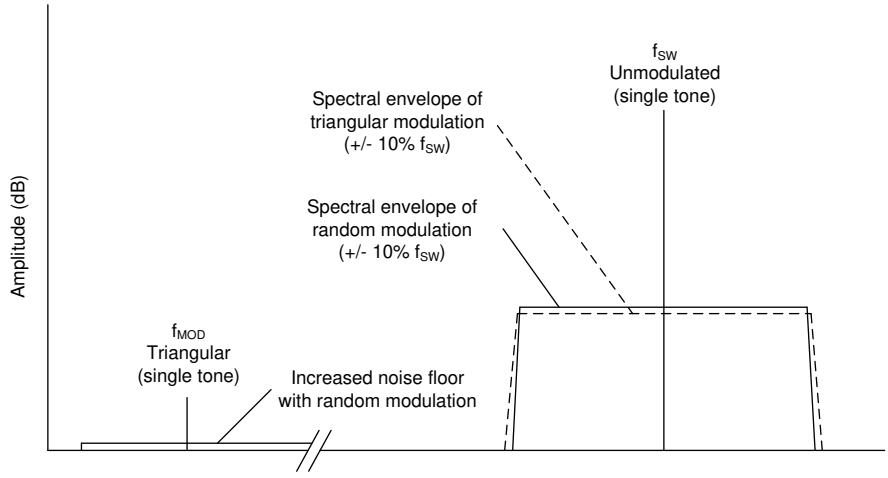


图 7-2. Spread Spectrum Modulation

7.3.5 Output Discharge

Output discharge is enabled or disabled, depending on the S-CONF setting. With output discharge enabled, the output voltage is pulled low by a discharge resistor R_{DIS} of typically 7 Ω. The output discharge function is enabled during thermal shutdown, UVLO, or when EN/SYNC is pulled low.

7.3.6 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, the device is enabled after the input voltage is above the undervoltage lockout threshold. The device is disabled after the input voltage falls below the undervoltage threshold.

7.3.7 Power-Good Output

The device has a power-good output. The PG pin goes high impedance once the FB pin voltage is above 95% of the nominal voltage, and is driven low after the voltage falls below typically 90% of the nominal voltage. 表 7-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 10 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 18 V. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND. PG has a deglitch time of typically 8 μs before going low.

表 7-2. Power Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN/SYNC = High)	$V_{FB} \geqslant V_{PG}$	√	
	$V_{FB} < V_{PG}$ after t_{PG}		√
Shutdown (EN/SYNC = Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

7.3.8 Noise Reduction and Soft-Start Capacitor (NR/SS)

A capacitor connected to this pin reduces the low frequency noise of the converter and sets the soft-start time. The larger the capacitor, the lower the noise and the longer the start-up time of the converter. The module has an internal 220-nF capacitor connected to the NR/SS pin. If no external capacitor is connected to the NR/SS pin, the default start-up time is 2.35 ms, although longer start-up times and additional noise reduction can be achieved with additional capacitance connected to the NR/SS pin. The maximum NR/SS cap is 3.3 μF for a start-up time of 35 ms.During soft start with a light load, the device skips switching pulses as needed to not discharge the output voltage. The device can start into a pre-biased output voltage.

The device achieves low noise by adding an R-C filter to the reference voltage, as shown in *Functional Block Diagram*. During start-up, the NR/SS capacitor is charged with a constant current of 75 μA (typical) to 0.8 V. Larger NR/SS capacitors provide for lower low frequency noise, as shown in 图 6-29.

7.3.9 Current Limit and Short-Circuit Protection

The device is protected against short circuits and overcurrent. The switch current limit prevents the device from high inductor current and from drawing excessive current from the input voltage rail. Excessive current can occur with a shorted, saturated inductor or a heavy load, shorted output circuit condition. If the inductor current reaches the threshold I_{SWpeak}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET is turned on again only when the low-side current is below the low-side sourcing current limit $I_{SWvalley}$.

Due to internal propagation delay, the actual current can exceed the static current limit, especially if the input voltage is high and very small inductances are used. The dynamic current limit is calculated as follows:

$$I_{peak(typ)} = I_{SWpeak} + \left(\frac{V_L}{L}\right) \times t_{PD} \quad (1)$$

where

- I_{SWpeak} is the static current limit, specified in *Electrical Characteristics*
- L is the inductance (2.2 µH for the TPSM8291x)
- V_L is the voltage across the inductor (VIN – VOUT)
- t_{PD} is the internal propagation delay, typically 50 ns

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. This can happen during light load conditions or a pre-biased output condition. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle.

7.3.10 Thermal Shutdown

The device goes into thermal shutdown after the junction temperature exceeds typically 170°C with a 20°C hysteresis.

7.4 Device Functional Modes

7.4.1 Fixed Frequency Pulse Width Modulation

To minimize output voltage ripple, the device operates in fixed frequency PWM operation down to no load. The switching frequency of 1 MHz or 2.2 MHz is selected using the S-CONF pin.

7.4.2 Low Duty Cycle Operation

For high input voltages or low output voltages, the 70-ns minimum on-time limits the maximum input to output voltage difference and the switching frequency selected. When the minimum on-time is reached, the output voltage rises above the regulation point. Refer to 表 8-2 for detailed design recommendations.

7.4.3 High Duty Cycle Operation (100% Duty Cycle)

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(\min)} = V_{OUT(\min)} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (2)$$

where

- $V_{OUT(min)}$ is the minimum output voltage the load can accept
- I_{OUT} is the output current
- $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the high-side MOSFET
- R_L is the DC resistance of the inductor used,

  76 mΩ for the TPSM8291x

To maintain fixed frequency switching, the device requires a minimum off-time of 50 ns (typical), 60 ns (maximum). If this limit is reached during a switching pulse, the device skips switching pulses to maintain output voltage regulation. If the input voltage decreases further, the device enters 100% mode.

7.4.4 Second Stage L-C Filter Compensation (Optional)

Most low-noise and low-ripple applications use a ferrite bead and bypass capacitor before the load. Using a second L-C filter is especially useful for low-noise and low-ripple applications with constant load current such as ADCs, DACs, and Jitter Cleaner. The second stage L-C filter is optional, and the device can be used without this filter. Without the filter, the device has a low output voltage noise of typically 16.6 µV_{RMS} shown in 图 6-29 with an output voltage ripple of 280 µV_{RMS} shown in 图 6-10. The second stage L-C filter attenuates the output voltage ripple by another approximately 30 dB shown in 图 6-12. To improve load regulation, the device can remote sense the output voltage after the second stage L-C filter and is internally compensated for the additional double pole generated by the L-C filter.

To keep the second stage L-C filter as small as possible, the internal compensation is optimized for a 10-nH to 50-nH inductance. A small ferrite bead or even a PCB trace provides sufficient inductance for output voltage ripple filtering. See 节 *8.2.2.2.3* for details.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The family of devices are optimized for low noise and low output voltage ripple.

8.2 Typical Applications

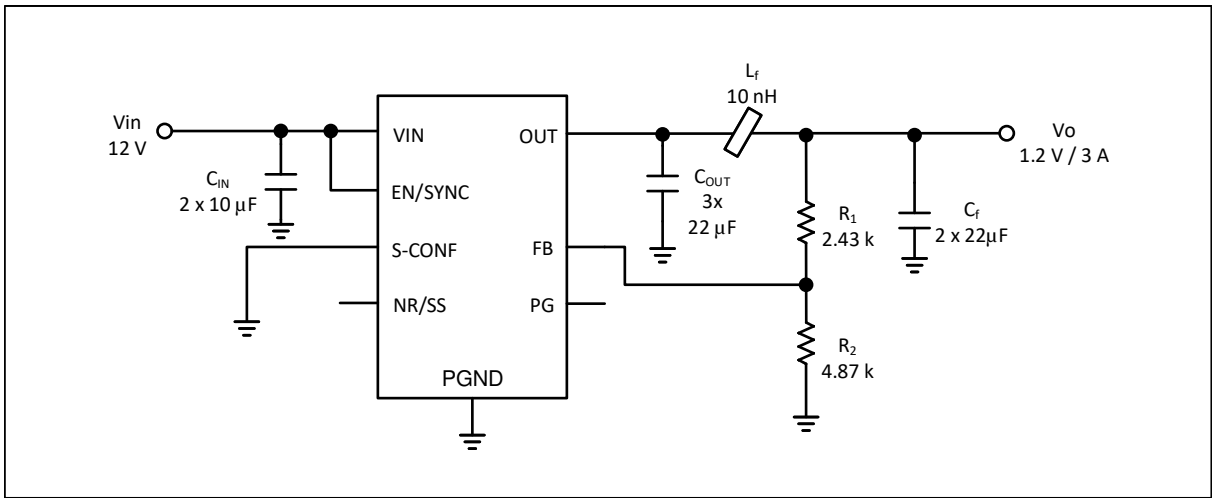


图 8-1. Typical Schematic

表 8-1 shows the list of components for the application curves in 节 8.2.3, unless otherwise noted.

表 8-1. List of Components

REFERENCE	PART NUMBER	DESCRIPTION	MANUFACTURER(1)
TPSM82913	TPSM82913	Low-noise and low-ripple buck module	Texas Instruments
C_{IN}	C2012X7S1E106K125AC	Ceramic capacitors: 2 × 10 µF ±10% 25-V ceramic capacitor X7S 0805	TDK
C_{OUT}	C2012X7S1A226M125AC	Ceramic capacitors: 3 × 22 µF, 10 V, ±20%, X7S, 0805	TDK
L_f	BLE18PS080SN1	Ferrite Bead	MuRata
C_f	C2012X7S1A226M125AC	Ceramic capacitor: 2 × 22 µF, 10 V, ±20%, X7S, 0805	TDK
$C_{NR/SS}$, C_{FF}	Optional, not shown	Ceramic capacitor	Standard
R1, R2		Resistor	Standard

(1) See the *Third-Party Products Disclaimer*

8.2.1 Design Requirements

The external components have to fulfill the needs of the application, but also meet the stability criteria of the control loop of the device. The device is optimized to work within a range of external components, and can be optimized for the following:

- Efficiency
- Output ripple
- Component count
- Lowest noise

Typical applications that have input voltages of ≤ 6 V use a 2.2-MHz switching frequency. Applications that have input voltages > 6 V can be optimized for efficiency using a 1-MHz switching frequency. In this case, the output voltage ripple doubles, which is typically acceptable when powering high speed ADCs. Optimization for powering clock and PLL circuits that need a 3.3-V output use a 2.2-MHz switching frequency, minimizing output voltage ripple and low frequency noise.

For the application cases that are not found in 表 8-2, there are two methods to design the TPSM8291x circuit. 节 *8.2.2.1* uses Webench to design the circuit automatically or the calculations in 节 *8.2.2.2* can be used instead.

表 8-2. Typical Single L-C Filter Design Recommendations

DESIGN GOAL	V_{IN}	V_{OUT}	F_{SW}	OUTPUT CAPACITORS [3]
Typical	12 V[1]	≤ 2.0 V[1]	1 MHz	3 × 22 µF, 10 V, 0805
Higher efficiency (with higher ripple and noise)	12 V	2.0 V < V_{OUT} ≤ 3.3 V	1 MHz	3 × 22 µF, 10 V, 0805
Low ripple, noise PLL and Clock Supply	12 V	2.6 V ≤ V_{OUT} ≤ 3.3 V	2.2 MHz	3 × 22 µF, 10 V, 0805
Typical	12 V	> 3.3 V	2.2 MHz	
Typical	5 V	≤ 3.3 V	2.2 MHz	3 × 22 µF, 10 V, 0805
Typical	5 V	> 3.3 V	2.2 MHz	1 × 47 µF, 1210 and 2 × 22 µF, 10 V, 0805

(1) The maximum input to output voltage difference is limited by the device maximum minimum on-time of 70 ns. This is especially important for input voltages above 12 V or output voltages below 1 V. See 节 *8.2.2.2.1*.
(2) For output capacitor part numbers, see 表 8-4.

The second stage L-C filter is optional, as the device can be used without this filter to achieve below 20- µ V_{RMS} noise typically. A second stage filter is added to provide additional attenuation of the output voltage ripple. The output voltage is sensed after the second L-C filter by connecting the FB resistors to the second stage L-C filter capacitor. This action provides remote sense, minimizing output voltage drop due to the ferrite bead. Refer to 表 8-3 for second stage L-C filter recommendations based on the output voltage.

表 8-3. Second Stage L-C (Ferrite Bead) Filter Design Recommendations

V_{OUT} (V)	FERRITE BEAD IMPEDANCE (AT 100 MHZ)[2]	OUTPUT CAPACITORS [1]
≤ 3.3 V	8 Ω to 20 Ω	2 × 22 µF, 10 V, 0805
> 3.3 V	8 Ω to 20 Ω	3 × 22 µF, 10 V, 0805

(1) For output capacitor part numbers, see 表 8-4.
(2) For second stage L-C filter part numbers, see 表 8-5.

8.2.2 Detailed Design Procedure

If the specific design is not found in the *表 8-2* section, TI recommends WEBENCH® to generate the design. Alternatively, the manual design procedure in *External Component Selection* can be followed.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8291x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. After in a TPSM8291x design, enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 External Component Selection

8.2.2.2.1 Switching Frequency Selection

The switching frequency can be chosen to optimize efficiency (1 MHz) or ripple, noise (2.2 MHz). Using the 2.2-MHz setting increases the gain of the feedback loop and can result in lower output noise. However, additional considerations for minimum on-time and duty cycle must also be considered. First, calculate the duty cycle using 方程式 3. Higher efficiency results in a shorter on-time, so a conservative approach is to use a higher efficiency than expected in the application.

$$D = \frac{V_{OUT}}{V_{IN} \times \eta} \tag{3}$$

where

- η is the estimated efficiency (use the value from the efficiency curves or 0.9 as an conservative assumption)

Then, calculate the on-time with both 1 MHz and 2.2 MHz using 方程式 4. The on-time must always remain above the minimum on-time of 70 ns. Use the maximum input voltage and maximum efficiency to determine the minimum duty cycle, D_{min}. Use the maximum switching frequency for f_{SW}.

$$t_{ON\_min} = \frac{D_{min}}{f_{SW\_max}} \tag{4}$$

then

- If t_{ON_min} min < 70 ns with 2.2 MHz, use 1 MHz.
- If t_{ON_min} min < 70 ns with 1 MHz, reduce the maximum input voltage.
- If t_{ON_min} min ⩾ 70 ns for both cases, use 1 MHz for highest efficiency, or 2.2 MHz for lowest noise and ripple.

8.2.2.2.2 Output Capacitor Selection

The effective output capacitance can range from 40 µF (minimum) up to 200 µF (maximum) for a single L-C system design. When using a second L-C filter, the first L-C filter must have output capacitance between 40 µF and 80 µF, the second stage L-C filter (if used) must have at least 20 µF of capacitance, and the total capacitance for both L-C filters must be less than 200 µF. Load transient testing and measuring the bode plot are good ways to verify stability.

TI recommends ceramic capacitors (X5R or X7R). Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. The ESR and ESL of the output capacitor are also important considerations in selecting the output capacitors for low noise applications. Smaller package sizes typically have lower ESL and ESR. 0805 or smaller packages are recommended, as long as they provide the required capacitance and voltage rating for stable operation. 表 8-4 lists recommended output capacitors.

表 8-4. Recommended Output Capacitors

CAPACITOR TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE (V)	PACKAGE
Bulk Capacitor	22 µF, X7S	TDK C2012X7S1A226M125AC	10	0805
Bulk Capacitor	47 µF, X7R	Murata GRM32ER71A476ME15L	10	1210

8.2.2.2.3 Ferrite Bead Selection for Second L-C Filter

Using a ferrite bead for the second stage L-C filter minimizes the external component count because most of the noise sensitive circuits use a RF bead for high frequency attenuation as a default component at their inputs.

Select a ferrite bead with sufficiently high inductance at full load, and with low DC resistance (below 10 mΩ) to keep the converter efficiency as high as possible. The ferrite bead inductance decreases with increased load current. Therefore, the ferrite bead must have a current rating much higher than the desired load current.

The recommendation is to choose a ferrite bead with an impedance of 8 Ω to 20 Ω at 100 MHz. Refer to 表 8-5 for possible ferrite beads.

表 8-5. Recommended Ferrite Beads

PART NUMBER	MANUFACTURER	SIZE	IMPEDANCE AT 100 MHZ	INDUCTANCE AT 100 MHz (CALCULATED)	DC RESISTANCE	CURRENT RATING
BLE18PS080SN1	MuRata	0603	8.5 Ω	13.5 nH	4 mΩ	5 A
74279221100	Wurth Elektronik	1206	10 Ω	15.9 nH	3 mΩ	10.5 A
7427922808	Wurth Electronik	0603	8 Ω	12.7 nH	5 mΩ	9.5 A

The internal compensation has been designed to be stable with up to 50 nH of inductance in the second stage filter. To achieve low ripple, the second L-C filter requires only 5-nH to 10-nH inductance. The inductance can be estimated from the ferrite bead impedance specification at 100 MHz, with the assumption that the inductance is similar at the selected converter switching frequency of 1 MHz or 2.2 MHz, and can be verified through tools available on some manufacturer websites. The inductance of a ferrite bead is calculated using 方程式 5:

$$L = \frac{Z}{(2 \times \pi \times f)} \tag{5}$$

where

- Z is the impedance of the ferrite bead in ohms at the specified frequency (usually 100 MHz)
- f is the specified frequency (usually 100 MHz)

8.2.2.2.4 Input Capacitor Selection

For the best output and input voltage filtering, Ti recommends X5R or X7R ceramic capacitors. The input bulk capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. TI recommends a 10-µF or larger input capacitor. Having two in parallel further improves the input voltage ripple filtering, minimizing noise coupling into adjacent circuits. The voltage rating of the cap must also be taken into consideration, and must provide the required 5-µF minimum effective capacitance after DC bias derating.

In addition to the bulk input cap, a smaller cap must be placed directly from the VIN pin to the PGND pin to minimize input loop parasitic inductance, thereby minimizing the high frequency noise of the device. The input cap placement affects the output noise, so care must be taken in placing both the bulk cap and bypass caps. 表 8-6 lists recommended input capacitors.

表 8-6. Recommended Input Capacitors

INPUT CAP TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE RATING (V)	PACKAGE SIZE
Bulk Cap	10 µF, X7S	TDK C2012X7S1E106K125AC	25	0805
Bypass Cap	2.2 nF, X7R	Murata GRM155R71E222KA01D	25	0402

8.2.2.2.5 Setting the Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.8 V to 5.5 V, according to 方程式 6. To keep the feedback network robust from noise, and to reduce the self-generated noise of resistors, set R2 equal to or lower than 5 kΩ. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* technical brief.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (6)$$

A feedforward capacitor (C_{FF}) is not required for proper operation, but can further improve output noise. However, care must be taken in choosing the C_{FF}, because the power-good (PG) function can not be valid with a large C_{FF} during start-up, and can cause spurious triggering of the PG pin during a large load transient. Refer to the *Pros and Cons Using a Feedforward Capacitor with a Low Dropout Regulator* application report for a discussion of the pros and cons of using a feedforward capacitor.

8.2.2.2.6 NR/SS Capacitor Selection

As described in 节 7.3.8, the NR/SS cap affects both the total noise and the soft-start time. When no NR/SS cap is connected, there is a default 2.35-ms soft-start time. The recommended value for a 5-ms soft-start time and good noise performance is 220 nF, as there is an internal 220 nF capacitor already in the module. The maximum NR/SS cap is 3.3 µF for a start-up time of 35 ms. Values greater than 1 µF have minimal improvement in noise performance. Use 方程式 7 and 方程式 8 to calculate the soft-start time based on desired soft-start time or the chosen capacitor value. Note that the C_{NRSS} in the equation below is the combination of the internal 220 nF cap and any external cap from the C_{NRSS} pin to GND.

$$tss(s) = \left(\frac{C_{NRSS} \times 0.8}{I_{NRSS}} \right) \quad (7)$$

$$C_{NRSS}(F) = \frac{(I_{NRSS} \times t_{ss})}{0.8} \quad (8)$$

8.2.3 Application Curves

V_{IN}=12 V, V_{OUT}=1.2 V, T_A=25°C, BOM = 表 8-1, (unless otherwise noted)

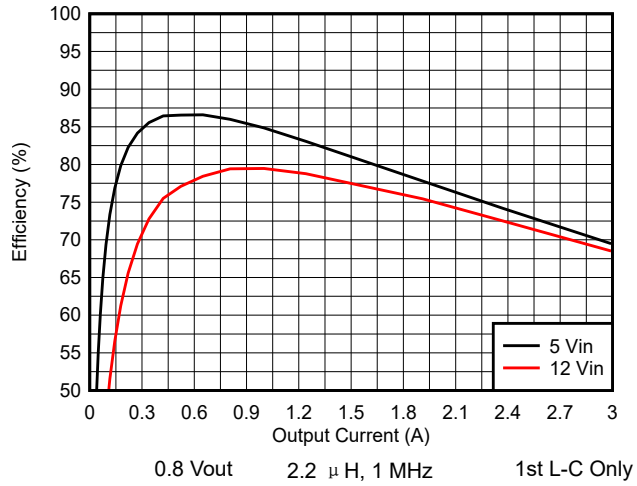


图 8-2. Efficiency vs Load Current

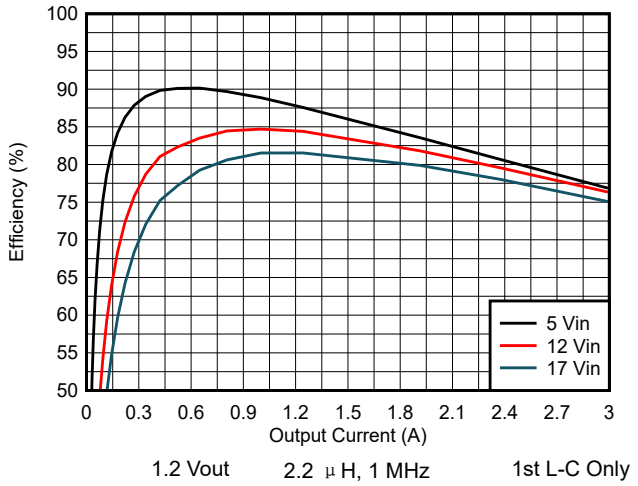


图 8-3. Efficiency vs Load Current

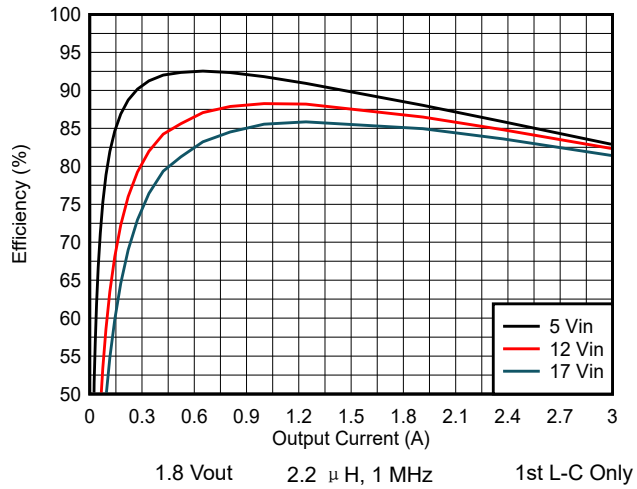


图 8-4. Efficiency vs Load Current

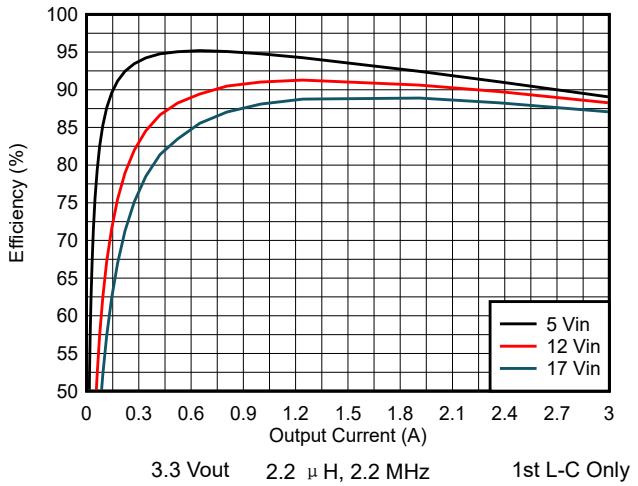


图 8-5. Efficiency vs Load Current

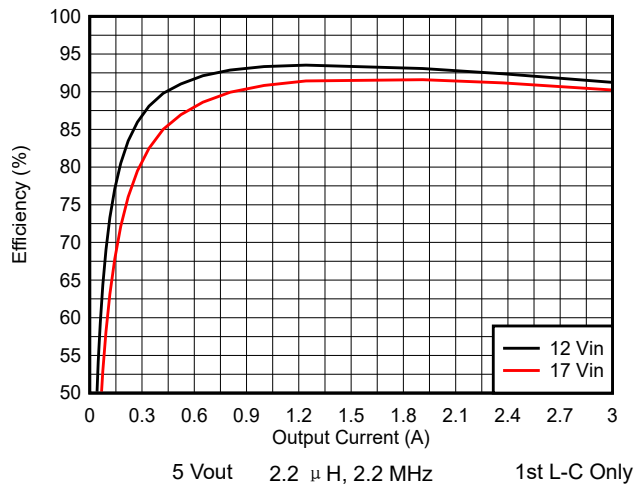


图 8-6. Efficiency vs Load Current

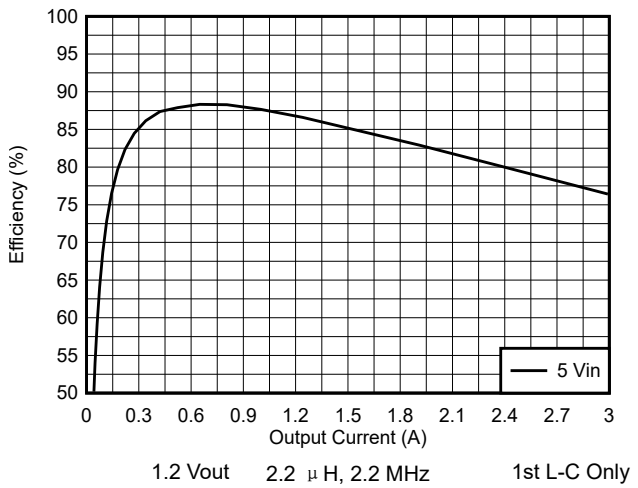
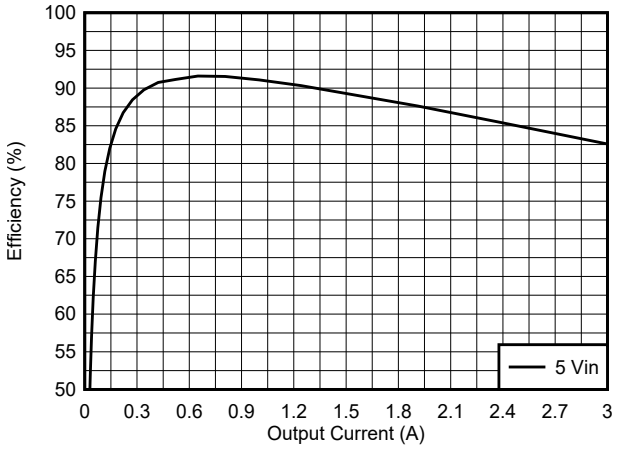
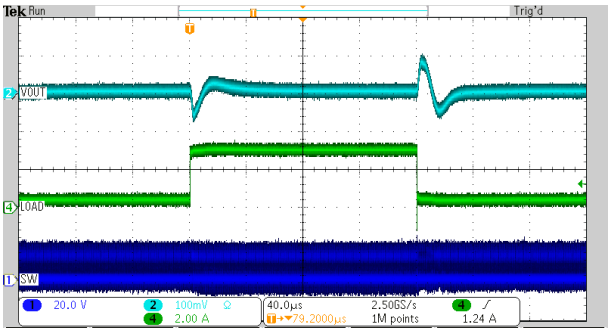


图 8-7. Efficiency vs Load Current



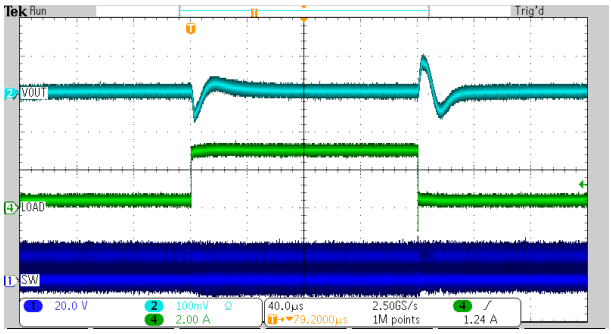
1.8 Vout 2.2 µH, 2.2 MHz 1st L-C Only

图 8-8. Efficiency vs Load Current



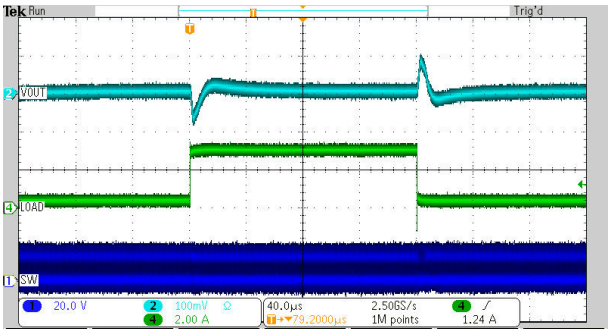
12 V to 1.2 V 1 MHz 1st L-C Only
300 mA to 3 A to 300 mA

图 8-9. Load Transient



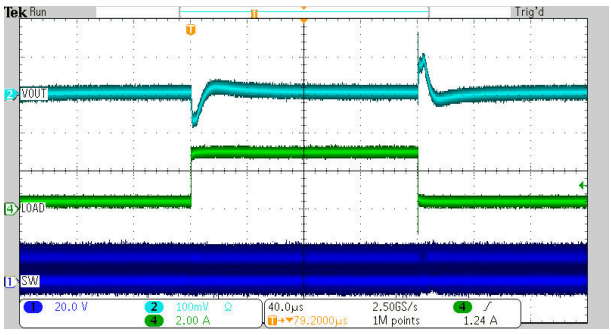
12 V to 1.2 V 1 MHz After 2nd L-C
300 mA to 3 A to 300 mA

图 8-10. Load Transient



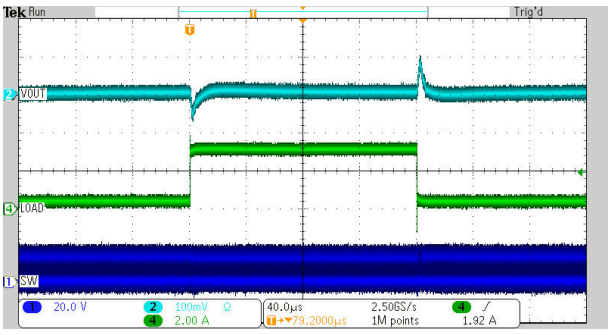
12 V to 1.8 V 1 MHz 1st L-C Only
300 mA to 3 A to 300 mA

图 8-11. Load Transient



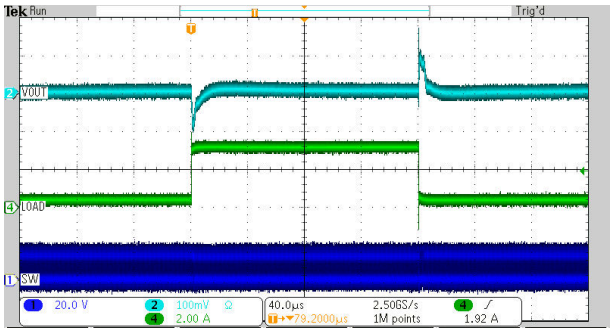
12 V to 1.8 V 1 MHz After 2nd L-C
300 mA to 3 A to 300 mA

图 8-12. Load Transient



12 V to 3.3 V 2.2 MHz 1st L-C Only
300 mA to 3 A to 300 mA

图 8-13. Load Transient



12 V to 3.3 V 2.2 MHz After 2nd L-C

300 mA to 3 A to 300 mA

图 8-14. Load Transient

8.3 Power Supply Recommendations

The power supply to the TPSM8291x must have a current rating according to the supply voltage, output voltage, and output current of the TPSM8291x.

8.4 Layout

8.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8291x demands careful attention to ensure best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* technical brief for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The TPSM8291x has an integrated input capacitor. However, placement of the input capacitors must be placed as close as possible to the VIN and PGND pins of the device. Route the input capacitors directly to the VIN and PGND pins avoiding vias.
- Place the output capacitor ground close to the PGND pin and route it directly avoiding vias.
- Sensitive traces, such as the connections to the NR/SS and FB pins must be connected with short traces and be routed away from any noise source.
- Connect the PSNS pin directly to the system GND plane with a via.
- The SW pin must not be connected and must be left floating. If the pin is soldered to PCB copper, the pour needs to be as small as possible with no inner layer connections. The pin is provided for probing the internal SW only, and not to be connected to any external component, as shown on the EVM.
- Place the second L-C filter, L_f and C_f, near the load to reduce any radiated coupling around the second L-C filter
- Place the FB resistors, R1 and R2, close to the FB pin and route the VOUT connection from R1 to the load as a remote sense trace. If a second L-C filter is used, this connection must be made after L_f.
- The recommended layout is implemented on the EVM and shown in the EVM user's guide.

8.4.2 Layout Example

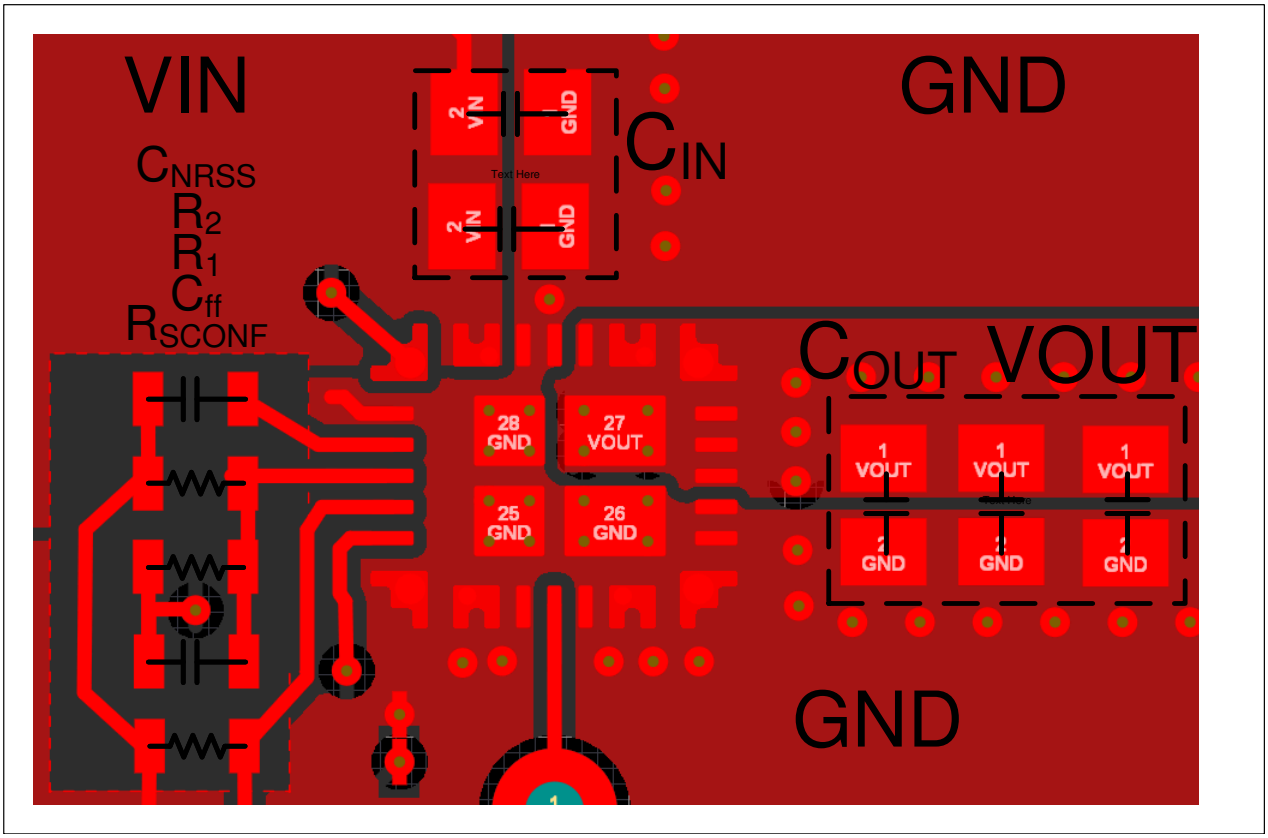


图 8-15. Recommended Layout for Single L-C Filter

备注

For a single L-C configuration, the feedback sense is placed near the VOUT capacitors. For a second L-C filter design, the feedback sense is placed near the load after the VOUT_FILT capacitors.

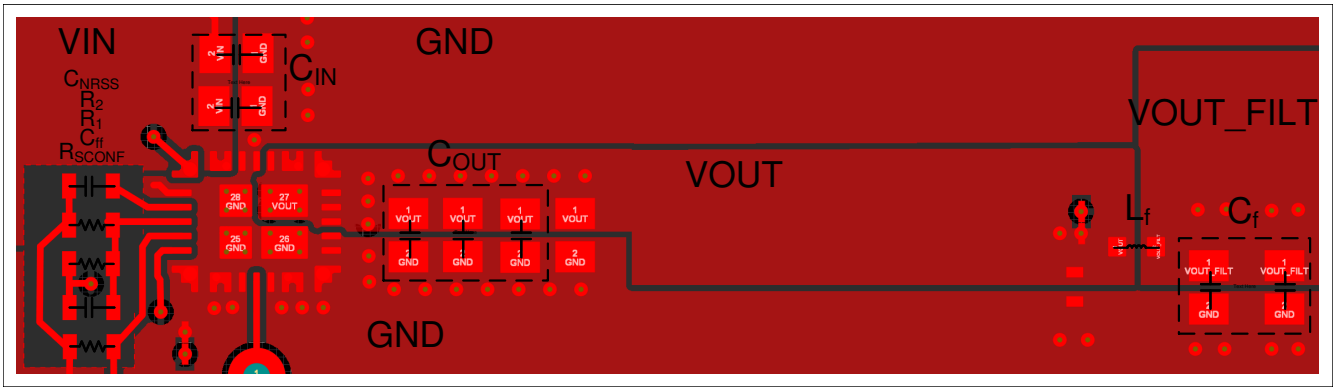


图 8-16. Recommended Layout for Design with Second L-C Filter

备注

The ferrite bead can be placed closer to the device as long as it is placed > 8 mm from the device. This placement avoids capacitive and electromagnetic coupling to the output of the ferrite bead. If the ferrite bead is placed < 8 mm, the filtering effect of the ferrite bead is greatly reduced. If the ferrite bead is routed through a via to the back side of the board, ensure adequate ground plane between the layers if the ferrite bead is in this area.

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8291x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. Once in a TPSM8291x design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* technical brief
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* technical brief
- Texas Instruments, *Pros and Cons Using a Feedforward Capacitor with a Low Dropout Regulator* application report

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM82912RDUR	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSM82912
TPSM82912RDUR.A	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSM82912
TPSM82913RDUR	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSM82913
TPSM82913RDUR-ET	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	82913-ET
TPSM82913RDUR-ET.A	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	82913-ET
TPSM82913RDUR.A	Active	Production	B0QFN (RDU) | 28	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSM82913

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

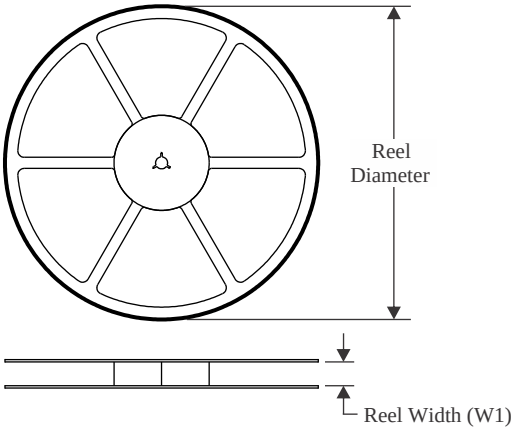
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

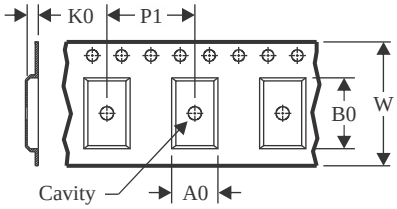
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

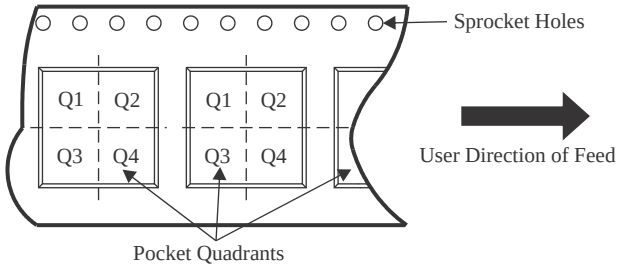


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

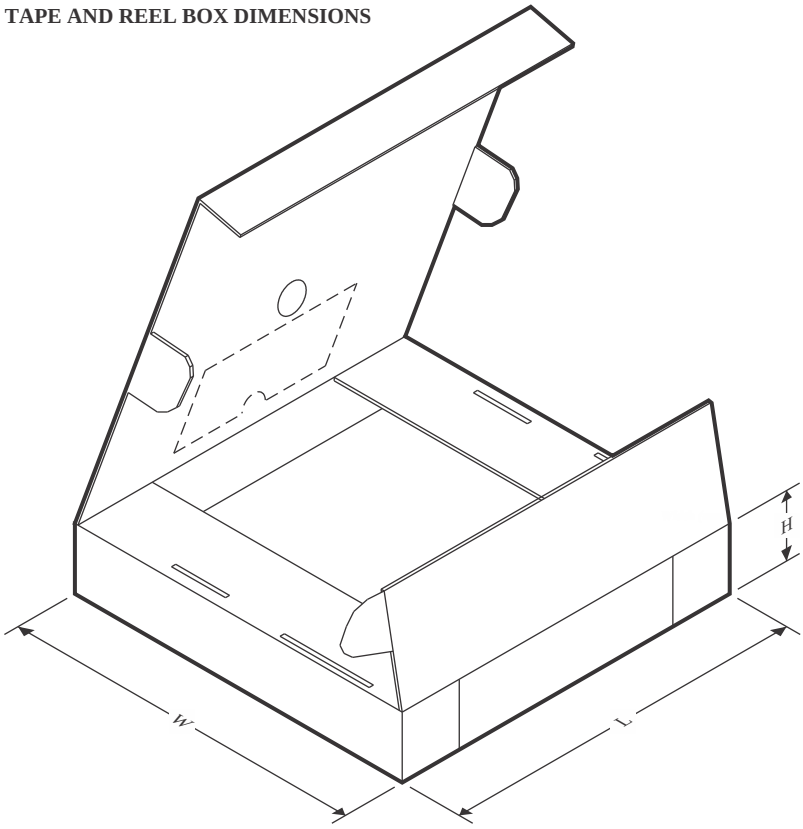
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM82912RDUR	B0QFN	RDU	28	1500	330.0	17.6	4.8	5.8	2.05	8.0	12.0	Q1
TPSM82913RDUR	B0QFN	RDU	28	1500	330.0	17.6	4.8	5.8	2.05	8.0	12.0	Q1
TPSM82913RDUR-ET	B0QFN	RDU	28	1500	330.0	17.6	4.8	5.8	2.05	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

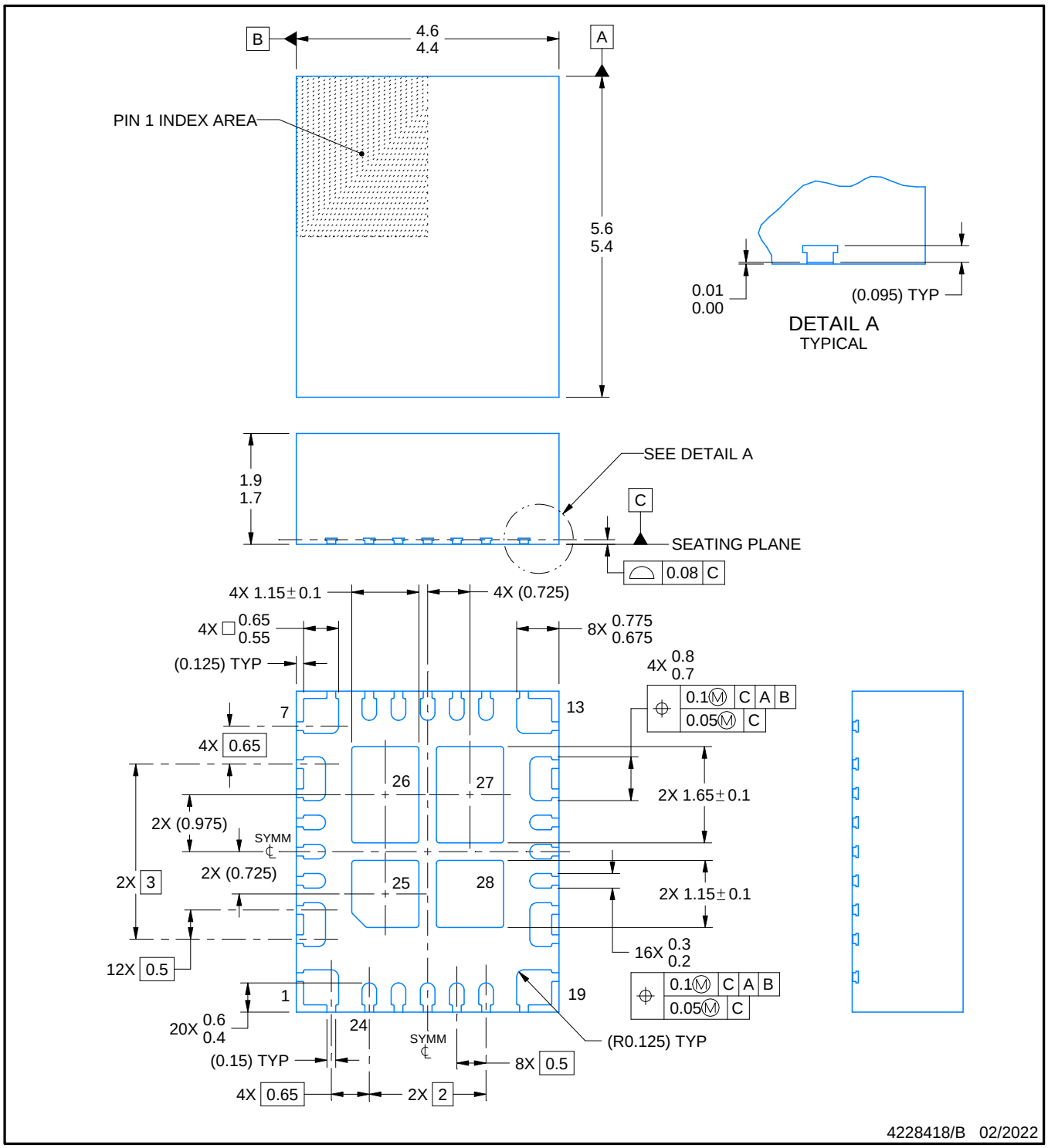
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM82912RDUR	B0QFN	RDU	28	1500	336.0	336.0	48.0
TPSM82913RDUR	B0QFN	RDU	28	1500	336.0	336.0	48.0
TPSM82913RDUR-ET	B0QFN	RDU	28	1500	336.0	336.0	48.0

RDU0028A

PACKAGE OUTLINE

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

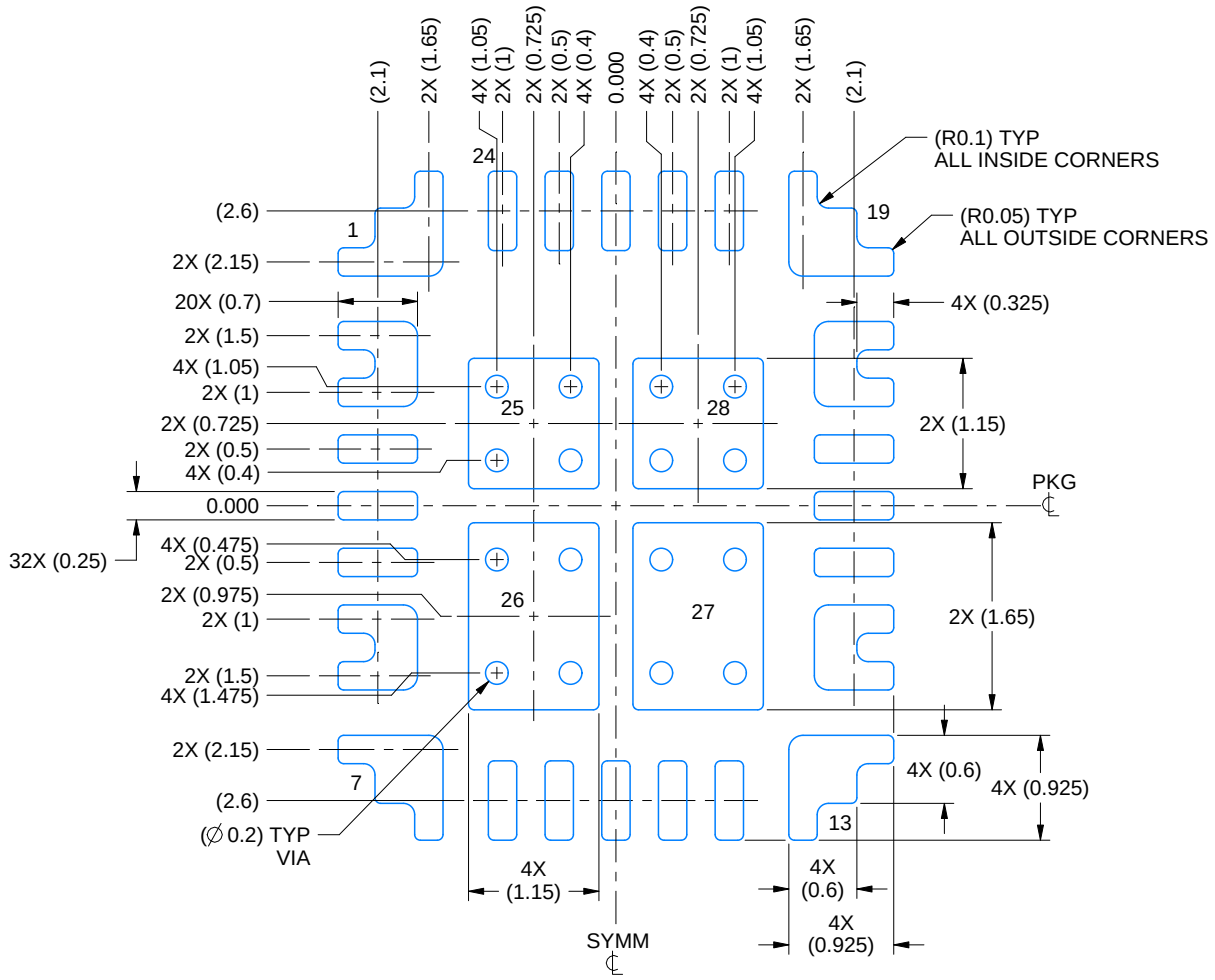
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

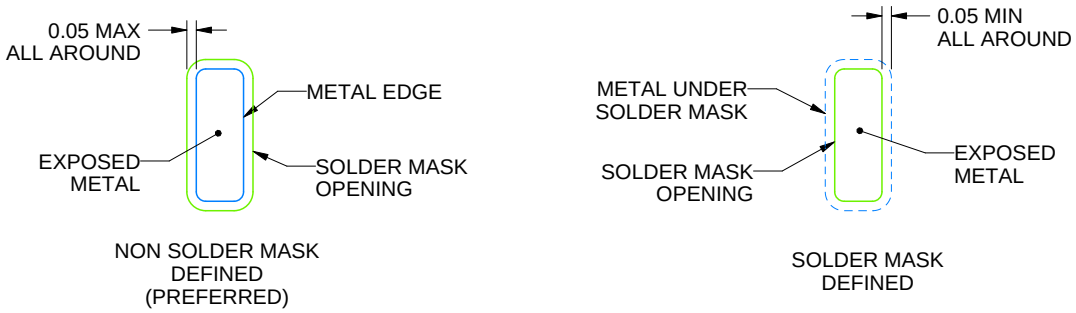
RDU0028A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

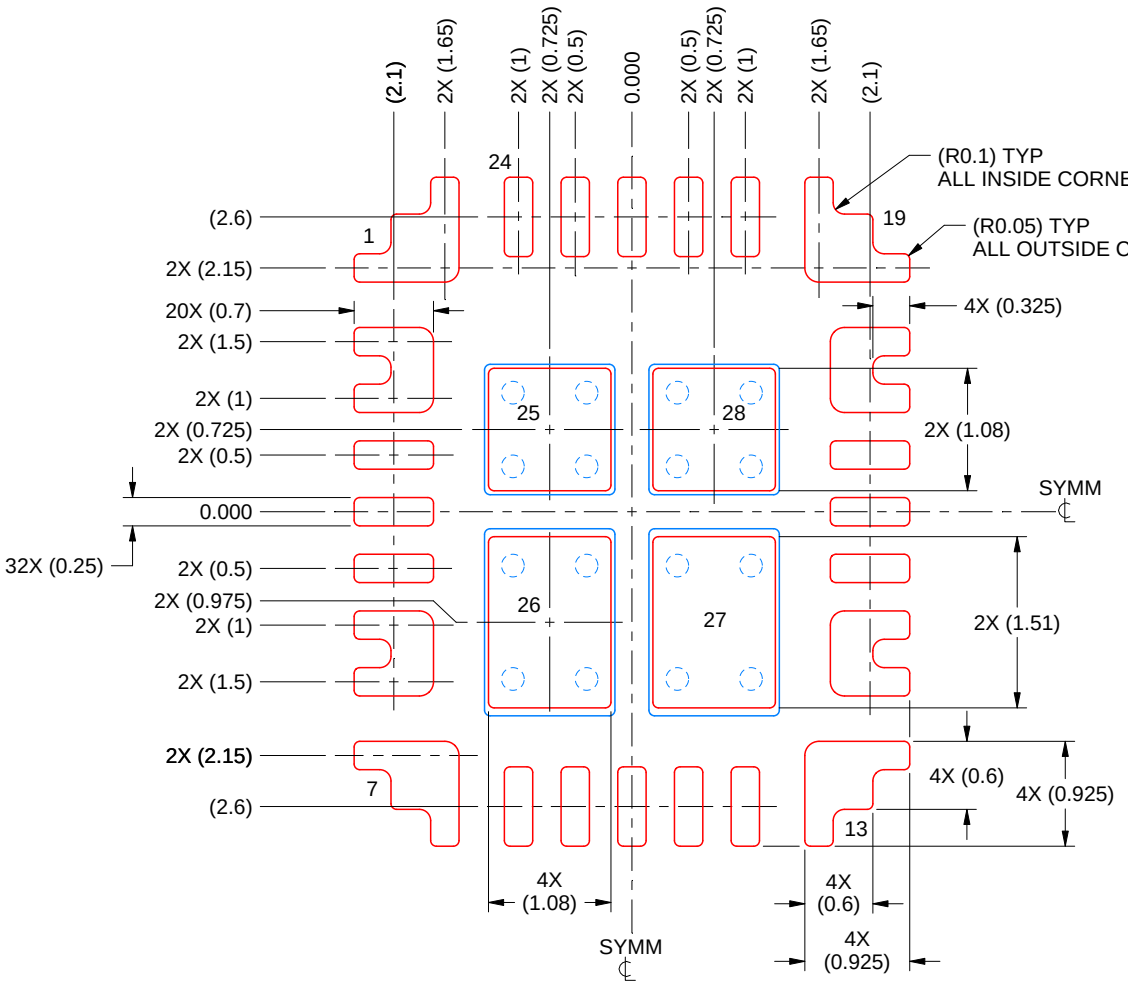


SOLDER MASK DETAILS

4228418/B 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 25 & 28: 89%
PADS 26 & 27: 86%

4228418/B 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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